GSM Power Management System

ADP3405

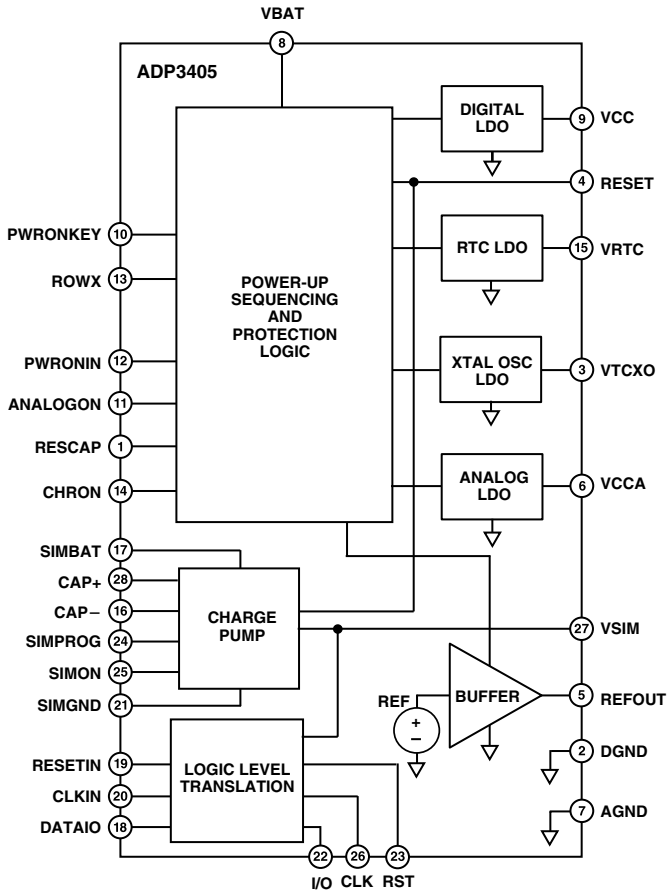
FEATURES

Handles all GSM Baseband Power Management Functions
Four LDOs Optimized for Specific GSM Subsystems
Charges Li-Mn Coin Cell for Real-Time Clock
Charge Pump and Logic Level Translators for 3 V and 5 V GSM SIM Modules
Narrow Body 4.4 mm 28-Lead TSSOP Package

APPLICATIONS

GSM/DCS/PCS Handsets
TeleMatic Systems
ICO/Iridium Terminals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3405 is a multifunction power management system IC optimized for GSM cell phones. The wide input voltage range of 3.0 V to 7.0 V makes the ADP3405 ideal for both single cell Li-Ion and three cell NiMH designs. The current consumption of the ADP3405 has been optimized for maximum battery life, featuring a ground current of only 150 μA when the phone is in standby (digital LDO, and SIM card supply active). An undervoltage lockout (UVLO) prevents the startup when there is not enough energy in the battery. All four integrated LDOs are optimized to power one of the critical sub-blocks of the phone. Their novel anyCAP® architecture requires only very small output capacitors for stability, and the LDOs are insensitive to the capacitors' equivalent series resistance (ESR). This makes them stable with any capacitor, including ceramic (MLCC) types for space-restricted applications.

A step-up converter is implemented to supply both the SIM module and the level translation circuitry to adapt logic signals for 3 V and 5 V SIM modules. Sophisticated controls are available for power-up during battery charging, keypad interface, and charging of an auxiliary backup battery for the real-time clock. These allow an easy interface between ADP3405, GSM processor, charger, and keypad. Furthermore, a reset circuit and a thermal shutdown function have been implemented to support reliable system design.

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ADP3405–SPECIFICATIONS

(–20°C ≤ T_A ≤ +85°C, VBAT = 3 V to 7 V, C_{VBAT} = C_{SIMBAT} = C_{VSIM} = 10 µF, C_{VCC} = C_{VCCA} = 2.2 µF, C_{VRTC} = 0.1 µF, C_{VTCXO} = 0.22 µF, C_{VCAP} = 0.1 µF, min. loads applied on all outputs, unless otherwise noted.)

ELECTRICAL CHARACTERISTICS[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SHUTDOWN SUPPLY CURRENT	I_{BAT}					
VBAT = Low (UVLO Low)		VBAT = 2.7 V		3	20	µA
VBAT = High (UVLO High)		VBAT = 3.6 V, VRTC On		12	30	µA
OPERATING GROUND CURRENT	I_{GND}					
VCC and VRTC On		Minimum Loads, VBAT = 3.6 V		100	140	µA
VCC, VRTC and VSIM On		Minimum Loads, VBAT = 3.6 V		150	240	µA
All LDOs and VSIM On		Minimum Loads, VBAT = 3.6 V		260	400	µA
All LDOs and VSIM On		Maximum Loads, VBAT = 3.6 V		15		mA
UVLO CHARACTERISTICS						
UVLO On Threshold	$VBAT_{UVLO}$			3.2	3.3	V
UVLO Hysteresis				200		mV
INPUT CHARACTERISTICS						
Input High Voltage	V_{IH}					
PWRONIN and ANALOGON			2			V
PWRONKEY			0.7 × VBAT			V
Input Low Voltage	V_{IL}					
PWRONIN and ANALOGON					0.4	V
PWRONKEY					0.3 × VBAT	V
PWRONKEY INPUT PULL-UP RESISTANCE TO VBAT			15	20	25	kΩ
CHRON CHARACTERISTICS						
CHRON Threshold	V_T		2.38	2.48	2.58	V
CHRON Hysteresis Resistance	R_{IN}	2.38 < CHRON < V_T	108	125	138	kΩ
CHRON Input Bias Current	I_B	CHRON > V_T			0.5	µA
ROWX CHARACTERISTICS						
ROWX Output Low Voltage	V_{OL}	PWRONKEY = Low I_{OL} = 200 µA			0.4	V
ROWX Output High Leakage Current	I_{IH}	PWRONKEY = High V(ROWX) = 5 V			1	µA
SHUTDOWN						
Thermal Shutdown Threshold[2]		Junction Temperature		160		°C
Thermal Shutdown Hysteresis		Junction Temperature		35		°C
DIGITAL LDO (VCC)						
Output Voltage	VCC	Line, Load, Temp	2.710	2.765	2.820	V
Line Regulation	DVCC	3 V < VBAT < 7 V, Min Load		2		mV
Load Regulation	DVCC	50 µA < I_{LOAD} < 100 mA, VBAT = 3.6 V		15		mV
Output Capacitor[3]	C_O		2.2			µF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV I_{LOAD} = 100 mA			215	mV
ANALOG LDO (VCCA)						
Output Voltage	VCCA	Line, Load, Temp	2.710	2.765	2.820	V
Line Regulation	DVCCA	3 V < VBAT < 7 V, Min Load		2		mV
Load Regulation	DVCCA	200 µA < I_{LOAD} < 130 mA, VBAT = 3.6 V		15		mV
Output Capacitor[3]	C_O		2.2			µF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV I_{LOAD} = 130 mA			215	mV
Ripple Rejection	DVBAT/ DVCCA	f = 217 Hz (t = 4.6 ms) VBAT = 3.6 V	65	70		dB
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz I_{LOAD} = 130 mA, VBAT = 3.6 V		75		µV rms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CRYSTAL OSCILLATOR LDO (VTCXO)						
Output Voltage	VTCXO	Line, Load, Temp	2.710	2.765	2.820	V
Line Regulation	ΔVTCXO	3 V < VBAT < 7 V, Min Load		2		mV
Load Regulation	ΔVTCXO	100 μA < I_{LOAD} < 5 mA, VBAT = 3.6 V		1		mV
Output Capacitor[3]	C_O		0.22			μF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV I_{LOAD} = 5 mA			150	mV
Ripple Rejection	ΔVBAT/ ΔVTCXO	f = 217 Hz (t = 4.6 ms), VBAT = 3.6 V	65	72		dB
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz I_{LOAD} = 5 mA, VBAT = 3.6 V		80		μV rms
VOLTAGE REFERENCE (REFOUT)						
Output Voltage	V_{REFOUT}	Line, Load, Temp	1.192	1.210	1.228	V
Line Regulation	ΔV_{REFOUT}	3 V < VBAT < 7 V, Min Load		2		mV
Load Regulation	ΔV_{REFOUT}	0 μA < I_{LOAD} < 50 μA, VBAT = 3.6 V		0.5		mV
Ripple Rejection	ΔVBAT/ ΔV_{REFOUT}	f = 217 Hz (t = 4.6 ms), VBAT = 3.6 V	65	75		dB
Maximum Capacitive Load	C_O		100			pF
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz VBAT = 3.6 V		40		μV rms
REAL-TIME CLOCK LDO/ BATTERY CHARGER (VRTC)						
Maximum Output Voltage	VRTC	I_{LOAD} ≤ 10 μA	2.810	2.850	2.890	V
Current Limit	I_{MAX}	3.050 V < VBAT < 7 V		175		μA
Off Reverse Leakage Current	I_L	2.0 V < VBAT < UVLO			1	μA
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 10 mV I_{LOAD} = 10 μA			170	mV
SIM CHARGE PUMP (VSIM)						
Output Voltage for 5 V SIM Modules	VSIM	0 mA ≤ I_{LOAD} ≤ 10 mA SIMPROG = High	4.70	5.00	5.30	V
Output Voltage for 3 V SIM Modules	VSIM	0 mA ≤ I_{LOAD} ≤ 6 mA SIMPROG = Low	2.82	3.00	3.18	V
GSM/SIM LOGIC TRANSLATION (GSM INTERFACE)						
Input High Voltage (SIMPROG, SIMON, RESETIN, CLKIN)	V_{IH}		VCC – 0.6			V
Input Low Voltage (SIMPROG, SIMON, RESETIN, CLKIN)	V_{IL}				0.6	V
DATAIO	V_{IL}	V_{OL} (I/O) = 0.4 V, I_{OL} (I/O) = 1 mA			0.230	V
		V_{OL} (I/O) = 0.4 V, I_{OL} (I/O) = 0 mA			0.335	V
	V_{IH}, V_{OH}	I_{IH}, I_{OH} = ±10 μA	VCC – 0.4			V
	I_{IL}	V_{IL} = 0 V			–0.9	mA
	V_{OL}	V_{IL} (I/O) = 0.4 V			0.420	V
DATAIO Pull-Up Resistance to VCC	R_{IN}		16	20	24	kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SIM INTERFACE						
VSIM = 5 V						
RST	V_{OL}	I = +200 µA			0.6	V
RST	V_{OH}	I = –20 µA	VSIM – 0.7			V
CLK	V_{OL}	I = +200 µA			0.5	V
CLK	V_{OH}	I = –20 µA	0.7 × VSIM			V
I/O	V_{IL}				0.4	V
I/O	V_{IH}, V_{OH}	I_{IH}, I_{OH} = ±20 µA	VSIM – 0.4			V
I/O	I_{IL}	V_{IL} = 0 V			–0.9	mA
I/O	V_{OL}	I_{OL} = +1 mA DATAIO ≤ 0.23 V			0.4	V
VSIM = 3 V						
RST	V_{OL}	I = +200 µA			0.2 × VSIM	V
RST	V_{OH}	I = –20 µA	0.8 × VSIM			V
CLK	V_{OL}	I = +20 µA			0.2 × VSIM	V
CLK	V_{OH}	I = –20 µA	0.7 × VSIM			V
I/O	V_{IL}				0.4	V
I/O	V_{IH}, V_{OH}	I_{IH}, I_{OH} = ±20 µA	VSIM – 0.4			V
I/O	I_{IL}	V_{IL}= 0 V			–0.9	mA
I/O	V_{OL}	I_{OL} = 1 mA DATAIO ≤ 0.23 V			0.4	V
I/O Pull-Up Resistance to VSIM	R_{IN}		8	10	12	kΩ
Max Frequency (CLK)	f_{MAX}	C_L = 30 pF	5			MHz
Prop Delay (CLK)	t_D			30	50	ns
Output Rise/Fall Times (CLK)	t_R, t_F	C_L = 30 pF		9	18	ns
Output Rise/Fall Times (I/O, RST)	t_R, t_F	C_L = 30 pF			1	µs
Duty Cycle (CLK)	D	D CLKIN = 50% f = 5 MHz	47		53	%
RESET GENERATOR (RESET)						
Output High Voltage	V_{OH}	I_{OH} = –15 µA	VCC – 0.3			V
Output Low Voltage	V_{OL}	I_{OL} = –15 µA			0.3	V
Delay Time Per Unit Capacitance Applied to RESCAP Pin	t_D		1.0			ms/nF

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]This feature is intended to protect against catastrophic failure of the device. Maximum allowed operating junction temperature is 125°C. Operation beyond 125°C could cause permanent damage to the device.

[3]Required for stability.

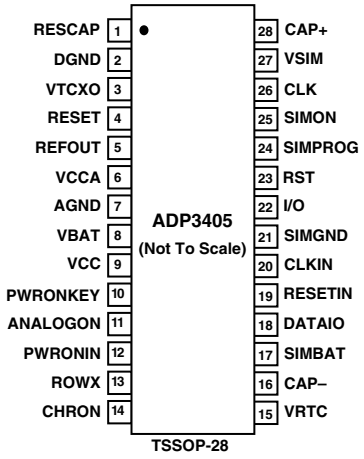
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin with Respect to Any GND Pin . . . . . –0.3 V, +10 V
Voltage on Any Pin May Not Exceed VBAT, with the Following Exceptions: VRTC, VSIM, CAP+, PWRONIN, I/O, CLK, RST
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –20°C to +85°C
Maximum Junction Temperature . . . . . 125°C
θ_{JA}, Thermal Impedance (TSSOP-28) . . 4-Layer Board 68°C/W
θ_{JA}, Thermal Impedance (TSSOP-28) . . 6-Layer Board 62°C/W
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*This is a stress rating only, operation beyond these limits can cause the device to be permanently damaged.

PIN CONFIGURATION



TSSOP-28

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3405ARU	–20°C to +85°C	28-Lead TSSOP	RU-28

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	RESCAP	Reset Delay Timing Cap
2	DGND	Digital Ground
3	VTCXO	Crystal Oscillator Low Dropout Regulator
4	RESET	Main Reset
5	REFOUT	Reference Output
6	VCCA	Analog Low Dropout Regulator
7	AGND	Analog Ground
8	VBAT	Battery Input Voltage
9	VCC	Digital Low Dropout Regulator
10	PWRONKEY	Power-On/-Off Key
11	ANALOGON	VTCXO Enable
12	PWRONIN	Power-On/-Off Signal from Microprocessor
13	ROWX	Microprocessor Keyboard Output
14	CHRON	Charger On/Off Input
15	VRTC	Real-Time Clock Supply/Coin Cell Battery Charger
16	CAP–	Negative Side of Boost Capacitor
17	SIMBAT	Battery Input for the SIM Charge Pump
18	DATAIO	Non-Level-Shifted Bidirectional Data I/O
19	RESETIN	Non-Level-Shifted SIM Reset
20	CLKIN	Non-Level-Shifted Clock
21	SIMGND	Charge Pump Ground
22	I/O	Level-Shifted Bidirectional SIM Data Input/Output
23	RST	Level-Shifted SIM Reset
24	SIMPROG	VSIM Programming: Low = 3 V, High = 5 V
25	SIMON	VSIM Enable
26	CLK	Level-Shifted SIM Clock
27	VSIM	SIM Supply
28	CAP+	Positive Side of Boost Capacitor

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3405 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table I. LDO Control Logic

Inputs					Outputs				
UVLO	**CHRON**	**PWRONKEY**	**PWRONIN**	**ANALOGON**	**VRTC**	**VCC**	**VCCA**	**REFOUT**	**VTCXO**
L	X	X	X	X	Off	Off	Off	Off	Off
H	**H**	X	X	X	On	On	On	On	On
H	X	**L**	X	X	On	On	On	On	On
H	L	H	L	X	On	Off	Off	Off	Off
H	L	H	**H**	L	On	On	Off	Off	Off
H	L	H	H	**H**	On	On	On	On	On

X = Don't care
Bold denotes the active control signal.

Table II. VSIM Control Logic

Inputs				Outputs
VCC	**RESET**	**SIMON**	**SIMPROG**	**VSIM**
Off	L	X	X	Off
On	L	X	X	Off
On	H	L	X	Off
On	H	H	L	3 V
On	H	H	H	5 V

X = Don't care

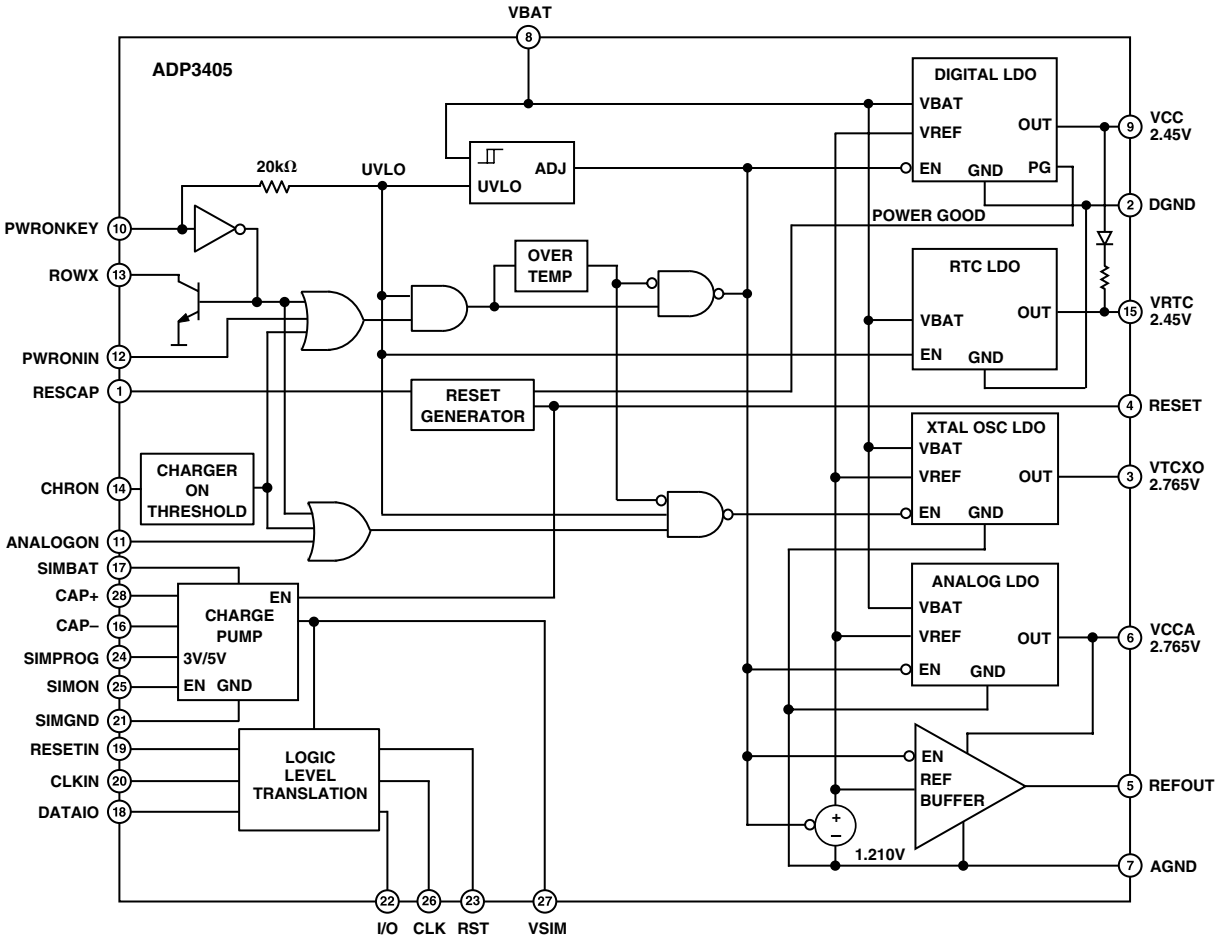
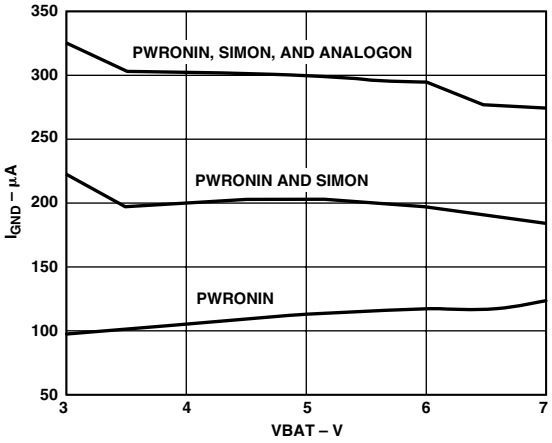
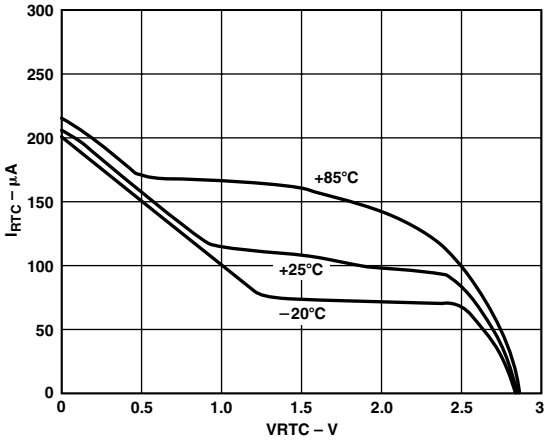


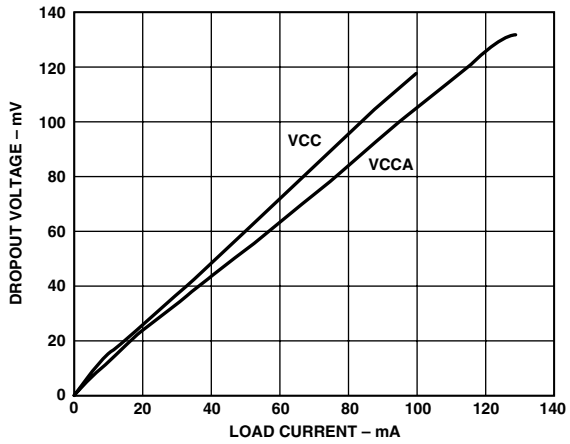
Figure 1. Functional Block Diagram



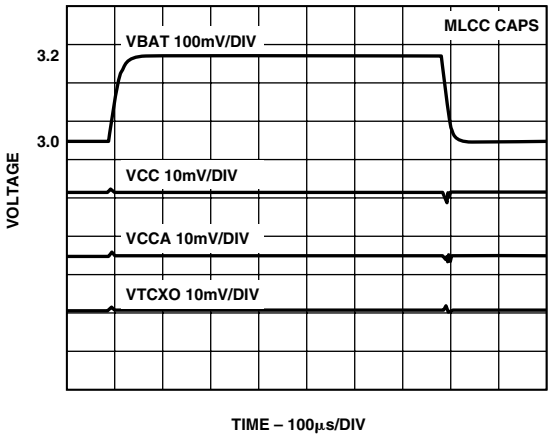
TPC 1. Ground Current vs. Battery Voltage



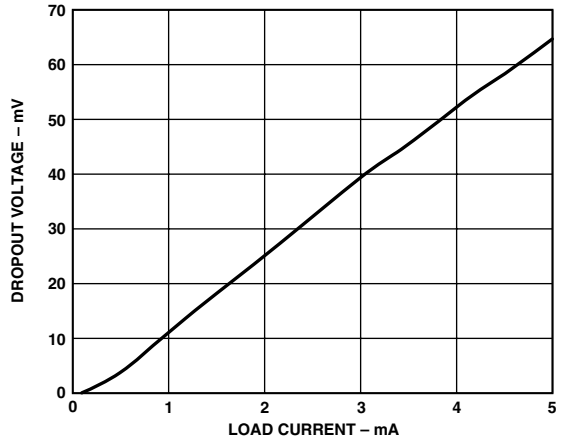
TPC 4. RTC I/V Characteristic



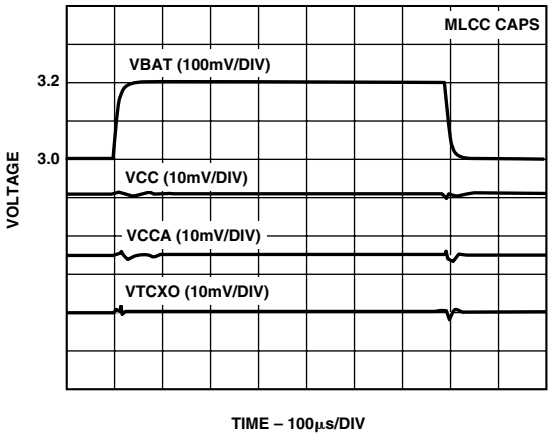
TPC 2. VCC, VCCA Dropout Voltage vs. Load Current



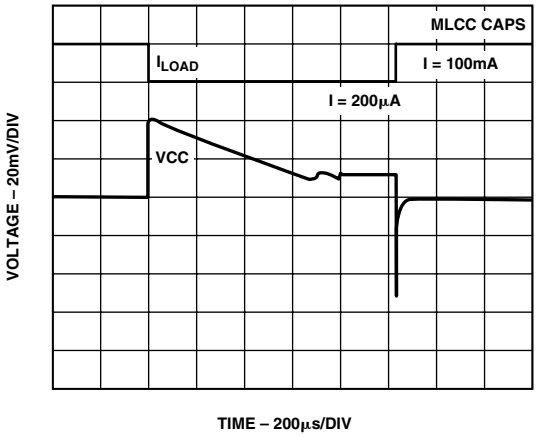
TPC 5. Line Transient Response, Maximum Loads



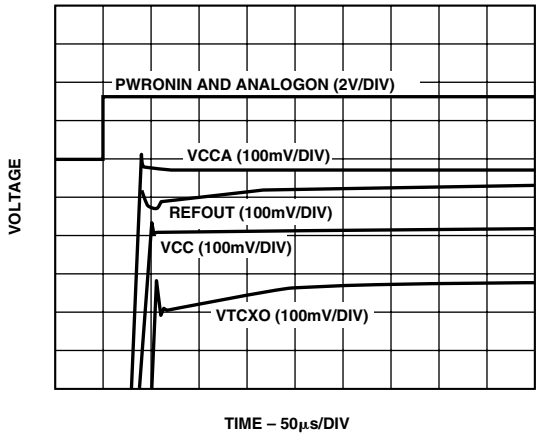
TPC 3. VTCXO Dropout Voltage vs. Load Current



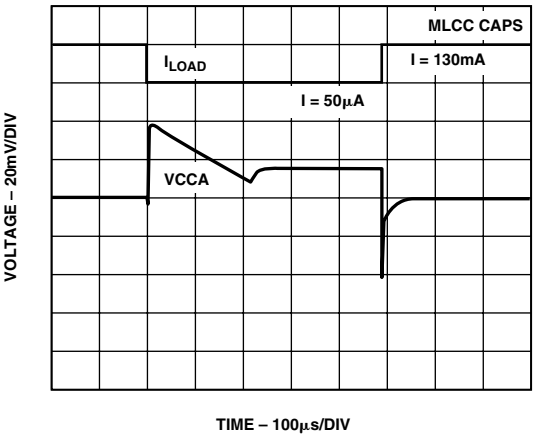
TPC 6. Line Transient Response, Minimum Loads



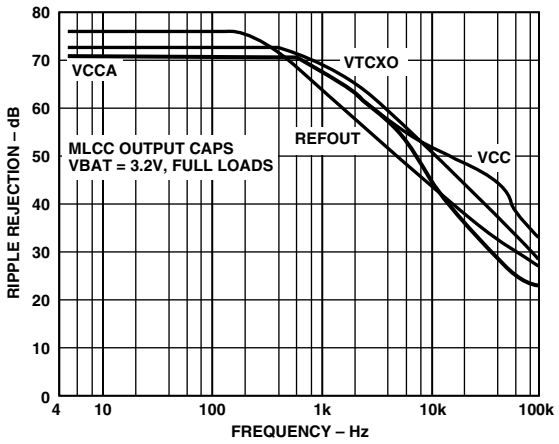
TPC 7. VCC Load Step



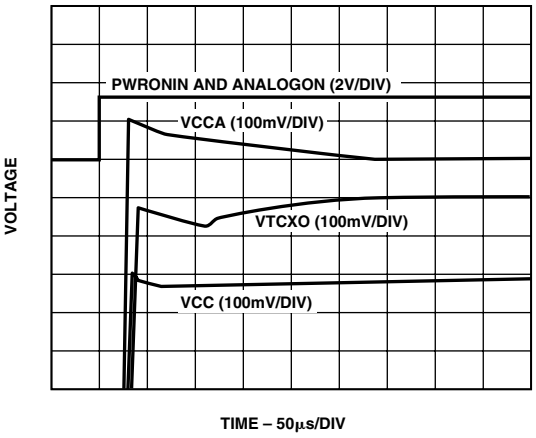
TPC 10. Turn-On Transients, Maximum Loads



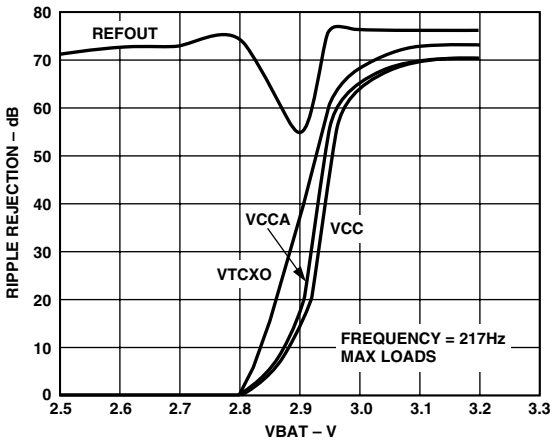
TPC 8. VCCA Load Step



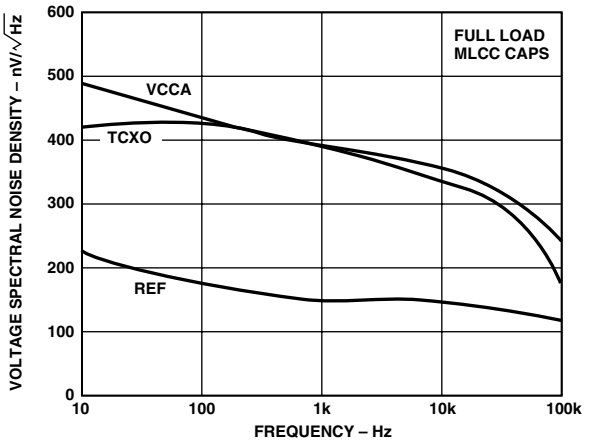
TPC 11. Ripple Rejection vs. Frequency



TPC 9. Turn-On Transients, Minimum Loads



TPC 12. Ripple Rejection vs. Battery Voltage



TPC 13. Output Noise Density

THEORY OF OPERATION

The ADP3405 is a power management chip optimized for use with the AD20msp425 GSM baseband chipsets in handset applications. Figure 1 shows a functional block diagram of the ADP3405.

The ADP3405 contains several blocks:

- Four Low Dropout Regulators (Digital, Analog, Crystal Oscillator, Real-Time Clock)
- Reset Generator
- Buffered Precision Reference
- SIM Interface Logic Level Translation (3 V/5 V)
- SIM Voltage Supply
- Power-On/-Off Logic
- Undervoltage Lockout

These functions have traditionally been done as either a discrete implementation or a custom ASIC design. ADP3405 combines the benefits of both worlds by providing an integrated standard product solution where every block is optimized to operate in a GSM environment while maintaining a cost-competitive solution.

Figure 2 shows the external circuitry associated with the ADP3405. Only a few support components, mainly decoupling capacitors, are required.

Input Voltage

The input voltage range for ADP3405 is 3 V to 7 V and optimized for a single Li-Ion cell or three NiMH/NiCd cells. The thermal impedance (θ_{JA}) of the ADP3405 is 62°C/W for 6-layer boards. The charging voltage for a high capacity NiMH cell can be as high as 5.5 V. Power dissipation should be calculated at maximum ambient temperatures and battery voltage in order not to exceed the 125°C maximum allowable junction temperature. Figure 3 shows the maximum total LDO output current as a function of ambient temperature and battery voltage.

However, high battery voltages normally occur only when the battery is being charged and the handset is not in conversation mode. In this mode there is a relatively light load on the LDOs. A fully charged Li-Ion battery is 4.25 V, where the LDOs deliver the maximum 240 mA up to the max 85°C ambient temperature.

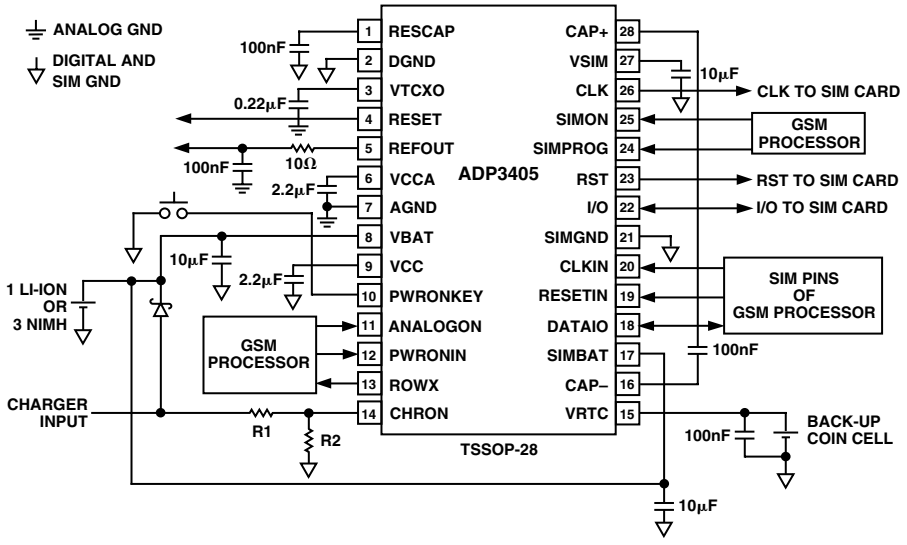


Figure 2. Typical Application Circuit

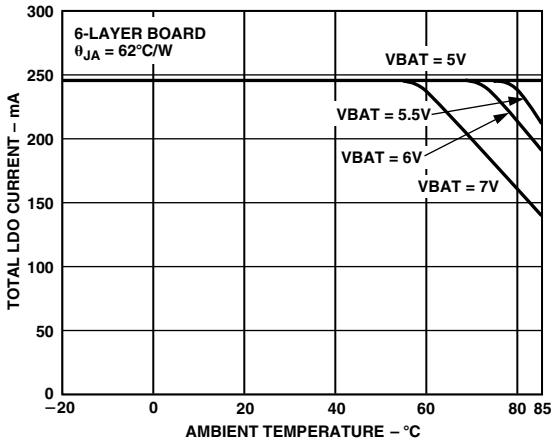


Figure 3. Total LDO Load Current vs. Temperature and VBAT

Low Dropout Regulators (LDOs)
The ADP3405 high-performance LDOs are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise. 2.2 µF tantalum or MLCC ceramic capacitors are recommended for use with the digital and analog LDOs, and 0.22 µF for the TCXO LDO.

Digital LDO (VCC)
The digital LDO (VCC) supplies all the digital circuitry in the handset (baseband processor, baseband converter, external memory, display, etc.). The LDO has been optimized for very low quiescent current (30 µA maximum) at light loads as this LDO is on at all times. This is due to both the structure of GSM and a new clocking scheme used in the AD20msp425. Figure 4 shows how the digital current varies as a function of time.

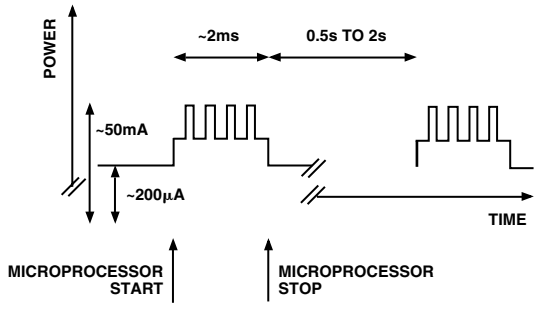


Figure 4. Digital Power as a Function of Time

Analog LDO (VCCA)
This LDO has the same features as the digital LDO. It has furthermore been optimized for good low frequency ripple rejection for use with analog sections in order to reject the ripple coming from the RF power amplifier. VCCA is rated to 130 mA load which is sufficient to supply the complete analog section of a baseband converter such as the AD6421/AD6425, including a 32 Ω earpiece. The analog LDO and the TCXO LDO can be controlled by ANALOGON.

TCXO LDO (VTCXO)
The TCXO LDO is intended as a supply for the temperature-compensated crystal oscillator, which needs its own ultralow noise supply. The output current is rated to 5 mA for the TCXO LDO.

RTC LDO (VRTC)
The RTC LDO charges a rechargable coin cell to run the real-time clock module. It has been targeted to charge Manganese Lithium batteries such as the ML series (ML621/ML1220) from Sanyo. The ML621 has a small physical size (6.8 mm diameter) and a nominal capacity of 2.5 mAh, which yields about 250 hours of backup time.

Figure 5 shows the use of VRTC with the Enhanced GSM Processor which is a part of the AD20msp425 chipset.

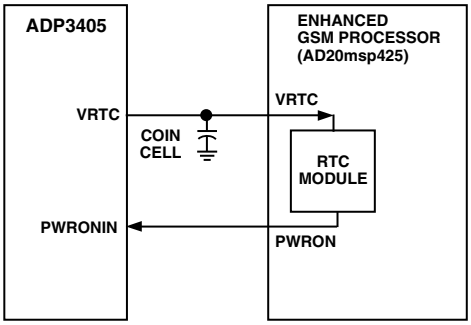


Figure 5. Connecting VRTC and PWRONIN to the AD20msp425 Chipset

The ADP3405 supplies current both for charging the coin cell and for the RTC module when the digital supply is off. The nominal charging voltage of 2.85 V ensures charging down to a main battery voltage of 3.0 V. The inherent current limit of VRTC ensures long cell life while the precise output voltage regulation charges the cell to more than 90% of its capacity. In addition, it features a very low quiescent current (10 µA) since this LDO is running all the time, even when the handset is switched off. It also has reverse current protection with low leakage which is needed when the main battery is removed and the coin cell supplies the RTC module.

The RTC module has a built-in alarm which, when it expires, will pull PWRONIN high, allowing an alarm function even if the handset is switched off.

Reference Output (REFOUT)
The reference output is a low-noise, high-precision reference with a guaranteed accuracy of 1.5% over temperature. The reference can be fed to the baseband converter, such as the AD6425, improving the absolute accuracy of the converters from 5% to 1.5%. This significantly reduces calibration time needed for the baseband converter during production.

SIM Interface
The SIM interface generates the needed SIM voltage—either 3 V or 5 V, dependent on SIM type, and also performs the needed logic level translation. Quiescent current is low, as the SIM card will be powered all the time. Note that DATAIO and I/O have integrated pull-up resistors as shown in Figure 6. See Table II for the control logic of the charge pump output, VSIM.

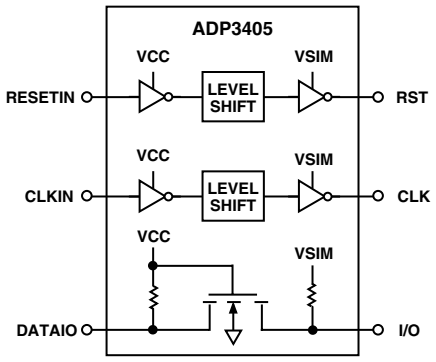


Figure 6. Schematic for Level Translators

Power-On/-Off

ADP3405 handles all issues regarding power-on/-off of the handset. It is possible to turn on the ADP3405 in three different ways:

- Pulling PWRONKEY low
- Pulling PWRONIN high
- CHRON exceeds threshold

Pulling PWRONKEY key low is the normal way of turning on the handset. This will turn on all the LDOs as long as PWRONKEY is held low. The microprocessor then starts and pulls PWRONIN high after which PWRONKEY can be released. PWRONIN going high will also turn on the handset. This is the case when the alarm in the RTC module expires.

An external charger can also turn on the phone. The turn-on threshold and hysteresis can be programmed via external resistors to allow full flexibility with any external charger and battery chemistry. These resistors are referred to as R1 and R2 in Figure 2.

Undervoltage Lockout (UVLO)

The UVLO function in the ADP3405 prevents startup when the initial voltage of the main battery is below the 3.0 V threshold. If the battery is this low with no load, there will be little or no capacity left. When the battery is greater than 3.0 V, as with the insertion of a fresh battery, the UVLO comparator trips, the RTC LDO is enabled, and the threshold is reduced to 2.9 V. This allows the handset to start normally until the battery voltage decays to 2.9 V open circuit. Once the 3.0 V threshold is exceeded, the RTC LDO is enabled. If, however, the backup coin cell is not connected, or is damaged or discharged below 1.5 V, the RTC LDO will not start on its own. In this situation, the RTC LDO will be started by enabling the VCC LDO.

Once the system is started, i.e., the phone is turned on and the VCC LDO is up and running, the UVLO function is entirely disabled. The ADP3405 is then allowed to run down to very low battery voltages, typically around 2 V. The battery voltage is normally monitored by the microprocessor and usually shuts the phone off at around 3.0 V.

If the phone is off, i.e., the VCC LDO is off, and the battery voltage drops below 2.9 V, the UVLO circuit disables startup and the RTC LDO. This is implemented with very low quiescent current, typically 3 μA, to protect the main battery against any damage. NiMH batteries can reverse polarity if the 3-cell battery voltage drops below 3.0 V and a current of more than about 40 μA continues to flow. Lithium ion batteries will lose their capacity, although the built-in safety circuits normally present in these cells will most likely prevent any damage.

RESET

ADP3405 contains reset circuitry that is active both at power-up and at power-down. RESET is held low at power-up. An internal power-good signal starts the reset delay. The delay is set by an external capacitor on RESCAP:

$$t_{RESET} = 1.0 \ \frac{ms}{nF} \times C_{RESCAP}$$

A 100 nF capacitor will produce a 100 ms reset time. At power-off, RESET will be kept low to prevent any spurious microprocessor starts. The current capability of RESET is low (a few hundred nA) when VCC is off, to minimize power consumption. Therefore, RESET should only be used to drive a single CMOS input. When VCC is on, RESET will drive about 15 μA.

Overtemperature Protection

The maximum die temperature for ADP3405 is 125°C. If the die temperature exceeds 160°C, the ADP3405 will disable all the LDOs except the RTC LDO, which has very limited current capabilities. The LDOs will not be re-enabled before the die temperature is below 125°C, regardless of the state of PWRONKEY, PWRONIN, and CHRON. This ensures that the handset will always power-off before the ADP3405 exceeds its absolute maximum thermal ratings.

APPLICATIONS INFORMATION

Input Capacitor Selection

For the input voltage, VBAT, of the ADP3405, a local bypass capacitor is recommended. Use a 5 μF to 10 μF, low ESR capacitor. Multilayer ceramic chip capacitors provide the best combination of low ESR and small size, but may not be cost-effective. A lower cost alternative may be to use a 5 μF to 10 μF tantalum capacitor with a small (1 μF to 2 μF) ceramic in parallel.

LDO Capacitor Selection

The performance of any LDO is a function of the output capacitor. The digital and analog LDOs require a 2.2 μF capacitor and the TCXO LDO requires a 0.22 μF capacitor. Larger values may be used, but the overshoot at startup will increase slightly. If a larger output capacitor is desired, be sure to check that the overshoot and settling time are acceptable for the application.

All the LDOs are stable with a wide range of capacitor types and ESR due to Analog Devices' anyCAP technology. The ADP3405 is stable with extremely low ESR capacitors (ESR ~ 0), such as multilayer ceramic capacitors, but care should be taken in their selection. Note that the capacitance of some capacitor types shows wide variations over temperature or with dc voltage. A good quality dielectric, X7R or better, is recommended.

The RTC LDO has a rechargeable coin cell or an electric double-layer capacitor as a load, but an additional 0.1 μF ceramic capacitor is recommended for stability and best performance.

Charge Pump Capacitor Selection

For the input (SIMBAT) and output (VSIM) of the SIM charge pump, use 10 μF low ESR capacitors. The use of low ESR capacitors improves the noise and efficiency of the SIM charge pump. Multilayer ceramic chip capacitors provide the best combination of low ESR and small size but may not be cost-effective. A lower cost alternative may be to use a 10 μF tantalum capacitor with a small (1 μF to 2 μF) ceramic capacitor in parallel.

For the lowest ripple and best efficiency, use a 0.1 µF, ceramic capacitor for the charge pump flying capacitor (CAP+ and CAP–). A good quality dielectric, such as X7R is recommended.

Setting the Charger Turn-On Threshold

The ADP3405 can be turned on when the charger input exceeds a programmable threshold voltage. The charger's threshold and hysteresis are set by selecting the values for R1 and R2 shown in Figure 2.

The turn-on threshold for the charger is calculated using:

$$V_{CHR} = \left[\left(\frac{R2 + R_{HYS}}{R2 \times R_{HYS}} \times R1\right) + 1\right] \times V_T$$

Where V_T is the CHRON threshold voltage and R_{HYS} is the CHRON hysteresis resistance.

The hysteresis is determined using:

$$V_{HYS} = \frac{V_T}{R_{HYS}} \times R1$$

Combining the above equations and solving for $R1$ and $R2$ gives the following formulas:

$$R1 = \frac{R_{HYS}}{V_T} \times V_{HYS}$$

$$R2 = \frac{R1 \times R_{HYS}}{\left(\frac{V_{CHR}}{V_T} - 1\right) \times R_{HYS} - R1}$$

Example: $R1$ = 10 kΩ and $R2$ = 30.2 kΩ gives a charger threshold (not counting the drop in the power Schottky diode) of 3.5 V ± 160 mV with a 200 mV ± 30 mV hysteresis.

Charger Diode Selection

The diode shown in Figure 2 is used to prevent the battery from discharging into the charger turn-on setting resistors, R1 and R2. A Schottky diode is recommended to minimize the voltage difference from the charger to the battery and the power dissipation. Choose a diode with a current rating high enough to handle both the battery charging current and the current the ADP3405 will draw if powered up during charging. The battery charging current is dependent on the battery chemistry and the charger circuit. The ADP3405 current will be dependent on the loading.

Printed Circuit Board Layout Considerations

Use the following general guidelines when designing printed circuit boards:

1. Split the battery connection to the VBAT and SIMBAT pins of the ADP3405. Use separate traces for each connection and locate the input capacitors as close to the pins as possible.
2. SIM input and output capacitors should be returned to the SIMGND and kept as close as possible to the ADP3405 to minimize noise. Traces to the SIM charge pump capacitor should be kept as short as possible to minimize noise.
3. VCCA and VTCXO capacitors should be returned to AGND.
4. VCC and VRTC capacitors should be returned to DGND.
5. Split the ground connections. Use separate traces or planes for the analog, digital, and power grounds, and tie them together at a single point, preferably close to the battery return.

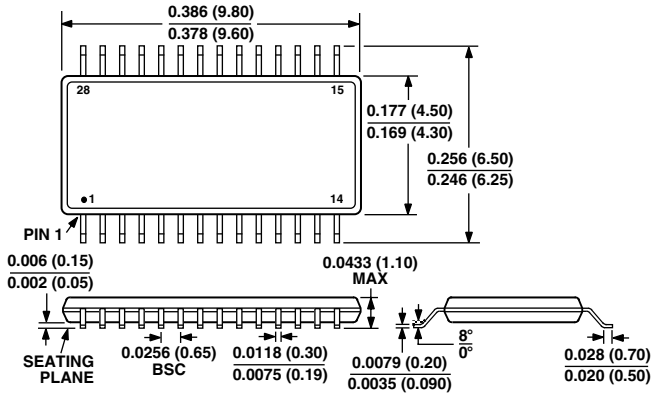
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OUTLINE DIMENSIONS

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