74ALVCH16841

20-bit bus interface D-type latch; 3-state

Rev. 3 — 12 September 2018 Product data sheet

1. General description

The 74ALVCH16841 has two 10-bit D-type latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable (nLE) and output enable ($n\overline{OE}$) control gates.

When $n\overline{OE}$ is LOW, the data in the registers appears at the outputs. When $n\overline{OE}$ is HIGH the outputs are in High-impedance OFF state. Operation of the $n\overline{OE}$ input does not affect the state of the flip-flops.

The 74ALVCH16841 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range of 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ±24 mA at V_{CC} = 3.0 V
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimize noise and ground bounce
- All data inputs have bushold
- Output drive capability 50 Ω transmission lines at 85 °C
- 3-state non-inverting outputs for bus oriented applications
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH16841DGG	−40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

nexperia

4. Functional diagram

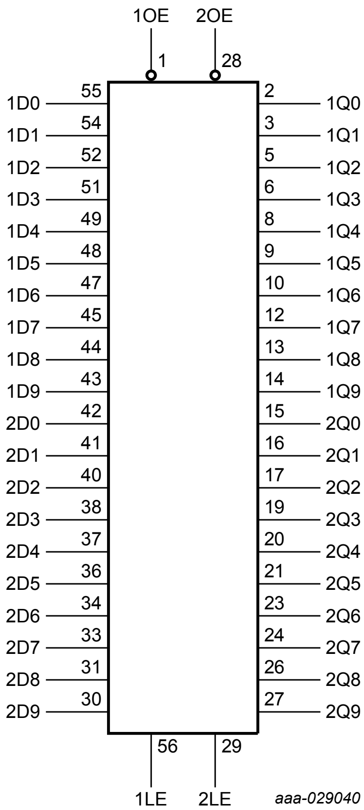


Fig. 1. Logic symbol

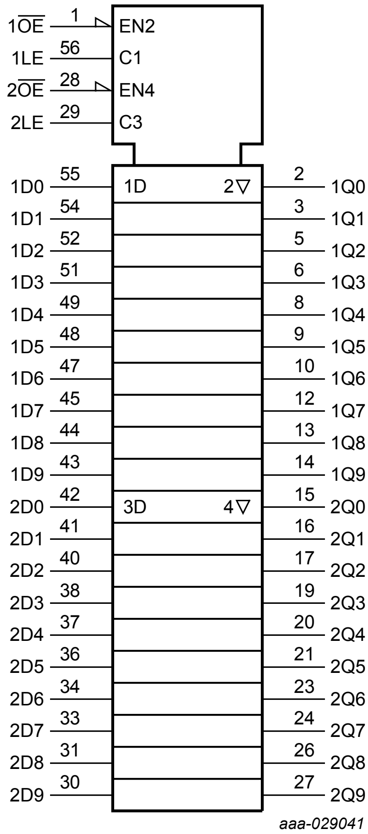


Fig. 2. IEC logic symbol

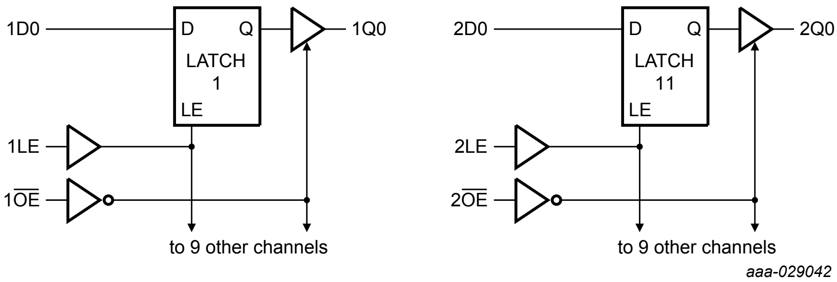


Fig. 3. Logic diagram

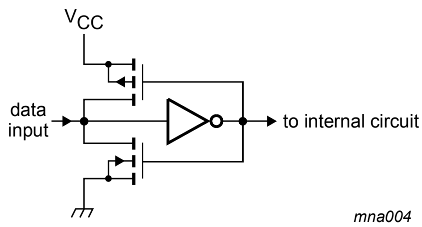


Fig. 4. Bushold circuit

5. Pinning information

5.1. Pinning

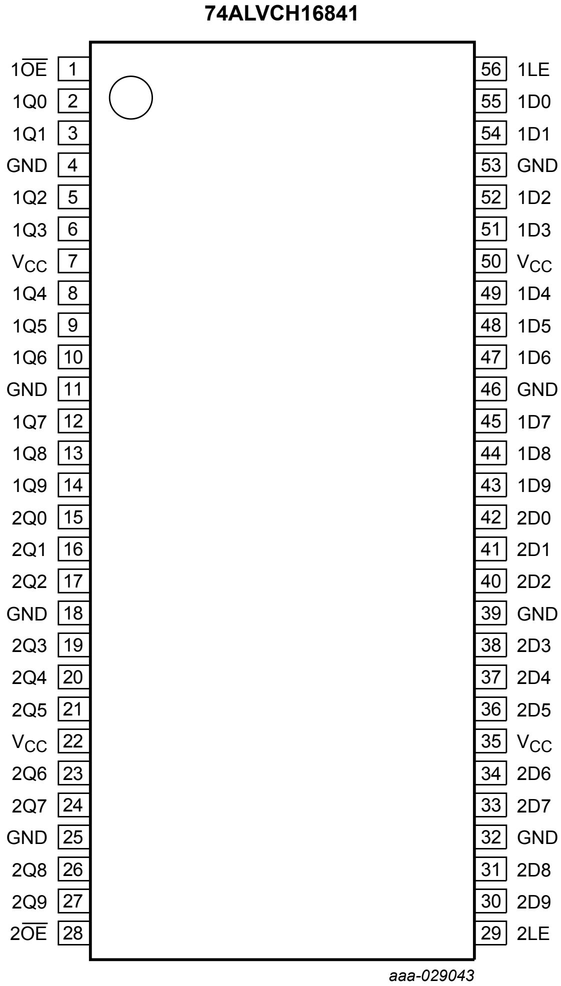


Fig. 5. Pin configuration SOT364-1 (TSSOP56)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8, 1D9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data input
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8, 2D9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data input
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8, 1Q9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data output
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8, 2Q9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data output
1$\overline{OE}$, 2$\overline{OE}$	1, 28	output enable inputs (active-LOW)
1LE, 2LE	56, 29	latch enable inputs
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V_{CC}	7, 22, 35, 50	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs			Outputs
$n\overline{OE}$	nLE	nDn	nQn
L	H	L	L
L	H	H	H
L	L	X	Q_0
H	X	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	For control pins	[1]	-0.5	+4.6	V
		For data inputs	[1]	-0.5	V_{CC} + 0.5	V
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	[2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	for maximum speed performance; 30 pF output load	2.3	2.7	V
		for maximum speed performance; 50 pF output load	3.0	3.6	V
V_I	input voltage		0	V_{CC}	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = -40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = -100 μA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	V_{CC} - 0.6	V_{CC} - 0.09	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 μA; V_{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.40	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.70	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	V
I_I	input leakage current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ or GND	-	0.1	5	μA
I_{OZ}	OFF-state output current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	-	0.1	10	μA
I_{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.2	40	μA
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ - 0.6 V; I_O = 0 A	-	150	750	μA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V	45	-	-	μA
		V_{CC} = 3.0 V; V_I = 0.8 V	75	150	-	μA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V	-45	-	-	μA
		V_{CC} = 3.0 V; V_I = 2.0 V	-75	-175	-	μA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V	500	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V	-500	-	-	μA
C_I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10; T_{amb} = -40 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{pd}	propagation delay	nDn to nQn; see Fig. 6	[2]				
		V_{CC} = 2.3 V to 2.7 V		1.0	2.5	5.0	ns
		V_{CC} = 2.7 V		1.0	2.6	4.7	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.4	3.9	ns
		nLE to nQn; see Fig. 7					
		V_{CC} = 2.3 V to 2.7 V		1.0	2.5	5.6	ns
		V_{CC} = 2.7 V		1.0	2.6	5.1	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.4	4.3	ns
t_{en}	enable time	n$\overline{OE}$ to nQn; see Fig. 9	[3]				
		V_{CC} = 2.3 V to 2.7 V		1.0	2.7	6.2	ns
		V_{CC} = 2.7 V		1.0	3.1	6.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.3	4.9	ns
t_{dis}	disable time	n$\overline{OE}$ to nQn; see Fig. 9	[4]				
		V_{CC} = 2.3 V to 2.7 V		1.1	2.2	5.3	ns
		V_{CC} = 2.7 V		1.3	3.1	4.3	ns
		V_{CC} = 3.0 V to 3.6 V		1.3	2.9	4.1	ns
t_{su}	set-up time	nDn to nLE; see Fig. 8					
		V_{CC} = 2.3 V to 2.7 V		1.3	0.1	-	ns
		V_{CC} = 2.7 V		1.1	0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	0.6	-	ns
t_h	hold time	nDn to nLE; see Fig. 8					
		V_{CC} = 2.3 V to 2.7 V		1.4	0.3	-	ns
		V_{CC} = 2.7 V		1.7	0.2	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.4	0.2	-	ns
t_W	pulse width	nLE HIGH; V_{CC} = 2.3 V to 3.6 V; see Fig. 7		3.3	1.5	-	ns
C_{PD}	power dissipation capacitance	per latch; V_I = GND to V_{CC}	[5]				
		outputs enabled		-	19	-	pF
		outputs disabled		-	3	-	pF

[1] Typical values are measured at T_{amb} = 25 °C
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

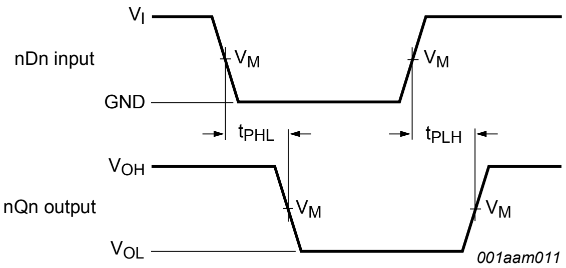
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

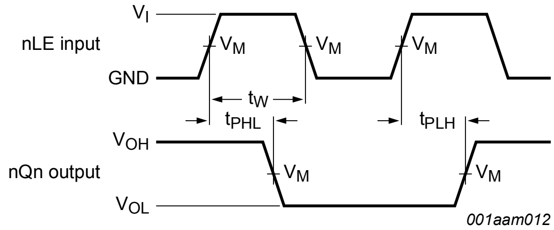
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

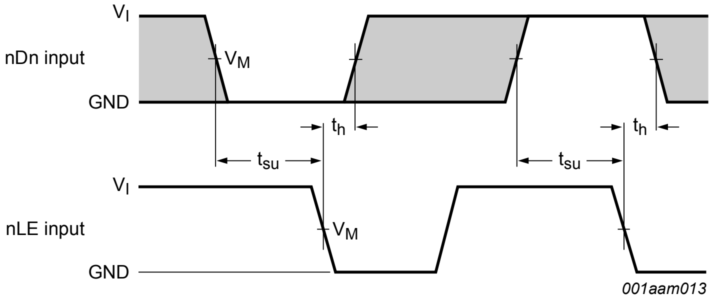
Fig. 6. Input (nDn) to output (nQn) propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

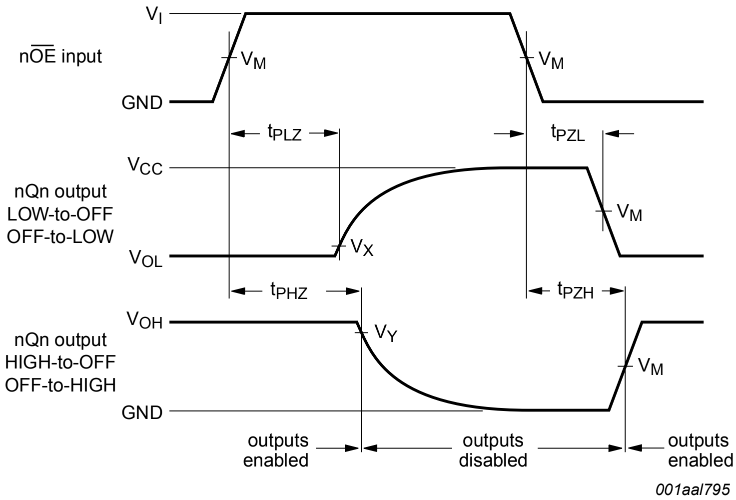
Fig. 7. Latch enable input (nLE) to data output (nQn) propagation delays and pulse width (nLE)



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 8. Data setup and hold times for input (nDn) to input (nLE)



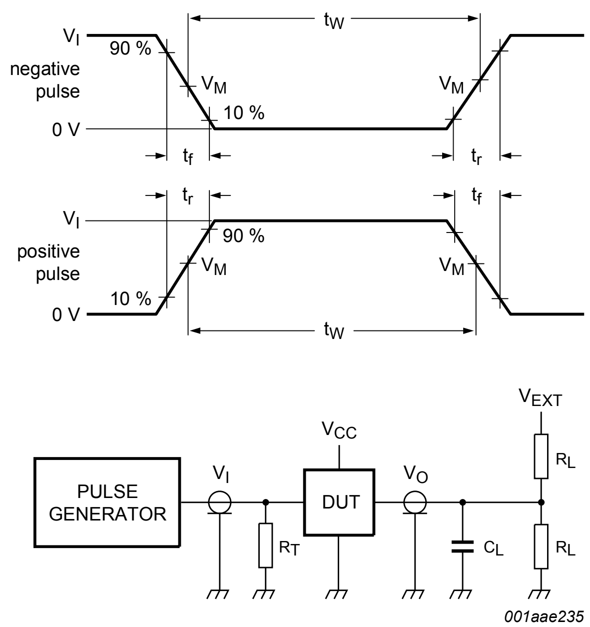
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 9. 3-State enable and disable times

Table 8. Measurement points

Input			Output		
V_{CC}	V_I	V_M	V_M	V_x	V_y
< 2.3 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

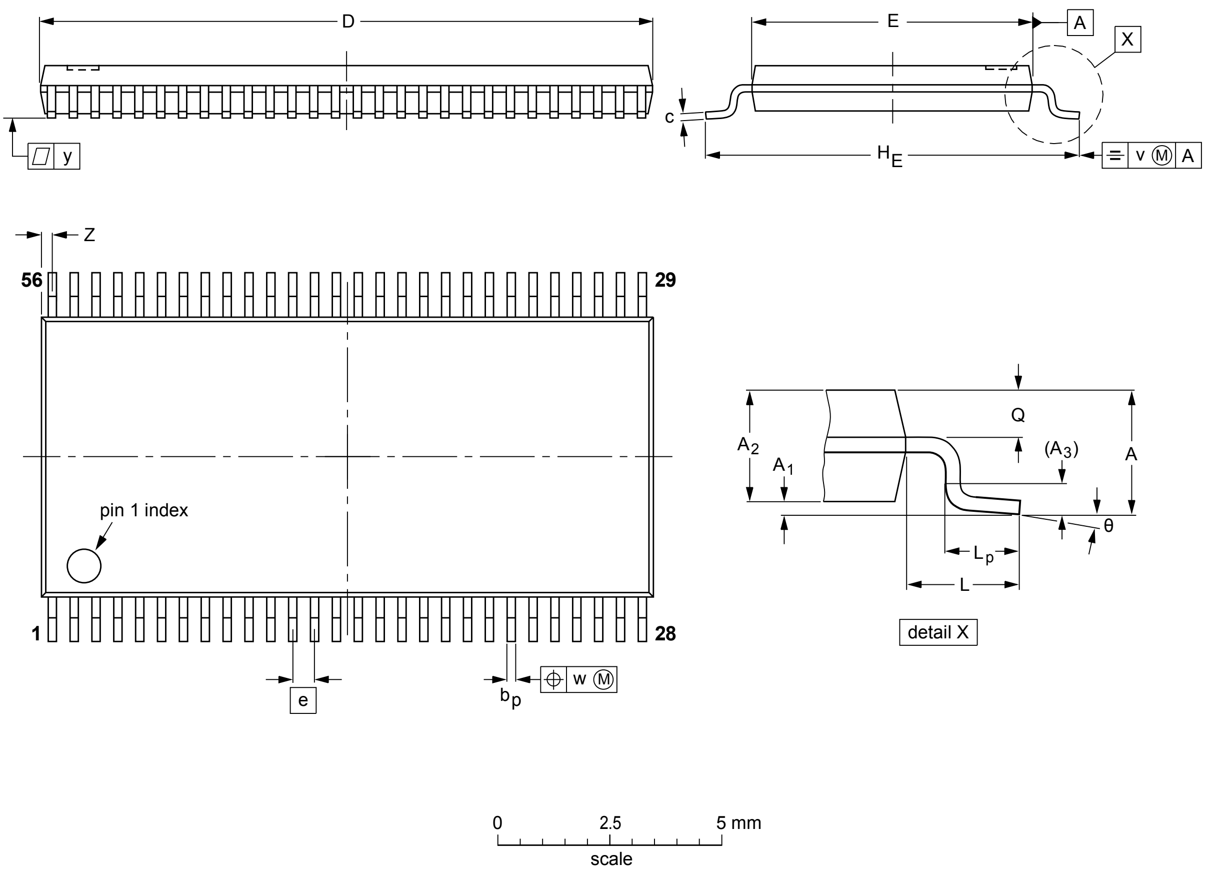
Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Input			Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
< 2.3 V	V_{CC}	≤ 2.0 ns	500 Ω	30 pF	GND	2 × V_{CC}	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	500 Ω	30 pF	GND	2 × V_{CC}	open
2.7 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V_{CC}	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V_{CC}	open

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 11. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16841 v.3	20180912	Product data sheet	-	74ALVCH16841 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ALVCH16841 v.2	19980727	Product specification	-	74ALVCH16841 v.1
74ALVCH16841 v.1	19980727	Product specification	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

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- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
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«JONHON» (основан в 1970 г.)

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