8-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with PGA and Reference

Data Sheet **AD7124-8**

FEATURES

- 3 power modes
- RMS noise
  - Low power: 24 nV rms at 1.17 SPS, gain = 128 (255 µA typical)
  - Mid power: 20 nV rms at 2.34 SPS, gain = 128 (355 µA typical)
  - Full power: 23 nV rms at 9.4 SPS, gain = 128 (930 µA typical)
- Up to 22 noise free bits in all power modes (gain = 1)
- Output data rate
  - Full power: 9.38 SPS to 19,200 SPS
  - Mid power: 2.34 SPS to 4800 SPS
  - Low power: 1.17 SPS to 2400 SPS
- Rail-to-rail analog inputs for gains > 1
- Simultaneous 50 Hz/60 Hz rejection at 25 SPS (single cycle settling)
- Diagnostic functions (which aid safe integrity level (SIL) certification)
- Crosspoint multiplexed analog inputs
  - 8 differential/15 pseudo differential inputs
- Programmable gain (1 to 128)
- Band gap reference with 15 ppm/°C drift maximum (65 µA)
- Matched programmable excitation currents
- Internal clock oscillator
- On-chip bias voltage generator
- Low-side power switch
- General-purpose outputs
- Multiple filter options
- Internal temperature sensor
- Self and system calibration
- Sensor burnout detection
- Automatic channel sequencer
- Per channel configuration
- Power supply: 2.7 V to 3.6 V and ±1.8 V
- Independent interface power supply
- Power-down current: 5 µA maximum
- Temperature range: −40°C to +105°C
- 32-lead LFCSP
- 3-wire or 4-wire serial interface
  - SPI, QSPI™, MICROWIRE™, and DSP compatible
  - Schmitt trigger on SCLK
- ESD: 4 kV

APPLICATIONS

- Temperature measurement
- Pressure measurement
- Industrial process control
- Instrumentation
- Smart transmitters

FUNCTIONAL BLOCK DIAGRAM

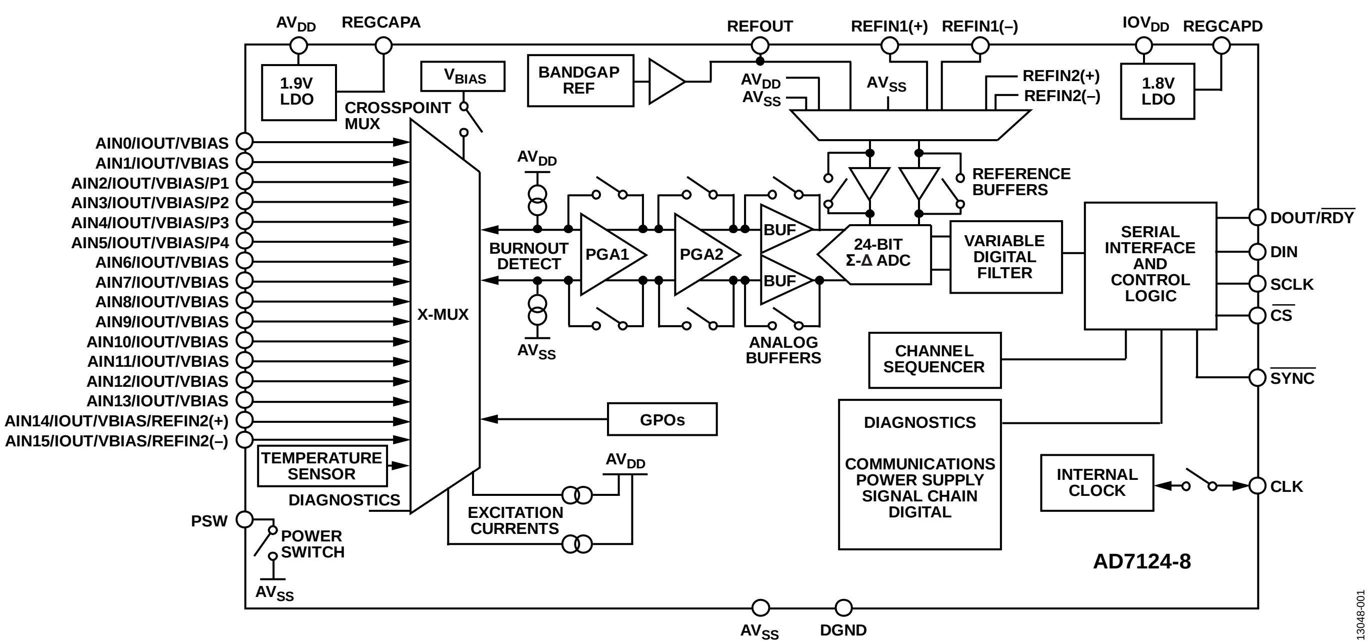

Figure 1.

Rev. B [Document Feedback]

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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GENERAL DESCRIPTION

The AD7124-8 is a low power, low noise, completely integrated analog front end for high precision measurement applications. The device contains a low noise, 24-bit Σ-Δ analog-to-digital converter (ADC), and can be configured to have 8 differential inputs or 15 single-ended or pseudo differential inputs. The on-chip low gain stage ensures that signals of small amplitude can be interfaced directly to the ADC.

One of the major advantages of the AD7124-8 is that it gives the user the flexibility to employ one of three integrated power modes. The current consumption, range of output data rates, and rms noise can be tailored with the power mode selected. The device also offers a multitude of filter options, ensuring that the user has the highest degree of flexibility.

The AD7124-8 can achieve simultaneous 50 Hz and 60 Hz rejection when operating at an output data rate of 25 SPS (single cycle settling), with rejection in excess of 80 dB achieved at lower output data rates.

The AD7124-8 establishes the highest degree of signal chain integration. The device contains a precision, low noise, low drift internal band gap reference and accepts an external differential reference, which can be internally buffered. Other key integrated features include programmable low drift excitation current sources, burnout currents, and a bias voltage generator, which sets the common-mode voltage of a channel to $AV_{DD}/2$. The low-side power switch enables the user to power down bridge sensors between conversions, ensuring the absolute minimal power consumption of the system. The device also allows the user the option of operating with either an internal clock or an external clock.

The integrated channel sequencer allows several channels to be enabled simultaneously, and the AD7124-8 sequentially converts on each enabled channel, simplifying communication with the device. As many as 16 channels can be enabled at any time, a channel being defined as an analog input or a diagnostic such as a power supply check or a reference check. This unique feature allows diagnostics to be interleaved with conversions. The AD7124-8 also supports per channel configuration. The device allows eight configurations or setups. Each configuration consists of gain, filter type, output data rate, buffering, and reference source. The user can assign any of these setups on a channel by channel basis.

The AD7124-8 also has extensive diagnostic functionality integrated as part of its comprehensive feature set. These diagnostics include a cyclic redundancy check (CRC), signal chain checks, and serial interface checks, which lead to a more robust solution. These diagnostics reduce the need for external components to implement diagnostics, resulting in reduced board space needs, reduced design cycle times, and cost savings. The failure modes effects and diagnostic analysis (FMEDA) of a typical application has shown a safe failure fraction (SFF) greater than 90% according to IEC 61508.

The device operates with a single analog power supply from 2.7 V to 3.6 V or a dual 1.8 V power supply. The digital supply has a range of 1.65 V to 3.6 V. It is specified for a temperature range of −40°C to +105°C. The AD7124-8 is housed in a 32-lead LFCSP package.

Note that, throughout this data sheet, multifunction pins, such as DOUT/$\overline{\text{RDY}}$, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{\text{RDY}}$, when only that function is relevant.

Table 1. AD7124-8 Overview

Parameter	Low Power Mode	Mid Power Mode	Full Power Mode
Maximum Output Data Rate	2400 SPS	4800 SPS	19,200 SPS
RMS Noise (Gain = 128)	24 nV	20 nV	23 nV
Peak-to-Peak Resolution at 1200 SPS (Gain = 1)	16.4 bits	17.1 bits	18 bits
Typical Current (ADC + PGA)	255 µA	355 µA	930 µA

SPECIFICATIONS

AV_{DD} = 2.9 V to 3.6 V (full power mode), 2.7 V to 3.6 V (mid and low power mode), IOV_{DD} = 1.65 V to 3.6 V, AV_{SS} = DGND = 0 V, REFINx(+) = 2.5 V, REFINx(−) = AV_{SS}, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
Output Data Rate, f_{ADC}					
Low Power Mode	1.17		2400	SPS	
Mid Power Mode	2.34		4800	SPS	
Full Power Mode	9.38		19,200	SPS	
No Missing Codes[2]	24			Bits	FS[3] > 2, $sinc^4$ filter
	24			Bits	FS[3] > 8, $sinc^3$ filter
Resolution					See the RMS Noise and Resolution section
RMS Noise and Update Rates					See the RMS Noise and Resolution section
Integral Nonlinearity (INL)					
Low Power Mode[2]	−4	±1	+4	ppm of FSR	Gain = 1
	−15	±2	+15	ppm of FSR	Gain > 1, T_A = −40°C to +85°C
	−20	±2	+20	ppm of FSR	Gain > 1, T_A = −40°C to +105°C
Mid Power Mode[2]	−4	±1	+4	ppm of FSR	Gain = 1
	−15	±2	+15	ppm of FSR	Gain > 1
Full Power Mode	−4	±1	+4	ppm of FSR	Gain = 1[2]
	−15	±2	+15	ppm of FSR	Gain > 1
Offset Error[4]					
Before Calibration		±15		µV	Gain = 1 to 8
		200/gain		µV	Gain = 16 to 128
After Internal Calibration/System Calibration		In order of noise			
Offset Error Drift vs. Temperature[5]					
Low Power Mode		10		nV/°C	Gain = 1 or gain > 16
		80		nV/°C	Gain = 2 to 8
		40		nV/°C	Gain = 16
Mid Power Mode		10		nV/°C	Gain = 1 or gain > 16
		40		nV/°C	Gain = 2 to 8
		20		nV/°C	Gain = 16
Full Power Mode		10		nV/°C	
Gain Error[4, 6]					
Before Internal Calibration	−0.0025		+0.0025	%	Gain = 1, T_A = 25°C
		−0.3		%	Gain > 1
After Internal Calibration	−0.016	+0.004	+0.016	%	Gain = 2 to 8, T_A = 25°C
		±0.025		%	Gain = 16 to 128
After System Calibration		In order of noise			
Gain Error Drift vs. Temperature		1	2	ppm/°C	
Power Supply Rejection					A_{IN} = 1 V/gain, external reference
Low Power Mode	84			dB	Gain = 2 to 16
	91			dB	Gain = 1 or gain > 16
Mid Power Mode[2]	89			dB	Gain = 2 to 16
	95			dB	Gain = 1 or gain > 16
Full Power Mode	96			dB	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Common-Mode Rejection[7]					
At DC[2]	85	90		dB	A_{IN} = 1 V, gain = 1
At DC	100	105		dB	A_{IN} = 1 V/gain, gain 2 or 4
	110	115		dB	A_{IN} = 1 V/gain, gain ≥ 8
$Sinc^3$, $Sinc^4$ Filter[2]					
At 50 Hz, 60 Hz	120			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	120			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	120			dB	60 SPS, 60 Hz ± 1 Hz
Fast Settling Filters[2]					
At 50 Hz	115			dB	First notch at 50 Hz, 50 Hz ± 1 Hz
At 60 Hz	115			dB	First notch at 60 Hz, 60 Hz ± 1 Hz
Post Filters[2]					
At 50 Hz, 60 Hz	130			dB	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	130			dB	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
Normal Mode Rejection[2]					
$Sinc^4$ Filter					
External Clock					
At 50 Hz, 60 Hz	120			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	82			dB	50 SPS, REJ60[8]=1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	120			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	120			dB	60 SPS, 60 Hz ± 1 Hz
Internal Clock					
At 50 Hz, 60 Hz	98			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	66			dB	50 SPS, REJ60[8] = 1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	92			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	92			dB	60 SPS, 60 Hz ± 1 Hz
$Sinc^3$ Filter					
External Clock					
At 50 Hz, 60 Hz	100			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	66			dB	50 SPS, REJ60[8] = 1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	100			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	100			dB	60 SPS, 60 Hz ± 1 Hz
Internal Clock					
At 50 Hz, 60 Hz	73			dB	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	52			dB	50 SPS, REJ60[8] = 1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
At 50 Hz	68			dB	50 SPS, 50 Hz ± 1 Hz
At 60 Hz	68			dB	60 SPS, 60 Hz ± 1 Hz
Fast Settling Filters					
External Clock					
At 50 Hz	40			dB	First notch at 50 Hz, 50 Hz ± 0.5 Hz
At 60 Hz	40			dB	First notch at 60 Hz, 60 Hz ± 0.5 Hz
Internal Clock					
At 50 Hz	24.5			dB	First notch at 50 Hz, 50 Hz ± 0.5 Hz
At 60 Hz	24.5			dB	First notch at 60 Hz, 60 Hz ± 0.5 Hz
Post Filters					
External Clock					
At 50 Hz, 60 Hz	86			dB	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	62			dB	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
Internal Clock					
At 50 Hz, 60 Hz	67			dB	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	50			dB	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS[9]					
Differential Input Voltage Ranges[10]		$\pm V_{REF}$/gain		V	V_{REF} = REFINx(+) − REFINx(−), or internal reference
Absolute A_{IN} Voltage Limits[2]					
Gain = 1 (Unbuffered)	AV_{SS} − 0.05		AV_{DD} + 0.05	V	
Gain = 1 (Buffered)	AV_{SS} + 0.1		AV_{DD} − 0.1	V	
Gain > 1	AV_{SS} − 0.05		AV_{DD} + 0.05	V	
Analog Input Current					
Gain > 1 or Gain = 1 (Buffered)					
Low Power Mode					
Absolute Input Current		±1		nA	
Differential Input Current		±0.2		nA	
Analog Input Current Drift		25		pA/°C	
Mid Power Mode					
Absolute Input Current		±1.2		nA	
Differential Input Current		±0.4		nA	
Analog Input Current Drift		25		pA/°C	
Full Power Mode					
Absolute Input Current		±3.3		nA	
Differential Input Current		±1.5		nA	
Analog Input Current Drift		25		pA/°C	
Gain = 1 (Unbuffered)					Current varies with input voltage
Absolute Input Current		±2.65		µA/V	
Analog Input Current Drift		1.1		nA/V/°C	
REFERENCE INPUT					
Internal Reference					
Initial Accuracy	2.5 − 0.2%	2.5	2.5 + 0.2%	V	T_A = 25°C
Drift		2	8	ppm/°C	T_A = 25°C to 105°C
		2	15	ppm/°C	T_A = −40°C to +105°C
Output Current			10	mA	
Load Regulation		50		µV/mA	
Power Supply Rejection		85		dB	
External Reference					
External REFIN Voltage[2]	1	2.5	AV_{DD}	V	REFIN = REFINx(+) − REFINx(−)
Absolute REFIN Voltage Limits[2]	AV_{SS} − 0.05		AV_{DD} + 0.05	V	Unbuffered
	AV_{SS} + 0.1		AV_{DD} − 0.1	V	Buffered
Reference Input Current					
Buffered					
Low Power Mode					
Absolute Input Current		±0.5		nA	
Reference Input Current Drift		10		pA/°C	
Mid Power Mode					
Absolute Input Current		±1		nA	
Reference Input Current Drift		10		pA/°C	
Full Power Mode					
Absolute Input Current		±3		nA	
Reference Input Current Drift		10		pA/°C	
Unbuffered					
Absolute Input Current		±12		µA	
Reference Input Current Drift		6		nA/°C	
Normal Mode Rejection					Same as for analog inputs
Common-Mode Rejection		100		dB	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
EXCITATION CURRENT SOURCES (IOUT0/IOUT1)					Available on any analog input pin
Output Current		50/100/250/ 500/750/1000		µA	
Initial Tolerance		±4		%	T_A = 25°C
Drift		50		ppm/°C	
Current Matching		±0.5		%	Matching between IOUT0 and IOUT1, V_{OUT} = 0 V
Drift Matching		5	30	ppm/°C	
Line Regulation (AV_{DD})		2		%/V	AV_{DD} = 3 V ± 5%
Load Regulation		0.2		%/V	
Output Compliance[2]	AV_{SS} − 0.05		AV_{DD} − 0.37	V	50 µA/100 µA/250 µA/500 µA current sources, 2% accuracy
	AV_{SS} − 0.05		AV_{DD} − 0.48	V	750 µA and 1000 µA current sources, 2% accuracy
BIAS VOLTAGE (V_{BIAS}) GENERATOR					Available on any analog input pin
V_{BIAS}		AV_{SS} + (AV_{DD} − AV_{SS})/2		V	
V_{BIAS} Generator Start-Up Time		6.7		µs/nF	Dependent on the capacitance connected to AIN
TEMPERATURE SENSOR					
Accuracy		±0.5		°C	
Sensitivity		13,584		codes/°C	
LOW-SIDE POWER SWITCH					
On Resistance (R_{ON})		7	10	Ω	
Allowable Current[2]			30	mA	Continuous current
BURNOUT CURRENTS					
A_{IN} Current		0.5/2/4		µA	Analog inputs must be buffered
DIGITAL OUTPUTS (P1 to P4)					
Output Voltage					
High, V_{OH}	AV_{DD} − 0.6			V	I_{SOURCE} = 100 µA
Low, V_{OL}			0.4	V	I_{SINK} = 100 µA
DIAGNOSTICS					
Power Supply Monitor Detect Level					
Analog Low Dropout Regulator (ALDO)			1.6	V	AV_{DD} − AV_{SS} ≥ 2.7 V
Digital LDO (DLDO)			1.55	V	IOV_{DD} ≥ 1.75 V
Reference Detect Level	0.7		1	V	REF_DET_ERR bit active if V_{REF} < 0.7 V
AINM/AINP Overvoltage Detect Level	AV_{DD} + 0.04			V	
AINM/AINP Undervoltage Detect Level			AV_{SS} − 0.04	V	
INTERNAL/EXTERNAL CLOCK					
Internal Clock					
Frequency	614.4 − 5%	614.4	614.4 + 5%	kHz	
Duty Cycle		50:50		%	
External Clock					
Frequency		2.4576		MHz	Internal divide by 4
Duty Cycle Range		45:55 to 55:45		%	
LOGIC INPUTS[2]					
Input Voltage					
Low, V_{INL}			0.3 × IOV_{DD}	V	1.65 V ≤ IOV_{DD} < 1.9 V
			0.35 × IOV_{DD}	V	1.9 V ≤ IOV_{DD} < 2.3 V
			0.7	V	2.3 V ≤ IOV_{DD} ≤ 3.6 V
High, V_{INH}	0.7 × IOV_{DD}			V	1.65 V ≤ IOV_{DD} < 1.9 V
	0.65 × IOV_{DD}			V	1.9 V ≤ IOV_{DD} < 2.3 V
	1.7			V	2.3 V ≤ IOV_{DD} < 2.7 V
	2			V	2.7 V ≤ IOV_{DD} ≤ 3.6 V
Hysteresis	0.2		0.6	V	1.65 V ≤ IOV_{DD} ≤ 3.6 V
Input Currents	−1		+1	µA	V_{IN} = IOV_{DD} or GND
Input Capacitance		10		pF	All digital inputs

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (INCLUDING CLK)					
Output Voltage[2]					
High, V_{OH}	IOV_{DD} − 0.35			V	I_{SOURCE} = 100 µA
Low, V_{OL}			0.4	V	I_{SINK} = 100 µA
Floating State Leakage Current	−1		+1	µA	
Floating State Output Capacitance		10		pF	
Data Output Coding		Offset binary			
SYSTEM CALIBRATION[2]					
Calibration Limit					
Full-Scale			1.05 × FS	V	
Zero-Scale	−1.05 × FS			V	
Input Span	0.8 × FS		2.1 × FS	V	
POWER SUPPLY VOLTAGES FOR ALL POWER MODES					
AV_{DD} to AV_{SS}					
Low Power Mode	2.7		3.6	V	
Mid Power Mode	2.7		3.6	V	
Full Power Mode	2.9		3.6	V	
IOV_{DD} to GND	1.65		3.6	V	
AV_{SS} to GND	−1.8	0	+1.8	V	
IOV_{DD} to AV_{SS}			5.4	V	
POWER SUPPLY CURRENTS[9, 11]					
I_{AVDD}, External Reference					
Low Power Mode					
Gain = 1[2]		125	135	µA	All buffers off
Gain = 1 I_{AVDD} Increase per AIN Buffer[2]		15	20	µA	
Gain = 2 to 8		205	235	µA	
Gain = 16 to 128		235	280	µA	
I_{AVDD} Increase per Reference Buffer[2]		10	15	µA	All gains
Mid Power Mode					
Gain = 1[2]		150	165	µA	All buffers off
Gain = 1 I_{AVDD} Increase per AIN Buffer[2]		30	35	µA	
Gain = 2 to 8		275	325	µA	
Gain = 16 to 128		330	405	µA	
I_{AVDD} Increase per Reference Buffer[2]		20	30	µA	All gains
Full Power Mode					
Gain = 1[2]		315	345	µA	All buffers off
Gain = 1 I_{AVDD} Increase per AIN Buffer[2]		90	125	µA	
Gain = 2 to 8		660	790	µA	
Gain = 16 to 128		875	1100	µA	
I_{AVDD} Increase per Reference Buffer[2]		85	110	µA	All gains
I_{AVDD} Increase					
Due to Internal Reference[2]		50	65	µA	Independent of power mode; the reference buffers are not required when using this reference
Due to V_{BIAS}[2]		15	20	µA	Independent of power mode
Due to Diagnostics[2]		4	5	µA	
I_{IOVDD}					
Low Power Mode		20	35	µA	
Mid Power Mode		25	40	µA	
Full Power Mode		55	85	µA	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-DOWN CURRENTS[11]					Independent of power mode
Standby Current					
I_{AVDD}		7	12	µA	LDOs on only
I_{IOVDD}		8	17	µA	
Power-Down Current					
I_{AVDD}		1	3	µA	
I_{IOVDD}		1	2	µA	

[1] Temperature range = −40°C to +105°C.
[2] These specifications are not production tested but are supported by characterization data at the initial product release.
[3] FS is the decimal equivalent of the FS[10:0] bits in the filter registers.
[4] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed gain and output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed gain and output data rate.
[5] Recalibration at any temperature removes these errors.
[6] Gain error applies to both positive and negative full-scale. A factory calibration is performed at gain = 1, T_A = 25°C.
[7] When gain > 1, the common-mode voltage is between (AV_{SS} + 0.1 + 0.1/gain) and (AV_{DD} − 0.1 − 0.5/gain).
[8] REJ60 is a bit in the filter registers. When the first notch of the sinc filter is at 50 Hz, a notch is placed at 60 Hz when REJ60 is set to 1. This gives simultaneous 50 Hz and 60 Hz rejection.
[9] When the gain is greater than 1, the analog input buffers are enabled automatically. The buffers can only be disabled when the gain equals 1.
[10] When V_{REF} = (AV_{DD} − AV_{SS}), the typical differential input equals 0.92 × V_{REF}/gain for the low and mid power modes and 0.86 × V_{REF}/gain for full power mode.
[11] The digital inputs are equal to IOV_{DD} or DGND with excitation currents and bias voltage generator disabled.

TIMING CHARACTERISTICS

AV_{DD} = 2.9 V to 3.6 V (full power mode), 2.7 V to 3.6 V (mid and low power mode), IOV_{DD} = 1.65 V to 3.6 V, AV_{SS} = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOV_{DD}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
t_3	100			ns	SCLK high pulse width
t_4	100			ns	SCLK low pulse width
t_{12}					Delay between consecutive read/write operations
	3/MCLK[3]			ns	Full power mode
	12/MCLK			ns	Mid power mode
	24/MCLK			ns	Low power mode
t_{13}				µs	DOUT/$\overline{RDY}$ high time if DOUT/$\overline{RDY}$ is low and the next conversion is available
		6		µs	Full power mode
		25		µs	Mid power mode
		50		µs	Low power mode
t_{14}					$\overline{SYNC}$ low pulse width
	3/MCLK			ns	Full power mode
	12/MCLK			ns	Mid power mode
	24/MCLK			ns	Low power mode
READ OPERATION					
t_1	0		80	ns	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
t_2[4]	0		80	ns	SCLK active edge[5] to data valid delay
t_5[6, 7]	10		80	ns	Bus relinquish time after $\overline{CS}$ inactive edge
t_6	0			ns	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7[8]					SCLK inactive edge to DOUT/$\overline{RDY}$ high
	10			ns	The DOUT_$\overline{RDY}$_DEL bit is cleared, the $\overline{CS}$_EN bit is cleared
	110			ns	The DOUT_$\overline{RDY}$_DEL bit is set, the $\overline{CS}$_EN bit is cleared
t_{7A}[7]	t_5			ns	Data valid after $\overline{CS}$ inactive edge, the $\overline{CS}$_EN bit is set

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
WRITE OPERATION					
t_8	0			ns	$\overline{CS}$ falling edge to SCLK active edge[5] setup time
t_9	30			ns	Data valid to SCLK edge setup time
t_{10}	25			ns	Data valid to SCLK edge hold time
t_{11}	0			ns	$\overline{CS}$ rising edge to SCLK edge hold time

[1] These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of IOV_{DD} and timed from a voltage level of $IOV_{DD}/2$.
[2] See Figure 3, Figure 4, Figure 5, and Figure 6.
[3] MCLK is the master clock frequency.
[4] These specifications are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[5] The SCLK active edge is the falling edge of SCLK.
[6] These specifications are derived from the measured time taken by the data output to change by 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. The times quoted in the timing characteristics are the true bus relinquish times of the device and, therefore, are independent of external bus loading capacitances.
[7] $\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although subsequent reads must not occur close to the next output update. In continuous read mode, the digital word can be read only once.
[8] When the $\overline{CS}$_EN bit is cleared, the DOUT/$\overline{RDY}$ pin changes from its DOUT function to its $\overline{RDY}$ function, following the last inactive edge of the SCLK. When $\overline{CS}$_EN is set, the DOUT pin continues to output the LSB of the data until the $\overline{CS}$ inactive edge.

Timing Diagrams

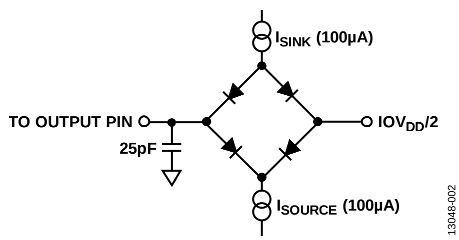


Figure 2. Load Circuit for Timing Characterization

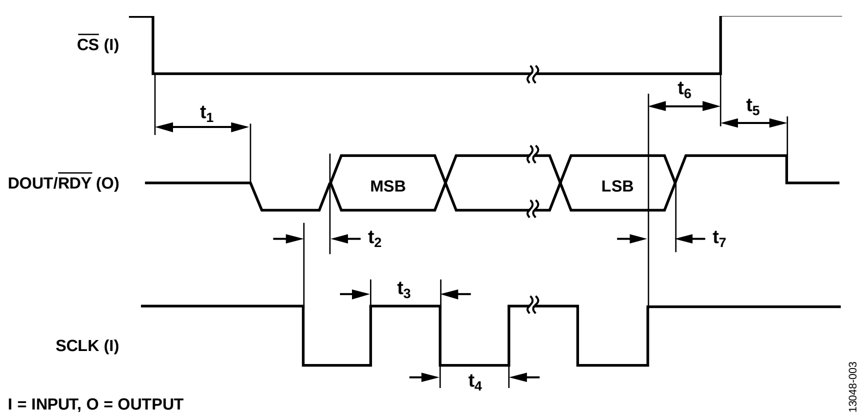


Figure 3. Read Cycle Timing Diagram ($\overline{CS}$_EN Bit Cleared)

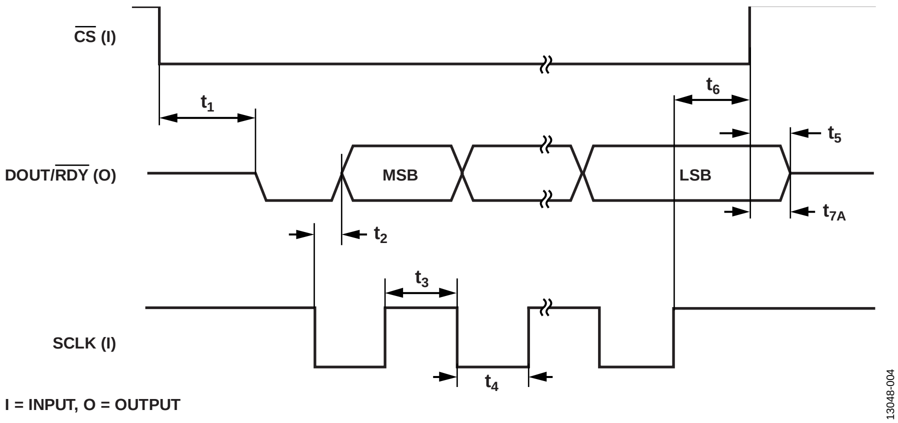


Figure 4. Read Cycle Timing Diagram ($\overline{\text{CS}}$_EN Bit Set)

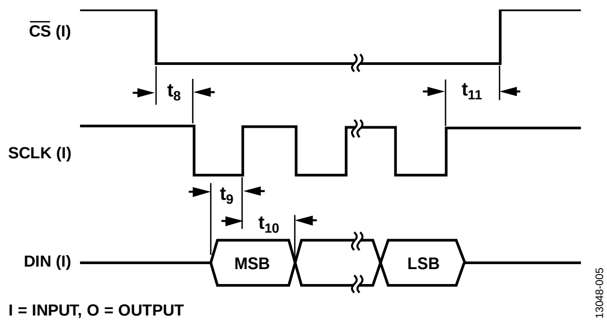


Figure 5. Write Cycle Timing Diagram

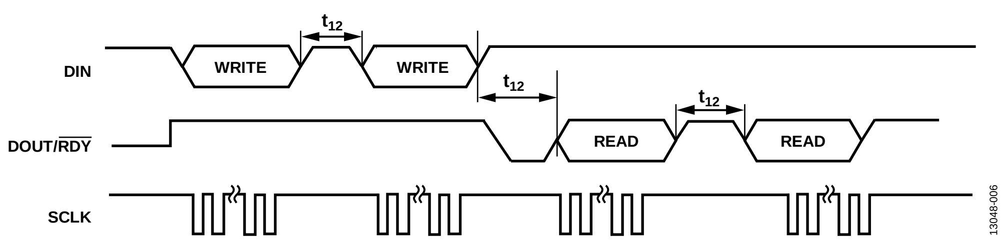


Figure 6. Delay Between Consecutive Serial Operations

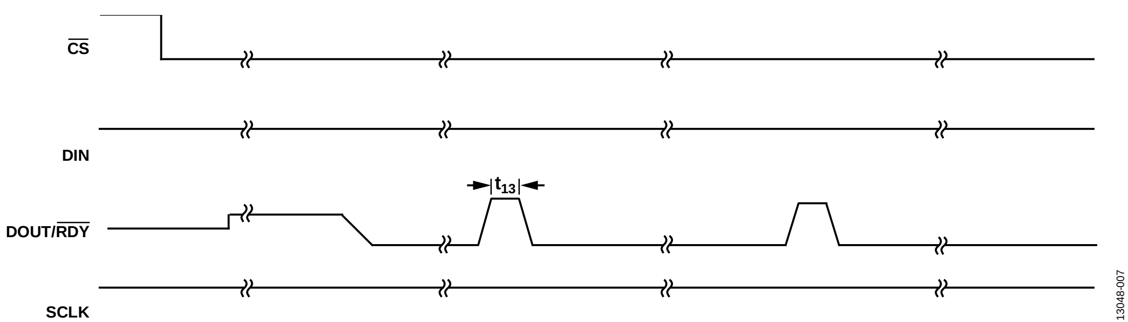


Figure 7. DOUT/$\overline{\text{RDY}}$ High Time when DOUT/$\overline{\text{RDY}}$ is Initially Low and the Next Conversion is Available

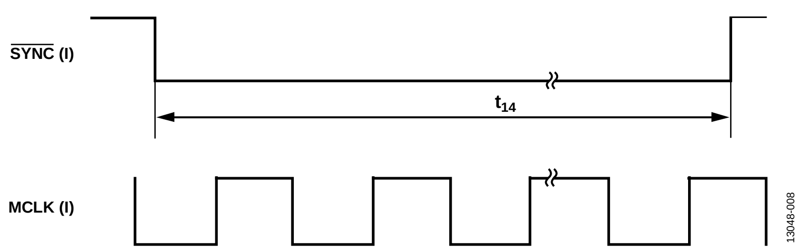


Figure 8. $\overline{\text{SYNC}}$ Pulse Width

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{DD} to AV_{SS}	−0.3 V to +3.96 V
IOV_{DD} to DGND	−0.3 V to +3.96 V
IOV_{DD} to DGND	−0.3 V to +3.96 V
IOV_{DD} to AV_{SS}	−0.3 V to +5.94 V
AV_{SS} to DGND	−1.98 V to +0.3 V
Analog Input Voltage to AV_{SS}	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AV_{SS}	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOV_{DD} + 0.3 V
AINx/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering	
Reflow	260°C
ESD Ratings	
Human Body Model (HBM)	4 kV
Field-Induced Charged Device Model (FICDM)	1250 V
Machine Model	400 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	32.5	32.71	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

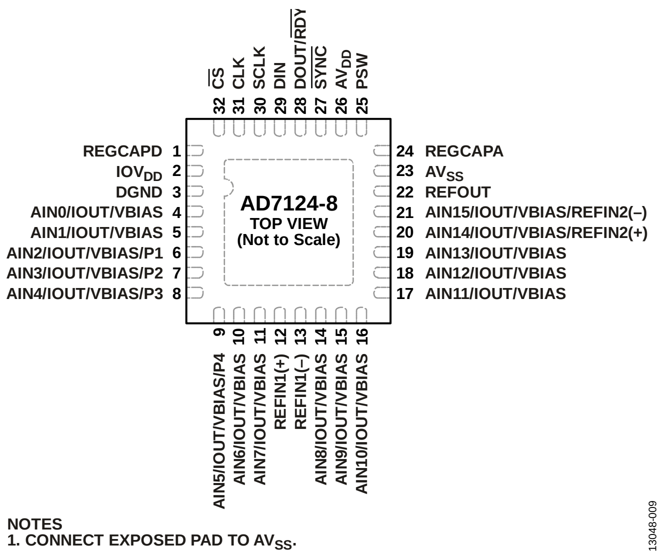


Figure 9. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	REGCAPD	Digital LDO Regulator Output. Decouple this pin to DGND with a 0.1 µF capacitor.
2	IOV_{DD}	Serial Interface Supply Voltage, 1.65 V to 3.6 V. IOV_{DD} is independent of AV_{DD}. Therefore, the serial interface can operate at 1.65 V with AV_{DD} at 3.6 V, for example.
3	DGND	Digital Ground Reference Point.
4	AIN0/IOUT/VBIAS	Analog Input 0/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT1 or IOUT0 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
5	AIN1/IOUT/VBIAS	Analog Input 1/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
6	AIN2/IOUT/VBIAS/P1	Analog Input 2/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 1. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AV_{SS} and AV_{DD}.
7	AIN3/IOUT/VBIAS/P2	Analog Input 3/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 2. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AV_{SS} and AV_{DD}.
8	AIN4/IOUT/VBIAS/P3	Analog Input 4/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 3. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AV_{SS} and AV_{DD}.

Pin No.	Mnemonic	Description
9	AIN5/IOUT/VBIAS/P4	Analog Input 5/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 4. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AV_{SS} and AV_{DD}.
10	AIN6/IOUT/VBIAS	Analog Input 6/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
11	AIN7/IOUT/VBIAS	Analog Input 7/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
12	REFIN1(+)	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(−). REFIN1(+) can be anywhere between AV_{DD} and AV_{SS} + 1 V. The nominal reference voltage (REFIN1(+) − REFIN1(−)) is 2.5 V, but the device functions with a reference from 1 V to AV_{DD}.
13	REFIN1(−)	Negative Reference Input. This reference input can be anywhere between AV_{SS} and AV_{DD} − 1 V.
14	AIN8/IOUT/VBIAS	Analog Input 8/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
15	AIN9/IOUT/VBIAS	Analog Input 9/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
16	AIN10/IOUT/VBIAS	Analog Input 10/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
17	AIN11/IOUT/VBIAS	Analog Input 11/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
18	AIN12/IOUT/VBIAS	Analog Input 12/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
19	AIN13/IOUT/VBIAS	Analog Input 13/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
20	AIN14/IOUT/VBIAS/ REFIN2(+)	Analog Input 14/Output of Internal Excitation Current Source/Bias Voltage/Positive Reference Input. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin also functions as a positive reference input for REFIN2(±). REFIN2(+) can be anywhere between AV_{DD} and AV_{SS} + 1 V. The nominal reference voltage (REFIN2(+) to REFIN2(−)) is 2.5 V, but the device functions with a reference from 1 V to AV_{DD}.

Pin No.	Mnemonic	Description
21	AIN15/IOUT/VBIAS/ REFIN2(−)	Analog Input 15/Output of Internal Excitation Current Source/Bias Voltage/Negative Reference Input. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin also functions as the negative reference input for REFIN2(±). This reference input can be anywhere between AV_{SS} and AV_{DD} − 1 V.
22	REFOUT	Internal Reference Output. The buffered output of the internal 2.5 V voltage reference is available on this pin.
23	AV_{SS}	Analog Supply Voltage. The voltage on AV_{DD} is referenced to AV_{SS}. The differential between AV_{DD} and AV_{SS} must be between 2.7 V and 3.6 V in mid or low power mode and between 2.9 V and 3.6 V in full power mode. AV_{SS} can be taken below 0 V to provide a dual power supply to the AD7124-8. For example, AV_{SS} can be tied to −1.8 V and AV_{DD} can be tied to +1.8 V, providing a ±1.8 V supply to the ADC.
24	REGCAPA	Analog LDO Regulator Output. Decouple this pin to AV_{SS} with a 0.1 µF capacitor.
25	PSW	Low-Side Power Switch to AV_{SS}.
26	AV_{DD}	Analog Supply Voltage, Relative to AV_{SS}.
27	$\overline{\text{SYNC}}$	Synchronization Input. This pin is a logic input that allows synchronization of the digital filters and analog modulators when using a number of AD7124-8 devices. When $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic, and the calibration control logic are reset, and the analog modulator is held in a reset state. $\overline{\text{SYNC}}$ does not affect the digital interface but does reset $\overline{\text{RDY}}$ to a high state if it is low.
28	DOUT/$\overline{\text{RDY}}$	Serial Data Output/Data Ready Output. DOUT/$\overline{\text{RDY}}$ functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can also be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{\text{RDY}}$ pin. When $\overline{\text{CS}}$ is low, the data/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.
29	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in the input shift register is transferred to the control registers within the ADC, with the register selection bits of the communications register identifying the appropriate register.
30	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK pin has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
31	CLK	Clock Input/Clock Output. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. This allows several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed.
32	$\overline{\text{CS}}$	Chip Select Input. This is an active low logic input that selects the ADC. Use $\overline{\text{CS}}$ to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{\text{CS}}$ can be hardwired low if the serial peripheral interface (SPI) diagnostics are unused, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT interfacing with the device.
	EP	Exposed Pad. Connect the exposed pad to AV_{SS}.

TERMINOLOGY

AINP
AINP refers to the positive analog input.

AINM
AINM refers to the negative analog input.

Integral Nonlinearity (INL)
INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 … 000 to 000 … 001), and full scale, a point 0.5 LSB above the last code transition (111 … 110 to 111 … 111). The error is expressed in ppm of the full-scale range.

Gain Error
Gain error is the deviation of the last code transition (111 … 110 to 111 … 111) from the ideal AINP voltage (AINM + V_{REF}/gain – 3/2 LSBs). Gain error applies to both unipolar and bipolar analog input ranges.

Gain error is a measure of the span error of the ADC. It includes full-scale errors but not zero-scale errors. For unipolar input ranges, it is defined as full-scale error minus unipolar offset error; whereas for bipolar input ranges it is defined as full-scale error minus bipolar zero error.

Offset Error
Offset error is the deviation of the first code transition from the ideal AINP voltage (AINM + 0.5 LSB) when operating in the unipolar mode.

In bipolar mode, offset error is the deviation of the midscale transition (0111 … 111 to 1000 … 000) from the ideal AINP voltage (AINM – 0.5 LSB).

Offset Calibration Range
In the system calibration modes, the AD7124-8 calibrates offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD7124-8 can accept and still calibrate offset accurately.

Full-Scale Calibration Range
The full-scale calibration range is the range of voltages that the AD7124-8 can accept in the system calibration mode and still calibrate full scale correctly.

Input Span
In system calibration schemes, two voltages applied in sequence to the AD7124-8 analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7124-8 can accept and still calibrate gain accurately.

TYPICAL PERFORMANCE CHARACTERISTICS

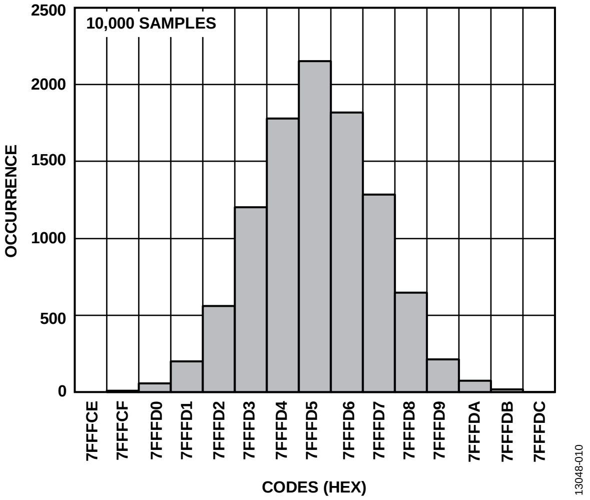


Figure 10. Noise Histogram Plot (Full Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 1)

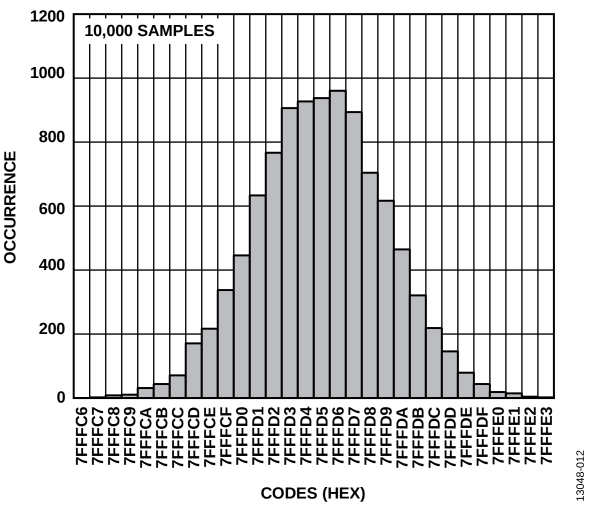


Figure 11. Noise Histogram Plot (Mid Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 1)

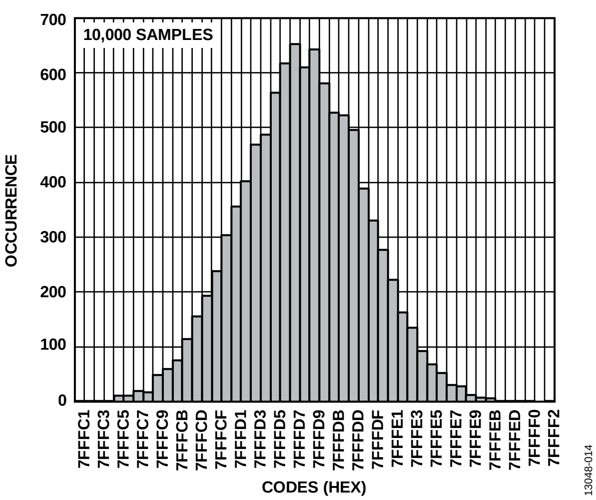


Figure 12. Noise Histogram Plot (Low Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 1)

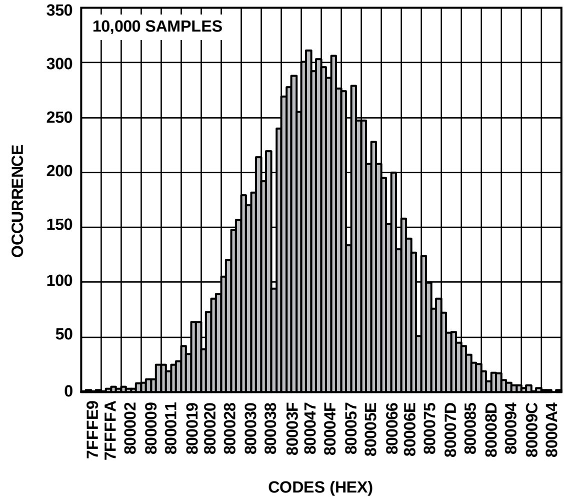


Figure 13. Noise Histogram Plot (Full Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 128)

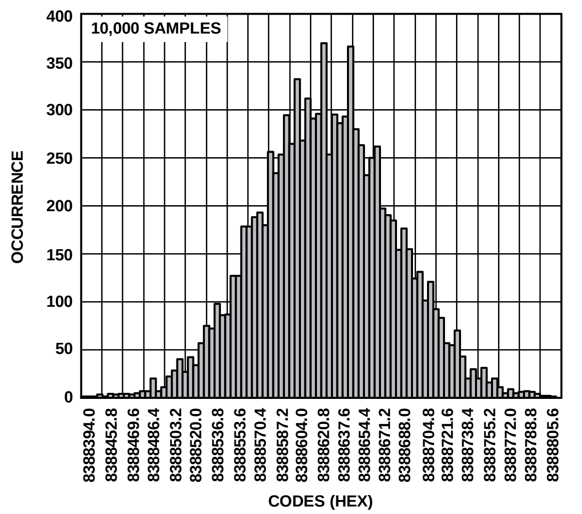


Figure 14. Noise Histogram Plot (Mid Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 128)

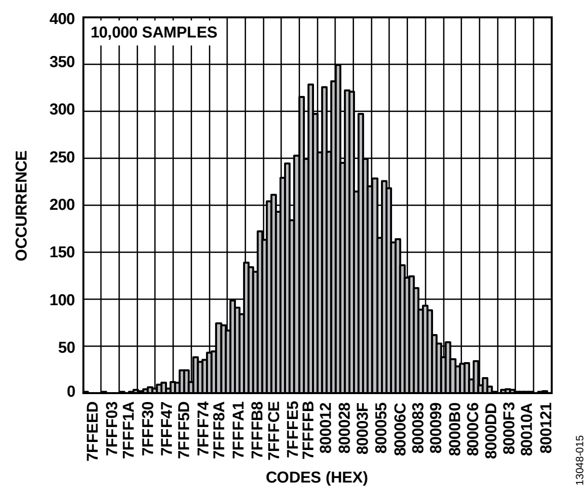


Figure 15. Noise Histogram Plot (Low Power Mode, Post Filter, Output Data Rate = 25 SPS, Gain = 128)

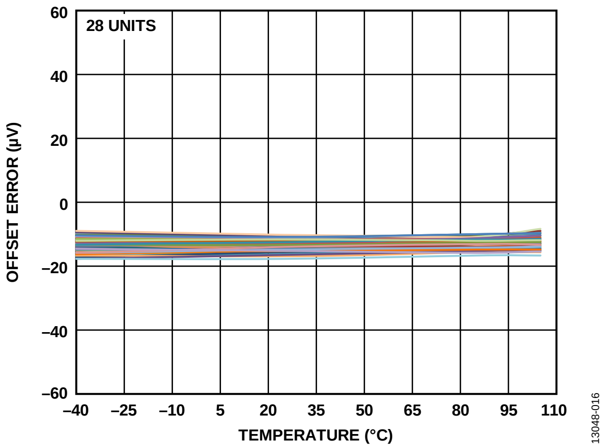


Figure 16. Input Referred Offset Error vs. Temperature (Gain = 8, Full Power Mode)

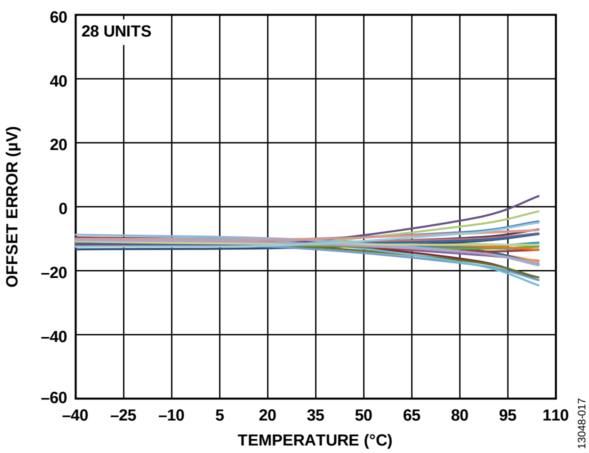


Figure 17. Input Referred Offset Error vs. Temperature (Gain = 8, Mid Power Mode)

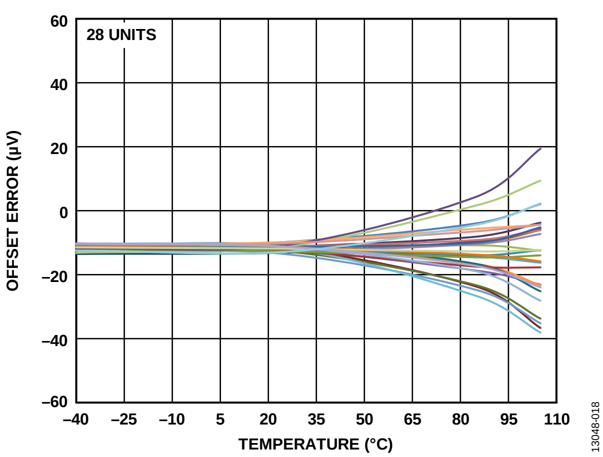


Figure 18. Input Referred Offset Error vs. Temperature (Gain = 8, Low Power Mode)

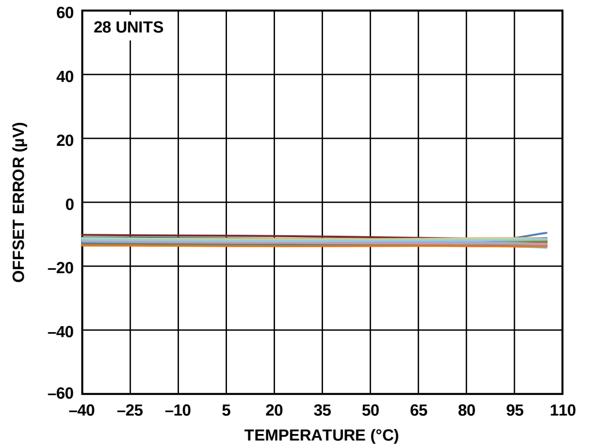


Figure 19. Input Referred Offset Error vs. Temperature (Gain = 16, Full Power Mode)

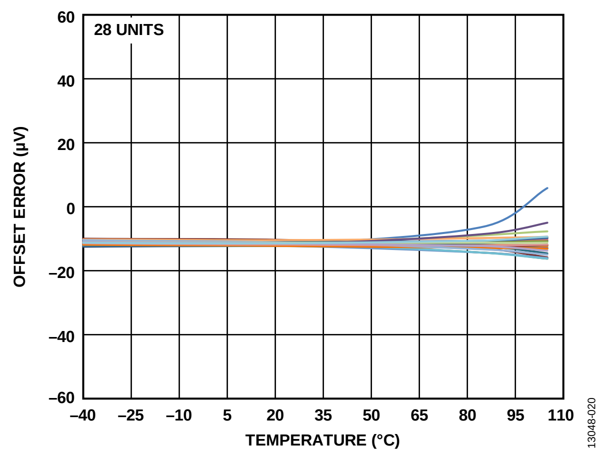


Figure 20. Input Referred Offset Error vs. Temperature (Gain = 16, Mid Power Mode)

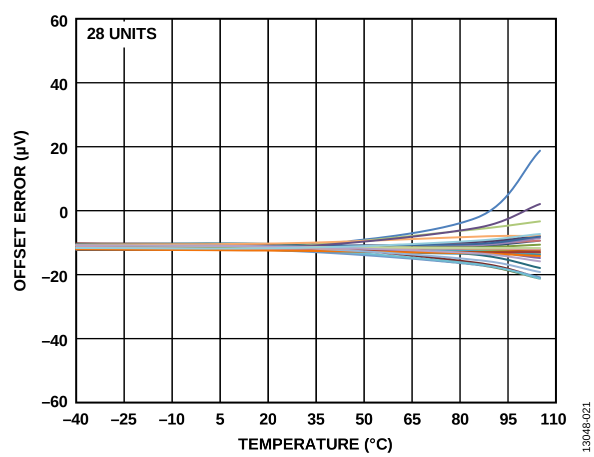


Figure 21. Input Referred Offset Error vs. Temperature (Gain = 16, Low Power Mode)

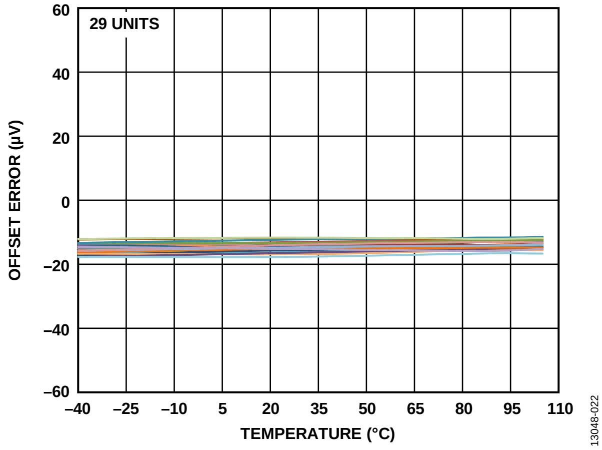


Figure 22. Input Referred Offset Error vs. Temperature (Gain = 1, Analog Input Buffers Enabled)

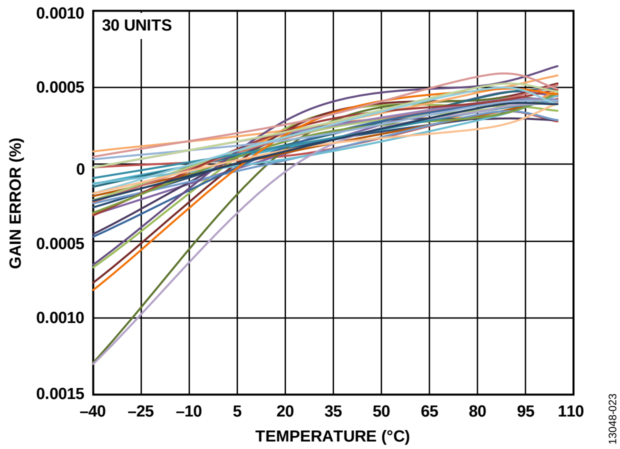


Figure 23. Input Referred Gain Error vs. Temperature (Gain = 1)

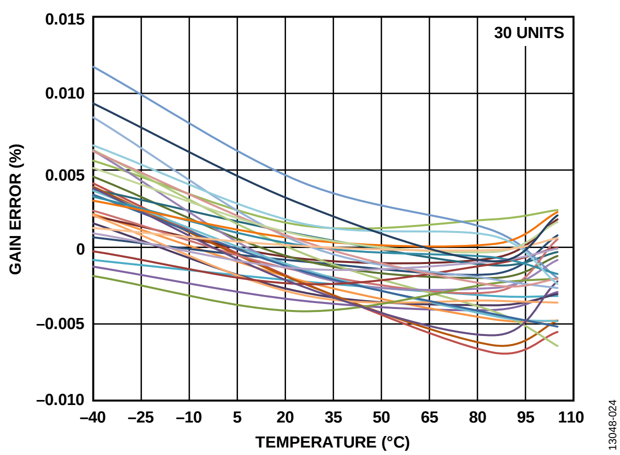


Figure 24. Input Referred Gain Error vs. Temperature (Gain = 8)

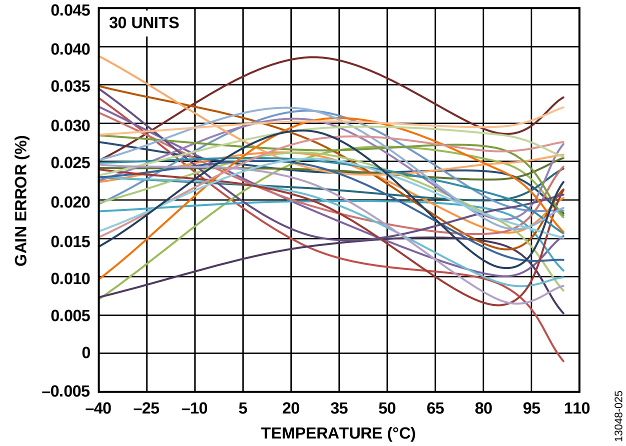


Figure 25. Input Referred Gain Error vs. Temperature (Gain = 16)

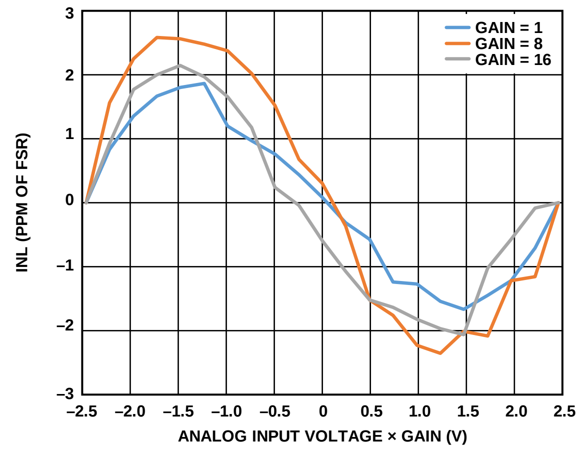


Figure 26. INL vs. Differential Input Signal (Analog Input × Gain), ODR = 50 SPS, External 2.5 V Reference

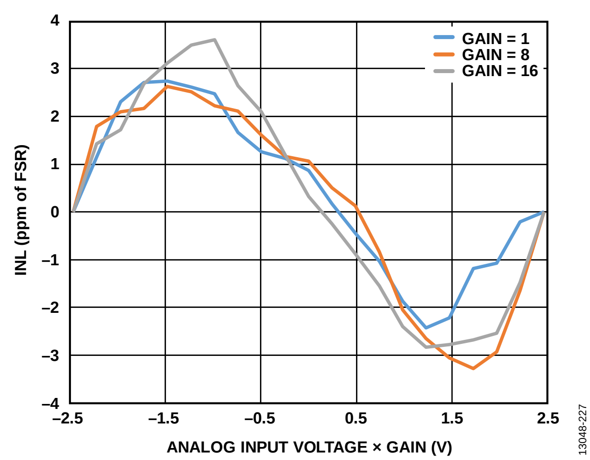


Figure 27. INL vs. Differential Input Signal (Analog Input × Gain), ODR = 50 SPS, Internal Reference

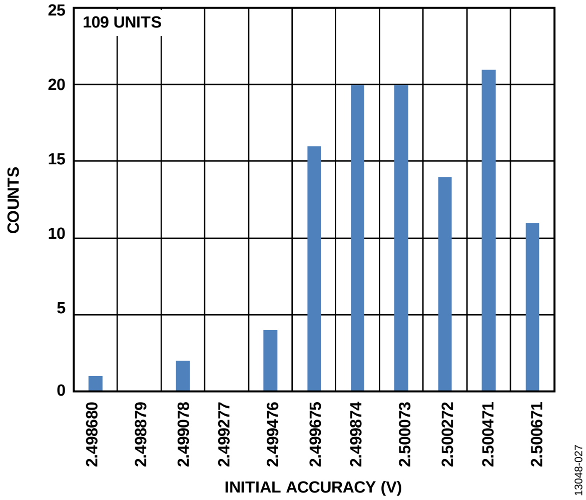


Figure 28. Internal Reference Voltage Histogram

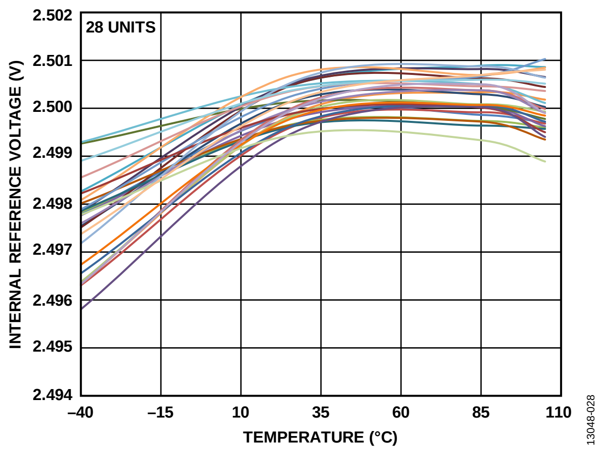


Figure 29. Internal Reference Voltage vs. Temperature

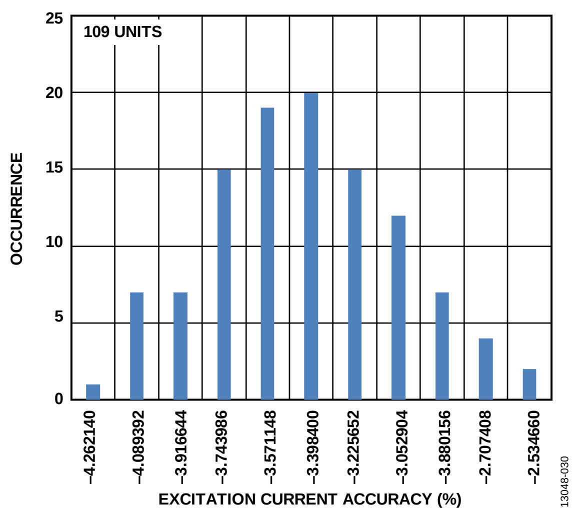


Figure 30. IOUTx Current Initial Accuracy Histogram (500 µA)

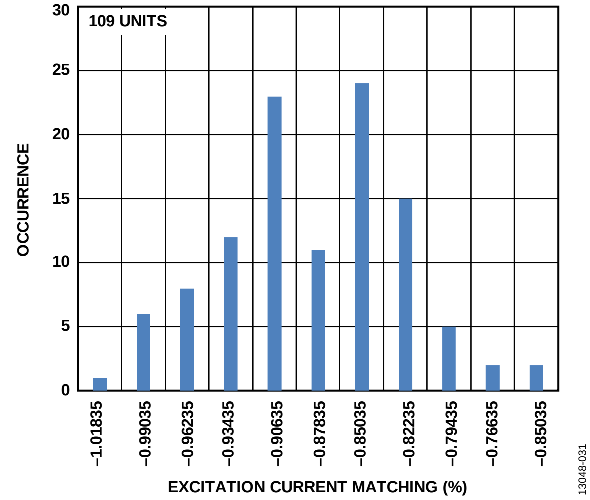


Figure 31. IOUTx Current Initial Matching Histogram (500 µA)

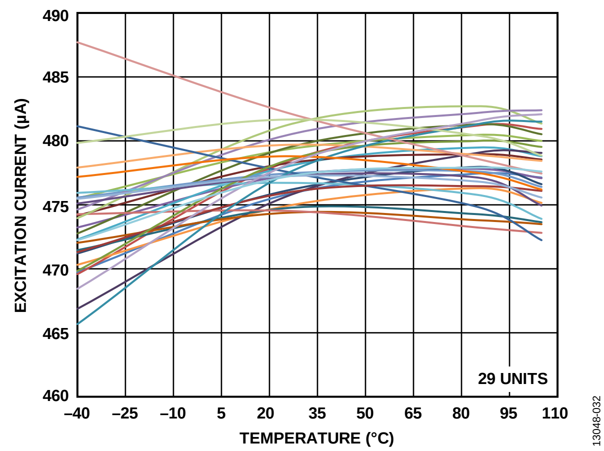


Figure 32. Excitation Current Drift (500 µA)

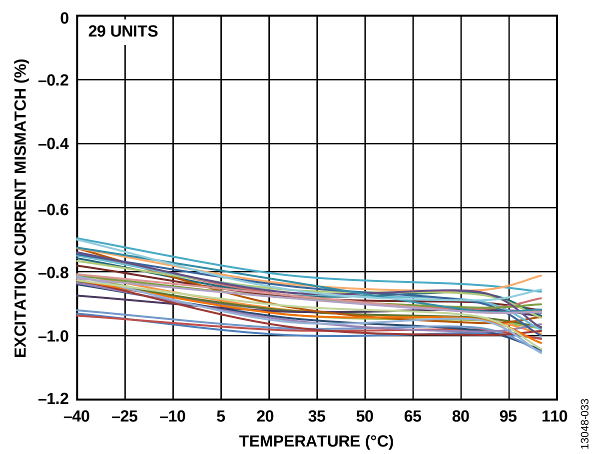


Figure 33. Excitation Current Drift Matching (500 µA)

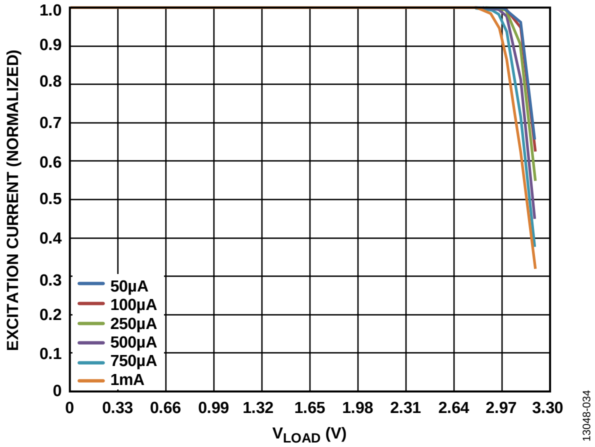


Figure 34. Output Compliance (AV_{DD} = 3.3 V)

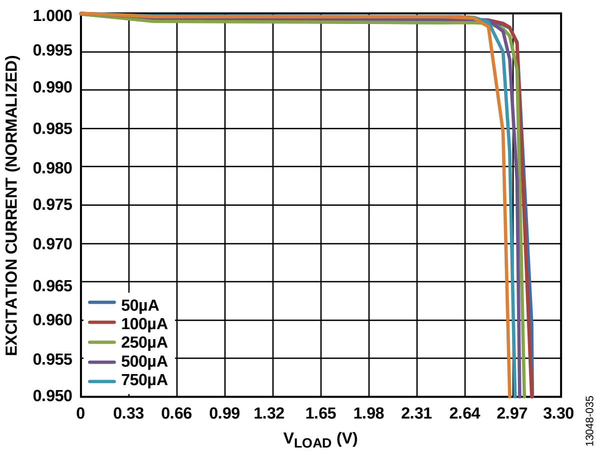


Figure 35. Output Compliance (AV_{DD} = 3.3 V)

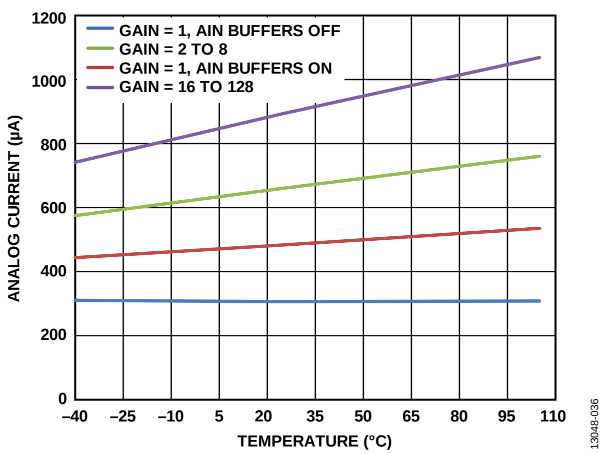


Figure 36. Analog Current vs. Temperature (Full Power Mode)

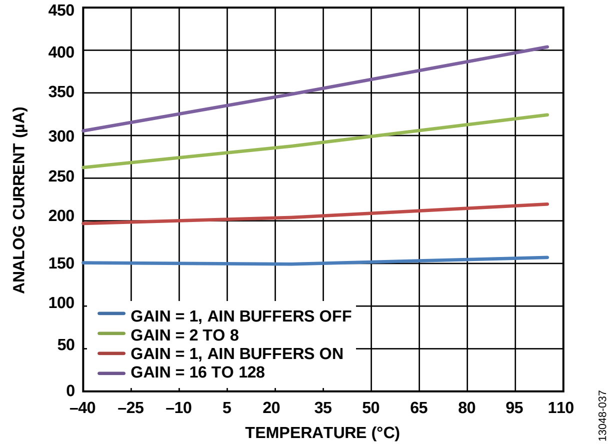


Figure 37. Analog Current vs. Temperature (Mid Power Mode)

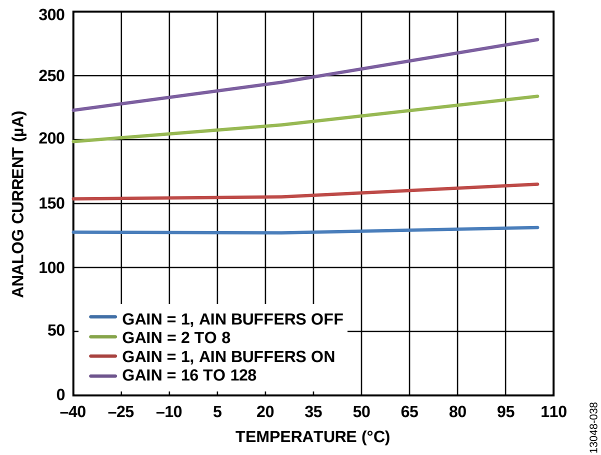


Figure 38. Analog Current vs. Temperature (Low Power Mode)

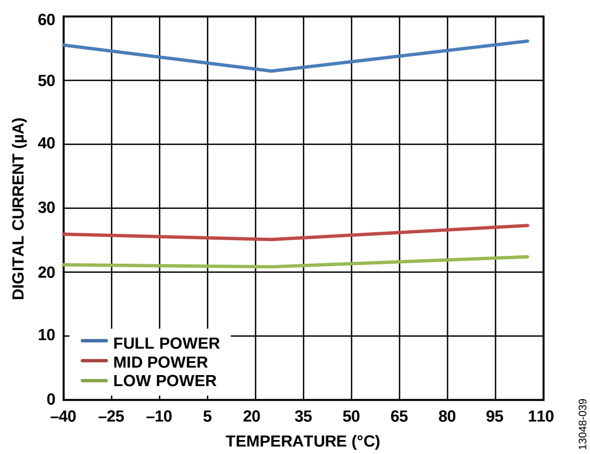


Figure 39. Digital Current vs. Temperature

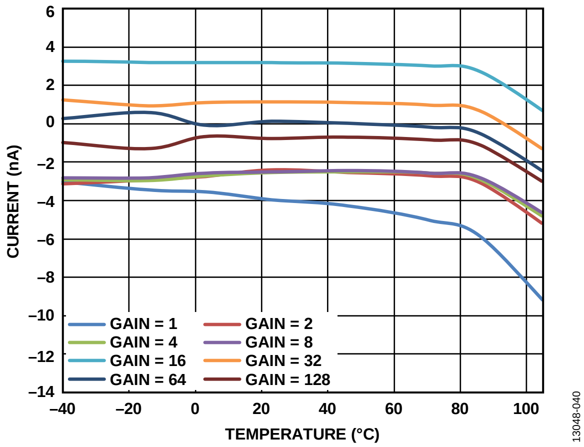


Figure 40. Absolute Analog Input Current vs. Temperature (Full Power Mode)

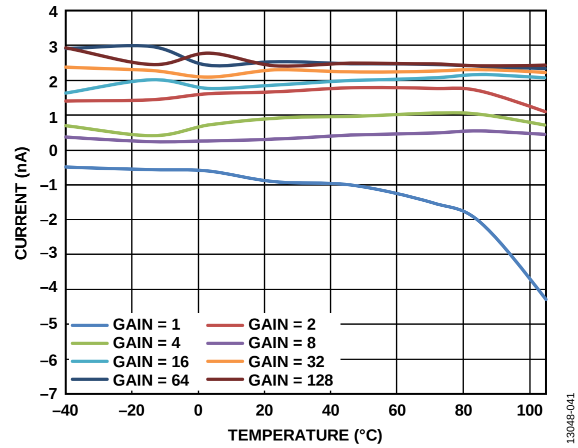


Figure 43. Differential Analog Input Current vs. Temperature (Full Power Mode)

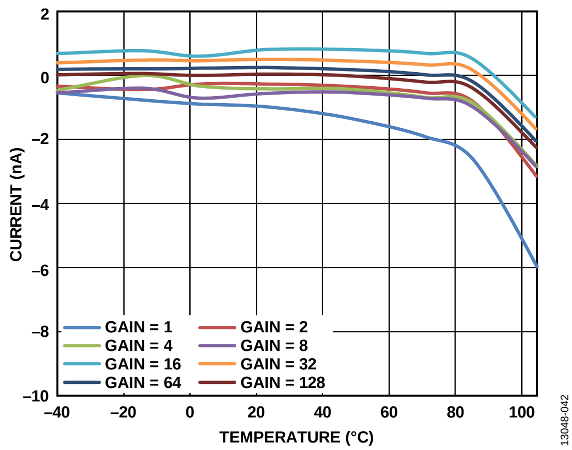


Figure 41. Absolute Analog Input Current vs. Temperature (Mid Power Mode)

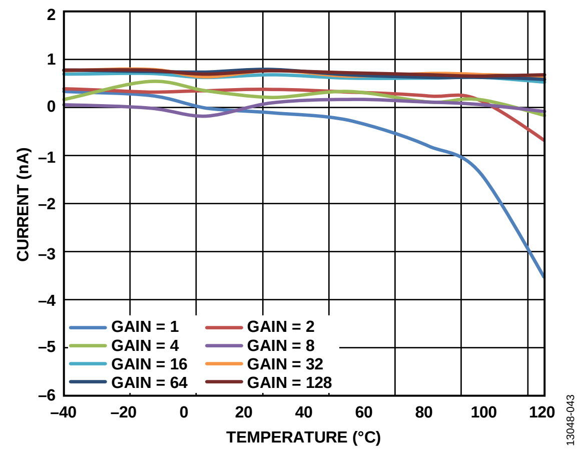


Figure 44. Differential Analog Input Current vs. Temperature (Mid Power Mode)

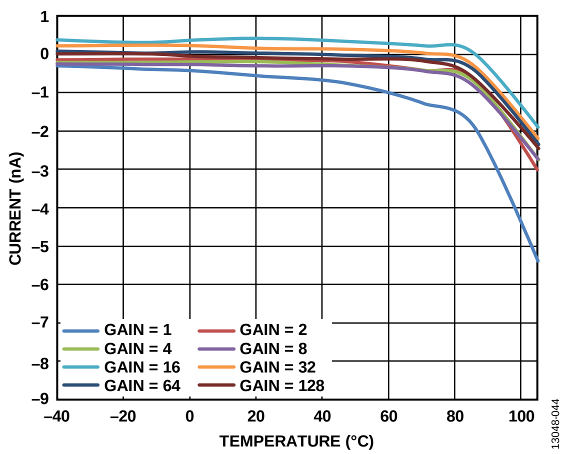


Figure 42. Absolute Analog Input Current vs. Temperature (Low Power Mode)

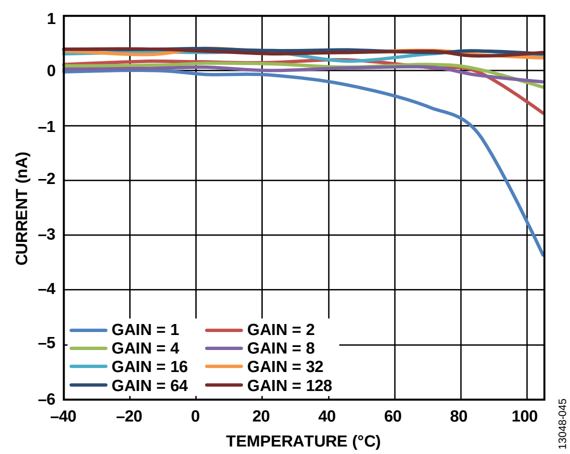


Figure 45. Differential Analog Input Current vs. Temperature (Low Power Mode)

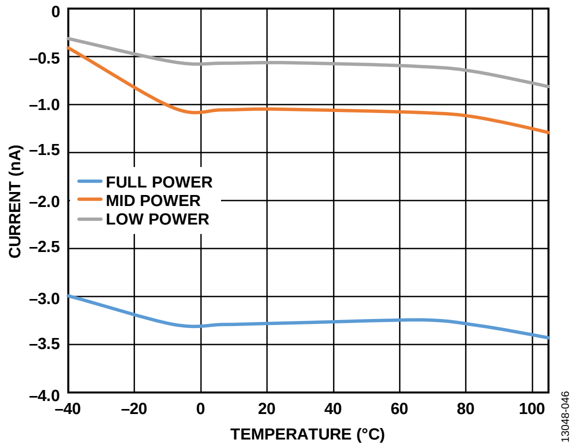


Figure 46. Reference Input Current vs. Temperature (Reference Buffers Enabled)

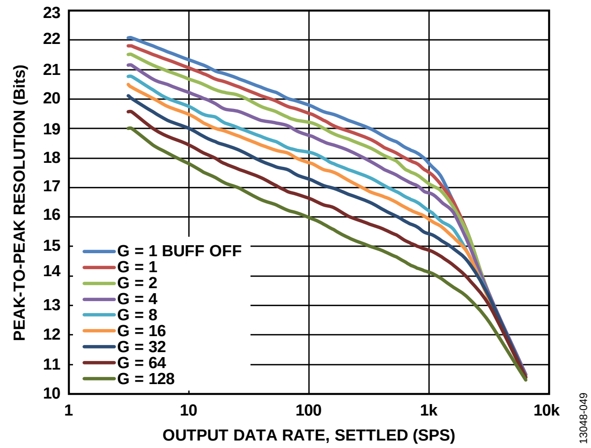


Figure 49. Peak-to-Peak Resolution vs. Output Data Rate (Settled), $Sinc^3$ Filter (Full Power Mode)

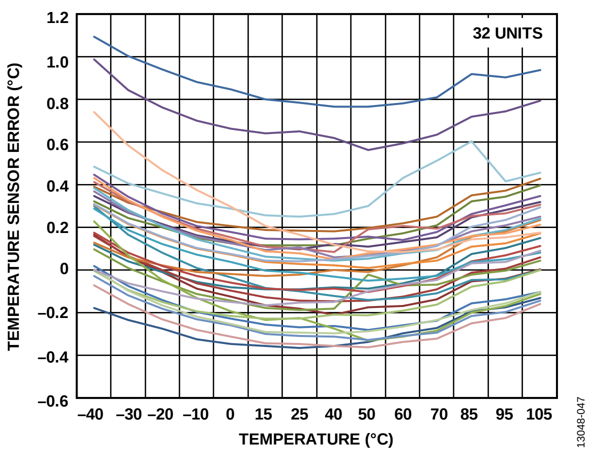


Figure 47. Temperature Sensor Accuracy

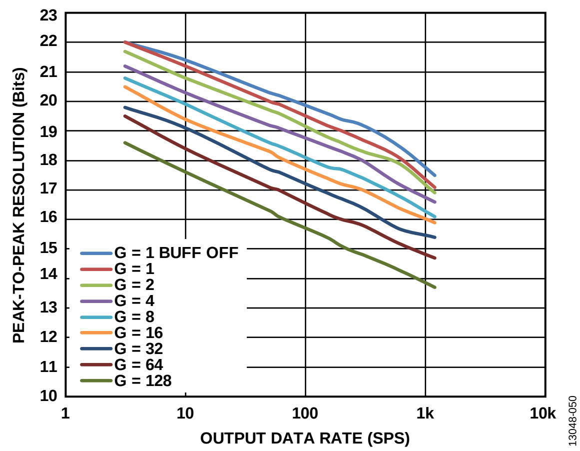


Figure 50. Peak-to-Peak Resolution vs. Output Data Rate, $Sinc^4 + Sinc^1$ Filter (Full Power Mode)

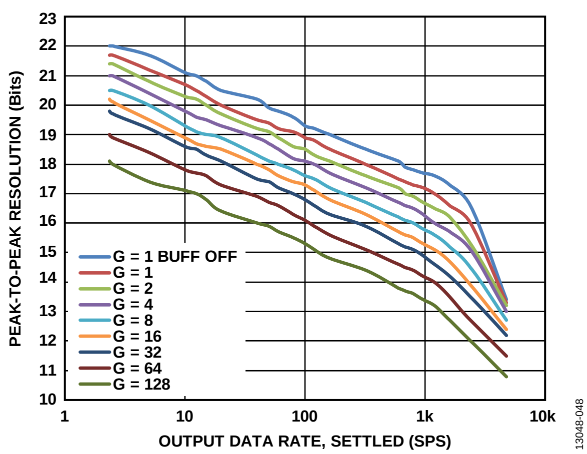


Figure 48. Peak-to-Peak Resolution vs. Output Data Rate (Settled), $Sinc^4$ Filter (Full Power Mode)

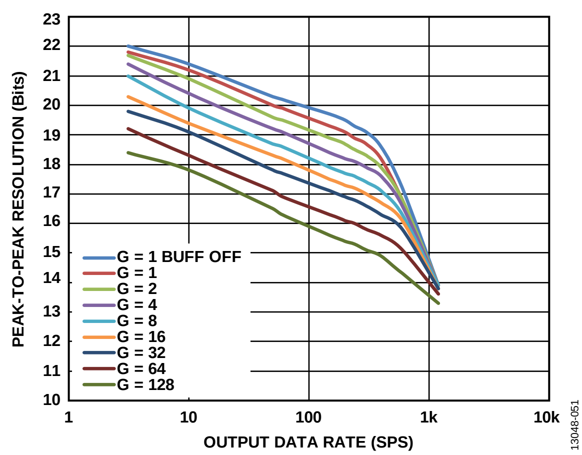


Figure 51. Peak-to-Peak Resolution vs. Output Data Rate, $Sinc^3 + Sinc^1$ Filter (Full Power Mode)

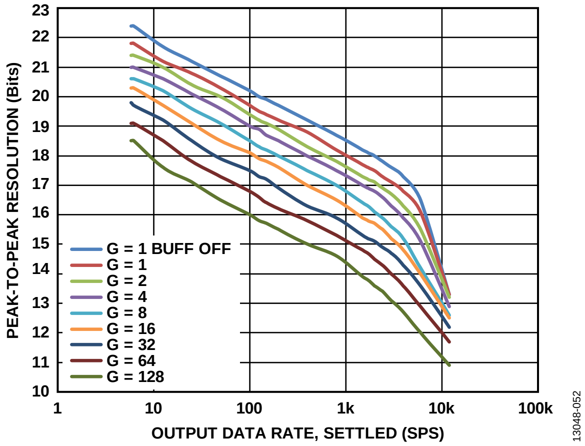


Figure 52. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc[4] Filter (Mid Power Mode)

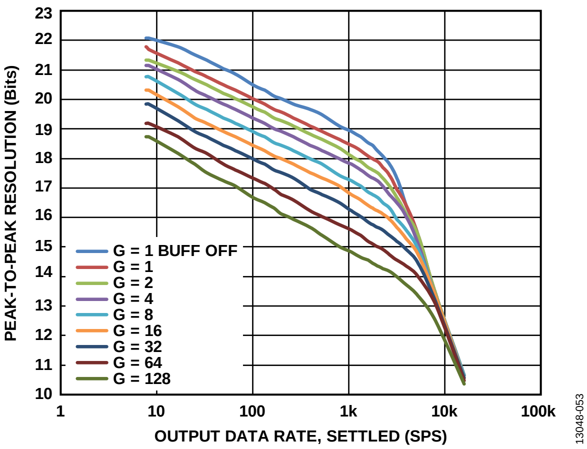


Figure 53. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc[3] Filter (Mid Power Mode)

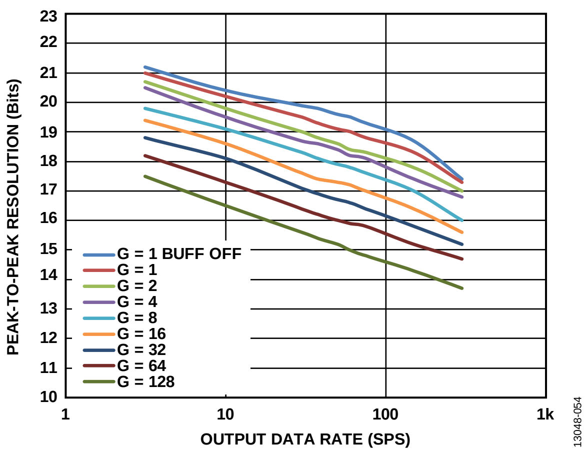


Figure 54. Peak-to-Peak Resolution vs. Output Data Rate, Sinc[4] + Sinc[1] Filter (Mid Power Mode)

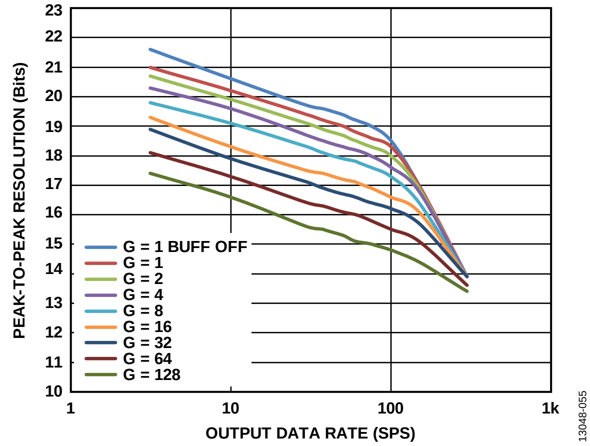


Figure 55. Peak-to-Peak Resolution vs. Output Data Rate, Sinc[3] + Sinc[1] Filter (Mid Power Mode)

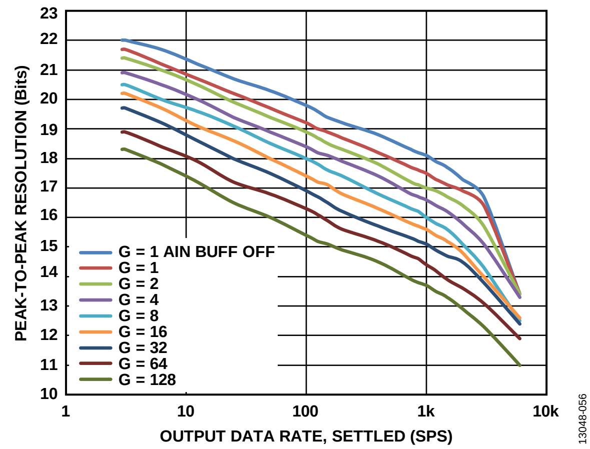


Figure 56. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc[4] Filter (Low Power Mode)

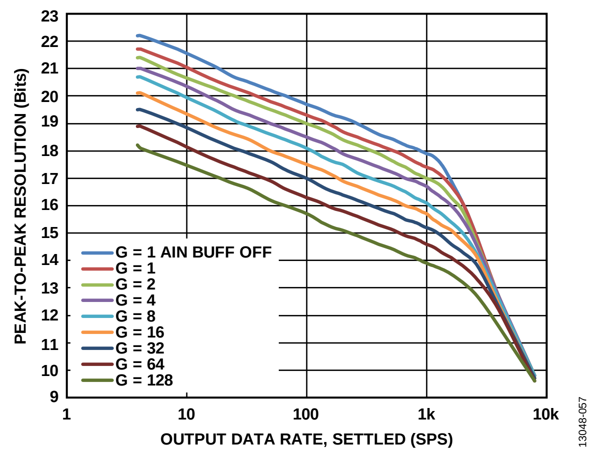


Figure 57. Peak-to-Peak Resolution vs. Output Data Rate (Settled), Sinc[3] Filter (Low Power Mode)

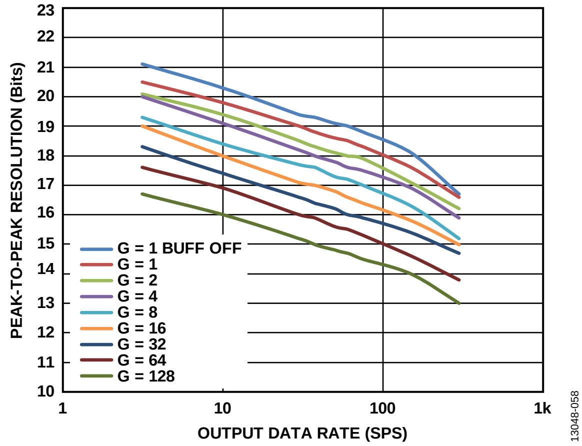


Figure 58. Peak-to-Peak Resolution vs. Output Data Rate, Sinc[4] + Sinc[1] Filter (Low Power Mode)

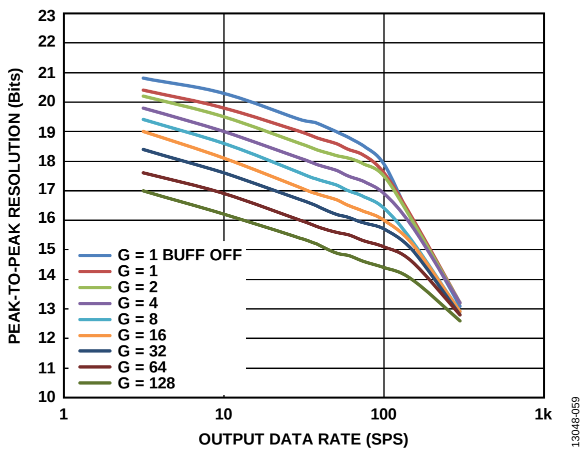


Figure 59. Peak-to-Peak Resolution vs. Output Data Rate, Sinc[3] + Sinc[1] Filter (Low Power Mode)

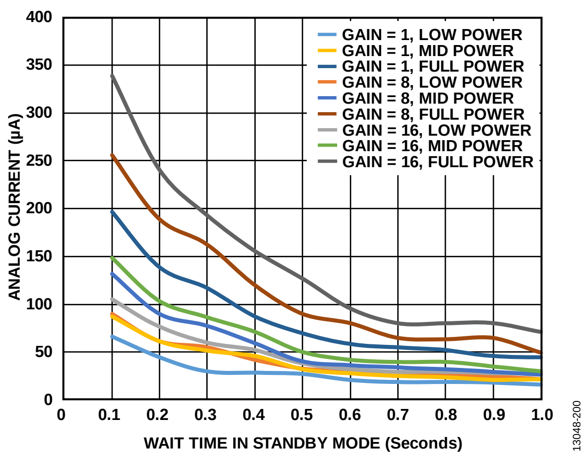


Figure 60. Analog Current vs. Wait Time in Standby Mode, ADC in Single Conversion Mode (50 SPS)

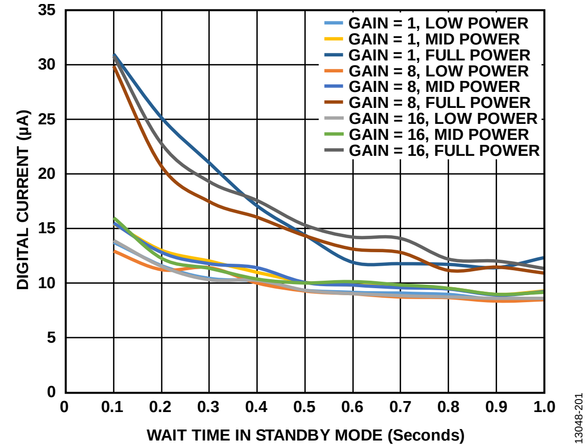


Figure 61. Digital Current vs. Wait Time in Standby Mode, ADC in Single Conversion Mode (50 SPS)

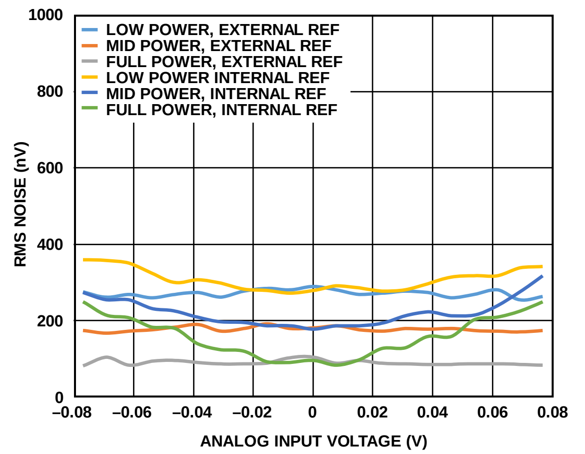


Figure 62. RMS Noise vs. Analog Input Voltage for the Internal Reference and External Reference (Gain = 32, 50 SPS)

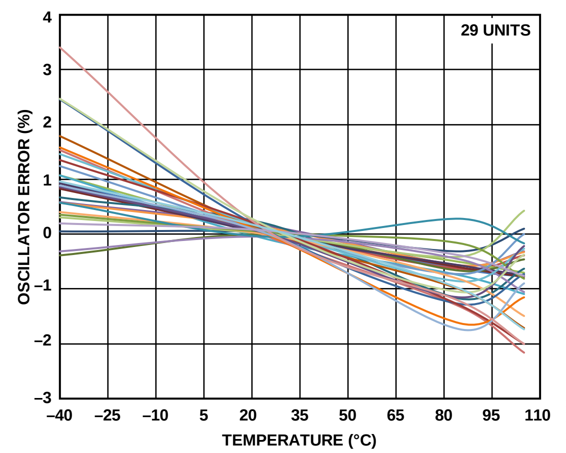


Figure 63. Internal Oscillator Error vs. Temperature

RMS NOISE AND RESOLUTION

Table 7 through Table 36 show the rms noise, peak-to-peak noise, effective resolution, and noise-free (peak-to-peak) resolution of the AD7124-8 for various output data rates, gain settings, and filters. The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the effective resolution is calculated using the rms noise, whereas the peak-to-peak resolution (shown in parentheses) is calculated based on peak-to-peak noise (shown in parentheses). The peak-to-peak resolution represents the resolution for which there is no code flicker.

Effective Resolution = Log_2*(Input Range/RMS Noise)*

Peak-to-Peak Resolution = Log_2*(Input Range/Peak-to-Peak Noise)*

FULL POWER MODE

Sinc⁴

Table 7. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.4	2.34	2.16	0.24 (1.5)	0.15 (0.89)	0.091 (0.6)	0.071 (0.41)	0.045 (0.26)	0.031 (0.17)	0.025 (0.15)	0.023 (0.14)
1920	10	2.5	2.3	0.23 (1.5)	0.14 (0.89)	0.094 (0.6)	0.076 (0.42)	0.048 (0.27)	0.03 (0.19)	0.025 (0.16)	0.025 (0.15)
960	20	5	4.6	0.31 (2.1)	0.22 (1.3)	0.13 (0.89)	0.1 (0.6)	0.069 (0.41)	0.044 (0.26)	0.035 (0.22)	0.034 (0.22)
480	40	10	9.2	0.42 (3)	0.3 (2.1)	0.19 (1.4)	0.14 (0.97)	0.09 (0.63)	0.063 (0.39)	0.053 (0.34)	0.043 (0.27)
384	50	12.5	11.5	0.48 (3.2)	0.33 (2.1)	0.2 (1.3)	0.16 (1.1)	0.1 (0.75)	0.068 (0.43)	0.059 (0.42)	0.048 (0.28)
320	60	15	13.8	0.51 (3.3)	0.35 (2.4)	0.23 (1.3)	0.17 (1.2)	0.11 (0.78)	0.077 (0.5)	0.064 (0.41)	0.056 (0.35)
240	80	20	18.4	0.6 (4.8)	0.41 (3)	0.28 (1.8)	0.19 (1.3)	0.13 (0.86)	0.09 (0.54)	0.072 (0.48)	0.063 (0.45)
120	160	40	36.8	0.86 (6.9)	0.55 (4.1)	0.37 (2.5)	0.29 (2)	0.2 (1.2)	0.13 (0.84)	0.11 (0.7)	0.098 (0.6)
60	320	80	73.6	1.2 (8.9)	0.76 (6.1)	0.53 (4.1)	0.4 (2.7)	0.26 (1.8)	0.18 (1.2)	0.15 (0.95)	0.14 (0.86)
30	640	160	147.2	1.7 (13)	1.1 (8.8)	0.74 (5.7)	0.57 (4.1)	0.38 (2.9)	0.26 (2)	0.22 (1.6)	0.19 (1.4)
15	1280	320	294.4	2.4 (19)	1.6 (13)	1.1 (8.4)	0.82 (6)	0.55 (4)	0.38 (2.5)	0.3 (2.3)	0.26 (1.8)
8	2400	600	552	3.3 (25)	2.3 (16)	1.5 (12)	1.2 (8)	0.76 (6)	0.53 (4)	0.43 (3.2)	0.37 (2.7)
4	4800	1200	1104	4.9 (38)	3.4 (25)	2.4 (20)	2 (13)	1.3 (9.1)	0.83 (6.4)	0.68 (4.8)	0.58 (4.3)
2	9600	2400	2208	8.8 (76)	6.8 (61)	4.9 (34)	4.3 (27)	2.6 (21)	1.7 (13)	1.3 (12)	1.2 (9.4)
1	19,200	4800	4416	72 (500)	38 (270)	21 (150)	13 (95)	7.5 (57)	4.4 (33)	3.3 (26)	2.8 (23)

Table 8. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.4	2.34	24 (21.7)	24 (21.4)	23.7 (21)	23.1 (20.5)	22.7 (20.2)	22.3 (19.8)	21.6 (19)	20.7 (18.1)
1920	10	2.5	24 (21.7)	24 (21.4)	23.7 (21)	23 (20.5)	22.6 (20.1)	22.3 (19.7)	21.6 (19)	20.7 (18.1)
960	20	5	23.9 (21.2)	23.5 (20.8)	23.2 (20.4)	22.5 (20)	22.1 (19.5)	21.8 (19.2)	21.1 (18.4)	20.1 (19.4)
480	40	10	23.5 (20.7)	23 (20.3)	22.6 (19.8)	22.1 (19.3)	21.7 (18.9)	21.2 (18.6)	20.5 (17.8)	19.8 (17.1)
384	50	12.5	23.3 (20.5)	22.9 (20.2)	22.5 (19.6)	21.9 (19.1)	21.5 (18.7)	21.1 (18.5)	20.4 (17.7)	19.6 (17)
320	60	15	23.2 (20.3)	22.8 (20)	22.4 (19.5)	21.8 (19)	21.4 (18.6)	21 (18.3)	20.2 (17.6)	19.4 (16.6)
240	80	20	23 (20)	22.6 (19.7)	22.1 (19.3)	21.6 (18.9)	21.2 (18.5)	20.7 (18.1)	20 (17.3)	19.2 (16.4)
120	160	40	22.5 (19.5)	22.1 (19.2)	21.7 (18.9)	21 (18.3)	20.6 (18)	20.1 (17.5)	19.5 (16.9)	18.6 (16)
60	320	80	22 (19.1)	21.6 (18.6)	21.2 (18.2)	20.6 (17.8)	20.2 (17.4)	19.7 (17)	19 (16.3)	18.1 (15.5)
30	640	160	21.5 (18.5)	21.1 (18.1)	20.7 (17.7)	20.1 (17.2)	19.7 (16.8)	19.2 (16.3)	18.5 (15.6)	17.6 (14.8)
15	1280	320	21 (18)	20.5 (17.6)	20.2 (17.2)	19.5 (16.7)	19.1 (16.3)	18.7 (15.9)	18 (15.1)	17.2 (14.4)
8	2400	600	20.5 (17.5)	20.1 (17.2)	19.7 (16.7)	19 (16.2)	18.6 (15.7)	18.2 (15.3)	17.5 (14.6)	16.7 (13.8)
4	4800	1200	20 (17)	19.5 (16.5)	19 (16)	18.3 (15.6)	17.9 (15.1)	17.5 (14.6)	16.8 (14)	16 (13.2)
2	9600	2400	19.1 (16)	18.5 (15.3)	18 (15.1)	17.2 (14.5)	16.9 (13.9)	16.5 (13.5)	15.9 (12.7)	15 (12)
1	19,200	4800	16.1 (13.3)	16 (13.2)	15.9 (13)	15.5 (12.7)	15.4 (12.4)	15.1 (12.2)	14.6 (11.5)	13.8 (10.8)

Sinc³

Table 9. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.4	3.13	2.56	0.37 (1.5)	0.15 (0.89)	0.096 (0.58)	0.07 (0.38)	0.046 (0.25)	0.033 (0.16)	0.023 (0.11)	0.017 (0.09)
1920	10	3.33	2.72	0.24 (1.5)	0.15 (0.89)	0.096 (0.6)	0.07 (0.4)	0.05 (0.26)	0.034 (0.17)	0.023 (0.12)	0.018 (0.09)
1280	20	5	5.44	0.31 (1.8)	0.18 (1.2)	0.12 (0.82)	0.09 (0.55)	0.059 (0.35)	0.041 (0.24)	0.033 (0.18)	0.027 (0.14)
640	30	10	8.16	0.4 (2.6)	0.26 (1.6)	0.17 (1.2)	0.11 (0.82)	0.088 (0.52)	0.055 (0.36)	0.048 (0.27)	0.039 (0.22)
384	50	16.67	13.6	0.53 (3.3)	0.3 (2.2)	0.2 (1.6)	0.17 (1.1)	0.1 (0.75)	0.075 (0.51)	0.062 (0.39)	0.056 (0.33)
320	60	20	16.32	0.55 (3.6)	0.37 (2.4)	0.24 (1.8)	0.19 (1.3)	0.12 (0.8)	0.084 (0.54)	0.068 (0.44)	0.06 (0.37)
160	120	40	32.64	0.78 (5.1)	0.53 (3.4)	0.35 (2.3)	0.26 (1.8)	0.17 (1.1)	0.12 (0.85)	0.1 (0.66)	0.097 (0.55)
80	240	80	65.28	1.1 (7)	0.73 (4.9)	0.49 (3.2)	0.37 (2.6)	0.25 (1.6)	0.17 (1.2)	0.14 (1)	0.12 (0.78)
40	480	160	130.56	1.5 (11)	1.1 (6.8)	0.67 (4.5)	0.52 (3.7)	0.34 (2.2)	0.25 (1.7)	0.19 (1.4)	0.17 (1.2)
20	960	320	261.12	2.3 (16)	1.5 (9.8)	0.99 (6.6)	0.75 (5.1)	0.53 (3.5)	0.35 (2.4)	0.28 (2.1)	0.25 (1.8)
10	1920	640	522.24	3.2 (26)	2.2 (16)	1.5 (11)	1.1 (8.5)	0.73 (5.5)	0.49 (3.9)	0.4 (3.2)	0.35 (2.7)
6	3200	1066.67	870.4	4.9 (38)	3.2 (24)	2.1 (15)	1.6 (12)	1 (7.7)	0.68 (5.6)	0.56 (4.2)	0.48 (3.6)
3	6400	2133.33	1740.8	25 (170)	13 (89)	7.1 (54)	4.3 (35)	2.4 (18)	1.5 (11)	1.1 (8.4)	0.9 (6.7)
2	9600	3200	2611.2	110 (820)	54 (390)	28 (210)	14 (110)	7.4 (57)	3.9 (27)	2.3 (17)	1.7 (13)
1	19,200	6400	5222.4	890 (6500)	430 (3000)	220 (1500)	110 (790)	55 (390)	28 (190)	14 (100)	7.6 (56)

Table 10. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.4	3.13	24 (21.7)	24 (21.4)	23.6 (21)	23.1 (20.6)	22.7 (20.3)	22.2 (19.9)	21.7 (19.3)	21 (18.7)
1920	10	3.33	24 (21.7)	24 (21.4)	23.6 (21)	23.1 (20.6)	22.6 (20.2)	22.2 (19.8)	21.7 (19.3)	21 (18.7)
1280	20	5	24 (21.4)	23.7 (21)	23.2 (20.5)	22.7 (20.1)	22.3 (19.8)	21.9 (19.3)	21.2 (18.7)	20.5 (18.1)
640	30	10	23.6 (20.9)	23.2 (20.5)	22.8 (20)	22.2 (19.5)	21.8 (19.2)	21.4 (18.7)	20.6 (18.1)	19.9 (17.4)
384	50	16.67	23.2 (20.5)	22.8 (20.1)	22.4 (19.6)	21.8 (19.1)	21.4 (18.7)	21 (18.2)	20.3 (17.6)	19.4 (16.9)
320	60	20	23.1 (20.4)	22.7 (20)	22.3 (19.4)	21.7 (18.9)	21.3 (18.6)	20.8 (18.1)	20.1 (17.4)	19.3 (16.7)
160	120	40	22.6 (19.9)	22.2 (19.5)	21.8 (19)	21.2 (18.4)	20.8 (18.1)	20.3 (17.5)	19.6 (26.9)	18.7 (16.1)
80	240	80	22.1 (19.4)	21.7 (19)	21.3 (18.6)	20.7 (17.9)	20.3 (17.6)	19.8 (17)	19.1 (16.3)	18.3 (15.6)
40	480	160	21.6 (18.8)	21.2 (18.5)	20.8 (18.1)	20.2 (17.4)	19.8 (17.1)	19.3 (16.5)	18.6 (15.8)	17.8 (15)
20	960	320	21.1 (18.3)	20.7 (18)	20.3 (17.5)	19.7 (16.9)	19.2 (16.4)	18.8 (16)	18.1 (15.2)	17.3 (14.4)
10	1920	640	20.6 (17.6)	20.1 (17.2)	19.7 (16.8)	19.1 (16.2)	18.7 (15.8)	18.3 (15.3)	17.6 (14.6)	16.8 (13.8)
6	3200	1066.67	19.9 (17)	19.6 (16.6)	19.2 (16.3)	18.6 (15.6)	18.2 (15.3)	17.8 (14.8)	17.1 (14.2)	16.3 (13.4)
3	6400	2133.33	17.6 (14.8)	17.6 (14.8)	17.4 (14.5)	17.2 (14.1)	17 (14.1)	16.7 (13.8)	16.3 (13.2)	15.4 (12.5)
2	9600	3200	15.5 (12.6)	15.5 (12.6)	15.4 (12.6)	15.4 (12.5)	15.4 (12.4)	15.3 (12.5)	15 (12.2)	14.5 (11.6)
1	19,200	6400	12.5 (9.7)	12.5 (9.7)	12.5 (9.7)	12.5 (9.6)	12.5 (9.6)	12.4 (9.6	12.4 (9.6)	12.3 (9.5)

Post Filters

Table 11. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Full Power Mode

Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	0.51 (3.3)	0.34 (2.1)	0.21 (1.3)	0.16 (0.97)	0.11 (0.65)	0.075 (0.41)	0.062 (0.34)	0.051(0.3)
20	0.53 (3.3)	0.36 (2.1)	0.23 (1.3)	0.18 (1)	0.11 (0.65)	0.078 (0.45)	0.062 (0.34)	0.051 (0.3)
25	0.57 (3.6)	0.37 (2.2)	0.25 (1.6)	0.18 (1.2)	0.12 (0.75)	0.082 (0.47)	0.062 (0.38)	0.055 (0.31)
27.27	0.6 (3.9)	0.38 (2.2)	0.26 (1.6)	0.19 (1.2)	0.13 (0.82)	0.084 (0.55)	0.072 (0.44)	0.063 (0.43)

Table 12. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode

Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	23.2 (20.5)	22.8 (20.2)	22.5 (19.9)	21.9 (19.3)	21.5 (18.9)	21 (18.5)	20.3 (17.8)	19.5 (17)
20	23.2 (20.5)	22.7 (20.2)	22.3 (19.9)	21.7 (19.2)	21.5 (18.9)	20.9 (18.4)	20.3 (17.8)	19.5 (17)
25	23.1 (20.4)	22.7 (20.1)	22.2 (19.6)	21.7 (19)	21.3 (18.7)	20.9 (18.3)	20.3 (17.7)	19.5 (17)
27.27	23 (20.3)	22.6 (20.1)	22.2 (19.5)	21.7 (19)	21.2 (18.5)	20.8 (18.1)	20.1 (17.4)	19.2 (16.5)

Fast Settling Filter ($Sinc^4$ + $Sinc^1$)

Table 13. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	2.63	0.19 (1.2)	0.11 (0.75)	0.077 (0.52)	0.063 (0.34)	0.036 (0.21)	0.027 (0.17)	0.021 (0.11)	0.019 (0.098)
120	8.42	0.32 (2.1)	0.2 (1.3)	0.13 (0.97)	0.1 (0.63)	0.067 (0.46)	0.045 (0.28)	0.039 (0.23)	0.031 (0.2)
24	42.11	0.69 (4.6)	0.44 (3)	0.29 (2.1)	0.23 (1.6)	0.14 (0.99)	0.1 (0.72)	0.081 (0.54)	0.07 (0.49)
20	50.53	0.71 (5.1)	0.49 (3.1)	0.3 (2.2)	0.25 (1.7)	0.16 (1.1)	0.11 (0.78)	0.09 (0.6)	0.082 (0.57)
2	505.26	2.4 (18)	1.6 (10)	1.1 (8.3)	0.87 (5.5)	0.56 (3.5)	0.47 (2.9)	0.33 (2.1)	0.3 (2)
1	1010.53	4.8 (35)	3 (20)	1.9 (12)	1.4 (8.8)	0.89 (5.2)	0.57 (3.7)	0.49 (3)	0.44 (3)

Table 14. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	2.63	24 (22)	24 (21.7)	23.9 (21.2)	23.3 (20.8)	23 (20.5)	22.5 (19.8)	21.8 (19.5)	21 (18.6)
120	8.42	23.9 (21.2)	23.6 (20.8)	23.3 (20.3)	22.5 (19.9)	22.2 (19.4)	21.9 (19.1)	20.9 (18.4)	20.2 (17.6)
24	42.11	22.8 (20)	22.4 (19.7)	22.1 (19.2)	21.4 (18.6)	21.1 (18.3)	20.5 (17.7)	19.9 (17.1)	19.1 (16.3)
20	50.53	22.7 (19.9)	22.3 (19.6)	22 (19.1)	21.2 (18.5)	20.9 (18.1)	20.4 (17.6)	19.7 (17)	18.9 (16.1)
2	505.26	21 (18.1)	20.6 (17.9)	20.2 (17.2)	19.5 (16.8)	19.1 (16.4)	18.4 (15.7)	17.8 (15.2)	17 (14.3)
1	1010.53	20 (17.1)	19.7 (16.9)	19.3 (16.6)	18.8 (16.1)	18.4 (15.9)	18.1 (15.4)	17.3 (14.7)	16.5 (13.7)

Fast Settling Filter ($Sinc^3$ + $Sinc^1$)

Table 15. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	2.78	0.22 (1.4)	0.13 (0.75)	0.081 (0.44)	0.048 (0.3)	0.039 (0.24)	0.026 (0.18)	0.025 (0.13)	0.019 (0.11)
120	8.89	0.31 (2.1)	0.21 (1.3)	0.13 (0.89)	0.1 (0.63)	0.068 (0.47)	0.047 (0.28)	0.036 (0.25)	0.033 (0.17)
24	44.44	0.7 (4.8)	0.46 (3.1)	0.29 (2.1)	0.22 (1.5)	0.14 (0.95)	0.098 (0.67)	0.079 (0.56)	0.071 (0.44)
20	53.33	0.77 (5.2)	0.5 (3.4)	0.31 (2.3)	0.24 (1.6)	0.17 (1)	0.11 (0.73)	0.09 (0.66)	0.077 (0.48)
2	533.33	6.1 (46)	3.2 (23)	1.8 (12)	1.1 (7.5)	0.65 (4.3)	0.4 (2.7)	0.31 (2.2)	0.27 (2)
1	1066.67	44 (320)	22 (160)	11 (80)	5.7 (40)	2.9 (22)	1.5 (11)	0.83 (6.2)	0.54 (4)

Table 16. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	2.78	24 (21.8)	24 (21.7)	23.9 (21.4)	23.6 (21)	22.9 (20.3)	22.5 (19.8)	21.6 (19.2)	21 (18.4)
120	8.89	24 (21.2)	23.5 (20.9)	23.2 (20.4)	22.6 (19.9)	22.1 (19.4)	21.7 (19.1)	21 (18.3)	20.2 (17.8)
24	44.44	22.8 (20)	22.4 (19.6)	22.1 (19.2)	21.4 (18.7)	21.1 (18.3)	20.6 (17.8)	19.9 (17.1)	19.1 (16.5)
20	53.33	22.6 (19.9)	22.3 (19.5)	22 (19.1)	21.3 (18.6)	20.8 (18.2)	20.4 (17.7)	19.7 (16.9)	19 (16.3)
2	533.33	19.7 (16.8)	19.6 (16.8)	19.4 (16.6)	19.1 (16.3)	18.9 (16.1)	18.6 (15.8)	17.9 (15.1)	17.2 (14.3)
1	1066.67	16.8 (13.9)	16.8 (13.9)	16.8 (13.9)	16.7 (13.9)	16.7 (13.8)	16.6 (13.8)	16.5 (13.6)	16.1 (13.3)

MID POWER MODE

Sinc⁴

Table 17. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.586	0.078	0.22 (1.4)	0.14 (0.88)	0.095 (0.6)	0.062 (0.38)	0.048 (0.24)	0.036 (0.17)	0.024 (0.14)	0.02 (0.1)
1920	2.5	0.625	0.575	0.25 (1.4)	0.17 (0.88)	0.11 (0.6)	0.073 (0.38)	0.048 (0.24)	0.037 (0.19)	0.024 (0.14)	0.021 (0.1)
960	5	1.25	1.15	0.34 (2)	0.21 (1.2)	0.13 (0.77)	0.085 (0.52)	0.064 (0.36)	0.052(0.25)	0.04 (0.21)	0.035 (0.2)
480	10	2.5	2.3	0.44 (2.8)	0.28 (1.8)	0.19 (1.1)	0.1 (0.82)	0.1 (0.55)	0.072 (0.41)	0.057 (0.34)	0.048 (0.28)
240	20	5	4.6	0.67 (3.8)	0.4 (2.4)	0.27 (1.6)	0.2 (1.1)	0.14 (0.85)	0.098 (0.64)	0.081 (0.47)	0.07 (0.43)
120	40	10	9.2	0.98 (6)	0.58 (3.6)	0.37 (2.3)	0.27 (1.7)	0.2 (1.1)	0.14 (0.87)	0.11 (0.74)	0.09 (0.57)
96	50	12.5	11.5	1 (7.4)	0.67 (4.2)	0.41 (2.5)	0.28 (1.9)	0.23 (1.3)	0.15 (0.95)	0.13 (0.78)	0.11 (0.7)
80	60	15	13.8	1.1 (7.2)	0.7 (4.3)	0.44 (3)	0.33 (2.1)	0.24 (1.4)	0.17 (1.1)	0.14 (0.89)	0.12 (0.75)
60	80	20	18.4	1.3 (8.4)	0.8 (5.1)	0.53 (3.4)	0.37 (2.4)	0.27 (1.6)	0.2 (1.3)	0.18 (1.1)	0.13 (0.82)
30	160	40	36.8	1.8 (11)	1.2 (7.6)	0.73 (4.6)	0.54 (3.4)	0.39 (2.4)	0.28 (1.9)	0.23 (1.4)	0.19 (1.2)
15	320	80	73.6	2.6 (17)	1.7 (11)	1 (6.6)	0.79 (4.7)	0.58 (3.4)	0.4 (2.5)	0.33 (2)	0.26 (1.5)
8	600	150	138	3.7 (23)	2.3 (15)	1.5 (9.6)	1.2 (7.2)	0.84 (5)	0.56 (4)	0.46 (2.8)	0.4 (2.6)
4	1200	300	276	5.3 (36)	3.6 (24)	2.4 (16)	1.9 (13)	1.3 (8.2)	0.85 (6)	0.68 (4.3)	0.6 (4.5)
2	2400	600	552	9.3 (72)	6.8 (53)	4.8 (35)	4.1 (34)	2.5 (19)	1.7 (13)	1.3 (10)	1.2 (9.7)
1	4800	1200	1104	71 (500)	37 (270)	21 (160)	13 (98)	7.2 (55)	4.3 (33)	3.1 (24)	2.6 (21)

Table 18. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.586	24 (21.8)	24 (21.4)	23.6 (21)	23.3 (20.6)	22.6 (20.3)	22.1 (19.7)	21.6 (19.1)	20.9 (18.5)
1920	2.5	0.625	24 (21.8)	23.8 (21.4)	23.5 (21)	23 (20.6)	22.6 (20.3)	22 (19.7)	21.6 (19.1)	20.8 (18.5)
960	5	1.25	23.8 (21.2)	23.5 (21)	23.2 (20.6)	22.8 (20.2)	22.2 (19.7)	21.5 (19.2)	20.9 (18.5)	20.1 (17.6)
480	10	2.5	23.4 (20.8)	23.1 (20.4)	22.7 (20.1)	22.2 (19.6)	21.5 (19.1)	21 (18.5)	20.4 (17.8)	19.6 (17.1)
240	20	5	22.8 (20.3)	22.5 (20)	22.1 (19.6)	21.6 (19.1)	21.1 (18.5)	20.6 (17.9)	19.9 (17.3)	19.1 (16.5)
120	40	10	22.3 (19.7)	22 (19.4)	21.7 (19)	21.1 (18.5)	20.6 (18.1)	20.1 (17.5)	19.4 (16.8)	18.7 (16)
96	50	12.5	22.2 (19.5)	21.8 (19.2)	21.5 (18.9)	21 (18.3)	20.4 (17.9)	19.9 (17.3)	19.2 (16.6)	18.5 (15.8)
80	60	15	22.1 (19.4)	21.7 (19.1)	21.4 (18.7)	20.9 (18.2)	20.3 (17.8)	19.8 (17.2)	19.1 (16.4)	18.4 (15.7)
60	80	20	21.9 (19.2)	21.5 (18.9)	21.1 (18.5)	20.7 (18)	20.1 (17.6)	19.6 (16.9)	18.9 (16.2)	18.2 (15.5)
30	160	40	21.4 (18.8)	21 (18.9)	20.7 (18.5)	20.2 (17.5)	19.6 (17)	19.1 (16.3)	18.4 (15.8)	17.7 (15)
15	320	80	20.9 (18.2)	20.5 (17.8)	20.2 (17.5)	19.6 (17)	19 (16.5)	18.6 (15.9)	17.9 (15.3)	17.2 (14.6)
8	600	150	20.4 (17.7)	20 (17.3)	19.7 (17)	19 (16.4)	18.5 (15.9)	18.1 (15.3)	17.4 (14.8)	16.6 (13.9)
4	1200	300	19.8 (17.1)	19.4 (16.7)	19 (16.3)	18.3 (15.6)	17.9 (15.2)	17.5 (14.7)	16.8 (14)	16 (13.1)
2	2400	600	19 (16.1)	18.5 (15.5)	18 (15.1)	17.2 (14.2)	16.9 (14)	16.5 (13.6)	15.8 (12.9)	15 (12)
1	4800	1200	16.1 (13.3)	16 (13.2)	15.9 (12.9)	15.5 (12.6)	15.4 (12.5)	15.1 (12.2)	14.6 (11.7)	13.9 (10.9)

Sinc³

Table 19. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.78	0.64	0.25 (1.5)	0.17 (1)	0.087 (0.58)	0.065 (0.4)	0.049 (0.27)	0.034 (0.19)	0.03 (0.16)	0.022 (0.11)
960	5	1.67	1.36	0.35 (2.2)	0.23 (1.3)	0.14 (0.82)	0.1 (0.58)	0.074 (0.43)	0.053 (0.31)	0.041 (0.22)	0.034 (0.17)
480	10	3.33	2.72	0.5 (3.1)	0.31 (1.9)	0.19 (1.3)	0.14 (0.89)	0.1 (0.63)	0.075 (0.44)	0.6 (0.35)	0.049 (0.28)
320	15	5	4.08	0.6 (3.8)	0.38 (2.4)	0.24 (1.6)	0.17 (1.1)	0.13 (0.8)	0.089 (0.54)	0.076 (0.46)	0.062 (0.35)
160	30	10	8.16	0.83 (5.6)	0.54 (3.3)	0.34 (2.2)	0.24 (1.6)	0.18 (1.1)	0.13 (0.77)	0.1 (0.65)	0.088 (0.53)
96	50	16.67	13.6	1.1 (7.5)	0.72 (4.4)	0.44 (2.9)	0.31 (2)	0.24 (1.5)	0.17 (1)	0.14 (0.82)	0.11 (0.7)
80	60	20	16.32	1.2 (7.7)	0.8 (4.8)	0.48 (3.1)	0.35 (2.2)	0.25 (1.6)	0.18 (1.1)	0.15 (0.94)	0.12 (0.77)
40	120	40	32.64	1.7 (11)	1.1 (7)	0.7 (4.6)	0.47 (3.2)	0.36 (2.2)	0.26 (1.7)	0.21 (1.5)	0.18 (1.1)
20	240	80	65.28	2.5 (16)	1.6 (9.7)	0.94 (6.2)	0.7 (5)	0.53 (3.2)	0.37 (2.3)	0.31 (2.1)	0.26 (1.8)
10	480	160	130.6	3.5 (24)	2.2 (15)	1.4 (9.3)	1 (7)	0.78 (5.3)	0.56 (3.9)	0.46 (3.1)	0.38 (2.5)
5	960	320	261.1	6.7 (53)	4.1 (34)	2.5 (19)	1.8 (14)	1.2 (8.7)	0.84 (6.4)	0.67 (5)	0.57 (3.9)
3	1600	533.33	435.2	25 (170)	13 (90)	7.1 (53)	4.2 (30)	2.4 (18)	1.5 (11)	1.1 (7.8)	0.89 (6.8)
2	2400	800	652.8	110 (740)	54 (360)	27 (200)	14 (110)	7.4 (51)	3.9 (29)	2.3 (16)	1.6 (12)
1	4800	1600	1306	880 (5800)	430 (3100)	220 (1500)	110 (760)	55 (400)	27 (180)	14 (110)	7.5 (56)

Table 20. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.78	24 (21.7)	23.8 (21.2)	23.6 (21)	23.2 (20.6)	22.6 (20.1)	22.1 (19.6)	21.3 (18.9)	20.7 (18.4)
960	5	1.67	23.8 (21.1)	23.4 (20.8)	23.1 (20.5)	22.6 (20)	22 (19.5)	21.5 19)	20.8 (18.4)	20.1 (17.8)
480	10	3.33	23.3 (20.6)	22.9 (20.3)	22.6 (19.9)	22.1 (19.4)	21.5 (18.9)	21 (18.4)	20.3 (17.8)	19.6 (17.1)
320	15	5	23 (20.3)	22.6 (20)	22.3 (19.6)	21.8 (19.1)	21.2 (18.6)	20.7 (18.1)	20 (17.4)	19.3 (16.8)
160	30	10	22.5 (19.8)	22.1 (19.5)	21.8 (19.1)	21.3 (18.6)	20.7 (18.1)	20.2 (17.6)	19.5 (16.9)	18.8 (16.2)
96	50	16.67	22.1 (19.4)	21.7 (19.1)	21.4 (18.7)	20.9 (18.2)	20.3 (17.7)	19.8 (17.2)	19.1 (16.5)	18.4 (15.8)
80	60	20	22 (19.3)	21.6 (19)	21.3 (18.6)	20.8 (18.1)	20.2 (17.6)	19.7 (17.1)	19.1 (16.3)	18.3 (15.6)
40	120	40	21.5 (18.8)	21.1 (18.5)	20.8 (18.1)	20.3 (17.6)	19.7 (17.1)	19.2 (16.5)	18.5 (15.7)	17.7 (15.1)
20	240	80	21 (18.3)	20.6 (18)	20.3 (17.6)	19.8 (17)	19.2 (16.6)	18.7 (16)	18 (15.2)	17.2 (14.4)
10	480	160	20.4 (17.7)	20.1 (17.3)	19.8 (17)	19.2 (16.4)	18.6 (15.9)	18.1 (15.3)	17.4 (14.6)	16.7 (13.9)
5	960	320	19.5 (16.5)	19.2 (16.2)	19 (16)	18.4 (15.4)	18 (15.1)	17.5 (14.6)	16.8 (13.9)	16.1 (13.3)
3	1600	533.33	17.6 (14.8)	17.5 (14.8)	17.4 (14.5)	17.2 (14.3)	17 (14.1)	16.7 (13.8)	16.1 (13.3)	15.4 (12.6)
2	2400	800	15.5 (12.7)	15.5 (12.7)	15.5 (12.6)	15.4 (12.6)	15.4 (12.6)	15.3 (12.4)	15 (12.3)	14.6 (11.7)
1	4800	1600	12.5 (9.7)	12.5 (9.7)	12.5 (9.7)	12.5 (9.7)	12.5 (9.6)	12.5 (9.6)	12.4 (9.5)	12.4 (9.4)

Post Filters

Table 21. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Mid Power Mode

Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	1.1 (6.3)	0.69 (4)	0.41 (2.5)	0.31 (2)	0.23 (1.4)	0.17 (0.96)	0.13 (0.79)	0.11 (0.61)
20	1.1 (6.9)	0.7 (4)	0.41 (2.5)	0.33 (2.1)	0.23 (1.5)	0.18 (0.96)	0.14 (0.81)	0.12 (0.67)
25	1.2 (8)	0.8 (4.6)	0.46 (2.8)	0.36 (2.3)	0.25 (1.5)	0.17 (1)	0.15 (0.9)	0.12 (0.74)
27.27	1.3 (9.2)	0.82 (4.8)	0.48 (2.8)	0.36 (2.3)	0.28 (1.6)	0.19 (1.1)	0.16 (1)	0.13 (0.79)

Table 22. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	22.1 (19.6)	21.8 (19.2)	21.5 (18.9)	20.9 (18.3)	20.4 (17.8)	19.8 (17.3)	19.2 (16.6)	18.4 (16)
20	22.1 (19.5)	21.8 (19.2)	21.5 (18.9)	20.9 (18.2)	20.4 (17.7)	19.8 (17.3)	19 (16.6)	18.3 (15.8)
25	22 (19.2)	21.6 (19.1)	21.4 (18.8)	20.7 (18.1)	20.3 (17.6)	19.7 (17.2)	18.9 (16.4)	18.2 (15.7)
27.27	21.9 (19)	21.5 (19)	21.3 (18.8)	20.7 (18.1)	21.1 (17.6)	19.7 (17.1)	18.9 (16.3)	18.2 (15.6)

Fast Settling Filter (Sinc[4] + Sinc[1])

Table 23. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.63	0.36 (2.4)	0.23 (1.5)	0.15 (0.82)	0.1 (0.71)	0.078 (0.44)	0.056 (0.35)	0.045 (0.26)	0.038 (0.21)
30	8.42	0.67 (4.2)	0.44 (2.7)	0.26 (1.6)	0.18 (1.1)	0.14 (0.8)	0.1 (0.54)	0.08 (0.48)	0.067 (0.41)
6	42.11	1.5 (9)	0.96 (6.1)	0.57 (3.7)	0.42 (2.6)	0.32 (1.9)	0.22 (1.5)	0.18 (1.1)	0.15 (0.95)
5	50.53	1.6 (9.3)	1 (7.7)	0.62 (4)	0.46 (3)	0.33 (2)	0.24 (1.6)	0.2 (1.3)	0.17 (1.2)
2	126.32	2.5 (15)	1.6 (11)	1 (7.2)	0.76 (4.9)	0.57 (3.7)	0.41 (2.7)	0.32 (2.4)	0.29 (1.9)
1	252.63	5.2 (21)	3.1 (19)	1.8 (11)	1.4 (9.8)	0.92 (6.2)	0.62 (4.2)	0.49 (3)	0.41 (3)

Table 24. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.63	23.7 (21)	23.4 (20.7)	23 (20.5)	22.5 (19.8)	21.9 (19.4)	21.4 (18.8)	20.7 (18.2)	20 (17.5)
30	8.42	22.8 (20.2)	22.4 (19.8)	22.2 (19.5)	21.7 (19.1)	21 (18.6)	20.6 (18.1)	19.9 (17.3)	19.1 (16.5)
6	42.11	21.7 (19.1)	21.3 (18.6)	21.1 (18.4)	20.5 (17.9)	19.9 (17.3)	19.4 (16.7)	18.7 (16)	18 (15.2)
5	50.53	21.5 (19)	21.2 (18.4)	20.9 (18.2)	20.4 (17.8)	19.8 (17.2)	19.3 (16.6)	18.5 (15.9)	17.8 (15)
2	126.32	20.9 (18.3)	20.5 (17.8)	20.2 (17.4)	19.6 (17)	19.1 (16.4)	18.6 (15.8)	17.9 (15.2)	17.1 (14.3)
1	252.63	19.9 (17.3)	19.6 (17)	19.4 (16.8)	18.8 (16)	18.4 (15.6)	17.9 (15.2)	17.3 (14.7)	16.5 (13.7)

Fast Settling Filter (Sinc[3] + Sinc[1])

Table 25. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.78	0.39 (2.4)	0.25 (1.5)	0.16 (1)	0.11 (0.67)	0.08 (0.48)	0.058 (0.31)	0.047 (0.27)	0.039 (0.23)
30	8.89	0.71 (4.2)	0.43 (2.5)	0.27 (1.6)	0.19 (1.1)	0.15 (1)	0.098 (0.64)	0.083 (0.47)	0.068 (0.4)
6	44.44	1.5 (9.5)	0.93 (6)	0.59 (3.8)	0.43 (2.6)	0.32 (2.1)	0.22 (1.5)	0.18 (1.1)	0.15 (0.98)
5	53.33	1.6 (11)	1 (6.9)	0.66 (4.2)	0.46 (2.8)	0.35 (2.3)	0.24 (1.6)	0.2 (1.2)	0.17 (1.1)
2	133.33	6 (37)	3.2 (20)	1.8 (11)	1 (7.2)	0.63 (4.5)	0.31 (3)	0.33 (2.2)	0.27 (1.8)
1	266.67	44 (320)	23 (160)	12 (83)	5.7 (41)	3 (20)	1.6 (9.9)	0.84 (6.4)	0.56 (3.5)

Table 26. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.78	23.6 (21)	23.3 (20.7)	22.9 (20.3)	22.5 (19.8)	21.9 (19.3)	21.4 (18.9)	20.7 (18.1)	19.9 (17.4)
30	8.89	22.7 (20.2)	22.5 (19.9)	22.2 (19.6)	21.7 (19.1)	21 (18.3)	20.6 (17.9)	19.8 (17.3)	19.1 (16.6)
6	44.44	21.7 (19)	21.4 (18.7)	21 (18.3)	20.5 (17.9)	19.9 (17.2)	19.4 (16.7)	18.7 (16.1)	18 (15.3)
5	53.33	21.5 (18.8)	21.2 (18.5)	20.9 (18.2)	20.4 (17.8)	19.8 (17.1)	19.3 (16.6)	18.6 (16)	17.8 (15.1)
2	133.33	19.7 (17)	19.6 (16.9)	19.4 (16.8)	19.2 (16.4)	18.9 (16.1)	18.5 (15.7)	17.8 (15.1)	17.1 (14.4)
1	266.67	16.8 (13.9)	16.7 (13.9)	16.7 (13.9)	16.7 (13.9)	16.7 (13.9)	16.6 (13.9)	16.5 (13.6)	16.1 (13.4)

LOW POWER MODE

Sinc⁴

Table 27. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.293	0.269	0.22 (1.2)	0.15 (0.89)	0.095 (0.67)	0.071 (0.41)	0.053 (0.26)	0.043 (0.2)	0.035 (0.16)	0.024 (0.12)
1920	1.25	0.3125	0.288	0.24 (1.5)	0.15 (0.89)	0.095 (0.67)	0.071 (0.41)	0.053 (0.26)	0.043 (0.2)	0.035 (0.16)	0.024 (0.12)
960	2.5	0.625	0.575	0.37 (2.1)	0.23 (1.2)	0.13 (0.82)	0.1 (0.61)	0.068 (0.37)	0.055 (0.26)	0.041 (0.23)	0.035 (0.17)
480	5	1.25	1.15	0.5 (3)	0.3 (1.7)	0.18 (1.2)	0.13 (0.77)	0.099 (0.56)	0.078 (0.39)	0.06 (0.31)	0.052 (0.26)
240	10	2.5	2.3	0.65 (4.1)	0.42 (2.5)	0.26 (1.9)	0.2 (1.1)	0.14 (0.8)	0.1 (0.6)	0.085 (0.5)	0.072 (0.43)
120	20	5	4.6	0.9 (5.8)	0.61 (3.5)	0.38 (2.5)	0.28 (1.7)	0.2 1.2)	0.15 (0.85)	0.12 (0.68)	0.096 (0.6)
60	40	10	9.2	1.3 (8)	0.82 (5)	0.53 (3.7)	0.38 (2.4)	0.29 (1.8)	0.21 (1)	0.17 (0.95)	0.14 (0.9)
48	50	12.5	11.5	1.4 (9.3)	0.95 (6)	0.6 (4.2)	0.46 (2.8)	0.32 (2.1)	0.24 (1.5)	0.2 (1.1)	0.16 (1)
40	60	15	13.8	1.6 (10)	0.99 (6.6)	0.64 (4.5)	0.47 (3.2)	0.35 (2.2)	0.26 (1.7)	0.21 (1.3)	0.17 (1.1)
30	80	20	18.4	1.8 (12)	1.2 (7.5)	0.77 (5.1)	0.55 (3.7)	0.4 (2.7)	0.3 (2)	0.25 (1.6)	0.19 (1.3)
15	160	40	36.8	2.6 (17)	1.8 (11)	1.1 (7.2)	0.85 (5.7)	0.56 (3.9)	0.41 (2.5)	0.33 (2.1)	0.28 (1.6)
8	300	75	69	3.7 (24)	2.5 (17)	1.6 (11)	1.2 (7.5)	0.87 (5.6)	0.58 (3.9)	0.48 (2.9)	0.39 (2.6)
4	600	150	138	5.2 (35)	4 (24)	2.6 (17)	2.1 (13)	1.4 (8.5)	1 (6)	0.76 (5.2)	0.6 (3.9)
2	1200	300	276	9.4 (57)	7.6 (47)	5.8 (36)	4.9 (32)	3 (19)	1.9 (11)	1.4 (9)	1.3 (7.8)
1	2400	600	552	72 (470)	39 (240)	22 (130)	16 (110)	8 (49)	4.8 (29)	3.3 (21)	2.6 (18)

Table 28. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.29311	24 (21.7)	23.8 (21.4)	23.7 (20.9)	23.2 (20.5)	22.7 (20.2)	21.8 (19.7)	21.3 (18.9)	20.6 (18.3)
1920	1.25	0.3125	24 (21.7)	23.8 (21.3)	23.6 (20.8)	23.1 (20.5)	22.6 (20.1)	21.8 (19.6)	21.2 (18.9)	20.6 (18.3)
960	2.5	0.625	23.7 (21.2)	23.4 (21)	23.2 (20.5)	22.6 (20)	22.1 (19.7)	21.4 (19.2)	20.8 (18.4)	20.1 (17.8)
480	5	1.25	23.3 (20.7)	23 (20.5)	22.7 (20)	22.1 (19.6)	21.6 (19.1)	20.9 (18.6)	20.3 (17.9)	19.5 (17.2
240	10	2.5	22.9 (20.2)	22.5 (19.9)	22.2 (19.4)	21.6 (19.1)	21.1 (18.6)	20.5 (18)	19.8 (17.2)	19.1 (16.5)
120	20	5	22.4 (19.7)	22 (19.4)	21.7 (18.9)	21.1 (18.5)	20.6 (18)	20 (17.5)	19.3 (16.8)	18.6 (16)
60	40	10	21.9 (19.2)	21.5 (18.9)	21.2 (18.4)	20.6 (18)	20.1 (17.4)	19.5 (16.9)	18.8 (16.3)	18.1 (15.4)
48	50	12.5	21.7 (19)	21.3 (18.7)	21 (18.2)	20.4 (17.8)	19.9 (17.2)	19.3 (16.7)	18.6 (16.1)	17.9 (15.2)
40	60	15	21.6 (18.9)	21.2 (18.5)	20.9 (18.1)	20.3 (17.6)	19.8 (17.1)	19.2 (16.5)	18.5 (15.9)	17.8 (15.1)
30	80	20	21.4 (18.7)	21 (18.3)	20.6 (17.9)	20.1 (17.4)	19.6 (16.8)	19 (16.2)	18.3 (15.6)	17.6 (14.9)
15	160	40	20.9 (18.2)	20.4 (17.8)	20.1 (17.4)	19.5 (16.8)	19.1 (16.3)	18.5 (15.7)	17.8 (15.2)	17.1 (14.5)
8	300	75	20.4 (17.7)	19.9 (17.2)	19.6 (16.8)	19 (16.3)	18.5 (15.8)	18 (15.3)	17.3 (14.7)	16.6 (13.9)
4	600	150	19.9 (17.1)	19.3 (16.7)	18.9 (16.2)	18.2 (15.6)	17.8 (15.2)	17.3 (14.7)	16.7 (13.9)	16 (13.3)
2	1200	300	19 (16.4)	18.3 (15.7)	17.7 (15.1)	17 (14.3)	16.7 (14)	16.3 (13.8)	15.7 (13.1)	14.9 (12.3)
1	2400	600	16.1 (13.4)	16 (13.4)	15.8 (13.3)	15.3 (12.5)	15.2 (12.5)	15 (12.4)	14.5 (11.9)	13.9 (11)

Sinc³

Table 29. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.39	0.32	0.26 (1.5)	0.17 (0.9)	0.099 (0.6)	0.072 (0.36)	0.055 (0.27)	0.039 (0.21)	0.032 (0.16)	0.026 (0.13)
480	5	1.67	1.36	0.51 (3.1)	0.31 (1.9)	0.2 (1.3)	0.15 (0.86)	0.11 (0.65)	0.078 (0.45)	0.063 (0.37)	0.05 (0.28)
240	10	3.33	2.72	0.75 (4.5)	0.45 (2.8)	0.29 (2)	0.21 (1.3)	0.16 (0.9)	0.11 (0.65)	0.085 (0.51)	0.071 (0.39)
160	15	5	4.08	0.88 (5.5)	0.55 (3.3)	0.3 (2.4)	0.26 (1.6)	0.19 (1.2)	0.14 (0.79)	0.1 (0.62)	0.089 (0.53)
80	30	10	8.16	1.3 (7.8)	0.77 (4.9)	0.47 (3.3)	0.36 (2.2)	0.27 (1.7)	0.19 (1.2)	0.15 (0.94)	0.12 (0.72)
48	50	16.67	13.6	2.7 (9.9)	1 (6.4)	0.63 (4.6)	0.47 (3.1)	0.36 (2.2)	0.26 (1.7)	0.2 (1.3)	0.16 (1)
40	60	20	16.32	1.8 (12)	1.1 (7)	0.71 (5)	0.52 (3.4)	0.39 (2.5)	0.27 (1.8)	0.21 (1.4)	0.18 (1.3)
20	120	40	32.64	2.5 (17)	1.6 (10)	0.9 (6.1)7	0.73 (5)	0.55 (3.7)	0.41 (2.5)	0.3 (1.9)	0.26 (1.6)
10	240	80	65.28	3.5 (25)	2.4 (16)	1.5 (9.9)	1.1 (7.6)	0.8 (5.3)	0.56 (3.5)	0.45 (2.8)	0.37 (2.3)
5	480	160	130.6	6.8 (48)	4.3 (32)	2.6 (19)	2 (15)	1.3 (9)	0.9 (6.5)	0.7 (4.5)	0.55 (3.3)
3	800	266.67	217.6	25 (180)	13 (98)	7.4 (53)	4.5 (34)	2.7 (18)	1.6 (11)	1.1 (7.7)	0.91 (6)
2	1200	400	326.4	110 (740)	55 (390)	28 (180)	15 (100)	7.6 (57)	4 (32)	2.4 (16)	1.6 (12)
1	2400	800	652.8	870 (5600)	430 (2900)	220 (1400)	110 (670)	56 (370)	28 (180)	14 (100)	7.6 (52)

Table 30. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.39	24 (21.7)	23.8 (21.4)	23.6 (21)	23 (20.7)	22.4 (20.1)	21.9 (19.5)	21.2 (18.9)	20.5 (18.2)
480	5	1.67	23.2 (20.6)	22.9 (20.3)	22.6 (19.9)	22 (19.5)	21.4 (18.9)	20.9 (18.4)	20.2 (17.7)	19.6 (17.1)
240	10	3.33	22.7 (20.1)	22.4 (19.8)	22.1 (19.3)	21.5 (18.9)	20.9 (18.4)	20.4 (17.9)	19.8 (17.2)	19.1 (16.6)
160	15	5	22.4 (19.8)	22.1 (19.5)	21.8 (19)	21.2 (18.6)	20.6 (18)	20.1 (17.6)	19.5 (16.9)	18.8 (16.2)
80	30	10	21.9 (19.3)	21.6 (19)	21.3 (18.5)	20.7 (18.1)	20.1 (17.5)	19.6 (17)	19 (16.3)	18.3 (15.7)
48	50	16.67	21.5 (18.9)	21.2 (18.6)	20.9 (18.1)	20.3 (17.6)	19.7 (17.1)	19.2 (16.5)	18.6 (15.9)	17.9 (15.2)
40	60	20	21.4 (18.7)	21.1 (18.4)	20.8 (17.9)	20.2 (17.5)	19.6 (16.9)	19.1 (16.4)	18.5 (15.8)	17.7 (15.1)
20	120	40	20.9 (18.2)	20.6 (17.9)	20.3 (17.4)	19.7 (16.9)	19.1 (16.4)	18.6 (15.9)	18 (15.3)	17.2 (14.6)
10	120	80	20.4 (17.6)	20 (17.2)	19.7 (16.9)	19.1 (16.3)	18.6 (15.9)	18.1 (15.4)	17.4 (14.8)	16.7 (14.1)
5	480	160	19.5 (16.7)	19.2 (16.3)	18.8 (16)	18.2 (15.4)	17.9 (15.1)	17.4 (14.6)	16.8 (14.1)	16.1 (13.5)
3	800	266.67	17.6 (14.8)	17.5 (14.6)	17.4 (14.5)	17.1 (14.2)	16.8 (14.1)	16.6 (13.8)	16.1 (13.3)	15.4 (12.7)
2	1200	400	15.5 (12.7)	15.5 (12.7)	15.4 (12.7)	15.4 (12.6)	15.3 (12.4)	15.2 (12.3)	15 (12.2)	14.5 (11.6)
1	2400	800	12.5 (9.8)	12.5 (9.8)	12.5 (9.8)	12.5 (9.8	12.5 (9.7)	12.5 (9.7)	12.5 (9.6)	12.3 (9.6)

Post Filters

Table 31. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Low Power Mode

Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	1.7 (12)	0.96 (5.8)	0.65 (4)	0.45 (2.6)	0.34 (1.9)	0.25 (1.5)	0.2 (1.2)	0.16 (0.92)
20	1.7 (11)	1.1 (6.4)	0.65 (4.2)	0.46 (2.6)	0.36 (1.9)	0.26 (1.5)	0.21 (1.2)	0.17 (0.93)
25	1.8 (11)	1.1 (6.7)	0.68 (4.2)	0.52 (2.7)	0.37 (2)	0.26 (1.6)	0.22 (1.2)	0.17 (1.1)
27.27	1.9 (11)	1.1 (7.3)	0.69 (4.4)	0.54 (2.9)	0.4 (2.1)	0.27 (1.8)	0.23 (1.4)	0.18 (1.3)

Table 32. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode

Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	21.5 (18.8)	21.3 (18.7)	20.9 (18.2)	21.4 (17.9)	19.8 (17.3)	19.3 (16.7)	18.6 (16.1)	17.9 (15.4)
20	21.5 (18.8)	21.2 (18.6)	20.9 (18.2)	20.4 (17.9)	19.7 (17.3)	19.2 (16.7)	18.6 (16.1)	17.8 (15.4)
25	21.4 (18.8)	21.2 (18.5)	20.8 (18.2)	20.2 (17.8)	19.7 (17.3)	19.2 (16.6)	18.5 (15.9)	17.8 (15.1)
27.27	21.3 (18.7)	21.1 (18.4)	20.8 (18.1)	20.2 (17.7)	19.6 (17.2)	19.1 (16.4)	18.4 (15.8)	17.7 (14.9)

Fast Settling Filter (Sinc[4] + Sinc[1])

Table 33. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Low Power Mode (Average by 8)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.27	0.53 (3.4)	0.34 (2.2)	0.19 (1.2)	0.16 (0.97)	0.1 (0.61)	0.082 (0.48)	0.065 (0.38)	0.058 (0.37)
30	7.27	0.89 (5.4)	0.6 (3.6)	0.36 (2.2)	0.27 (1.8)	0.21 (1.2)	0.15 (0.93)	0.12 (0.65)	0.093 (0.59)
6	36.36	2.1 (12)	1.4 (8.3)	0.82 (5.6)	0.64 (3.9)	0.43 (2.7)	0.33 (2.1)	0.25 (1.6)	0.21 (1.4)
5	43.64	2.2 (13)	1.4 (9.7)	0.93 (6.5)	0.71 (4.2)	0.5 (3.1)	0.35 (2.4)	0.28 (1.7)	0.23 (1.5)
2	109.1	3.7 (25)	2.5 (18)	1.5 (10)	1.3 (7.5)	0.86 (5.6)	0.59 (3.5)	0.47 (3.2)	0.39 (2.4)
1	218.18	8.4 (52)	5.4 (34)	3.3 (21)	2.6 (16)	1.6 (9.8)	0.97 (6.1)	0.75 (5.4)	0.63 (4.7)

Table 34. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode (Average by 8)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.27	23.2 (20.5)	22.8 (20.1)	22.7 (20)	21.9 (19.3)	21.5 (19)	20.9 (18.3)	20.2 (17.6)	19.4 (16.7)
30	7.27	22.4 (19.8)	22 (19.4)	21.7 (19.1)	21.1 (18.4)	20.5 (18)	20 (17.4)	19.4 (16.9)	18.7 (16)
6	36.36	21.2 (18.6)	20.8 (18.1)	20.5 (17.8)	19.9 (17.3)	19.5 (16.8)	18.9 (16.2)	18.3 (15.6)	17.5 (14.8)
5	43.64	21.1 (18.5)	20.7 (18)	20.4 (17.6)	19.8 (17.2)	19.3 (16.6)	18.8 (16)	18.1 (15.5)	17.4 (14.7)
2	109.1	20.4 (17.6)	19.9 (17.1)	19.6 (16.9)	18.9 (16.3)	18.5 (15.8)	18 (15.4)	17.3 (14.6)	16.6 (14)
1	218.18	19.2 (16.6)	18.8 (16.2)	18.5 (15.9)	17.9 (15.2)	17.6 (15)	17.3 (14.7)	16.7 (13.8)	15.9 (13)

Fast Settling Filter (Sinc[3] + Sinc[1])

Table 35. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Low Power Mode (Average by 8)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.5	0.53 (3.6)	0.33 (2.1)	0.21 (1.4)	0.15 (0.93)	0.11 (0.6)	0.073 (0.44)	0.064 (0.39)	0.051 (0.29)
30	8	0.92 (5.4)	0.58 (3.4)	0.4 (2.3)	0.28 (1.6)	0.2 (1.1)	0.14 (0.79)	0.11 (0.62)	0.094 (0.51)
6	40	2.1 (13)	1.3 (8.3)	0.83 (6)	0.61 (4.1)	0.44 (3)	0.33 (2.1)	0.26 (1.6)	0.21 (1.3)
5	48	2.3 (14)	1.5 (8.6)	0.87 (6.6)	0.7 (4.4)	0.5 (3.3)	0.36 (2.3)	0.3 (1.7)	0.23 (1.4)
2	120	11 (72)	5.9 (39)	3.2 (23)	1.9 (15)	1.1 (8.5)	0.7 (4.7)	0.5 (3.3)	0.4 (2.4)
1	240	88 (530)	45 (250)	22 (140)	11 (82)	5.8 (40)	3 (22)	01.6 (11)	0.94 (6.3)

Table 36. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode (Average by 8)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.5	23.2 (20.4)	22.8 (20.2)	22.5 (19.8)	22 (19.4)	21.4 (19)	21 (18.4)	20.2 (17.6)	19.6 (17)
30	8	22.4 (19.8)	22 (19.5)	21.6 (19)	21.1 (18.6)	20.6 (18.1)	20.1 (17.6)	19.4 (16.9)	18.7 (16.2)
6	40	21.2 (18.6)	20.9 (18.2)	20.5 (17.7)	20 (17.2)	19.4 (16.7)	18.9 (16.2)	18.2 (15.6)	17.5 (14.9)
5	48	21 (18.4)	20.7 (18.1)	20.4 (17.5)	19.8 (17)	19.3 (16.5)	18.7 (16.1)	18 (15.5)	17.4 (14.8)
2	120	18.7 (16.1)	18.7 (16)	18.6 (15.8)	18.3 (15.3)	18.1 (15.2)	17.8 (15)	17.3 (14.6)	16.6 (14)
1	240	15.8 (13.2)	15.8 (13.2)	15.8 (13.2)	15.7 (12.9)	15.7 (12.9)	15.7 (12.8)	15.6 (12.8)	15.3 (12.6)

GETTING STARTED

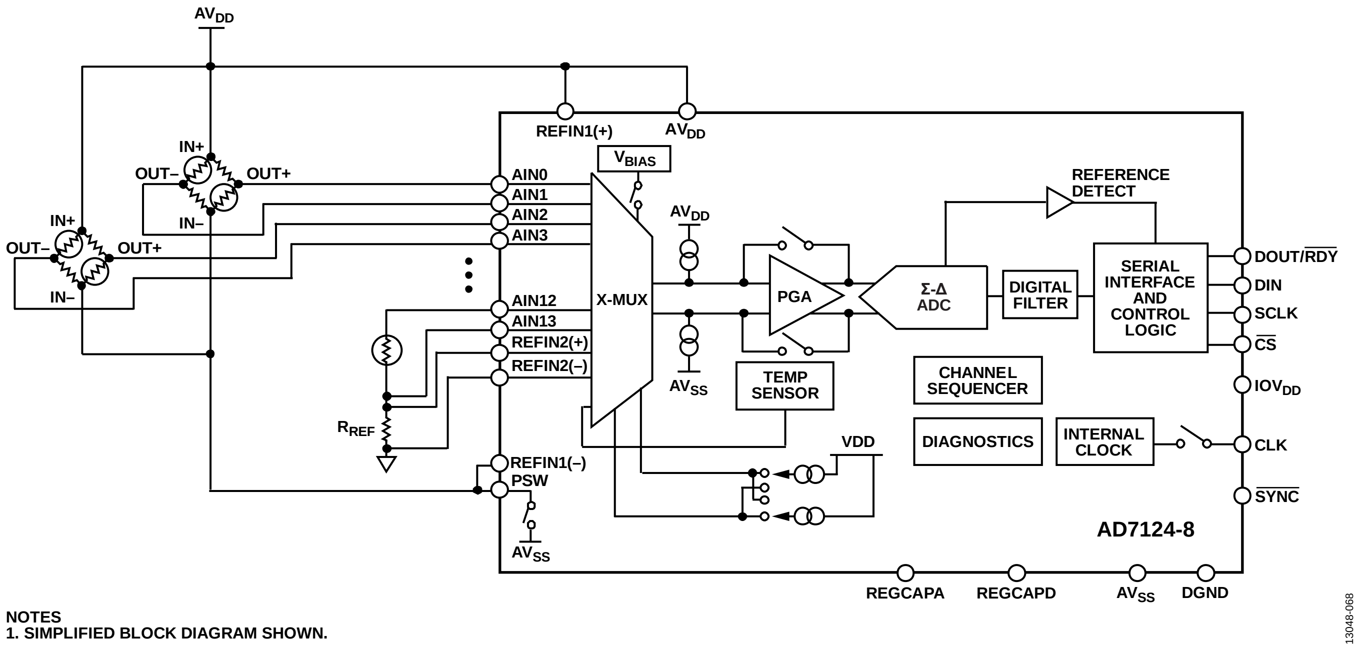


Figure 64. Basic Connection Diagram

OVERVIEW

The AD7124-8 is a low power ADC that incorporates a Σ-Δ modulator, buffer, reference, gain stage, and on-chip digital filtering, which is intended for the measurement of wide dynamic ranges, low frequency signals (such as those in pressure transducers), weigh scales, and temperature measurement applications.

Power Modes

The AD7124-8 offers three power modes: high power mode, mid power mode, and low power mode. This allows the user total flexibility in terms of speed, rms noise, and current consumption.

Analog Inputs

The device can have 8 differential or 15 pseudo differential analog inputs. The analog inputs can be buffered or unbuffered. The AD7124-8 uses flexible multiplexing; thus, any analog input pin can be selected as a positive input (AINP) and any analog input pin can be selected as a negative input (AINM).

Multiplexer

The on-chip multiplexer increases the channel count of the device. Because the multiplexer is included on chip, any channel changes are synchronized with the conversion process.

Reference

The device contains a 2.5 V reference, which has a drift of 15 ppm/°C maximum.

Reference buffers are also included on chip, which can be used with the internal reference and externally applied references.

Programmable Gain Array (PGA)

The analog input signal can be amplified using the PGA. The PGA allows gains of 1, 2, 4, 8, 16, 32, 64, and 128.

Burnout Currents

Two burnout currents, which can be programmed to 500 nA, 2 µA, or 4 µA, are included on chip to detect the presence of the external sensor.

Σ-Δ ADC and Filter

The AD7124-8 contains a fourth-order Σ-Δ modulator followed by a digital filter. The device has the following filter options:

- $Sinc^4$
- $Sinc^3$
- Fast filter
- Post filter
- Zero latency

Channel Sequencer

The AD7124-8 allows up to 16 configurations, or channels. These channels can consist of analog inputs, reference inputs, or power supplies such that diagnostic functions, such as power supply monitoring, can be interleaved with conversions. The sequencer automatically converts all enabled channels. When each enabled channel is selected, the time required to generate the conversion is equal to the settling time for the selected channel.

Per Channel Configuration

The AD7124-8 allows up to eight different setups, each setup consisting of a gain, output data rate, filter type, and a reference source. Each channel is then linked to a setup.

Serial Interface

The AD7124-8 has a 3-wire or 4-wire SPI. The on-chip registers are accessed via the serial interface.

Clock

The device has an internal 614.4 kHz clock. Use either this clock or an external clock as the clock source for the device. The internal clock can also be made available on a pin if a clock source is required for external circuitry.

Temperature Sensor

The on-chip temperature sensor monitors the die temperature.

Digital Outputs

The AD7124-8 has four general-purpose digital outputs. These can be used for driving external circuitry. For example, an external multiplexer can be controlled by these outputs.

Calibration

Both internal calibration and system calibration are included on chip; therefore, the user has the option of removing offset or gain errors internal to the device only, or removing the offset or gain errors of the complete end system.

Excitation Currents

The device contains two excitation currents that can be set independently to 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, or 1 mA.

Bias Voltage

A bias voltage generator is included on chip so that signals from thermocouples can be biased suitably. The bias voltage is set to $AV_{DD}/2$ and can be made available on any input. It can supply multiple channels.

Bridge Power Switch (PSW)

A low-side power switch allows the user to power down bridges that are interfaced to the ADC.

Diagnostics

The AD7124-8 includes numerous diagnostics features such as

- Reference detection
- Overvoltage/undervoltage detection
- CRC on SPI communications
- CRC on the memory map
- SPI read/write checks

These diagnostics allow a high level of fault coverage in an application.

POWER SUPPLIES

The AD7124-8 operates with an analog power supply voltage from 2.7 V to 3.6 V in low or mid power mode and from 2.9 V to 3.6 V in full power mode. The device accepts a digital power supply from 1.65 V to 3.6 V.

The device has two independent power supply pins: AV_{DD} and IOV_{DD}.

- AV_{DD} is referred to AV_{SS}. AV_{DD} powers the internal analog regulator that supplies the ADC.
- IOV_{DD} is referred to DGND. This supply sets the interface logic levels on the SPI interface and powers an internal regulator for operation of the digital processing.

Single Supply Operation (AV_{SS} = DGND)

When the AD7124-8 is powered from a single supply that is connected to AV_{DD}, AV_{SS} and DGND can be shorted together on one single ground plane. With this setup, an external level shifting circuit is required when using truly bipolar inputs to shift the common-mode voltage. Recommended regulators include the ADP162, which has a low quiescent current.

Split Supply Operation (AV_{SS} ≠ DGND)

The AD7124-8 can operate with AV_{SS} set to a negative voltage, allowing true bipolar inputs to be applied. This allows a truly fully differential input signal centered around 0 V to be applied to the AD7124-8 without the need for an external level shifting circuit. For example, with a 3.6 V split supply, AV_{DD} = +1.8 V and AV_{SS} = −1.8 V. In this use case, the AD7124-8-internally level shifts the signals, allowing the digital output to function between DGND (nominally 0 V) and IOV_{DD}.

When using a split supply for AV_{DD} and AV_{SS}, the absolute maximum ratings must be considered (see the Absolute Maximum Ratings section). Ensure that IOV_{DD} is set below 3.6 V to stay within the absolute maximum ratings for the device.

DIGITAL COMMUNICATION

The AD7124-8 has a 3-wire or 4-wire SPI interface that is compatible with QSPI, MICROWIRE, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

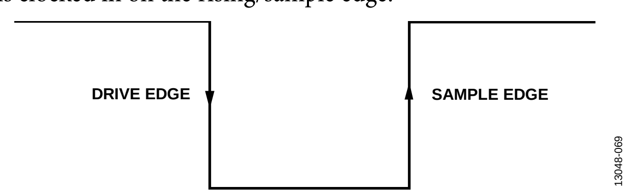


Figure 65. SPI Mode 3, SCLK Edges

Accessing the ADC Register Map

The communications register controls access to the full register map of the ADC. This register is an 8-bit, write only register. On power-up or after a reset, the digital interface defaults to a state where it expects a write to the communications register; therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is accessed and if the next operation is a read or write. The register address bits (Bit 5 to Bit 0) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to its default state, where it expects a write operation to the communications register.

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire device, including the register contents. Alternatively, if $\overline{\text{CS}}$ is used with the digital interface, returning $\overline{\text{CS}}$ high resets the digital interface to its default state and aborts any current operation.

Figure 66 and Figure 67 illustrate writing to and reading from a register by first writing the 8-bit command to the communications register followed by the data for the addressed register.

Reading the ID register is the recommended method for verifying correct communication with the device. The ID register is a read only register and contains the value 0x12 for the AD7124-8. The communication register and ID register details are described in Table 37 and Table 38.

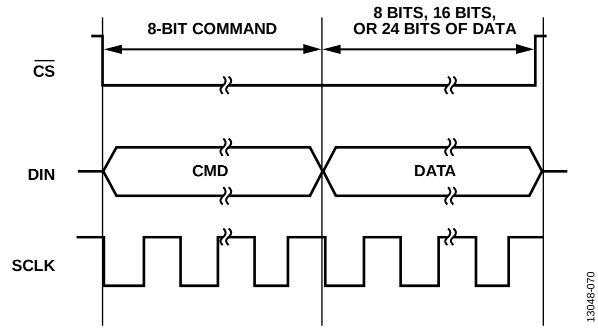


Figure 66. Writing to a Register (8-Bit Command with Register Address Followed by Data of 8 Bits, 16 Bits, or 24 Bits; Data Length Is Dependent on the Register Selected)

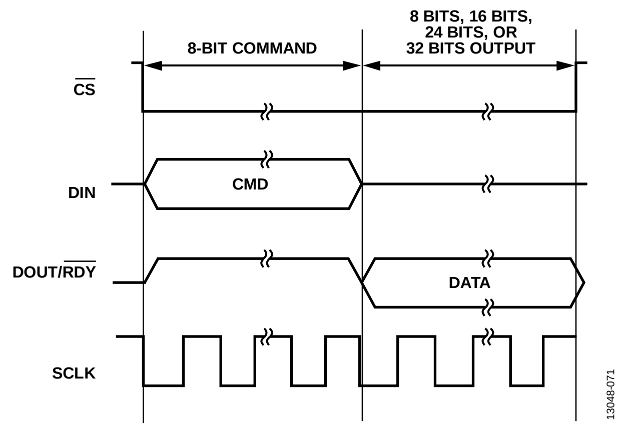


Figure 67. Reading from a Register (8-Bit Command with Register Address Followed by Data of 8 Bits, 16 Bits, 24 Bits, or 32 Bits; Data Length on DOUT Is Dependent on the Register Selected, CRC Enabled)

Table 37. Communications Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{\text{WEN}}$	R/$\overline{\text{W}}$	RS[5:0]						0x00	W

Table 38. ID Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x05	ID	[7:0]	DEVICE_ID				SILICON_REVISION				0x12	R

CONFIGURATION OVERVIEW

After power-on or reset, the AD7124-8 default configuration is as follows:

- Channel: Channel 0 is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. Setup 0 is selected.
- Setup: the input and reference buffers are disabled, the gain is set to 1, and the external reference is selected.
- ADC control: the AD7124-8 is in low power mode, continuous conversion mode and the internal oscillator is enabled and selected as the master clock source.
- Diagnostics: the only diagnostic enabled is the SPI_IGNORE_ERR function.

Note that only a few of the register setting options are shown; this list is just an example. For full register information, see the On-Chip Registers section.

Figure 68 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration (see Box A in Figure 68)
- Setup (see Box B in Figure 68)
- Diagnostics (see Box C in Figure 68)
- ADC control (see Box D in Figure 68)

Channel Configuration

The AD7124-8 has 16 independent analog input channels and eight independent setups. The user can select any of the analog input pairs on any channel, as well as any of the eight setups for any channel, giving the user full flexibility in the channel configuration. This also allows per channel configuration when using all differential inputs because each channel can have its own dedicated setup.

Along with the analog inputs, signals such as the power supply or reference can also be used as inputs; they are routed to the multiplexer internally when selected. The AD7124-8 allows the user to define 16 configurations, or channels, to the ADC. This allows diagnostics to be interleaved with conversions.

Channel Registers

Use the channel registers to select which input pins are either the positive analog input or the negative analog input for that channel. This register also contains a channel enable/disable bit and the setup selection bits, which are used to select which of the eight available setups to use for this channel.

When the AD7124-8 is operating with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 15. If a channel is disabled, it is skipped by the sequencer. Details of the channel register for Channel 0 are shown in Table 39.

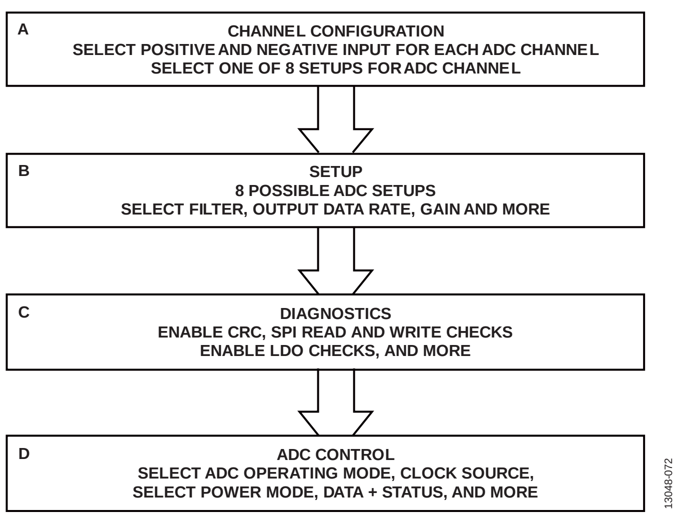


Figure 68. Suggested ADC Configuration Flow

Table 39. Channel 0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x09	CHANNEL_0	[15:8]	Enable	Setup			0		AINP[4:3]		0x8001	RW
		[7:0]	AINP[2:0]			AINM[4:0]						

ADC Setups

The AD7124-8 has eight independent setups. Each setup consists of the following four registers:

- Configuration register
- Filter register
- Offset register
- Gain register

For example, Setup 0 consists of Configuration Register 0, Filter Register 0, Offset Register 0, and Gain Register 0. Figure 69 shows the grouping of these registers. The setup is selectable from the channel registers detailed in the Channel Configuration section. This allows each channel to be assigned to one of eight separate setups. Table 40 through Table 43 show the four registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 7.

Configuration Registers

The configuration registers allow the user to select the output coding of the ADC by selecting between bipolar and unipolar. In bipolar mode, the ADC accepts negative differential input voltages, and the output coding is offset binary. In unipolar mode, the ADC accepts only positive differential voltages, and the coding is straight binary. In either case, the input voltage must be within the AV_{DD} and AV_{SS} supply voltages. The user can also select the reference source using these registers. Four options are available: an internal 2.5 V reference, an external reference connected between REFIN1(+) and REFIN1(−), an external reference connected between REFIN2(+) and REFIN2(−), or AV_{DD} to AV_{SS}. The PGA gain is also set; gains of 1, 2, 4, 8, 16, 32, 64, and 128 are provided. The analog input buffers and reference input buffers for the setup can also be enabled using this register.

Filter Registers

The filter registers select which digital filter is used at the output of the ADC modulator. The filter type and the output data rate are selected by setting the bits in this register. For more information, see the Digital Filter section.

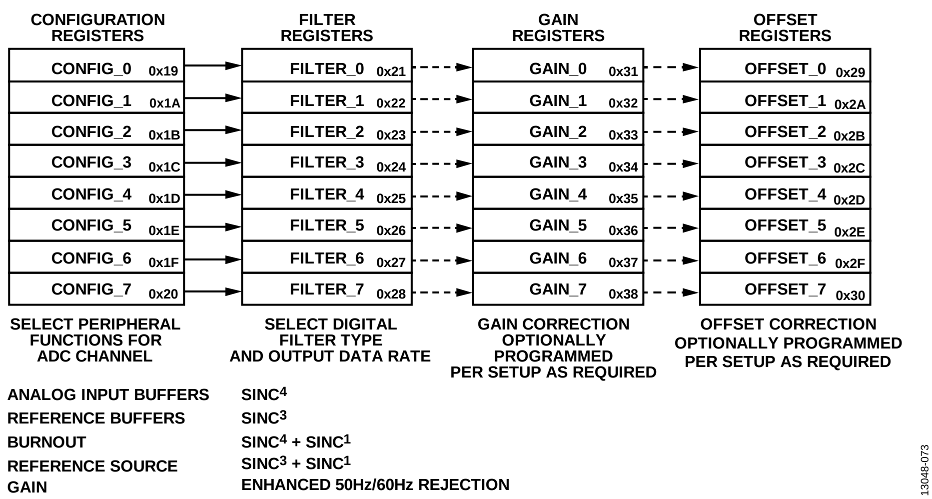


Figure 69. ADC Setup Register Grouping

Table 40. Configuration 0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x19	CONFIG_0	[15:8]	0				Bipolar	Burnout		REF_BUFP	0x0860	RW
		[7:0]	REF_BUFM	AIN_BUFP	AIN_BUFM	REF_SEL		PGA				

Table 41. Filter 0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x28	FILTER_0	[23:9]	Filter			REJ60	POST_FILTER			SINGLE_CYCLE	0x060180	RW
		[15:8]	0					FS[10:8]				
		[7:0]	FS[7:0]									

Table 42. Offset 0 Register

Reg.	Name	Bits	Bits[23:0]	Reset	RW
0x29	OFFSET_0	[23:0]	Offset[23:0]	0x800000	RW

Table 43. Gain 0 Register

Reg.	Name	Bits	Bits[23:0]	Reset	RW
0x31	GAIN_0	[23:0]	Gain[23:0]	0x5XXXXX	RW

Offset Registers

The offset registers hold the offset calibration coefficient for the ADC. The power-on reset value of an offset register is 0x800000. The offset registers are 24-bit read/write registers. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user or if the offset registers are written to by the user.

Gain Registers

The gain registers are 24-bit registers that hold the gain calibration coefficient for the ADC. The gain registers are read/write registers. The gain is factory calibrated at a gain of 1; thus, the default value varies from device to device. The default value is automatically overwritten if an internal or system full-scale calibration is initiated by the user. For more information on calibration, see the Calibration section.

Diagnostics

The ERROR_EN register enables and disables the numerous diagnostics on the AD7124-8. By default, the SPI_IGNORE function is enabled, which indicates inappropriate times to communicate with the ADC (for example, during power-up and during a reset). Other diagnostics include

- SPI read and write checks, which ensure that only valid registers are accessed
- SCLK counter, which ensures that the correct number of SCLK pulses are used
- SPI CRC
- Memory map CRC
- LDO checks

When a diagnostic is enabled, the corresponding flag is contained in the error register. All enabled flags are OR'ed to control the ERR flag in the status register. Thus, if an error occurs (for example, the SPI CRC check detects an error), the relevant flag (for example, the SPI_CRC_ERR flag) in the error register is set. The ERR flag in the status register is also set. This is useful when the status bits are appended to conversions. The ERR bit indicates if an error has occurred. The user can then read the error register for more details on the error source.

The frequency of the on-chip oscillator can also be monitored on the AD7124-8. The MCLK_COUNT register monitors the master clock pulses. Table 44 to Table 46 give more detail on the diagnostic registers. See the Diagnostics section for more detail on the diagnostics available.

ADC Control Register

The ADC control register configures the core peripherals for use by the AD7124-8 and the mode for the digital interface. The power mode (full power, mid power, or low power) is selected via this register. Also, the mode of operation is selected, for example, continuous conversion or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes. In addition, this register contains the clock source select bits and the internal reference enable bits. The reference select bits are contained in the setup configuration registers (see the ADC Setups section for more information).

The digital interface operation is also selected via the ADC control register. This register allows the user to enable the data plus status read and continuous read mode. For more details, see the Digital Interface section. The details of this register are shown in Table 47.

Table 44. Error Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x06	Error	[23:16]	0				LDO_CAP_ERR	ADC_CAL_ERR	ADC_CONV_ERR	ADC_SAT_ERR	0x000000	R
		[15:8]	AINP_OV_ERR	AINP_UV_ERR	AINM_OV_ERR	AINM_UV_ERR	REF_DET_ERR	0	DLDO_PSM_ERR	0		
		[7:0]	ALDO_PSM_ERR	SPI_IGNORE_ERR	SPI_SCLK_CNT_ERR	SPI_READ_ERR	SPI_WRITE_ERR	SPI_CRC_ERR	MM_CRC_ERR	0		

Table 45. Error Enable Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x07	ERROR_EN	[23:16]	0	MCLK_CNT_EN	LDO_CAP_CHK_TEST_EN	LDO_CAP_CHK		ADC_CAL_ERR_EN	ADC_CONV_ERR_EN	ADC_SAT_ERR_EN	0x000040	RW
		[15:8]	AINP_OV_ERR_EN	AINP_UV_ERR_EN	AINM_OV_ERR_EN	AINM_UV_ERR_EN	REF_DET_ERR_EN	DLDO_PSM_TRIP_TEST_EN	DLDO_PSM_ERR_EN	ALDO_PSM_TRIP_TEST_EN		
		[7:0]	ALDO_PSM_ERR_EN	SPI_IGNORE_ERR_EN	SPI_SCLK_CNT_ERR_EN	SPI_READ_ERR_EN	SPI_WRITE_ERR_EN	SPI_CRC_ERR_EN	MM_CRC_ERR_EN	0		

Table 46. MCLK Count Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x08	MCLK_COUNT	[7:0]	MCLK_COUNT								0x00	R

Table 47. ADC Control Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADC_CONTROL	[15:8]	0			DOUT_$\overline{\text{RDY}}$_DEL	CONT_READ	DATA_STATUS	$\overline{\text{CS}}$_EN	REF_EN	0x0000	RW
		[7:0]	POWER_MODE		Mode				CLK_SEL			

Understanding Configuration Flexibility

In Figure 70, Figure 71, and Figure 72, the registers shown in black font are programmed for this configuration. The registers shown in gray font are redundant.

The most straightforward implementation of the AD7124-8 is to use differential inputs with adjacent analog inputs and run all of them with the same setup, gain correction, and offset correction register. For example, the user requires four differential inputs. In this case, the user selects the following differential inputs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7.

Programming the gain and offset registers is optional for any use case, as indicated by the dashed lines between the register blocks. If an internal or system offset or full-scale calibration is performed, the gain and offset registers for the selected channel are automatically updated.

An alternative way to implement these four fully differential inputs is by taking advantage of the eight available setups. Motivation for this includes having a different speed, noise, or gain requirement on some of the four differential inputs vs. other inputs, or there may be a specific offset or gain correction for particular channels. Figure 71 shows how each of the differential inputs can use a separate setup, allowing full flexibility in the configuration of each channel.

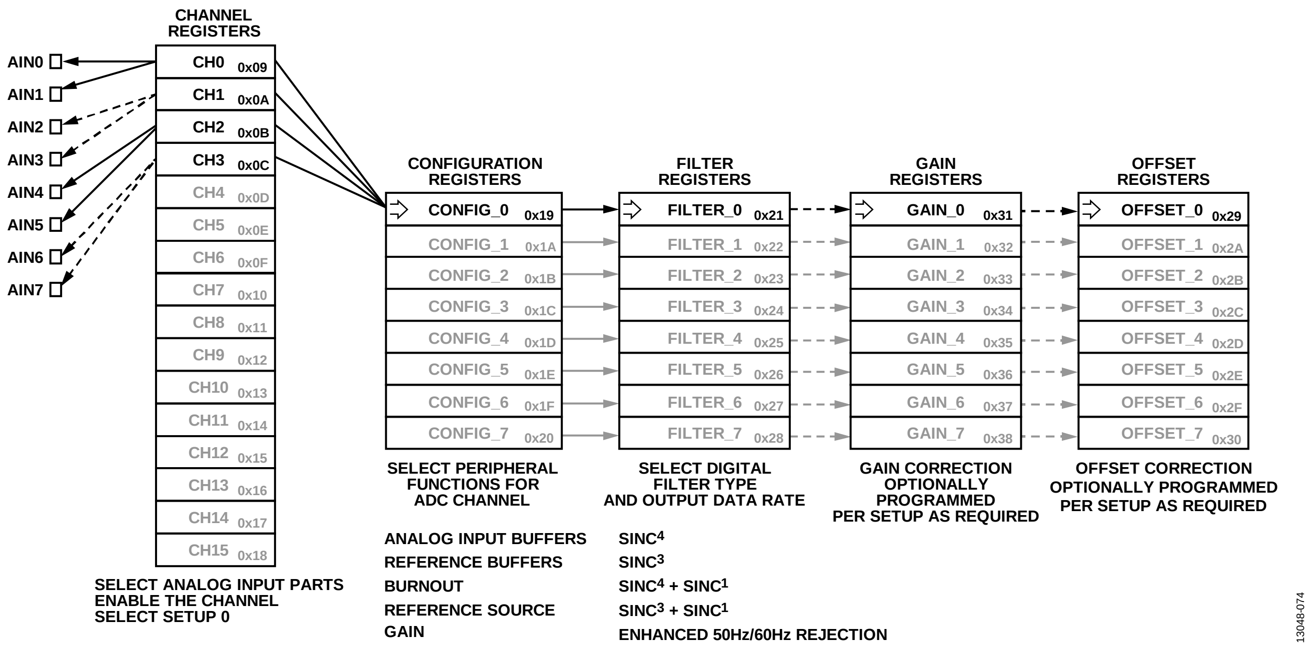


Figure 70. Four Fully Differential Inputs, All Using a Single Setup (CONFIG_0, FILTER_0, GAIN_0, OFFSET_0)

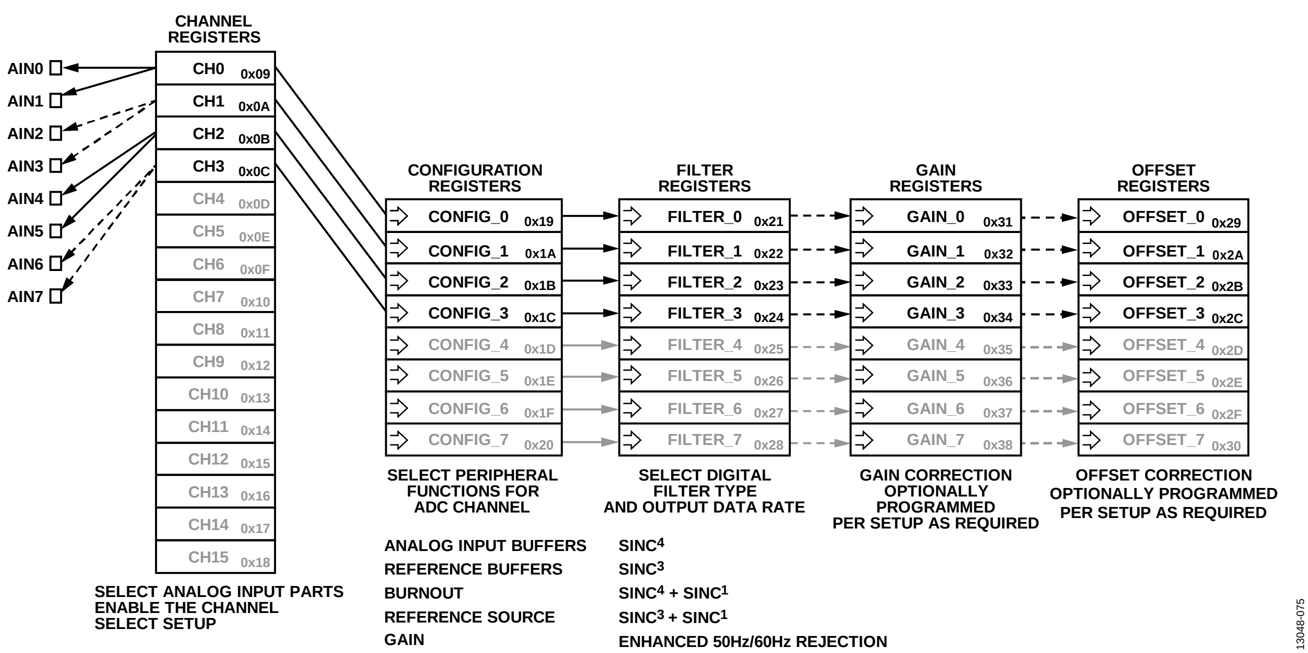


Figure 71. Four Fully Differential Inputs with a Separate Setup per Channel

Figure 72 shows an example of how the channel registers span between the analog input pins and the setup configurations downstream. In this random example, two differential inputs and two single-ended inputs are required. The single-ended inputs are the AIN0/AIN7 and AIN6/AIN7 combinations. The first differential input pair (AIN0/AIN1) uses Setup 0. The two single-ended input pairs (AIN0/AIN7 and AIN6/AIN7) are set up as diagnostics; therefore, they use a separate setup (Setup 1). The final differential input (AIN2/AIN3) also uses a separate setup: Setup 2.

Given that three setups are selected for use, the CONFIG_0, CONFIG_1, and CONFIG_2 registers are programmed as required, and the FILTER_0, FILTER_1, and FILTER_2 registers are also programmed as required. Optional gain and offset correction can be employed on a per setup basis by programming the GAIN_0, GAIN_1, and GAIN_2 registers and the OFFSET_0, OFFSET_1, and OFFSET_2 registers.

In the example shown in Figure 72, the CHANNEL_0 to CHANNEL_3 registers are used. Setting the MSB (the enable bit) in each of these registers enables the four combinations via the crosspoint multiplexer. When the AD7124-8 converts, the sequencer transitions in ascending sequential order from CHANNEL_0 to CHANNEL_1 to CHANNEL_2, and then on to CHANNEL_3 before looping back to CHANNEL_0 to repeat the sequence.

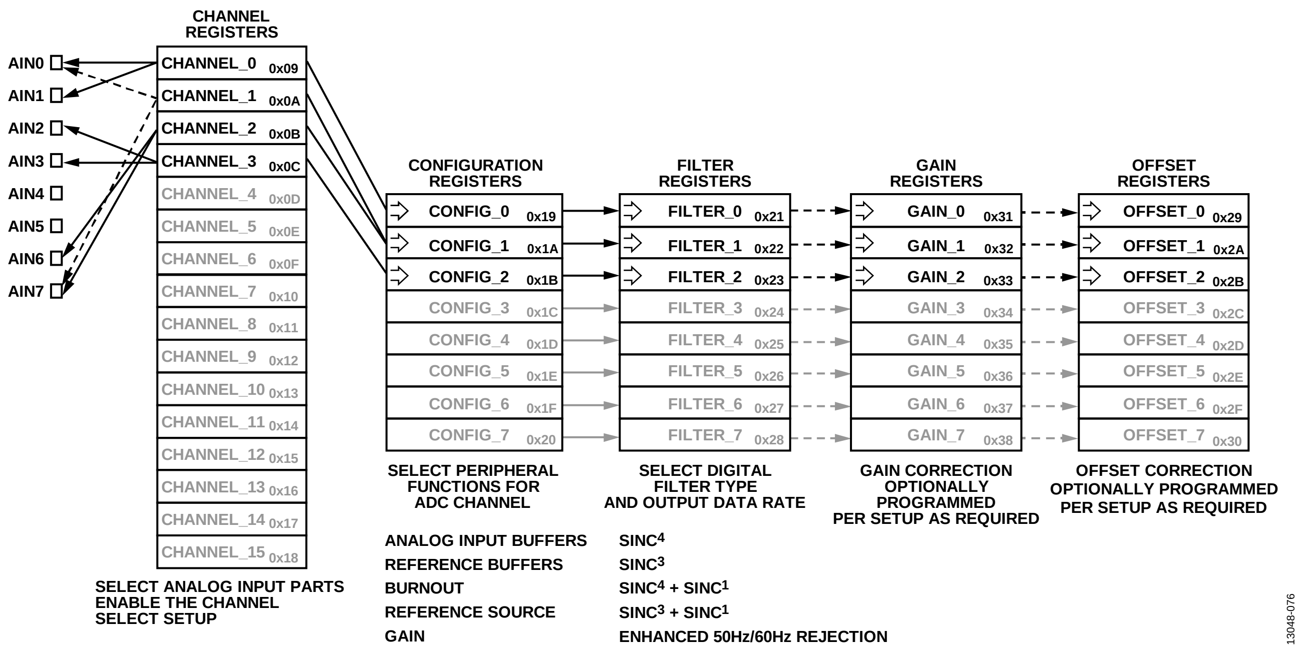


Figure 72. Mixed Differential and Single-Ended Configuration Using Multiple Shared Setups

ADC CIRCUIT INFORMATION

ANALOG INPUT CHANNEL

The AD7124-8 uses flexible multiplexing; thus, any of the analog input pins, AIN0 to AIN15, can be selected as a positive input or a negative input. This feature allows the user to perform diagnostics such as checking that pins are connected. It also simplifies printed circuit board (PCB) design. For example, the same PCB can accommodate 2-wire, 3-wire, and 4-wire resistance temperature detectors (RTDs).

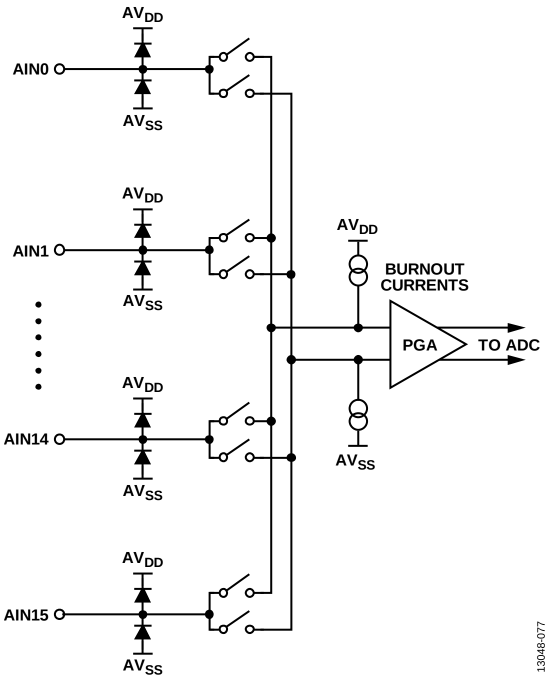


Figure 73. Analog Input Multiplexer Circuit

The channels are configured using the AINP[4:0] bits and the AINM[4:0] bits in the channel registers (see Table 48). The device can be configured to have 8 differential inputs, 15 pseudo differential inputs, or a combination of both. When using differential inputs, use adjacent analog input pins to form the input pair. Using adjacent pins minimizes any mismatch between the channels.

The inputs can be buffered or unbuffered at a gain of 1 but are automatically buffered when the gain exceeds 1. The AINP and AINM buffers are enabled/disabled separately using the AIN_BUFP and AIN_BUFM bits in the configuration register (see Table 49). In buffered mode, the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive type sensors such as strain gages or RTDs.

When the device is operated in unbuffered mode, the device has a higher analog input current. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor (RC) combinations on the input pins can cause gain errors, depending on the output impedance of the source that is driving the ADC input.

The absolute input voltage in unbuffered mode (gain = 1) includes the range between AV_{SS} − 50 mV and AV_{DD} + 50 mV. The absolute input voltage range in buffered mode at a gain of 1 is restricted to a range between AV_{SS} + 100 mV and AV_{DD} − 100 mV. The common-mode voltage must not exceed these limits; otherwise, linearity and noise performance degrade.

When the gain is greater than 1, the analog input buffers are automatically enabled. The PGA placed in front of the input buffers is rail-to-rail; thus, in this case, the absolute input voltage includes the range from AV_{SS} − 50 mV to AV_{DD} + 50 mV.

Table 48. Channel Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x09 to 0x18	CHANNEL_0 to CHANNEL_15	[15:8]	Enable	Setup			0		AINP[4:3]		0x8001	RW
		[7:0]	AINP[2:0]			AINM[4:0]						

Table 49. Configuration Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x19 to 0x20	CONFIG_0 to CONFIG_7	[15:8]	0				Bipolar	Burnout		REF_BUFP	0x0860	RW
		[7:0]	REF_BUFM	AIN_BUFP	AIN_BUFM	REF_SEL		PGA				

PROGRAMMABLE GAIN ARRAY (PGA)

When the gain stage is enabled, the output from the multiplexer is applied to the input of the PGA. The presence of the PGA means that signals of small amplitude can be gained within the AD7124-8 and still maintain excellent noise performance.

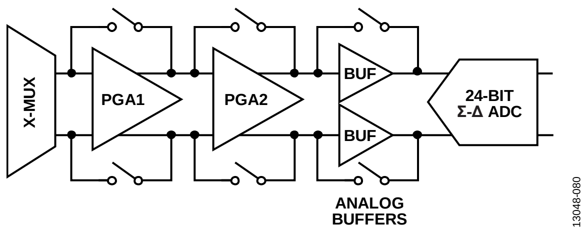


Figure 74. PGA

The AD7124-8 can be programmed to have a gain of 1, 2, 4, 8, 16, 32, 64, or 128 by using the PGA bits in the configuration register (see Table 49). The PGA consists of two stages. For a gain of 1, both stages are bypassed. For gains of 2 to 8, a single stage is used, whereas for gains greater than 8, both stages are used.

The analog input range is $\pm V_{REF}$/gain. Therefore, with an external 2.5 V reference, the unipolar ranges are from 0 mV to 19.53 mV to 0 V to 2.5 V, and the bipolar ranges are from ±19.53 mV to ±2.5 V. For high reference values, for example, $V_{REF} = AV_{DD}$, the analog input range must be limited. Consult the Specifications section for more details on these limits.

REFERENCE

The AD7124-8 has an embedded 2.5 V reference. The embedded reference is a low noise, low drift reference with 15 ppm/°C drift maximum. Including the reference on the AD7124-8 reduces the number of external components needed in applications such as thermocouples, leading to a reduced PCB size.

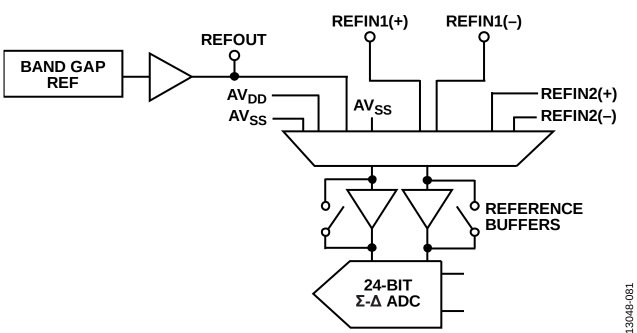


Figure 75. Reference Connections

This reference can be used to supply the ADC (by setting the REF_EN bit in the ADC_CONTROL register to 1) or an external reference can be applied. For external references, the ADC has a fully differential input capability for the channel. In addition, the user can select one of two external reference options (REFIN1 or REFIN2). The reference source for the AD7124-8 is selected using the REF_SEL bits in the configuration register (see Table 49). When the internal reference is selected, it is internally connected to the modulator. It can also be made available on the REFOUT pin. A 0.1 µF decoupling capacitor is required on REFOUT when the internal reference is active.

The common-mode range for the differential reference inputs is from AV_{SS} − 50 mV to AV_{DD} + 50 mV when the reference buffers are disabled. The reference inputs can also be buffered on-chip. The buffers require 100 mV of headroom. The reference voltage of REFIN (REFINx(+) − REFINx(−)) is 2.5 V nominal, but the AD7124-8 is functional with reference voltages from 1 V to AV_{DD}.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the devices, the effect of the low frequency noise in the excitation source is removed, because the application is ratiometric. If the AD7124-8 is used in nonratiometric applications, use a low noise reference.

The recommended 2.5 V reference voltage sources for the AD7124-8 include the ADR4525, which is a low noise, low power reference. Note that the reference input provides a high impedance, dynamic load when unbuffered. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors if the reference inputs are unbuffered, depending on the output impedance of the source driving the reference inputs.

Reference voltage sources typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFINx(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. In this situation, using the reference buffers is required.

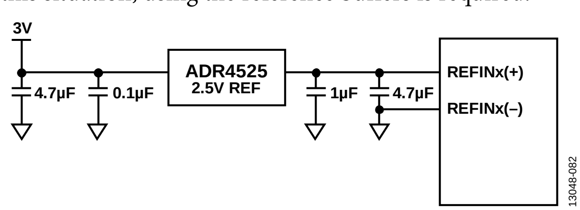


Figure 76. ADR4525 to AD7124-8 Connections

BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7124-8 can accept either unipolar or bipolar input voltage ranges, which allows the user to tune the ADC input range to the sensor output range. When a split power supply is used, the device accepts truly bipolar inputs. When a single power supply is used, a bipolar input range does not imply that the device can tolerate negative voltages with respect to system AV_{SS}. Unipolar and bipolar signals on the AINP input are referenced to the voltage on the AINM input. For example, if AINM is 1.5 V and the ADC is configured for unipolar mode with a gain of 1, the input voltage range on the AINP input is 1.5 V to 3 V when $V_{REF} = AV_{DD} = 3$ V. If the ADC is configured for bipolar mode, the analog input range on the AINP input is 0 V to AV_{DD}. The bipolar/unipolar option is chosen by programming the bipolar bit in the configuration register.

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00 … 00, a midscale voltage resulting in a code of 100 … 000, and a full-scale input voltage resulting in a code of 111 … 111. The output code for any analog input voltage can be represented as

$$Code = (2^N \times A_{IN} \times Gain)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000 … 000, a zero differential input voltage resulting in a code of 100 … 000, and a positive full-scale input voltage resulting in a code of 111 … 111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(A_{IN} \times Gain/V_{REF}) + 1]$$

where:
N = 24.
A_{IN} is the analog input voltage.
Gain is the gain setting (1 to 128).

EXCITATION CURRENTS

The AD7124-8 also contains two matched, software configurable, constant current sources that can be programmed to equal 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, or 1 mA. These current sources can be used to excite external resistive bridges or RTD sensors. Both current sources source currents from AV_{DD} and can be directed to any of the analog input pins (see Figure 77).

The pins on which the currents are made available are programmed using the IOUT1_CH and IOUT0_CH bits in the IO_CONTROL_1 register (see Table 50). The magnitude of each current source is individually programmable using the IOUT1 and IOUT0 bits in the IO_CONTROL_1 register. In addition, both currents can be output to the same analog input pin.

Note that the on-chip reference does not need to be enabled when using the excitation currents.

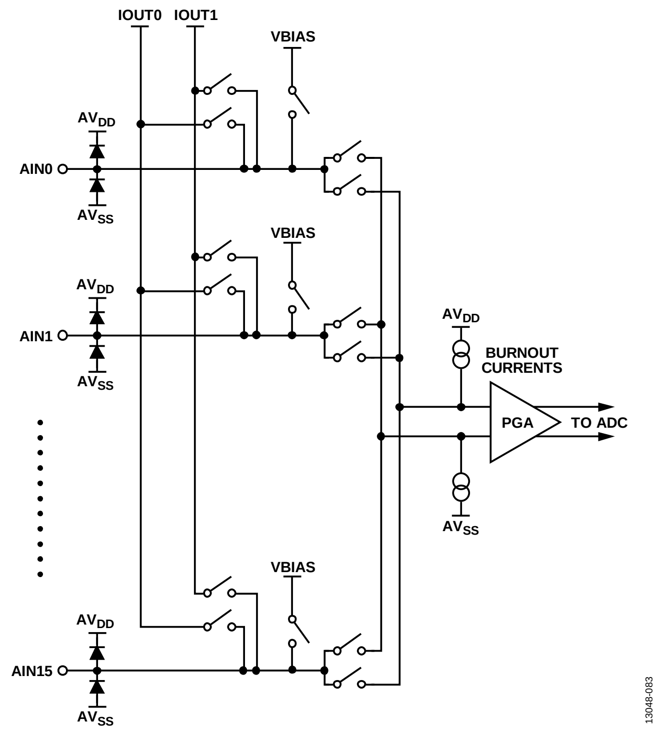


Figure 77. Excitation Current and Bias Voltage Connections

BRIDGE POWER-DOWN SWITCH

In bridge applications such as strain gauges and load cells, the bridge itself consumes the majority of the current in the system. For example, a 350 Ω load cell requires 8.6 mA of current when excited with a 3 V supply. To minimize the current consumption of the system, the bridge can be disconnected (when it is not being used) using the bridge power-down switch. The switch can withstand 30 mA of continuous current, and it has an on resistance of 10 Ω maximum. The PDSW bit in the IO_CONTROL_1 register controls the switch.

Table 50. Input/Output Control 1 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x03	IO_CONTROL_1	[23:16]	GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1	0x000000	RW
		[15:8]	PDSW	0	IOUT1			IOUT0				
		[7:0]	IOUT1_CH				IOUT0_CH					

LOGIC OUTPUTS

The AD7124-8 has four general-purpose digital outputs: P1 to P4. These are enabled using the GPIO_CTRL bits in the IO_CONTROL_1 register (see Table 50). The pins can be pulled high or low using the GPIO_DATx bits in the register; that is, the value at the pin is determined by the setting of the GPIO_DATx bits. The logic levels for these pins are determined by AV_{DD} rather than by IOV_{DD}. When the IO_CONTROL_1 register is read, the GPIO_DATx bits reflect the actual value at the pins; this is useful for short-circuit detection.

These pins can be used to drive external circuitry, for example, an external multiplexer. If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled via the AD7124-8 general-purpose output pins. The general-purpose output pins can be used to select the active multiplexer pin. Because the operation of the multiplexer is independent of the AD7124-8, reset the modulator and filter using the $\overline{\text{SYNC}}$ pin or by writing to the mode or configuration register each time that the multiplexer channel is changed.

BIAS VOLTAGE GENERATOR

A bias voltage generator is included on the AD7124-8 (see Figure 77). It biases the negative terminal of the selected input channel to $(AV_{DD} – AV_{SS})/2$. This function is useful in thermocouple applications, as the voltage generated by the thermocouple must be biased around some dc voltage if the ADC operates from a single power supply. The bias voltage generator is controlled using the VBIASx bits in the IO_CONTROL_2 register (see Table 52). The power-up time of the bias voltage generator is dependent on the load capacitance. Consult the Specifications section for more details.

CLOCK

The AD7124-8 includes an internal 614.4 kHz clock on chip. This internal clock has a tolerance of ±5%. Use either the internal clock or an external clock as the clock source to the AD7124-8. The clock source is selected using the CLK_SEL bits in the ADC_CONTROL register (see Table 53).

The internal clock can also be made available at the CLK pin. This is useful when several ADCs are used in an application and the devices must be synchronized. The internal clock from one device can be used as the clock source for all ADCs in the system. Using a common clock, the devices can be synchronized by applying a common reset to all devices, or the $\overline{\text{SYNC}}$ pin can be pulsed.

POWER MODES

The AD7124-8 has three power modes: full power mode, mid power mode, and low power mode. The mode is selected using the POWER_MODE bits in the ADC_CONTROL register. The power mode affects the power consumption of the device as well as changing the master clock frequency. A 614.4 kHz clock is used by the device. However, this clock is internally divided, the division factor being dependent on the power mode. Thus, the range of output data rates and performance is affected by the power mode.

Table 51. Power Modes

Power Mode	Master Clock (kHz)	Output Data Rate[1] (SPS)	Current
Full Power	614.4	9.37 to 19,200	See the Specifications section
Mid Power	153.6	2.34 to 4800	
Low Power	76.8	1.17 to 2400	

[1] Unsettled, using a $sinc^3/sinc^4$ filter.

Table 52. Input/Output Control 2 Register

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x04	IO_CONTROL_2	VBIAS15	VBIAS14	VBIAS13	VBIAS12	VBIAS11	VBIAS10	VBIAS9	VBIAS8	0x0000	RW
		VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0		

Table 53. ADC Control Register

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADC_CONTROL	0			DOUT_RDY_DEL	CONT_READ	DATA_STATUS	$\overline{\text{CS}}$_EN	REF_EN	0x0000	RW
		POWER_MODE		Mode				CLK_SEL			

STANDBY AND POWER-DOWN MODES

In standby mode, most blocks are powered down. The LDOs remain active so that registers maintain their contents. If enabled, the reference, internal oscillator, digital outputs P1 to P4, the bias voltage generator, and the low-side power switch remain active. These blocks can be disabled also, if required, by setting the corresponding bits appropriately. The excitation currents, reference detection, and LDO capacitor detection functions are disabled in standby mode.

Other diagnostics remain active if enabled when the ADC is in standby mode. Diagnostics can be enabled or disabled while in standby mode. However, any diagnostics that require the master clock (undervoltage/overvoltage detection, LDO trip tests, memory map CRC, and MCLK counter) must be enabled when the ADC is in continuous conversion mode or idle mode; these diagnostics do not function if enabled in standby mode.

The standby current is typically 15 µA when the LDOs only are enabled. If functions such as the bias voltage generator remain active in standby mode, the current increases by 36 µA typically. If the internal oscillator remains active in standby mode, the current increases by 22 µA typically. When exiting standby mode, the AD7124-8 requires 130 MCLK cycles to power up and settle.

In power-down mode, all blocks are powered down, including the LDOs. All registers lose their contents, and the digital outputs P1 to P4 are placed in tristate. To prevent accidental entry to power-down mode, the ADC must first be placed into standby mode. Exiting power-down mode requires 64 SCLK cycles with $\overline{\text{CS}}$ = 0 and DIN = 1, that is, a serial interface reset. The AD7124-8 requires 2 ms typically to power up and settle. The POR_FLAG in the status register can be monitored to determine the end of the power up/settling period. After this time, the user can access the on-chip registers. The power-down current is 2 µA typically.

DIGITAL INTERFACE

The programmable functions of the AD7124-8 are controlled using a set of on-chip registers. Data is written to these registers via the serial interface. Read access to the on-chip registers is also provided by this interface. All communications with the device must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation, and determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the devices begins with a write operation to the communications register, followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register, followed by a read operation from the selected register.

The serial interface of the AD7124-8 consists of four signals: $\overline{\text{CS}}$, DIN, SCLK, and DOUT/$\overline{\text{RDY}}$. The DIN line transfers data into the on-chip registers, whereas DOUT/$\overline{\text{RDY}}$ accesses data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT/$\overline{\text{RDY}}$) occur with respect to the SCLK signal. The DOUT/$\overline{\text{RDY}}$ pin also operates as a data ready signal; the line goes low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high before the data register updates to indicate when not to read from the device, to ensure that a data read is not attempted while the register is being updated. $\overline{\text{CS}}$ is used to select a device. It can decode the AD7124-8 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7124-8 with $\overline{\text{CS}}$ decoding the devices. Figure 3 shows the timing for a read operation from the output shift register of the AD7124-8. Figure 4 shows the timing for a write operation to the input shift register. A delay is required between consecutive SPI communications. Figure 5 shows the delay required between SPI read/write operations. It is possible to read the same word from the data register several times, even though the DOUT/$\overline{\text{RDY}}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations are complete before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{\text{CS}}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{\text{RDY}}$ lines communicate with the AD7124-8. The end of the conversion can be monitored using the $\overline{\text{RDY}}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{\text{CS}}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idle high between data transfers.

The AD7124-8 can be operated with $\overline{\text{CS}}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{\text{CS}}$, because $\overline{\text{CS}}$ normally occurs after the falling edge of SCLK in DSPs. SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

$\overline{\text{CS}}$ must be used to frame read and write operations and the $\overline{\text{CS}}$_EN bit in the ADC_CONTROL register must be set when the diagnostics SPI_READ_ERR, SPI_WRITE_ERR, or SPI_SCLK_CNT_ERR are enabled.

The serial interface can be reset by writing a series of 1s on the DIN input. See the Reset section for more details. Reset returns the interface to the state in which it is expecting a write to the communications register

The AD7124-8 can be configured to continuously convert or perform a single conversion (see Figure 78 through Figure 80).

Single Conversion Mode

In single conversion mode, the AD7124-8 performs a single conversion and is placed in standby mode after the conversion is complete. The AD7124-8 requires 130 MCLK cycles to exit standby mode. If a master clock is present (external master clock or the internal oscillator is enabled), DOUT/$\overline{\text{RDY}}$ goes low to indicate the completion of a conversion. When the data-word is read from the data register, DOUT/$\overline{\text{RDY}}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{\text{RDY}}$ is high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, DOUT/$\overline{\text{RDY}}$ goes high and remains high until a valid conversion is available and $\overline{\text{CS}}$ is low. As soon as the conversion is available, DOUT/$\overline{\text{RDY}}$ goes low. The ADC then selects the next channel and begins a conversion. The user can read the present conversion while the next conversion is being performed. As soon as the next conversion is complete, the data register is updated; therefore, the user has a limited period in which to read the conversion. When the ADC has performed a single conversion on each of the selected channels, it returns to idle mode.

If the DATA_STATUS bit in the ADC_CONTROL register is set to 1, the contents of the status register are output along with the conversion each time that the data read is performed. The four LSBs of the status register indicate the channel to which the conversion corresponds.

Continuous Conversion Mode

Continuous conversion is the default power-up mode. The AD7124-8 converts continuously, and the $\overline{\text{RDY}}$ bit in the status register goes low each time a conversion is complete. If $\overline{\text{CS}}$ is low, the DOUT/$\overline{\text{RDY}}$ line also goes low when a conversion is complete. To read a conversion, write to the communications register, indicating that the next operation is a read of the data register. When the data-word is read from the data register, DOUT/$\overline{\text{RDY}}$ goes high. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion; otherwise the new conversion word is lost.

When several channels are enabled, the ADC automatically sequences through the enabled channels, performing one conversion on each channel. When all channels are converted, the sequence starts again with the first channel. The channels are converted in order from lowest enabled channel to highest enabled channel. The data register is updated as soon as each conversion is available. The DOUT/$\overline{\text{RDY}}$ pin pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel.

If the DATA_STATUS bit in the ADC_CONTROL register is set to 1, the contents of the status register, along with the conversion data, are output each time the data register is read. The status register indicates the channel to which the conversion corresponds.

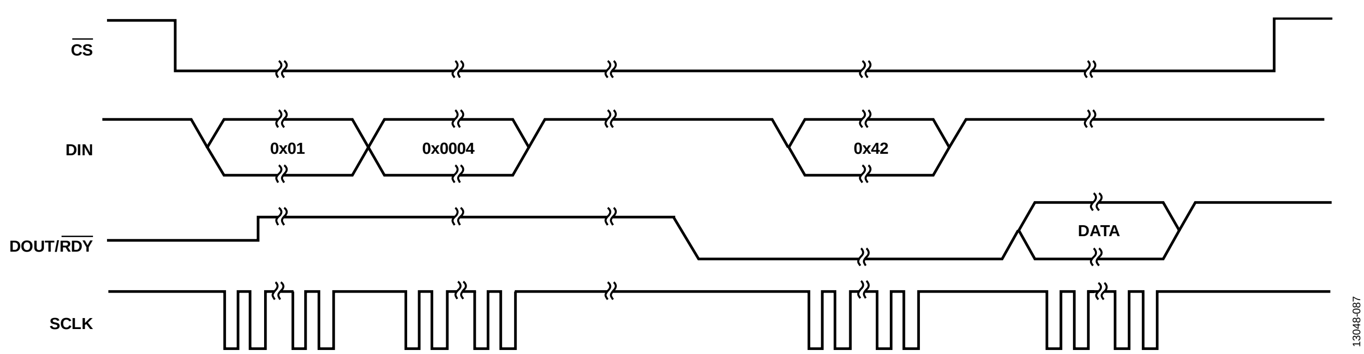


Figure 78. Single Conversion Configuration

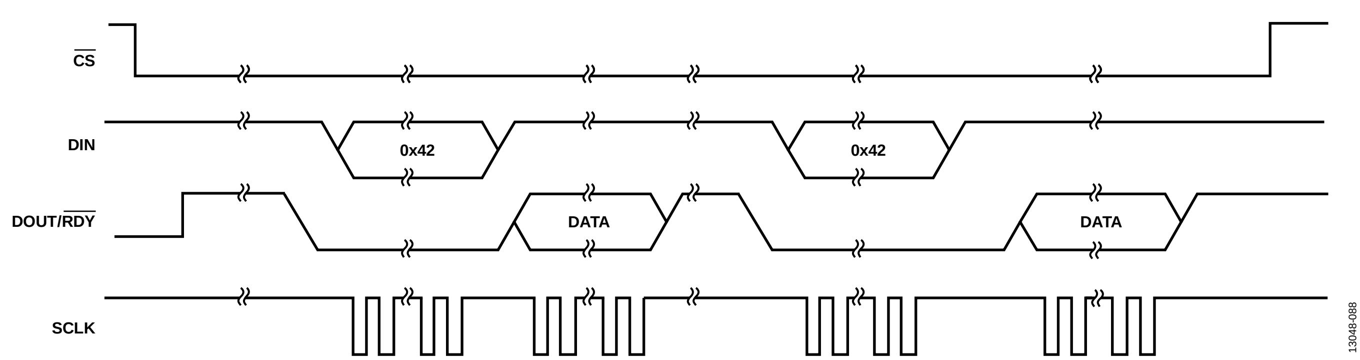


Figure 79. Continuous Conversion Configuration

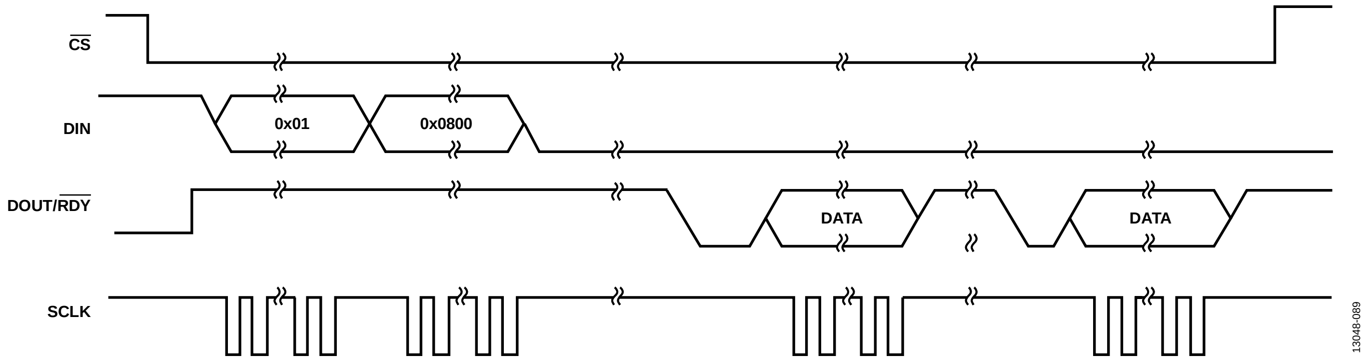


Figure 80. Continuous Read Configuration

Continuous Read Mode

In continuous read mode, it is not required to write to the communications register before reading ADC data; apply the required number of SCLKs after DOUT/RDY goes low to indicate the end of a conversion. When the conversion is read, DOUT/RDY returns high until the next conversion is available. In this mode, the data can be read only once. Ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7124-8 to read the word, the serial output register is reset when the next conversion is complete, and the new conversion is placed in the output serial register. The ADC must be configured for continuous conversion mode to use continuous read mode.

To enable continuous read mode, set the CONT_READ bit in the ADC_CONTROL register. When this bit is set, the only serial interface operations possible are reads from the data register. To exit continuous read mode, issue a dummy read of the ADC data register command (0x42) while RDY is low. Alternatively, apply a software reset, that is, 64 SCLKs with CS = 0 and DIN = 1. This resets the ADC and all register contents. These are the only commands that the interface recognizes after it is placed in continuous read mode. DIN must be held low in continuous read mode until an instruction is to be written to the device.

If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if DATA_STATUS is set in the ADC_CONTROL register. The status register indicates the channel to which the conversion corresponds.

DATA_STATUS

The contents of the status register can be appended to each conversion on the AD7124-8. This is a useful function if several channels are enabled. Each time a conversion is output, the contents of the status register are appended. The four LSBs of the status register indicate to which channel the conversion corresponds. In addition, the user can determine if any errors are being flagged via the ERROR_FLAG bit. To append the status register contents to every conversion, the DATA_STATUS bit in the ADC_CONTROL register is set to 1.

SERIAL INTERFACE RESET (DOUT_RDY_DEL AND CS_EN BITS)

The instant at which the DOUT/RDY pin changes from being a DOUT pin to a RDY pin is programmable on the AD7124-8. By default, the DOUT/RDY pin changes functionality after a period of time following the last SCLK rising edge, the SCLK edge on which the LSB is read by the processor. This time is 10 ns minimum by default and, by setting the DOUT_RDY_DEL bit in the ADC_CONTROL register to 1, can be extended to 110 ns minimum.

By setting the CS_EN bit in the ADC_CONTROL register to 1, the change of functionality is controlled by the CS rising edge. In this case, the DOUT/RDY pin continues to output the LSB of the register being read until CS is taken high. Only on the CS rising edge does the pin change from a DOUT pin to a RDY pin. This configuration is useful if the CS signal is used to frame all read operations. If CS is not used to frame all read operations, set CS_EN to 0 so that DOUT/RDY changes functionality following the last SCLK edge in the read operation.

CS_EN must be set to 1 and the CS signal must be used to frame all read and write operations when the SPI_READ_ERR, SPI_WRITE_ERR, and SPI_SCLK_CNT_ERR diagnostic functions are enabled.

The serial interface is always reset on the CS rising edge, that is, the interface is reset to a known state whereby it awaits a write to the communications register. Therefore, if a read or write operation is performed by performing multiple 8- bit data transfers, CS must be held low until the all bits are transferred.

RESET

The circuitry and serial interface of the AD7124-8 can be reset by writing 64 consecutive 1s to the device. This resets the logic, the digital filter, and the analog modulator, and all on-chip registers are reset to their default values. A reset is automatically performed on power-up. A reset requires a time of 90 MCLK cycles. The POR_FLAG bit in the status register is set to 1 when the reset is initiated and then is set to 0 when the reset is complete. A reset is useful if the serial interface becomes asynchronous due to noise on the SCLK line.

CALIBRATION

The AD7124-8 provides four calibration modes that can be used to eliminate the offset and gain errors on a per setup basis:

- Internal zero-scale calibration mode
- Internal full-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

Only one channel can be active during calibration. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register.

The default value of the offset register is 0x800000, and the nominal value of the gain register is 0x5XXXXX. The calibration range of the ADC gain is from 0.4 × V_{REF}/gain to 1.05 × V_{REF}/gain.

The following equations show the calculations that are used in each calibration mode. In unipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right) \times \frac{Gain}{0x400000} \times 2$$

In bipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right) \times \frac{Gain}{0x400000} + 0x800000$$

To start a calibration, write the relevant value to the mode bits in the ADC_CONTROL register. The DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register are updated, the $\overline{RDY}$ bit in the status register is reset, the DOUT/$\overline{RDY}$ pin returns low (if $\overline{CS}$ is low), and the AD7124-8 reverts to idle mode.

During an internal offset calibration, the selected positive analog input pin is disconnected, and it is connected internally to the selected negative analog input pin. For this reason, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference.

To perform an internal full-scale calibration, a full-scale input voltage is automatically connected to the selected analog input for this calibration. A full-scale calibration is recommended each time the gain of a channel is changed to minimize the full-scale error. When performing internal calibrations, the internal full-scale calibration must be performed before the internal zero-scale calibration. Therefore, write the value 0x800000 to the offset register before performing the internal full-scale calibration, which ensures that the offset register is at its default value.

System calibrations expect the system zero-scale (offset) and system full-scale (gain) voltages to be applied to the ADC pins before initiating the calibration modes. As a result, errors external to the ADC are removed. The system zero-scale calibration must be performed before the system full-scale calibration.

From an operational point of view, treat a calibration like another ADC conversion. Set the system software to monitor the $\overline{RDY}$ bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of a calibration via a polling sequence or an interrupt-driven routine.

An internal/system offset calibration and system full-scale calibration requires a time equal to the settling time of the selected filter to be completed. The internal full-scale calibration requires a time equal to one settling period for a gain of 1 and a time of four settling periods for gains greater than 1.

A calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy and is accurate for all output data rates. A new calibration is required for a given channel if the reference source or the gain for that channel is changed.

Offset and system full-scale calibrations can be performed in any power mode. Internal full-scale calibrations can be performed in the low power or mid power modes only. Thus, when using full power mode, the user must select mid or low power mode to perform the internal full-scale calibration. However, an internal full-scale calibration performed in low or mid power mode is valid in full power mode, if the same gain is used.

The offset error is typically ±15 μV for gains of 1 to 8 and ±200/gain μV for higher output data rates. An internal or system offset calibration reduces the offset error to the order of the noise. The gain error is factory calibrated at ambient temperature and at a gain of 1. Following this calibration, the gain error is ±0.0025% maximum. Therefore, internal full-scale calibrations at a gain of 1 are not supported on the AD7124-8. For other gains, the gain error is −0.3%. An internal full-scale calibration at ambient temperature reduces the gain error to ±0.016% maximum for gains of 2 to 8 and ±0.025% typically for higher gains. A system full-scale calibration reduces the gain error to the order of the noise.

The AD7124-8 provides the user with access to the on-chip calibration registers, allowing the microprocessor to read the calibration coefficients of the device and to write its own calibration coefficients from prestored values in the EEPROM. A read or write of the offset and gain registers can be performed at any time except during an internal or self-calibration. The values in the calibration registers are 24 bits wide. The span and offset of the device can also be manipulated using the registers.

SPAN AND OFFSET LIMITS

Whenever a system calibration mode is used, the amount of offset and span that can be accommodated is limited. The overriding requirement in determining the amount of offset and gain that can be accommodated by the device is the requirement that the positive full-scale calibration limit is $\leq 1.05 \times V_{REF}$/gain. This allows the input range to go 5% above the nominal range. The built-in headroom in the AD7124-8 analog modulator ensures that the device still operates correctly with a positive full-scale voltage, which is 5% beyond the nominal.

The range of input span in both the unipolar and bipolar modes has a minimum value of $0.8 \times V_{REF}$/gain and a maximum value of $2.1 \times V_{REF}$/gain. However, the span, which is the difference between the bottom of the AD7124-8 input range and the top of its input range, must account for the limitation on the positive full-scale voltage. The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. The offset must account for the limitation on the positive full-scale voltage. In unipolar mode, there is considerable flexibility in handling negative (with respect to AINM) offsets. In both unipolar and bipolar modes, the range of positive offsets that can be handled by the device depends on the selected span. Therefore, in determining the limits for system zero-scale and full-scale calibrations, the user must ensure that the offset range plus the span range does exceed $1.05 \times V_{REF}$/gain. This is best illustrated by looking at a few examples.

If the device is used in unipolar mode with a required span of $0.8 \times V_{REF}$/gain, the offset range that the system calibration can handle is from $-1.05 \times V_{REF}$/gain to $+0.25 \times V_{REF}$/gain. If the device is used in unipolar mode with a required span of V_{REF}/gain, the offset range that the system calibration can handle is from $-1.05 \times V_{REF}$/gain to $+0.05 \times V_{REF}$/gain. Similarly, if the device is used in unipolar mode and required to remove an offset of $0.2\times V_{REF}$/gain, the span range that the system calibration can handle is $0.85 \times V_{REF}$/gain.

If the device is used in bipolar mode with a required span of $\pm 0.4 \times V_{REF}$/gain, then the offset range that the system calibration can handle is from $-0.65 \times V_{REF}$/gain to $+0.65 \times V_{REF}$/gain. If the device is used in bipolar mode with a required span of $\pm V_{REF}$/gain, the offset range the system calibration can handle is from $-0.05 \times V_{REF}$/gain to $+0.05 \times V_{REF}$/gain. Similarly, if the device is used in bipolar mode and required to remove an offset of $\pm 0.2 \times V_{REF}$/gain, the span range that the system calibration can handle is $\pm 0.85 \times V_{REF}$/gain.

SYSTEM SYNCHRONIZATION

The $\overline{\text{SYNC}}$ input allows the user to reset the modulator and the digital filter without affecting any of the setup conditions on the device. This allows the user to start gathering samples of the analog input from a known point in time, that is, the rising edge of $\overline{\text{SYNC}}$. Take $\overline{\text{SYNC}}$ low for at least four master clock cycles to implement the synchronization function.

If multiple AD7124-8 devices are operated from a common master clock, they can be synchronized so that their data registers are updated simultaneously. A falling edge on the $\overline{\text{SYNC}}$ pin resets the digital filter and the analog modulator and places the AD7124-8 into a consistent, known state. While the $\overline{\text{SYNC}}$ pin is low, the AD7124-8 is maintained in this state. On the $\overline{\text{SYNC}}$ rising edge, the modulator and filter exit this reset state and, on the next clock edge, the device starts to gather input samples again. In a system using multiple AD7124-8 devices, a common signal to their $\overline{\text{SYNC}}$ pins synchronizes their operation. This is normally performed after each AD7124-8 has performed its own calibration or has calibration coefficients loaded into its calibration registers. The conversions from the AD7124-8 devices are then synchronized.

The device exits reset on the master clock falling edge following the $\overline{\text{SYNC}}$ low to high transition. Therefore, when multiple devices are being synchronized, pull the $\overline{\text{SYNC}}$ pin high on the master clock rising edge to ensure that all devices begin sampling on the master clock falling edge. If the $\overline{\text{SYNC}}$ pin is not taken high in sufficient time, it is possible to have a difference of one master clock cycle between the devices; that is, the instant at which conversions are available differs from device to device by a maximum of one master clock cycle.

The $\overline{\text{SYNC}}$ pin can also be used as a start conversion command. In this mode, the rising edge of $\overline{\text{SYNC}}$ starts conversion and the falling edge of $\overline{\text{RDY}}$ indicates when the conversion is complete. The settling time of the filter must be allowed for each data register update. For example, if the ADC is configured to use the sinc^4 filter and zero latency is disabled, the settling time equals $4/f_{ADC}$ where f_{ADC} is the output data rate when continuously converting on a single channel.

DIGITAL FILTER

Table 54. Filter Registers

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x21 to 0x28	FILTER_0 to FILTER_7	Filter			REJ60	POST_FILTER			SINGLE_CYCLE	0x060180	RW
		0					FS[10:8]				
		FS[7:0]									

The AD7124-8 offers a great deal of flexibility in the digital filter. The device has several filter options. The option selected affects the output data rate, settling time, and 50 Hz and 60 Hz rejection. The following sections describe each filter type, indicating the available output data rates for each filter option. The filter response along with the settling time and 50 Hz and 60 Hz rejection is also discussed.

The filter bits in the filter register select between the sinc type filter.

SINC⁴ FILTER

When the AD7124-8 is powered up, the $sinc^4$ filter is selected by default. This filter gives excellent noise performance over the complete range of output data rates. It also gives the best 50 Hz/ 60 Hz rejection, but it has a long settling time. In Figure 81, the blocks shown in gray are unused.

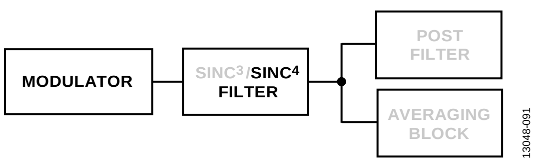


Figure 81. $Sinc^4$ Filter

$Sinc^4$ Output Data Rate/Settling Time

The output data rate (the rate at which conversions are available on a single channel when the ADC is continuously converting) is equal to

$$f_{ADC} = f_{CLK}/(32 \times FS[10:0])$$

where:

f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency (614.4 kHz in full power mode, 153.6 kHz in mid power mode, and 76.8 kHz in low power mode).
FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

The output data rate can be programmed from

- 9.38 SPS to 19,200 SPS for full power mode
- 2.35 SPS to 4800 SPS for mid power mode
- 1.17 SPS to 2400 SPS for low power mode

The settling time for the $sinc^4$ filter is equal to

$$t_{SETTLE} = (4 \times 32 \times FS[10:0] + Dead\ Time)/f_{CLK}$$

where *Dead Time* = 60 when *FS[10:0]* = 1 and 94 when *FS[10:0]* > 1

When a channel change occurs, the modulator and filter are reset. The settling time is allowed to generate the first conversion after the channel change. Subsequent conversions on this channel occur at $1/f_{ADC}$.

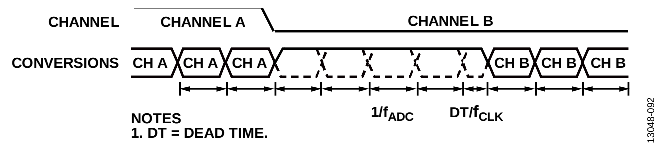


Figure 82. $Sinc^4$ Channel Change

When conversions are performed on a single channel and a step change occurs, the ADC does not detect the change in the analog input. Therefore, it continues to output conversions at the programmed output data rate. However, it is at least four conversions later before the output data accurately reflects the analog input. If the step change occurs while the ADC is processing a conversion, then the ADC takes five conversions after the step change to generate a fully settled result.

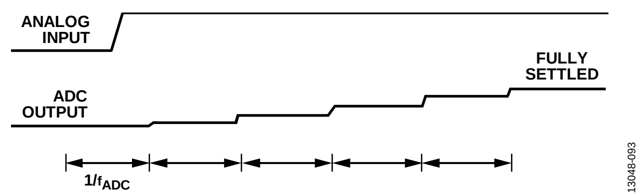


Figure 83. Asynchronous Step Change in the Analog Input

The 3 dB frequency for the $sinc^4$ filter is equal to

$$f_{3dB} = 0.23 \times f_{ADC}$$

Table 55 gives some examples of the relationship between the values in the FS[10:0] bits and the corresponding output data rate and settling time.

Table 55. Examples of Output Data Rates and the Corresponding Settling Times for the $Sinc^4$ Filter

Power Mode	FS[10:0]	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4 kHz)	1920	10	400.15
	384	50	80.15
	320	60	66.82
Mid Power (f_{CLK} = 153.6 kHz)	480	10	400.61
	96	50	80.61
	80	60	67.28
Low Power (f_{CLK} = 76.8 kHz)	240	10	401.22
	48	50	81.22
	40	60	67.89

Sinc[4] Zero Latency

Zero latency is enabled by setting the SINGLE_CYCLE bit in the filter register to 1. With zero latency, the conversion time when continuously converting on a single channel approximately equals the settling time. The benefit of this mode is that a similar period of time elapses between all conversions irrespective of whether the conversions occur on one channel or whether several channels are used. When the analog input is continuously sampled on a single channel, the output data rate equals

$$f_{ADC} = f_{CLK}/(4 \times 32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency.
FS[10:0] is the decimal equivalent of the FS[10:0] bits in the setup filter register.

When the user selects another channel, there is an extra delay in the first conversion of

$$Dead\ Time/f_{CLK}$$

where *Dead Time* = 60 when FS[10:0] = 1 and 94 when FS[10:0] > 1.

At low output data rates, this extra delay has little impact on the value of the settling time. However, at high output data rates, the delay must be considered. Table 56 summarizes the output data rate when continuously converting on a single channel and the settling time when switching between channels for a sample of FS[10:0] values.

When switching between channels, the AD7124-8 allows the complete settling time to generate the first conversion after the channel change. Therefore, the ADC automatically operates in zero latency mode when several channels are enabled—setting the SINGLE_CYCLE bit has no benefits.

Table 56. Examples of Output Data Rates and the Corresponding Settling Times for the Sinc[4] Filter (Zero Latency)

Power Mode	FS[10:0]	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4 kHz)	1920	2.5	400.15
	384	12.5	80.15
	320	15	66.82
Mid Power (f_{CLK} = 153.6 kHz)	480	2.5	400.61
	96	12.5	80.61
	80	15	67.28
Low Power (f_{CLK} = 76.8 kHz)	240	2.5	401.22
	48	12.5	81.22
	40	15	67.89

When the analog input is constant or a channel change occurs, valid conversions are available at a near constant output data rate. When conversions are being performed on a single channel and a step change occurs on the analog input, the ADC continues to output fully settled conversions if the step change is synchronized with the conversion process. If the step change is asynchronous, one conversion is output from the ADC, which is not completely settled (see Figure 84).

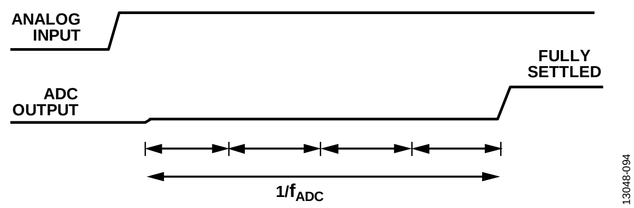


Figure 84. Sinc[4] Zero Latency Operation

Sequencer

The description in the Sinc[4] Filter section is valid when manually switching channels, for example, writing to the device to change channels. When multiple channels are enabled, the on-chip sequencer is automatically used; the device automatically sequences between all enabled channels. In this case, the first conversion takes the complete settling time as listed in Table 55. For all subsequent conversions, the time needed for each conversion is the settling time also, but the dead time is reduced to 30.

Sinc[4] 50 Hz and 60 Hz Rejection

Figure 85 shows the frequency response of the sinc[4] filter when the output data rate is programmed to 50 SPS and zero latency is disabled. For the same configuration but with zero latency enabled, the filter response remains the same but the output data rate is 12.5 SPS. The sinc[4] filter provides 50 Hz (±1 Hz) rejection in excess of 120 dB minimum, assuming a stable master clock.

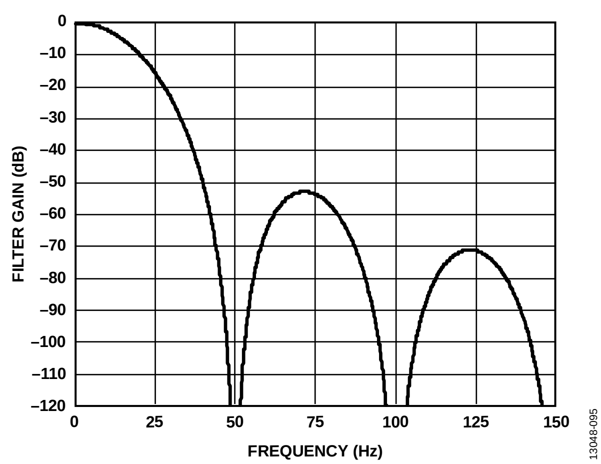


Figure 85. Sinc[4] Filter Response (50 SPS Output Data Rate, Zero Latency Disabled or 12.5 SPS Output Data Rate, Zero Latency Enabled)

Figure 86 shows the frequency response of the $sinc^4$ filter when the output data rate is programmed to 60 SPS and zero latency is disabled. For the same configuration but with zero latency enabled, the filter response remains the same but the output data rate is 15 SPS. The $sinc^4$ filter provides 60 Hz (±1 Hz) rejection of 120 dB minimum, assuming a stable master clock.

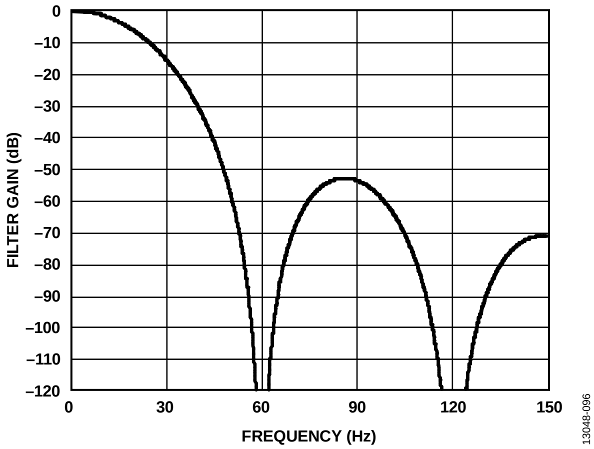


Figure 86. $Sinc^4$ Filter Response (60 SPS Output Data Rate, Zero Latency Disabled or 15 SPS Output Data Rate, Zero Latency Enabled)

When the output data rate is 10 SPS with zero latency disabled or 2.5 SPS with zero latency enabled, simultaneous 50 Hz and 60 Hz rejection is obtained. The $sinc^4$ filter provides 50 Hz (±1 Hz) and 60 Hz (±1 Hz) rejection of 120 dB minimum, assuming a stable master clock.

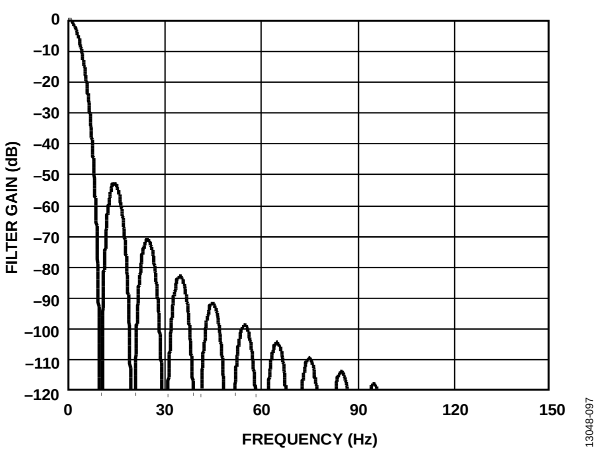


Figure 87. $Sinc^4$ Filter Response (10 SPS Output Data Rate, Zero Latency Disabled or 2.5 SPS Output Data Rate, Zero Latency Enabled)

Simultaneous 50 Hz/60 Hz rejection can also be achieved using the REJ60 bit in the filter register. When the sinc filter places a notch a 50 Hz, the REJ60 bit places a first order notch at 60 Hz. The output data rate is 50 SPS when zero latency is disabled and 12.5 SPS when zero latency is enabled. Figure 88 shows the frequency response of the $sinc^4$ filter. The filter provides 50 Hz ± 1 Hz and 60 Hz ± 1 Hz rejection of 82 dB minimum, assuming a stable master clock.

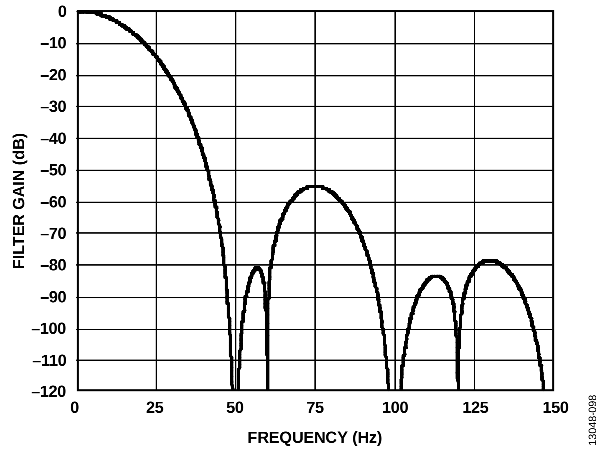


Figure 88. $Sinc^4$ Filter Response (50 SPS Output Data Rate, Zero Latency Disabled or 12.5 SPS Output Data Rate, Zero Latency Enabled, REJ60 = 1)

SINC³ FILTER

A $sinc^3$ filter can be used instead of the $sinc^4$ filter. The filter is selected using the filter bits in the filter register. This filter has good noise performance, moderate settling time, and moderate 50 Hz and 60 Hz (±1 Hz) rejection. In Figure 89, the blocks shown in gray are unused.

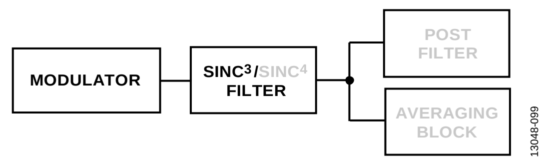


Figure 89. $Sinc^3$ Filter

Sinc³ Output Data Rate and Settling Time

The output data rate (the rate at which conversions are available on a single channel when the ADC is continuously converting) equals

$$f_{ADC} = f_{CLK}/(32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency (614.4 kHz in full power mode, 153.6 kHz in mid power mode and 76.8 kHz in low power mode).
FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

The output data rate can be programmed from

- 9.38 SPS to 19,200 SPS for full power mode
- 2.35 SPS to 4800 SPS for mid power mode
- 1.17 SPS to 2400 SPS for low power mode

The settling time for the $sinc^3$ filter is equal to

$$t_{SETTLE} = (3 \times 32 \times FS[10:0] + Dead\ Time)/f_{CLK}$$

where *Dead Time* = 60 when *FS[10:0]* = 1 and 94 *FS[10:0]* >1.

The 3 dB frequency is equal to

$$f_{3dB} = 0.272 \times f_{ADC}$$

Table 57 gives some examples of FS[10:0] settings and the corresponding output data rates and settling times.

Table 57. Examples of Output Data Rates and the Corresponding Settling Times for the Sinc^3 Filter

Power Mode	FS[10:0]	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4 kHz)	1920	10	300.15
	384	50	60.15
	320	60	50.15
Mid Power (f_{CLK} = 153.6 kHz)	480	10	300.61
	96	50	60.61
	80	60	50.61
Low Power (f_{CLK} = 76.8 kHz)	240	10	301.22
	48	50	61.22
	40	60	51.22

When a channel change occurs, the modulator and filter are reset. The complete settling time is allowed to generate the first conversion after the channel change (see Figure 90). Subsequent conversions on this channel are available at $1/f_{ADC}$.

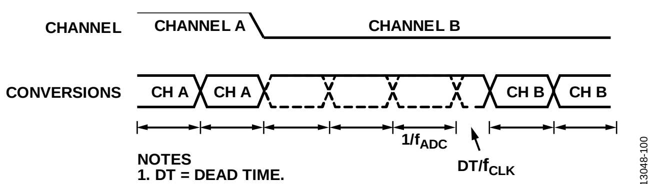


Figure 90. Sinc^3 Channel Change

When conversions are performed on a single channel and a step change occurs, the ADC does not detect the change in the analog input. Therefore, it continues to output conversions at the programmed output data rate. However, it is at least three conversions later before the output data accurately reflects the analog input. If the step change occurs while the ADC is processing a conversion, the ADC takes four conversions after the step change to generate a fully settled result.

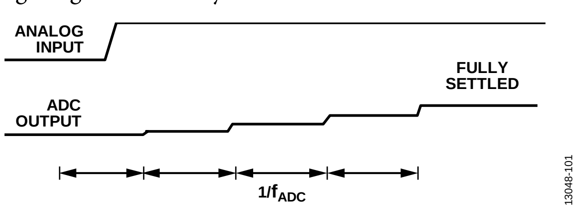


Figure 91. Asynchronous Step Change in the Analog Input

Sinc^3 Zero Latency

Zero latency is enabled by setting the SINGLE_CYCLE bit in the filter register to 1. With zero latency, the conversion time when continuously converting on a single channel approximately equals the settling time. The benefit of this mode is that a similar period of time elapses between all conversions irrespective of whether the conversions occur on one channel or whether several channels are used.

When the analog input is continuously sampled on a single channel, the output data rate equals

$$f_{ADC} = f_{CLK}/(3 \times 32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency.
FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register.

When switching channels, there is an extra delay in the first conversion of

$$Dead\ Time/f_{CLK}$$

where *Dead Time* = 60 when FS[10:0] = 1 or 94 when FS > 1.

At low output data rates, this extra delay has little impact on the value of the settling time. However, at high output data rates, the delay must be considered. Table 58 summarizes the output data rate when continuously converting on a single channel and the settling time when switching between channels for a sample of FS[10:0].

When the user selects another channel, the AD7124-8 allows the complete settling time to generate the first conversion after the channel change. Therefore, the ADC automatically operates in zero latency mode when several channels are enabled—setting the SINGLE_CYCLE bit has no benefits.

When the analog input is constant or a channel change occurs, valid conversions are available at a near constant output data rate. When conversions are being performed on a single channel and a step change occurs on the analog input, the ADC continues to output fully settled conversions if the step change is synchronized with the conversion process. If the step change is asynchronous, one conversion is output from the ADC that is not completely settled (see Figure 92).

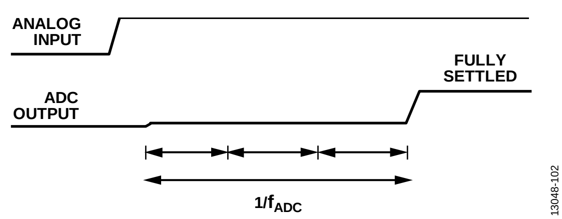


Figure 92. Sinc^3 Zero Latency Operation

Table 58. Examples of Output Data Rates and the Corresponding Settling Times for the Sinc^3 Filter (Zero Latency)

Power Mode	FS[10:0]	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4 kHz)	1920	3.33	300.15
	384	16.67	60.15
	320	20	50.15
Mid Power (f_{CLK} = 153.6 kHz)	480	3.33	300.61
	96	16.67	60.61
	80	20	50.61
Low Power (f_{CLK} = 76.8 kHz)	240	3.33	301.22
	48	16.67	61.22
	40	20	51.22

Sequencer

The description in the Sinc3 Filter section is valid when manually switching channels, for example, writing to the device to change channels. When multiple channels are enabled, the on-chip sequencer is automatically used; the device automatically sequences between all enabled channels. In this case, the first conversion takes the complete settling time as listed in Table 57. For all subsequent conversions, the time needed for each conversion is also the settling time, but the dead time is reduced to 30.

Sinc^3 50 Hz and 60 Hz Rejection

Figure 93 shows the frequency response of the sinc^3 filter when the output data rate is programmed to 50 SPS and zero latency is disabled. For the same configuration but with zero latency enabled, the filter response remains the same but the output data rate is 16.67 SPS. The sinc^3 filter gives 50 Hz ± 1 Hz rejection of 95 dB minimum for a stable master clock.

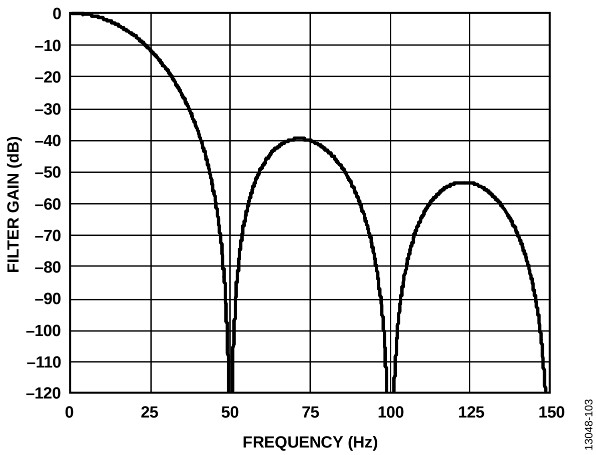


Figure 93. Sinc^3 Filter Response (50 SPS Output Data Rate, Zero Latency Disabled or 16.67 SPS Output Data Rate, Zero Latency Enabled)

Figure 94 shows the frequency response of the sinc^3 filter when the output data rate is programmed to 60 SPS and zero latency is disabled. For the same configuration but with zero latency enabled, the filter response remains the same but the output data rate is 20 SPS. The sinc^3 filter has rejection of 95 dB minimum at 60 Hz ± 1 Hz, assuming a stable master clock.

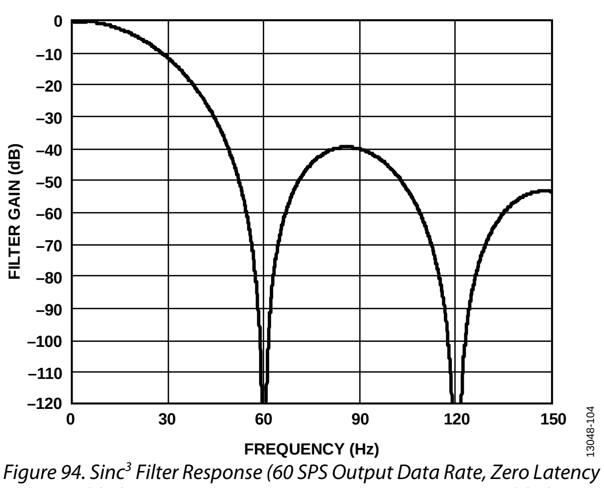


Figure 94. Sinc^3 Filter Response (60 SPS Output Data Rate, Zero Latency Disabled or 20 SPS Output Data Rate, Zero Latency Enabled)

When the output data rate is 10 SPS with zero latency disabled or 3.33 SPS with zero latency enabled, simultaneous 50 Hz and 60 Hz rejection is obtained. The sinc^3 filter has rejection of 100 dB minimum at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz (see Figure 95).

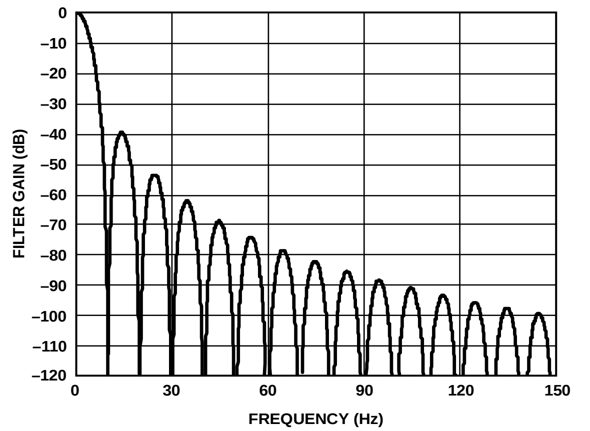


Figure 95. Sinc^3 Filter Response (10 SPS Output Data Rate, Zero Latency Disabled or 3.33 SPS Output Data Rate, Zero Latency Enabled)

Simultaneous 50 Hz and 60 Hz rejection can also be achieved using the REJ60 bit in the filter register. When the sinc filter places a notch a 50 Hz, the REJ60 bit places a first order notch at 60 Hz. The output data rate is 50 SPS when zero latency is disabled and 16.67 SPS when zero latency is enabled. Figure 96 shows the frequency response of the sinc^3 filter with this configuration. Assuming a stable clock, the rejection at 50 Hz and 60 Hz (±1 Hz) is in excess of 67 dB minimum.

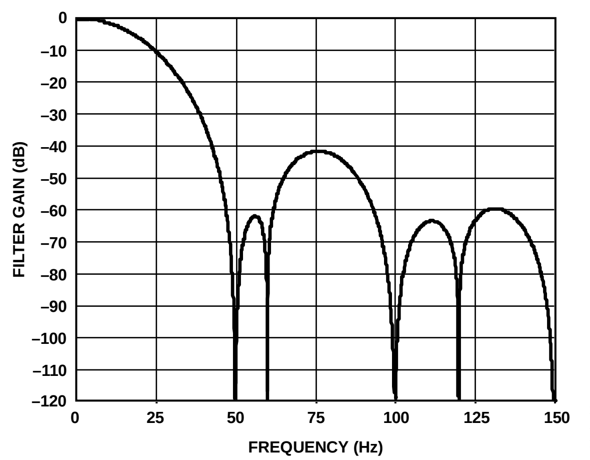


Figure 96. Sinc^3 Filter Response (50 SPS Output Data Rate, Zero Latency Disabled or 16.67 SPS Output Data Rate, Zero Latency Enabled, REJ60 = 1)

FAST SETTLING MODE (SINC^4 + SINC^1 FILTER)

In fast settling mode, the settling time is close to the inverse of the first filter notch; therefore, the user can achieve 50 Hz and/or 60 Hz rejection at an output data rate close to 1/50 Hz or 1/60 Hz. The settling time is approximately equal to 1/output data rate. Therefore, the conversion time is near constant when converting on a single channel or when converting on several channels.

Enable the fast settling mode using the filter bits in the filter register. In fast settling mode, a $sinc^1$ filter is included after the $sinc^4$ filter. The $sinc^1$ filter averages by 16 in the full power and mid power modes and averages by 8 in the low power mode. In Figure 97, the blocks shown in gray are unused.

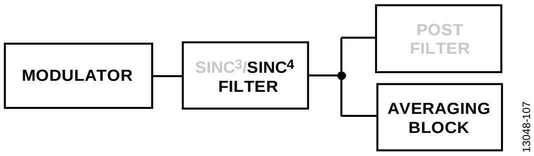


Figure 97. Fast Settling Mode, $Sinc^4 + Sinc^1$ Filter

Output Data Rate and Settling Time, $Sinc^4 + Sinc^1$ Filter

When continuously converting on a single channel, the output data rate is

$$f_{ADC} = f_{CLK}/((4 + Avg - 1) \times 32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency (614.4 kHz in full power mode, 153.6 kHz in mid power mode, and 76.8 kHz in low power mode).
Avg is 16 for the full or mid power mode and 8 for low power mode.
FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

When another channel is selected by the user, there is an extra delay in the first conversion. The settling time is equal to

$$t_{SETTLE} = ((4 + Avg - 1) \times 32 \times FS[10:0] + Dead\ Time)/ f_{CLK}$$

where *Dead Time* = 94.

The 3 dB frequency is equal to

$$f_{3dB} = 0.44 \times f_{ADC}$$

Table 59 lists sample FS[10:0] settings and the corresponding output data rates and settling times.

Table 59. Examples of Output Data Rates and the Corresponding Settling Times (Fast Settling Mode, $Sinc^4 + Sinc^1$)

Power Mode	FS[10:0]	First Notch (Hz)	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4 kHz, Average by 16)	120	10	8.42	118.9
	24	50	42.11	23.9
	20	60	50.53	19.94
Mid Power (f_{CLK} = 153.6 kHz, Average by 16)	30	10	8.42	119.36
	6	50	42.11	24.36
	5	60	50.53	20.4
Low Power (f_{CLK} = 76.8 kHz, Average by 8)	30	10	7.27	138.72
	6	50	36.36	28.72
	5	60	43.64	24.14

When the analog input is constant or a channel change occurs, valid conversions are available at a near constant output data rate.

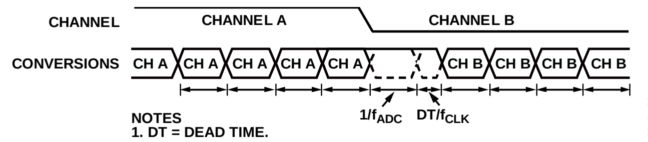


Figure 98. Fast Settling, $Sinc^4 + Sinc^1$ Filter

When the device is converting on a single channel and a step change occurs on the analog input, the ADC does not detect the change and continues to output conversions. If the step change is synchronized with the conversion, only fully settled results are output from the ADC. However, if the step change is asynchronous to the conversion process, there is one intermediate result, which is not completely settled (see Figure 99).

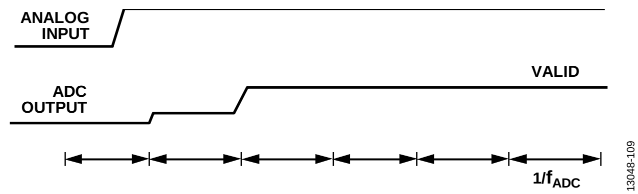


Figure 99. Step Change on the Analog Input, $Sinc^4 + Sinc^1$ Filter

Sequencer

The description in the Fast Settling Mode ($Sinc^4 + Sinc^1$ Filter) section is valid when manually switching channels, for example, writing to the device to change channels. When multiple channels are enabled, the on-chip sequencer is automatically used; the device automatically sequences between all enabled channels. In this case, the first conversion takes the complete settling time as listed in Table 59. For all subsequent conversions, the time needed for each conversion is also the settling time, but the dead time is reduced to 30.

50 Hz and 60 Hz Rejection, $Sinc^4 + Sinc^1$ Filter

Figure 100 shows the frequency response when FS[10:0] is set to 24 in the full power mode or 6 in the mid power mode or low power mode. Table 59 lists the corresponding output data rate. The sinc filter places the first notch at

$$f_{NOTCH} = f_{CLK}/(32 \times FS[10:0])$$

The $sinc^1$ filter places notches at f_{NOTCH}/Avg (Avg equaling 16 for the full power mode and mid power mode and equaling 8 for the low power mode). Notches are also placed at multiples of this frequency; therefore, when FS[10:0] is set to 6 in the full power mode or mid power mode, a notch is placed at 800 Hz due to the sinc filter and notches are placed at 50 Hz and multiples of 50 Hz due to the averaging. In low power mode, a notch is placed at 400 Hz due to the sinc filter and notches are placed at 50 Hz and multiples of 50 Hz due to the averaging.

The notch at 50 Hz is a first-order notch; therefore, the notch is not wide. This means that the rejection at 50 Hz exactly is good, assuming a stable master clock. However, in a band of 50 Hz ± 1 Hz, the rejection degrades significantly. The rejection at 50 Hz ± 0.5 Hz is 40 dB minimum, assuming a stable clock; therefore, a good master clock source is recommended when using fast settling mode.

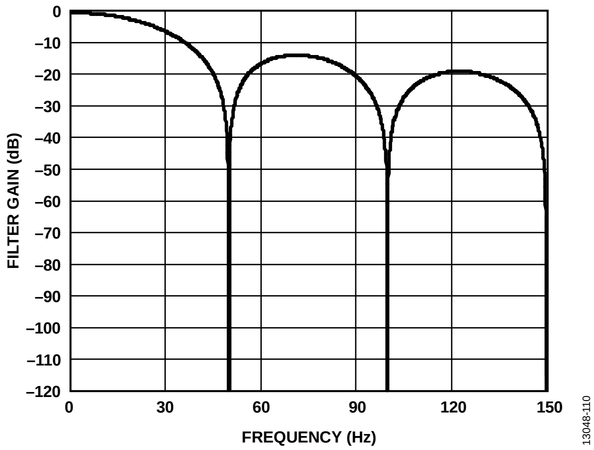


Figure 100. 50 Hz Rejection

Figure 101 shows the filter response when FS[10:0] is set to 20 in full power mode or 5 in the mid power and low power modes. In this case, a notch is placed at 60 Hz and multiples of 60 Hz. The rejection at 60 Hz ± 0.5 Hz is equal to 40 dB minimum.

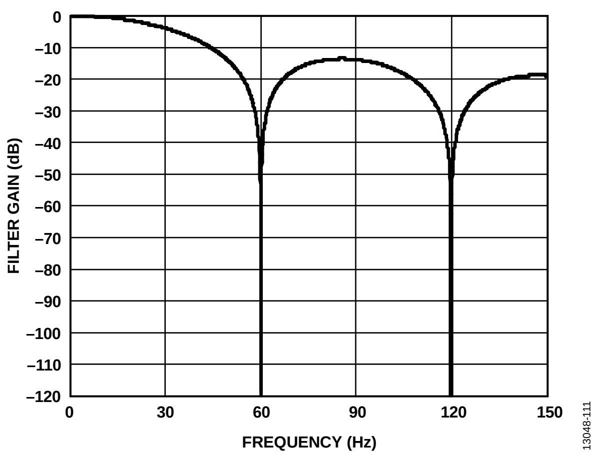


Figure 101. 60 Hz Rejection

Simultaneous 50 Hz/60 Hz rejection is achieved when FS[10:0] is set to 384 in full power mode or 30 in the mid power and low power modes. Notches are placed at 10 Hz and multiples of 10 Hz, thereby giving simultaneous 50 Hz and 60 Hz rejection. The rejection at 50 Hz ± 0.5 Hz and 60 Hz ± 0.5 Hz is 44 dB typically.

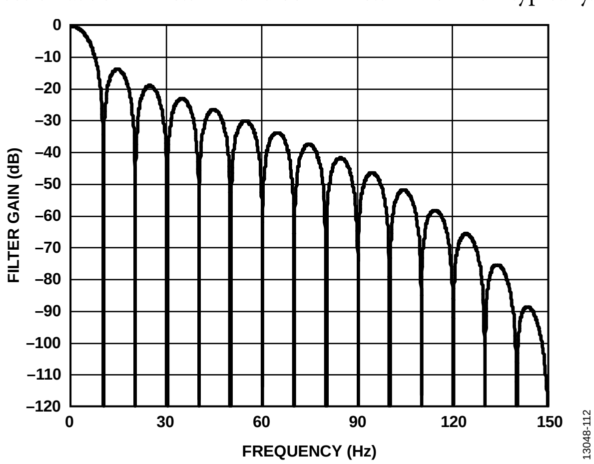


Figure 102. Simultaneous 50 Hz and 60 Hz Rejection

FAST SETTLING MODE (SINC³ + SINC¹ FILTER)

In fast settling mode, the settling time is close to the inverse of the first filter notch; therefore, the user can achieve 50 Hz and/or 60 Hz rejection at an output data rate close to 1/50 Hz or 1/60 Hz. The settling time is approximately equal to 1/output data rate. Therefore, the conversion time is near constant when converting on a single channel or when converting on several channels.

Enable the fast settling mode using the filter bits in the filter register. In fast settling mode, a sinc¹ filter is included after the sinc³ filter. The sinc1 filter averages by 16 in the full power and mid power modes and averages by 8 in low power mode. In Figure 103, the blocks shown in gray are unused.

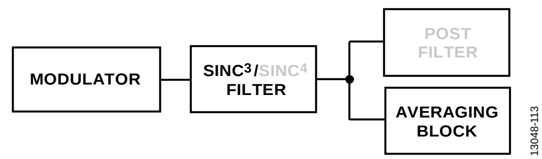


Figure 103. Fast Settling Mode, Sinc³ + Sinc¹ Filter

Output Data Rate and Settling Time, Sinc³ + Sinc¹ Filter

When continuously converting on a single channel, the output data rate is

$$f_{ADC} = f_{CLK}/((3 + Avg - 1) \times 32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency (614.4 kHz in full power mode, 153.6 kHz in mid power mode, and 76.8 kHz in low power mode).
Avg is 16 in full or mid power mode and 8 in low power mode.
FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

When another channel is selected by the user, there is an extra delay in the first conversion. The settling time is equal to

$$t_{SETTLE} = ((3 + Avg - 1) \times 32 \times FS[10:0] + Dead\ Time)/ f_{CLK}$$

where *Dead Time* = 94.

The 3 dB frequency is equal to

$$f_{3dB} = 0.44 \times f_{NOTCH}$$

Table 60 lists some sample FS[10:0] settings and the corresponding output data rates and settling times.

Table 60. Examples of Output Data Rates and the Corresponding Settling Times (Fast Settling Mode, Sinc³ + Sinc¹)

Power Mode	FS[10:0]	First Notch (Hz)	Output Data Rate (SPS)	Settling Time (ms)
Full Power (f_{CLK} = 614.4 kHz, Average by 16)	120	10	8.89	112.65
	24	50	44.44	22.65
	20	60	53.33	18.9
Mid Power (f_{CLK} = 153.6 kHz, Average by 16)	30	10	8.89	113.11
	6	50	44.44	23.11
	5	60	53.33	19.36
Low Power (f_{CLK} = 76.8 kHz, Average by 8)	30	10	8	126.22
	6	50	40	26.22
	5	60	48	22.06

When the analog input is constant or a channel change occurs, valid conversions are available at a near constant output data rate.

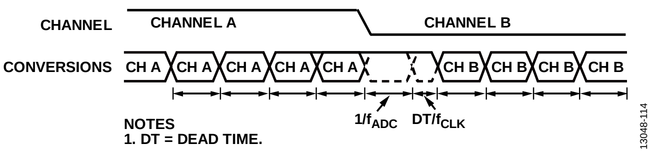


Figure 104. Fast Settling, $Sinc^3 + Sinc^1$ Filter

When the device is converting on a single channel and a step change occurs on the analog input, the ADC does not detect the change and continues to output conversions. When the step change is synchronized with the conversion, only fully settled results are output from the ADC. However, if the step change is asynchronous to the conversion process, one intermediate result is not completely settled (see Figure 105).

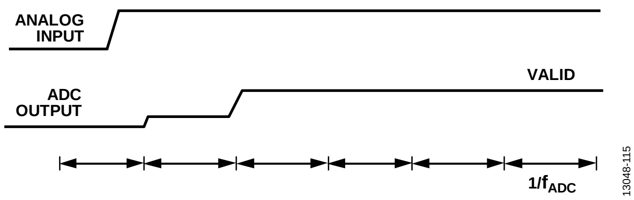


Figure 105. Step Change on the Analog Input, $Sinc^3 + Sinc^1$ Filter

Sequencer

The description in the Fast Settling Mode ($Sinc^3 + Sinc^1$ Filter) section is valid when manually switching channels, for example, writing to the device to change channels. When multiple channels are enabled, the on-chip sequencer is automatically used; the device automatically sequences between all enabled channels. In this case, the first conversion takes the complete settling time as listed in Table 60. For all subsequent conversions, the time needed for each conversion is also the settling time, but the dead time is reduced to 30.

50 Hz and 60 Hz Rejection, $Sinc^3 + Sinc^1$ Filter

Figure 106 shows the frequency response when FS[10:0] is set to 24 in the full power mode or 6 in the mid power mode or low power mode. Table 60 lists the corresponding output data rate.

The sinc filter places the first notch at

$$f_{NOTCH} = f_{CLK}/(32 \times FS[10:0])$$

The averaging block places notches at f_{NOTCH}/Avg (Avg equaling 16 for the full power mode and mid power mode and equaling 8 for the low power mode). Notches are also placed at multiples of this frequency; therefore, when FS[10:0] is set to 6 in full power mode or mid power mode, a notch is placed at 800 Hz due to the sinc filter and notches are placed at 50 Hz and multiples of 50 Hz due to the averaging. In low power mode, a notch is placed at 400 Hz due to the sinc filter and notches are placed at 50 Hz and multiples of 50 Hz due to the averaging.

The notch at 50 Hz is a first-order notch; therefore, the notch is not wide. This means that the rejection at 50 Hz exactly is good, assuming a stable master clock. However, in a band of 50 Hz ± 1 Hz, the rejection degrades significantly. The rejection at 50 Hz ± 0.5 Hz is 40 dB minimum, assuming a stable clock; therefore, a good master clock source is recommended when using fast settling mode.

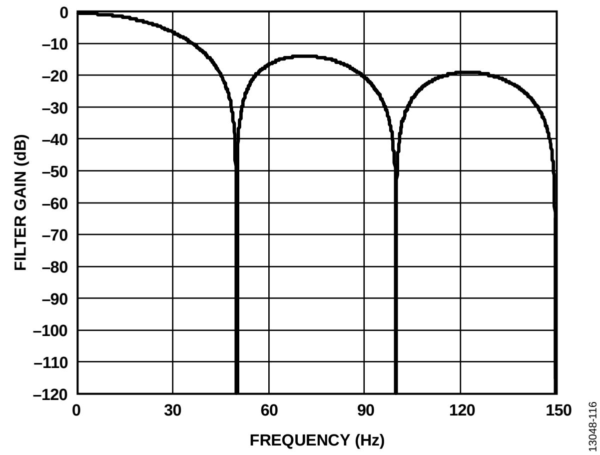


Figure 106. 50 Hz Rejection

Figure 107 shows the filter response when FS[10:0] is set to 20 in full power mode or 5 in the mid power and low power modes. In this case, a notch is placed at 60 Hz and multiples of 60 Hz. The rejection at 60 Hz ± 0.5 Hz is equal to 40 dB minimum.

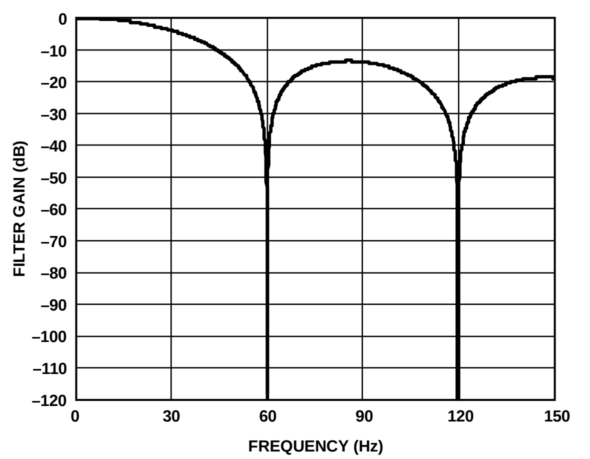


Figure 107. 60 Hz Rejection

Simultaneous 50 Hz/60 Hz rejection is achieved when FS[10:0] is set to 384 in full power mode or 30 in the mid power and low power modes. Notches are placed at 10 Hz and multiples of 10 Hz, thereby giving simultaneous 50 Hz and 60 Hz rejection. The rejection at 50 Hz ± 0.5 Hz and 60 Hz ± 0.5 Hz is 42 dB typically.

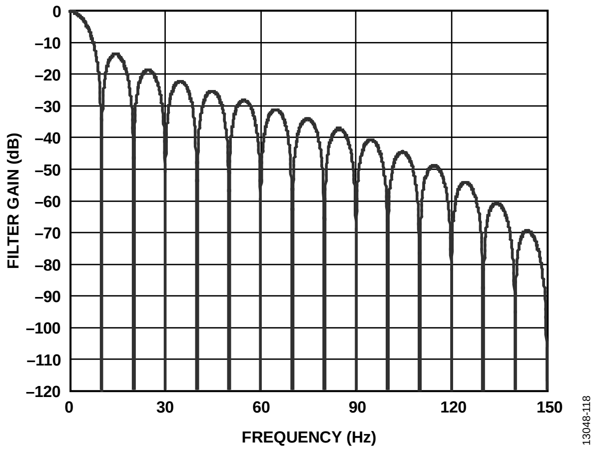


Figure 108. Simultaneous 50 Hz and 60 Hz Rejection

POST FILTERS

The post filters provide rejection of 50 Hz and 60 Hz simultaneously and allow the user to trade off settling time and rejection. These filters can operate up to 27.27 SPS or can reject up to 90 dB of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz interference. These filters are realized by post filtering the output of the $sinc^3$ filter. The filter bits must be set to all 1s to enable the post filter. The post filter option to use is selected using the POST_FILTER bits in the filter register. In Figure 109, the blocks shown in gray are unused.

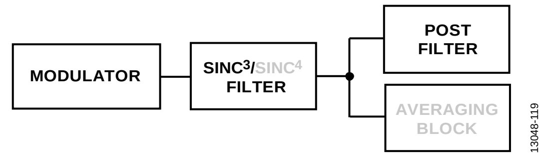


Figure 109. Post Filters

Table 61 shows the output data rates with the accompanying settling times and the rejection.

When continuously converting on a single channel, the first conversion requires a time of t_{SETTLE}. Subsequent conversions occur at $1/f_{ADC}$. When multiple channels are enabled (either manually or using the sequencer), the settling time is required to generate a valid conversion on each enabled channel.

Table 61. AD7124-8 Post Filters: Output Data Rate, Settling Time (t_{SETTLE}), and Rejection

Output Data Rate (SPS)	f_{3dB} (Hz)	t_{SETTLE}, Full Power Mode (ms)	t_{SETTLE}, Mid Power Mode (ms)	t_{SETTLE}, Low Power Mode (ms)	Simultaneous Rejection of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz (dB)[1]
27.27	17.28	38.498	38.998	39.662	47
25	15.12	41.831	42.331	42.995	62
20	13.38	51.831	52.331	52.995	86
16.67	12.66	61.831	62.331	62.995	92

[1] Stable master clock used.

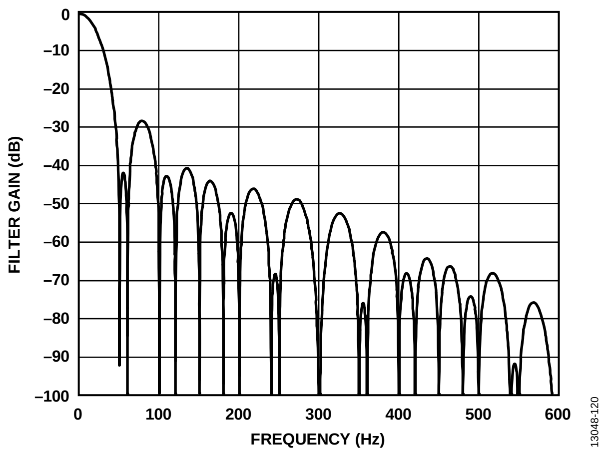


Figure 110. DC to 600 Hz, 27.27 SPS Output Data Rate, 36.67 ms Settling Time

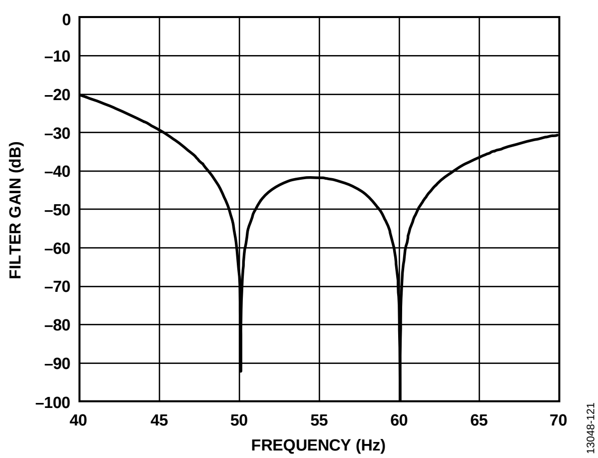


Figure 111. Zoom in 40 Hz to 70 Hz, 27.27 SPS Output Data Rate, 36.67 ms Settling Time

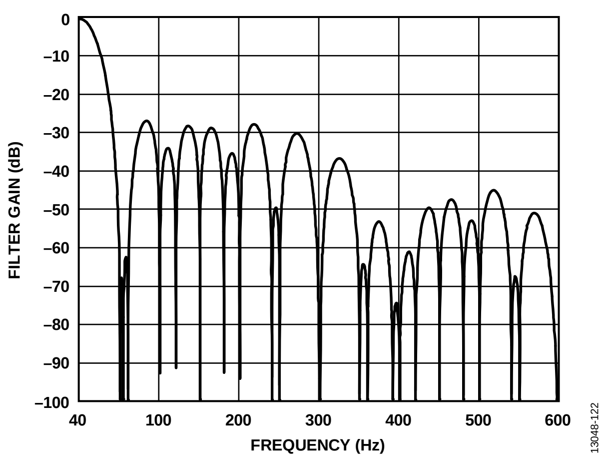


Figure 112. DC to 600 Hz, 25 SPS Output Data Rate, 40 ms Settling Time

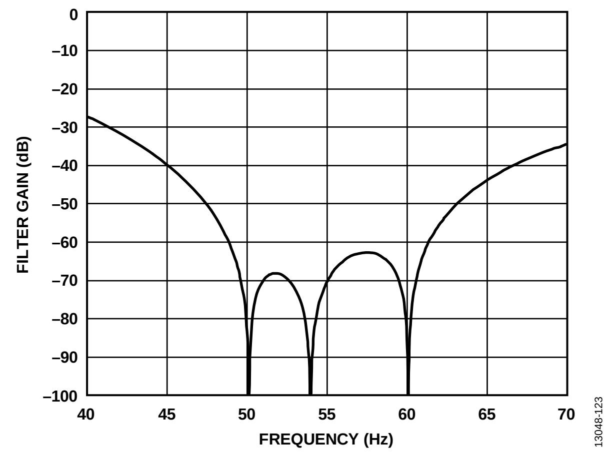


Figure 113. Zoom in 40 Hz to 70 Hz, 25 SPS Output Data Rate, 40 ms Settling Time

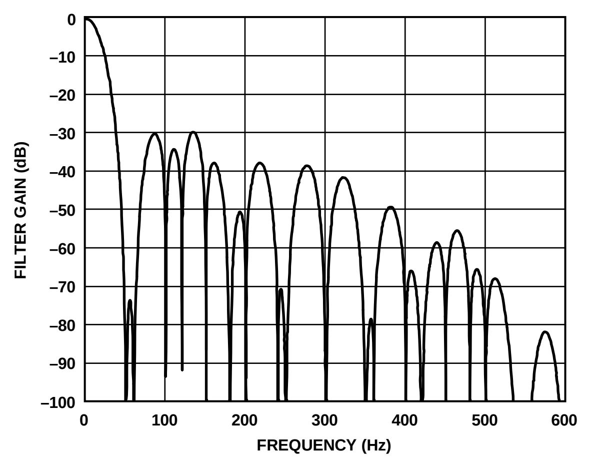


Figure 114. DC to 600 Hz, 20 SPS Output Data Rate, 50 ms Settling Time

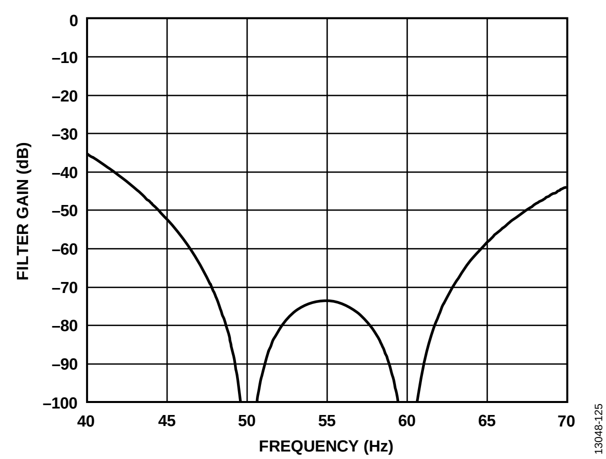


Figure 115. Zoom in 40 Hz to 70 Hz, 20 SPS Output Data Rate, 50 ms Settling Time

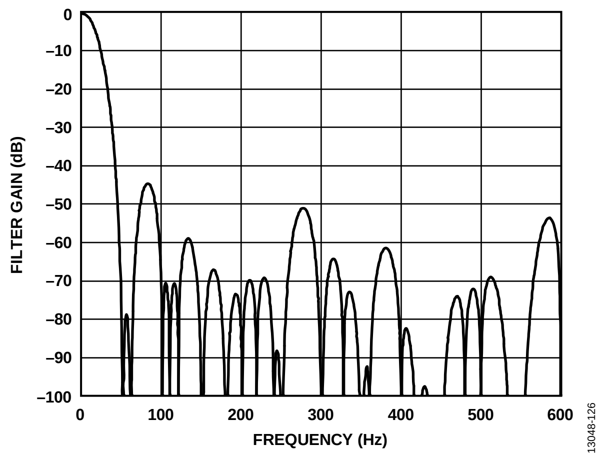


Figure 116. DC to 600 Hz,16.667 SPS Output Data Rate, 60 ms Settling Time

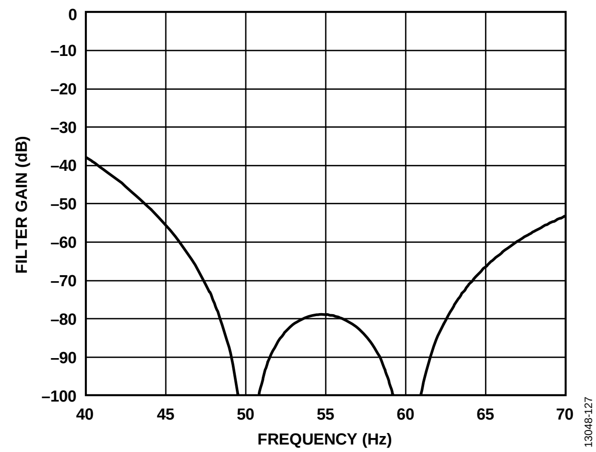


Figure 117. Zoom in 40 Hz to 70 Hz, 16.667 SPS Output Data Rate, 60 ms Settling Time

SUMMARY OF FILTER OPTIONS

The AD7124-8 has several filter options. The filter that is chosen affects the output data rate, settling time, the rms noise, the stop band attenuation, and the 50 Hz and 60 Hz rejection.

Table 62 shows some sample configurations and the corresponding performance in terms of throughput and 50 Hz and 60 Hz rejection.

Table 62. Filter Summary[1]

Filter	Power Mode	Output Data Rate (SPS)	REJ60	50 Hz Rejection (dB)[2]
$Sinc^4$	All	10	0	120 dB (50 Hz and 60 Hz)
	All	50	0	120 dB (50 Hz only)
	All	50	1	82 dB (50 Hz and 60 Hz)
	All	60	0	120 dB (60 Hz only)
$Sinc^4$, Zero Latency	All	12.5	0	120 dB (50 Hz only)
	All	12.5	1	82 dB (50 Hz and 60 Hz)
	All	15	0	120 dB (60 Hz only)
$Sinc^3$	All	10	0	100 dB (50 Hz and 60 Hz)
	All	50	0	95 dB (50 Hz only)
	All	50	1	67 dB (50 Hz and 60 Hz)
	All	60	0	95 dB (60 Hz only)
Fast Settling ($Sinc^4$ + $Sinc^1$)	Full/mid	50.53	0	40 dB (60 Hz only)
	Low	43.64	0	40 dB (60 Hz only)
	Full/mid	42.11	0	40 dB (50 Hz only)
	Low	36.36	0	40 dB (50 Hz only)
	Full/mid	8.4	0	40 dB (50 Hz and 60 Hz)
	Low	7.27	0	40 dB (50 Hz and 60 Hz)
Fast Settling ($Sinc^3$ + $Sinc^1$)	Full/mid	53.33	0	40 dB (60 Hz only)
	Low	48	0	40 dB (60 Hz only)
	Full/mid	44.44	0	40 dB (50 Hz only)
	Low	40	0	40 dB (50 Hz only)
	Full/mid	8.89	0	40 dB (50 Hz and 60 Hz)
	Low	8	0	40 dB (50 Hz and 60 Hz)
Post Filter	All	27.27	0	47 dB (50 Hz and 60 Hz)
	All	25	0	62 dB (50 Hz and 60 Hz)
	All	20	0	85 dB (50 Hz and 60 Hz)
	All	16.67	0	90 dB (50 Hz and 60 Hz)

[1] These calculations assume a stable master clock.
[2] For fast settling mode, the 50 Hz/60 Hz rejection is measured in a band of ±0.5 Hz around 50 Hz and/or 60 Hz. For all other modes, a region of ±1 Hz around 50 Hz and/or 60 Hz is used.

DIAGNOSTICS

The AD7124-8 has numerous diagnostic functions on chip. Use these features to ensure

- Read/write operations are to valid registers only
- Only valid data is written to the on-chip registers
- Appropriate decoupling is used on the LDOs
- The external reference, if used, is present
- The ADC modulator and filter are working within specification

SIGNAL CHAIN CHECK

Functions such as the reference and power supply voltages can be selected as inputs to the ADC. The AD7124-8 can therefore check the voltages connected to the device. The AD7124-8 also generates an internal 20 mV signal that can be applied internally to a channel by selecting the V_20MV_P to V_20MV_M channel in the channel register. The PGA can be checked using this function. As the PGA setting is increased, for example, the signal as a percent of the analog input range is reduced by a factor of two. This allows the user to check that the PGA is functioning correctly.

REFERENCE DETECT

The AD7124-8 includes on-chip circuitry to detect if there is a valid reference for conversions or calibrations when the user selects an external reference as the reference source. This is a valuable feature in applications such as RTDs or strain gages where the reference is derived externally.

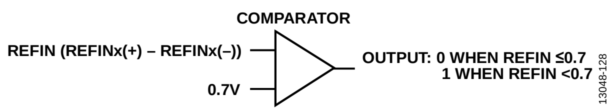


Figure 118. Reference Detect Circuitry

This feature is enabled when the REF_DET_ERR_EN bit in the ERROR_EN register is set to 1. If the voltage between the selected REFINx(+) and REFINx(−) pins goes below 0.7 V, or either the REFINx(+) or REFINx(−) inputs are open circuit, the AD7124-8 detects that it no longer has a valid reference. In this case, the REF_DET_ERR bit in the error register is set to 1. The ERR bit in the status register is also set.

If the AD7124-8 is performing normal conversions and the REF_DET_ERR bit becomes active, the conversion results revert to all 1s. Therefore, it is not necessary to continuously monitor the status of the REF_DET_ERR bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC data register is all 1s.

If the AD7124-8 is performing either offset or full-scale calibrations and the REF_DET_ERR bit becomes active, the updating of the respective calibration register is inhibited to avoid loading incorrect coefficients to the register, and the REF_DET_ERR bit is set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, check the status of the REF_DET_ERR bit at the end of the calibration cycle.

The reference detect flag may be set when the device exits of standby mode. Therefore, read the error register after exiting standby mode to reset the flag to 0.

CALIBRATION, CONVERSION, AND SATURATION ERRORS

The conversion process and calibration process can also be monitored by the AD7124-8. These diagnostics check the analog input used as well as the modulator and digital filter during conversions or calibration. The functions can be enabled using the ADC_CAL_ERR_EN, ADC_CONV_ERR_EN, and ADC_SAT_ERR_EN bits in the ERROR_EN register. With these functions enabled, the ADC_ CAL_ERR, ADC_CONV_ERR, and ADC_SAT_ERR bits are set if an error occurs.

The ADC_CONV_ERR flag is set if there is an overflow or underflow in the digital filter. The ADC conversion clamps to all 0s or all 1s also. This flag is updated in conjunction with the update of the data register and can be cleared only by a read of the error register.

The ADC_SAT_ERR flag is set if the modulator outputs 20 consecutive 1s or 0s. This indicates that the modulator has saturated.

When an offset calibration is performed, the resulting offset coefficient must be between 0x7FFFFF and 0xF80000. If the coefficient is outside this range, the offset register is not updated and the ADC_CAL_ERR flag is set. During a full-scale calibration, overflow of the digital filter is checked. If an overflow occurs, the error flag is set and the gain register is not updated.

OVERVOLTAGE/UNDERVOLTAGE DETECTION

The overvoltage/undervoltage monitors check the absolute voltage on the AINx analog input pins. The absolute voltage must be within specification to meet the datasheet specifications. If the ADC is operated outside the datasheet limits, linearity degrades.

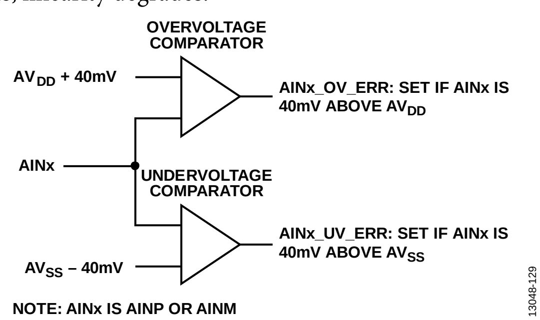


Figure 119. Analog Input Overvoltage/Undervoltage Monitors

The positive (AINP) and negative (AINM) analog inputs can be separately checked for overvoltages and undervoltages. The AINP_OV_ERR_EN and AINP_UV_ERR_EN bits in the ERROR_EN register enable the overvoltage/undervoltage diagnostics respectively. An overvoltage is flagged when the voltage on AINP exceeds AV_{DD} while an undervoltage is flagged when the voltage on AINP goes below AV_{SS}. Similarly, an overvoltage/undervoltage check on the negative analog input pin is enabled using the AINM_OV_ERR_EN and AINM_UV_ERR_EN bits in the ERROR_EN register. The error flags are AINP_OV_ERR, AINP_UV_ERR, AINM_OV_ERR, and AINM_UV_ERR in the error register.

When this function is enabled, the corresponding flags may be set in the error register. Therefore, the user must read the error register when the overvoltage/undervoltage checks are enabled to ensure that the flags are reset to 0.

POWER SUPPLY MONITORS

Along with converting external voltages, the ADC can monitor the voltage on the AV_{DD} pin and the IOV_{DD} pin. When the inputs of AV_{DD} to AV_{SS} or IOV_{DD} to DGND are selected, the voltage (AV_{DD} to AV_{SS} or IOV_{DD} to DGND) is internally attenuated by 6, and the resulting voltage is applied to the Σ-Δ modulator. This is useful because variations in the power supply voltage can be monitored.

LDO MONITORING

There are several LDO checks included on the AD7124-8. Like the external power supplies, the voltage generated by the analog and digital LDOs are selectable as inputs to the ADC. In addition, the AD7124-8 can continuously monitor the LDO voltages.

Power Supply Monitor

The voltage generated by the ALDO and DLDO can be monitored by enabling the ALDO_PSM_ERR_EN bit and the DLDO_PSM_ERR_EN bit, respectively, in the ERROR_EN register. When enabled, the output voltage of the LDO is continuously monitored. If the ALDO voltage drops below 1.6 V, the ALDO_PSM_ERR flag is asserted. If the DLDO voltage drops below 1.55 V, the DLDO_PSM_ERR flag is asserted. The bit remains set until the corresponding LDO voltage recovers. However, the bit is only cleared when the error register is read.

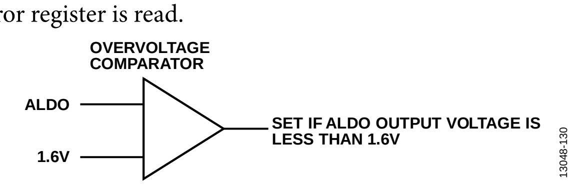


Figure 120. Analog LDO Monitor

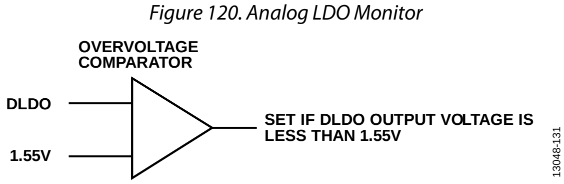


Figure 121. Digital LDO Monitor

The AD7124-8 can also test the circuitry used for the power supply monitoring. When the ALDO_PSM_TRIP_TEST_EN or DLDO_PSM_TRIP_TEST_EN bits are set, the input to the test circuitry is tied to GND rather than the LDO output. Set the corresponding ALDO_PSM_ERR or DLDO_PSM_ERR bit.

LDO Capacitor Detect

The analog and digital LDOs require an external decoupling capacitor of 0.1 µF. The AD7124-8 can check for the presence of this decoupling capacitor. Using the LDO_CAP_CHK bits in the ERROR_EN register, the LDO being checked is turned off and the voltage at the LDO output is monitored. If the voltage falls, this is considered a fail and the LDO_CAP_ERR bit in the error register is set.

Only the analog LDO or digital LDO can be tested for the presence of the decoupling capacitor at any one time. This test also interferes with the conversion process.

The circuitry used to check for missing decoupling capacitors can also be tested by the AD7124-8. When the LDO_CAP_CHK_TEST_EN bit in the ERROR_EN register is set, the decoupling capacitor is internally disconnected from the LDO, forcing a fault condition. Therefore, when the LDO capacitor test is performed, a fault condition is reported, that is, the LDO_CAP_ERR bit in the error register is set.

MCLK COUNTER

A stable master clock is important as the output data rate, filter settling time, and the filter notch frequencies are dependent on the master clock. The AD7124-8 allows the user to monitor the master clock. When the MCLK_CNT_EN bit in the ERROR_EN register is set, the MCLK_COUNT register increments by 1 every 131 master clock cycles. The user can monitor this register over a fixed period of time. The master clock frequency can be determined from the result in the MCLK_COUNT register. The MCLK_COUNT register wraps around after it reaches its maximum value.

SPI SCLK COUNTER

The SPI SCLK counter counts the number of SCLK pulses used in each read and write operation. $\overline{CS}$ must frame every read and write operation when this function is used. All read and write operations are multiples of eight SCLK pulses (8, 16, 32, 40, 48). If the SCLK counter counts the SCLK pulses and the result is not a multiple of eight, an error is flagged; the SPI_SCLK_CNT_ERR bit in the error register is set. If a write operation is being performed and the SCLK contains an incorrect number of SCLK pulses, the value is not written to the addressed register and the write operation is aborted.

The SCLK counter is enabled by setting the SPI_SCLK_CNT_ERR_EN bit in the ERROR_EN register.

SPI READ/WRITE ERRORS

Along with the SCLK counter, the AD7124-8 can also check the read and write operations to ensure that valid registers are being addressed. When the SPI_READ_ERR_EN bit or the SPI_WRITE_ERR_EN bit in the ERROR_EN register are set, the AD7124-8 checks the address of the read/write operations. If the user attempts to write to or read from any register other than the user registers described in this data sheet, an error is flagged; the SPI_READ_ERR bit or the SPI_WRITE_ERR bit in the error register is set and the read/write operation is aborted.

This function, along with the SCLK counter and the CRC, makes the serial interface more robust. Invalid registers are not written to or read from. An incorrect number of SCLK pulses can cause the serial interface to go asynchronous and incorrect registers to be accessed. The AD7124-8 protects against these issues via the diagnostics.

SPI_IGNORE ERROR

At certain times, the on-chip registers are not accessible. For example, during power-up, the on-chip registers are set to their default values. The user must wait until this operation is complete before reading from or writing to registers. Also, when offset or gain calibrations are being performed, registers cannot be accessed. The SPI_IGNORE_ERR bit in the error register indicates when the on-chip registers cannot be accessed. This diagnostic is enabled by default. The function can be disabled using the SPI_IGNORE_ERR_EN bit in the ERROR_EN register.

Any read or write operations performed when SPI_IGNORE_ERR is enabled are ignored.

CHECKSUM PROTECTION

The AD7124-8 has a checksum mode that can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERR bit is set in the error register. However, to ensure that the register write was successful, read back the register and verify the checksum.

For CRC checksum calculations, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

The CRC_ERR_EN bit in the ERROR_EN register enables and disables the checksum.

The checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8-bit to 24-bit data. For a read transaction, the checksum is calculated using the command word and the 8-bit to 32-bit data output. Figure 122 and Figure 123 show SPI write and read transactions, respectively.

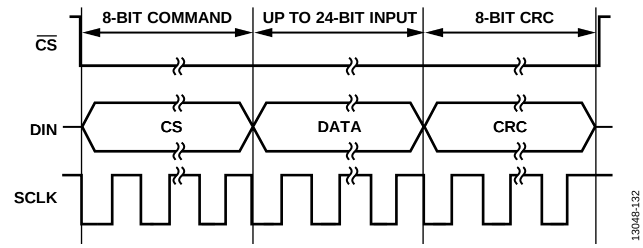


Figure 122. SPI Write Transaction with CRC

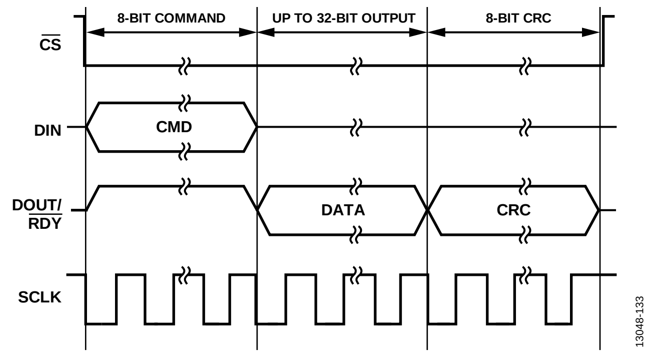


Figure 123. SPI Read Transaction with CRC

If checksum protection is enabled when continuous read mode is active, there is an implied read data command of 0x42 before every data transmission that must be accounted for when calculating the checksum value. This ensures a nonzero checksum value even if the ADC data equals 0x000000.

MEMORY MAP CHECKSUM PROTECTION

For added robustness, a CRC calculation is performed on the on-chip registers as well. The status register, data register, and MCLK counter register are not included in this check as their contents change continuously. The CRC is performed at a rate of 1/2400 seconds. Each time that the memory map is accessed, the CRC is recalculated. Events that cause the CRC to be recalculated are

- A user write
- An offset/full-scale calibration
- When the device is operated in single conversion mode and the ADC goes into idle mode following the completion of the conversion
- When exiting continuous read mode (the CONT_READ bit in the ADC_CONTROL register is set to 0)

The memory map CRC function is enabled by setting the MM_CRC_ERR_EN bit in the ERROR_EN register to 1. If an error occurs, the MM_CRC_ERR bit in the error register is set to 1.

CRC Calculation

The checksum, which is 8 bits wide, is generated using the polynomial

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR (exclusive OR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

Example of a Polynomial CRC Calculation—24-Bit Word: 0x654321 (8-Bit Command and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

```
Initial value          011001010100001100100001
                       01100101010000110010000100000000          left shifted eight bits
x8 + x2 + x + 1    =            100000111                        polynomial
  1001001000000110010000100000000      XOR result
  100000111                            polynomial
     1000110001100100001000000000      XOR result
     100000111                         polynomial
         11111110010000100000000       XOR result
         100000111                     polynomial value
          1111101110000100000000       XOR result
          100000111                    polynomial value
           111100000000100000000       XOR result
           100000111                   polynomial value
            11100111000100000000       XOR result
            100000111                  polynomial value
             1100100100100000000       XOR result
             100000111                 polynomial value
              100101010100000000       XOR result
              100000111                polynomial value
                 101101100000000       XOR result
                 100000111             polynomial value
                  1101011000000        XOR result
                   100000111           polynomial value
                    101010110000       XOR result
                    100000111          polynomial value
                      1010001000       XOR result
                      100000111        polynomial value
                        10000110       checksum = 0x86
```

BURNOUT CURRENTS

The AD7124-8 contains two constant current generators that can be programmed to 0.5 µA, 2 µA, or 4 µA. One generator sources current from AV_{DD} to AINP, and one sinks current from AINM to AV_{SS}. These currents enable open wire detection.

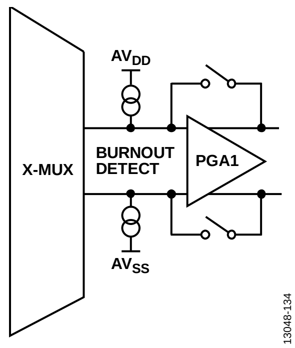


Figure 124. Burnout Currents

The currents are switched to the selected analog input pair. Both currents are either on or off. The burnout bits in the configuration register enable/disable the burnout currents along with setting the amplitude. Use these currents to verify that an external transducer is still operational before attempting to take measurements on that channel. After the burnout currents are turned on, they flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resulting voltage measured is near full scale, the user must verify why this is the case. A near full-scale reading can mean that the front-end sensor is open circuit. It can also mean that the front-end sensor is overloaded and is justified in outputting full scale, or that the reference may be absent and the REF_DET_ERR bit is set, thus clamping the data to all 1s.

When a conversion is close to full scale, the user must check these three cases before making a judgment. If the voltage measured is 0 V, it may indicate that the transducer has short circuited. For normal operation, these burnout currents are turned off by setting the burnout bits to zero. The current sources work over the normal absolute input voltage range specifications with buffers on.

TEMPERATURE SENSOR

Embedded in the AD7124-8 is a temperature sensor that is useful to monitor the die temperature. This is selected using the AINP[4:0] and AINM[4:0] bits in the channel register. The sensitivity is 13,584 codes/°C, approximately. The equation for the temperature sensor is

$$Temperature\ (°C) = ((Conversion - 0x800000)/13{,}584) - 272.5$$

The temperature sensor has an accuracy of ±0.5°C typically.

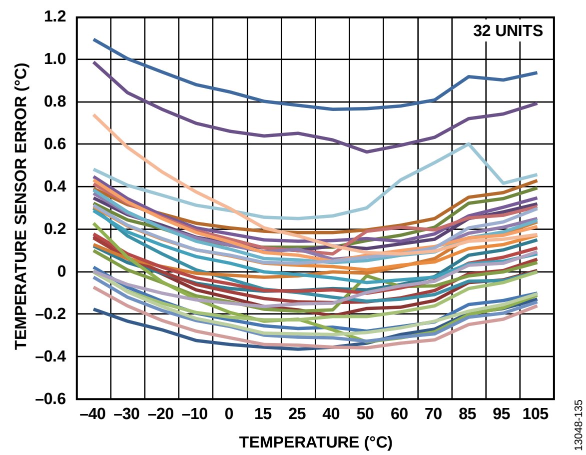


Figure 125. Temperature Sensor Error vs. Temperature

GROUNDING AND LAYOUT

The analog inputs and reference inputs are differential and, therefore, most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the device removes common-mode noise on these inputs. The analog and digital supplies to the AD7124-8 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the master clock frequency.

The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7124-8 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7124-8 is high and the noise levels from the converter are so low, care must be taken with regard to grounding and layout.

The PCB that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it results in the best shielding.

In any layout, the user must keep in mind the flow of currents in the system, ensuring that the paths for all return currents are as close as possible to the paths the currents took to reach their destinations.

Avoid running digital lines under the device because this couples noise onto the die and allows the analog ground plane to run under the AD7124-8 to prevent noise coupling. The power supply lines to the AD7124-8 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, whereas signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. The AD7124-8 has two power supply pins—AV_{DD} and IOV_{DD}. The AV_{DD} pin is referenced to AV_{SS}, and the IOV_{DD} pin is referenced to DGND. Decouple AV_{DD} with a 1 µF tantalum capacitor in parallel with a 0.1 µF capacitor to AV_{SS} on each pin. Place the 0.1 µF capacitor as close as possible to the device on each supply, ideally right up against the device. Decouple IOV_{DD} with a 1 µF tantalum capacitor in parallel with a 0.1 µF capacitor to DGND. All analog inputs must be decoupled to AV_{SS}. If an external reference is used, decouple the REFINx(+) and REFINx(−) pins to AV_{SS}.

The AD7124-8 also has two on-board LDO regulators—one that regulates the AV_{DD} supply and one that regulates the IOV_{DD} supply. For the REGCAPA pin, it is recommended that a 0.1 µF capacitor to AV_{SS} be used. Similarly, for the REGCAPD pin, it is recommended that a 0.1 µF capacitor to DGND be used.

If using the AD7124-8 with split supply operation, a separate plane must be used for AV_{SS}.

APPLICATIONS INFORMATION

The AD7124-8 offers a low cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, the device is more immune to noisy environments, making it ideal for use in sensor measurement, and industrial and process control applications.

TEMPERATURE MEASUREMENT USING A THERMOCOUPLE

Figure 126 outlines a connection from a thermocouple to the AD7124-8. In a thermocouple application, the voltage generated by the thermocouple is measured with respect to an absolute reference; thus, the internal reference is used for this conversion. The cold junction measurement uses a ratiometric configuration, so the reference is provided externally.

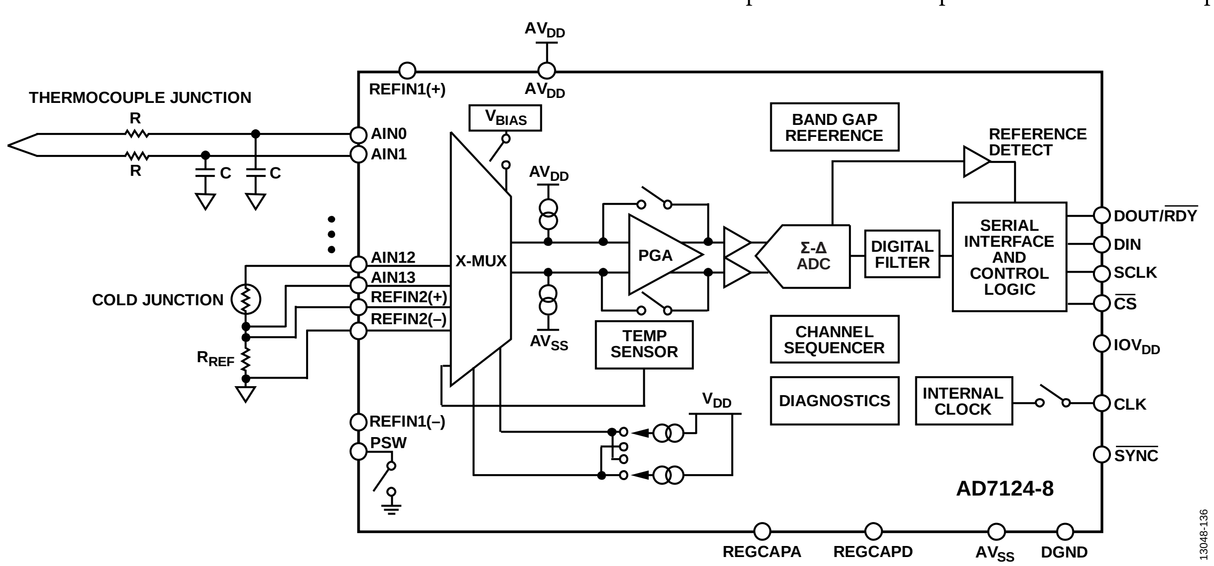
Because the signal from the thermocouple is small, the AD7124-8 is operated with the PGA enabled to amplify the signal from the thermocouple. As the input channel is buffered, large decoupling capacitors can be placed on the front end to eliminate any noise pickup that may be present in the thermocouple leads. The bias voltage generator provides a common-mode voltage so that the voltage generated by the thermocouple is biased up to (AV_{DD} − AV_{SS})/2. For thermocouple voltages that are centered about ground, the AD7124-8 can be operated with a split power supply (±1.8 V).

The cold junction compensation is performed using a thermistor in Figure 126. The on-chip excitation current supplies the thermistor. In addition, the reference voltage for the cold junction measurement is derived from a precision resistor in series with the thermistor. This allows a ratiometric measurement so that variation of the excitation current has no effect on the measurement (it is the ratio of the precision reference resistance to the thermistor resistance that is measured).

Most conversions are read from the thermocouple, with the cold junction being read only periodically as the cold junction temperature is stable or slow moving. If a T-type thermocouple is used, it can measure a temperature from −200°C to +400°C. The voltage generated over this temperature range is −8.6 mV to +17.2 mV. The AD7124-8 internal reference equals 2.5 V. Therefore, the PGA is set to 128. If the thermocouple uses the AIN0/AIN1 channel and the thermistor is connected to the AIN12/AIN13 channel, the conversion process is as follows:

1. Reset the ADC.
2. Select the power mode.
   Set the CHANNEL_0 register analog input to AIN0/AIN1. Assign Setup 0 to this channel. Configure Setup 0 to have a gain of 128 and select the internal reference. Select the filter type and set the output data rate.
3. Enable VBIAS on AIN0.
4. Set the CHANNEL_1 register analog input to AIN12/AIN13. Assign Setup 1 to this channel. Configure Setup 1 to have a gain of 1 and select the external reference REFIN2(±). Select the filter type and set the output data rate.
5. Enable the excitation current (IOUTx) and select a suitable value. Output this current to the AIN4 pin.
6. Enable the AIN0/AIN1 channel. Wait until $\overline{RDY}$ goes low. Read the conversion.
7. Continue to read nine further conversions from the AIN0/AIN1 channel.
8. Disable CHANNEL_0 and enable CHANNEL_1.
9. Wait until $\overline{RDY}$ goes low. Read one conversion.
10. Repeat Step 5 to Step 8.

Using the linearization equation for the T-type thermocouple, process the thermocouple voltage along with the thermistor voltage and compute the actual temperature at the thermocouple head.



NOTES
1. SIMPLIFIED BLOCK DIAGRAM SHOWN.

Figure 126. Thermocouple Application

The external antialias filter is omitted for clarity. However, such a filter is required to reject any interference at the modulator frequency and multiples of the modulator frequency. In addition, some filtering may be needed for EMI purposes. Both the analog inputs and the reference inputs can be buffered, which allows the user to connect any RC combination to the reference or analog input pins.

The required power mode depends on the performance required from the system along with the current consumption allowance for the system. In a field transmitter, low current consumption is essential. In this application, the low power mode or mid power mode is most suitable. In process control applications, power consumption is not a priority. Thus, full power mode may be selected. The full power mode offers higher throughput and lower noise.

The AD7124-8 on-chip diagnostics allow the user to check the circuit connections, monitor power supply, reference, and LDO voltages, check all conversions and calibrations for any errors, as well as monitor any read/write operations. In thermocouple applications, the circuit connections are verified using the reference detect and the burnout currents. The REF_DET_ERR flag is set if the external reference REFIN2(±) is missing. The burnout currents (available in the configuration registers) detect an open wire. For example, if the thermocouple is not connected and the burnout currents are enabled on the channel, the ADC outputs a conversion that is equal to or close to full scale. For best performance, enable the burnout currents periodically to check the connections but disable them as soon as the connections are verified for they add an error to the conversions. The decoupling capacitors on the LDOs can also be checked. The ADC indicates if the capacitor is not present.

As part of the conversion process, the analog input overvoltage/undervoltage monitors are useful for detecting any excessive voltages on AINP and AINM. The power supply voltages and reference voltages are selectable as inputs to the ADC. Thus, the user can periodically check these voltages to confirm whether they are within the system specification. Also, the user can check that the LDO voltages are within specification. The conversion process and calibration process can also be checked. This ensures that any invalid conversions or calibrations are flagged to the user.

Finally, the CRC check, SCLK counter, and the SPI read/write checks make the interface more robust as any read/write operation that is not valid is detected. The CRC check highlights if any bits are corrupted when being transmitted between the processor and the ADC.

TEMPERATURE MEASUREMENT USING AN RTD

To optimize a 3-wire RTD configuration, two identically matched current sources are required. The AD7124-8, which contains two well matched current sources, is ideally suited to these applications. One possible 3-wire configuration is shown in Figure 127. In this 3-wire configuration, the lead resistances result in errors if only one current (output at AIN0) is used, as the excitation current flows through RL1, developing a voltage error between AIN1 and AIN2. In the scheme outlined, the second RTD current source (available at AIN3) compensates for the error introduced by the excitation current flowing through RL1. The second RTD current flows through RL2. Assuming that RL1 and RL2 are equal (the leads are normally of the same material and of equal length) and that the excitation currents match, the error voltage across RL2 equals the error voltage across RL1, and no error voltage is developed between AIN1 and AIN2. Twice the voltage is developed across RL3; however, because this is a common-mode voltage it does not introduce errors. The reference voltage for the AD7124-8 is also generated using one of the matched current sources. It is developed using a precision resistor and applied to the differential reference pins of the ADC. This scheme ensures that the analog input voltage span remains ratiometric to the reference voltage. Any errors in the analog input voltage due to the temperature drift of the excitation current are compensated by the variation of the reference voltage.

As an example, the PT100 measures temperature from −200°C to +600°C. The resistance is 100 Ω typically at 0°C and 313.71 Ω at 600°C. If the 500 μA excitation currents are used, the maximum voltage generated across the RTD when using the full temperature range of the RTD is

$$500\ \mu A \times 313.71\ \Omega = 156.86\ mV$$

This is amplified to 2.51 V within the AD7124-8 if the gain is programmed to 16.

The voltage generated across the reference resistor must be at least 2.51 V. Therefore, the reference resistor value must equal at least

$$2.51\ V/500\ \mu A = 5020\ \Omega$$

Therefore, a 5.11 kΩ resistor can be used.

$$5.11\ k\Omega \times \textit{Excitation Current} = 5.11\ k\Omega \times 500\ \mu A = 2.555\ V$$

One other consideration is the output compliance. The output compliance equals AV_{DD} − 0.37 V. If a 3.3 V analog supply is used, the voltage at AIN0 must be less than (3.3 V − 0.37 V) = 2.93 V. From the previous calculations, this specification is met because the maximum voltage at AIN0 equals the voltage across the reference resistor plus the voltage across the RTD, which equals

$$2.555\ V + 156.86\ mV = 2.712\ V$$

A typical procedure for reading the RTD is as follows:

1. Reset the ADC.
2. Select the power mode.
3. Set the CHANNEL_0 register analog input to AIN1/AIN2. Assign Setup 0 to this channel. Configure Setup 0 to have a gain of 16 and select the reference source REFIN2(±). Select the filter type and set the output data rate.
4. Program the excitation currents to 500 µA and output the currents on the AIN0 and AIN3 pins.
5. Wait until $\overline{\text{RDY}}$ goes low. Read the conversion value.
6. Repeat Step 4.

In the processor, implement the linearization routine for the PT100.

The external antialias filter is omitted for clarity. However, such a filter is required to reject any interference at the modulator frequency and multiples of the modulator frequency. Also, some filtering may be needed for EMI purposes. Both the analog inputs and reference inputs can be buffered, which allows the user to connect any RC combination to the reference or analog input pins.

On the AD7124-8, the excitation currents can be made available at the input pins, for example, the AIN3 pin can function as an analog input as well as outputting the current source. This option allows multiple sensors to be connected to the ADC using a minimum pin count. However, the resistor of the antialiasing filter is in series with the RTD. This introduces an error in the conversions as there is a voltage generated across the antialiasing resistor. To minimize the error, minimize the resistance of the antialiasing filter.

The power mode to use depends on the performance required from the system along with the current consumption allowance for the system. In a field transmitter, low current consumption is essential. In this application, the low power mode or mid power mode is most suitable. In process control applications, power consumption is not a priority. Thus, full power mode may be selected. The full power mode offers higher throughput and lower noise.

The AD7124-8 on-chip diagnostics allow the user to check the circuit connections, monitor the power supply, reference, and LDO voltages, check all conversions and calibrations for any errors, as well as monitor any read/write operations. In RTD applications, the circuit connections are verified using the reference detect and the burnout currents. The REF_DET_ERR flag is set if the external reference REFIN2(±) is missing. The burnout currents (available in the configuration registers) detect an open wire. The decoupling capacitors on the LDOs can also be checked. The ADC indicates if the capacitor is not present.

As part of the conversion process, the analog input overvoltage/undervoltage monitors are useful to detect any excessive voltages on AINP and AINM. The power supply voltages and reference voltages are selectable as inputs to the ADC. Thus, the user can periodically check these voltages to confirm whether they are within the system specification. Also, the user can check that the LDO voltages are within specification. The conversion process and calibration process can also be checked. This ensures that any invalid conversions or calibrations are flagged to the user.

Finally, the CRC check, SCLK counter, and the SPI read/write checks make the interface more robust as any read/write operation that is not valid is detected. The CRC check highlights if any bits are corrupted when being transmitted between the processor and the ADC.

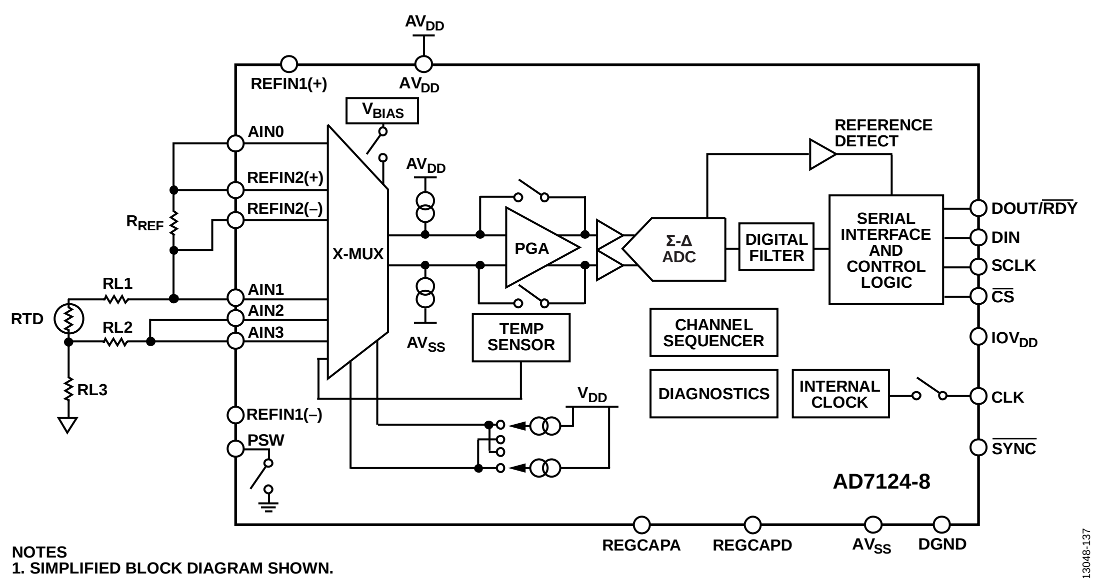


Figure 127. 3-Wire RTD Application

FLOWMETER

Figure 128 shows the AD7124-8 being used in a flowmeter application that consists of two pressure transducers, with the rate of flow being equal to the pressure difference. The pressure transducers are arranged in a bridge network and give a differential output voltage between its OUT+ and OUT− terminals. With rated full-scale pressure (in this case, 300 mmHg) on the transducer, the differential output voltage is 3 mV/V of the input voltage (that is, the voltage between the IN+ and IN− terminals).

Assuming a 3 V excitation voltage, the full-scale output range from the transducer is 9 mV. The excitation voltage for the bridge can directly provide the reference for the ADC, as the reference input range includes the supply voltage.

A second advantage of using the AD7124-8 in transducer-based applications is that the low-side power switch can be fully utilized in low power applications. The low-side power switch is connected in series with the cold side of the bridges. In normal operation, the switch is closed and measurements are taken. In applications where power is of concern, the AD7124-8 can be placed in standby mode, thus significantly reducing the power consumed in the application. In addition, the low-side power switch can be opened while in standby mode, thus avoiding unnecessary power consumption by the front-end transducers. When the device is taken out of standby mode, and the low-side power switch is closed, the user must ensure that the front-end circuitry is fully settled before attempting a read from the AD7124-8. The power switch can be closed prior to taking the device out of standby, if needed. This allows time for the sensor to power up and settle before the ADC powers up and begins sampling the analog input.

In the diagram, temperature compensation is performed using a thermistor. The on-chip excitation current supplies the thermistor. In addition, the reference voltage for the temperature measurement is derived from a precision resistor in series with the thermistor. This allows a ratiometric measurement so that variation of the excitation current has no effect on the measurement (it is the ratio of the precision reference resistance to the thermistor resistance that is measured).

If the sensor sensitivity is 3 mV/V and the excitation voltage is 3 V, the maximum output from the sensor is 9 mV. The AD7124-8 PGA can be set to 128 to amplify the sensor signal.

The AD7124-8 PGA amplifies the signal to

$$9 \text{ mV} \times 128 = 1.152 \text{ V}$$

This value does not exceed the reference voltage (3 V).

A typical procedure for reading the sensors is as follows:

1. Reset the ADC.
2. Select the power mode.
3. Set the CHANNEL_0 register analog input to AIN0/AIN1. Assign Setup 0 to this channel. Configure Setup 0 to have a gain of 128 and select the reference source to REFIN1(±). Select the filter type and set the output data rate.
4. Set the CHANNEL_1 register analog input to AIN2/AIN3. Assign Setup 0 to this channel (both channels use the same setup).
5. Set the CHANNEL_2 register analog input to AIN4/AIN5. Assign Setup 1 to this channel. Configure Setup 1 to have a gain of 1 and select the reference source REFIN2(±). Select the filter type and set the output data rate.
6. Program the excitation current and output the current on the AIN4 pin.
7. Enable both CHANNEL_0 and CHANNEL_1. Enable the DATA_STATUS bit to identify the channel from which the conversion originated. The ADC automatically sequences through these channels.
8. Wait until $\overline{\text{RDY}}$ goes low. Read the conversion value.
9. Repeat Step 8 until the temperature is to be read (every 10 conversions of the pressure sensor readings, for example).
10. Disable CHANNEL_0 and CHANNEL_1. Enable CHANNEL_2.
11. Wait until $\overline{\text{RDY}}$ goes low. Read the conversion.
12. Repeat Step 6 to Step 10.

In the processor, the conversion information is converted to pressure and the flow rate can be calculated. The processor typically contains a lookup table for each pressure sensor so its variation with temperature can be compensated.

The external antialias filter is omitted for clarity. However, such a filter is required to reject any interference at the modulator frequency and multiples of the modulator frequency. Also, some filtering may be needed for EMI purposes. Both the analog inputs and reference inputs can be buffered, which allows the user to connect any RC combination to the reference or analog input pins.

The power mode to use depends on the performance required from the system along with the current consumption allowance for the system. In a field transmitter, low current consumption is essential. In this application, low power mode or mid power mode is most suitable. In process control applications, power consumption is not a priority. Thus, full power mode may be selected. Full power mode offers higher throughput and lower noise.

The AD7124-8 on-chip diagnostics allow the user to check the circuit connections, monitor power supply, reference, and LDO voltages, check all conversions and calibrations for any errors, as well as monitor any read/write operations. The REF_DET_ERR flag is set if the external reference REFIN2(±) or REFIN1(±) is missing. The decoupling capacitors on the LDOs can also be checked. The ADC indicates if the capacitor is not present.

As part of the conversion process, the analog input overvoltage/undervoltage monitors are useful to detect any excessive voltages on AINP and AINM. The power supply voltages and reference voltages are selectable as inputs to the ADC. Thus, the user can periodically check these voltages to confirm whether they are within the system specification. In addition, the user can check that the LDO voltages are within specification. The conversion process and calibration process can also be checked. This ensures that any invalid conversions or calibrations are flagged to the user.

Finally, the CRC check, SCLK counter, and the SPI read/write checks make the interface more robust as any read/write operation that is not valid is detected. The CRC check highlights if any bits are corrupted when being transmitted between the processor and the ADC.

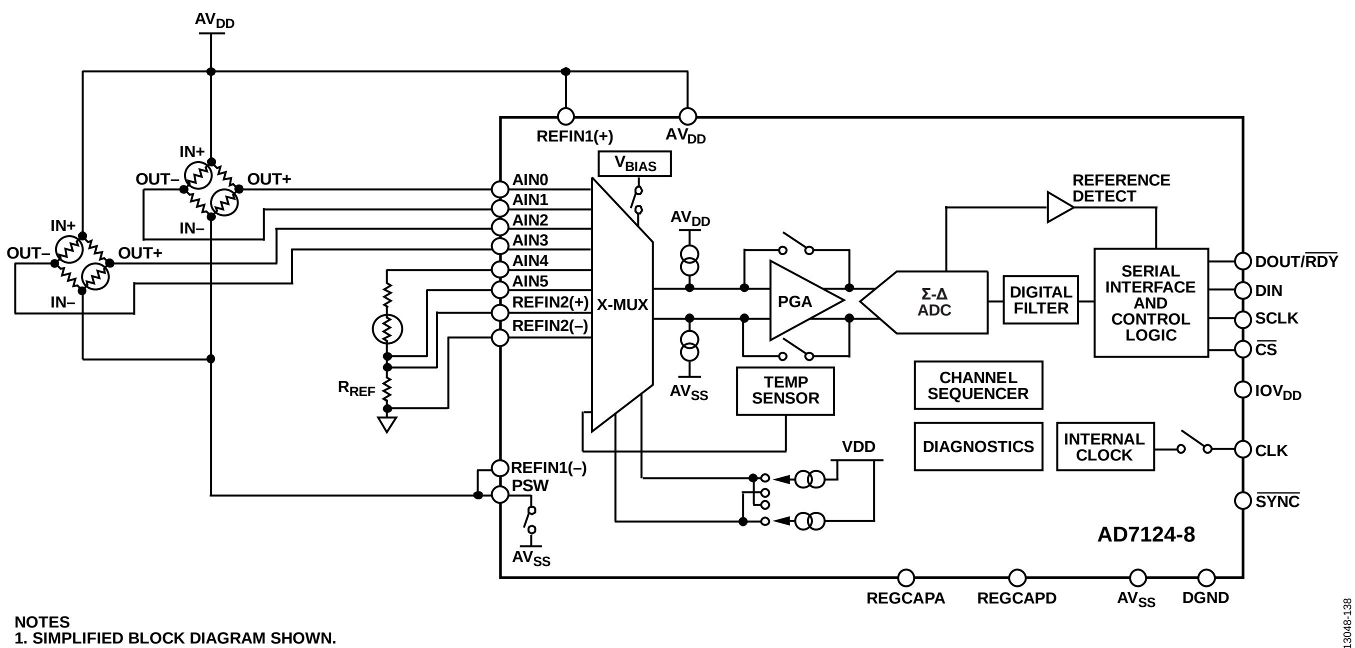


Figure 128. Flowmeter Application

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers that are described in the following sections. In the following descriptions, set implies a Logic 1 state and cleared implies a Logic 0 state, unless otherwise noted.

Table 63. Register Summary

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	WEN	R/W	RS[5:0]						0x00	W
0x00	Status	RDY	ERROR_FLAG	0	POR_FLAG	CH_ACTIVE				0x00	R
0x01	ADC_ CONTROL	0			DOUT_RDY_ DEL	CONT_READ	DATA_STATUS	CS_EN	REF_EN	0x0000	RW
		POWER_MODE		Mode				CLK_SEL			
0x02	Data	Data [23:16]								0x000000	R
		Data [15:8]									
		Data [7:0]									
0x03	IO_ CONTROL_1	GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1	0x000000	RW
		PDSW	0	IOUT1			IOUT0				
		IOUT1_CH				IOUT0_CH					
0x04	IO_ CONTROL_2	VBIAS15	VBIAS14	VBIAS13	VBIAS12	VBIAS11	VBIAS10	VBIAS9	VBIAS8	0x0000	RW
		VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0		
0x05	ID	DEVICE_ID				SILICON_REVISION				0x12	R
0x06	Error	0				LDO_CAP_ERR	ADC_CAL_ERR	ADC_CONV_ ERR	ADC_SAT_ERR	0x000000	R
		AINP_OV_ERR	AINP_UV_ERR	AINM_OV_ERR	AINM_UV_ ERR	REF_DET_ERR	0	DLDO_PSM_ ERR	0		
		ALDO_PSM_ ERR	SPI_IGNORE_ ERR	SPI_SCLK_CNT_ ERR	SPI_READ_ ERR	SPI_WRITE_ ERR	SPI_CRC_ERR	MM_CRC_ERR	0		
0x07	ERROR_EN	0	MCLK_CNT_EN	LDO_CAP_CHK_ TEST_EN	LDO_CAP_CHK		ADC_CAL_ERR_ EN	ADC_CONV_ ERR_EN	ADC_SAT_ ERR_EN	0x000040	RW
		AINP_OV_ERR_ EN	AINP_UV_ERR_ EN	AINM_OV_ERR_ EN	AINM_UV_ ERR_EN	REF_DET_ERR_ EN	DLDO_PSM_ TRIP_TEST_EN	DLDO_PSM_ ERR_EN	ALDO_PSM_ TRIP_TEST_EN		
		ALDO_PSM_ ERR_EN	SPI_IGNORE_ ERR_EN	SPI_SCLK_CNT_ ERR_EN	SPI_READ_ ERR_EN	SPI_WRITE_ ERR_EN	SPI_CRC_ERR_EN	MM_CRC_ERR_ EN	0		
0x08	MCLK_ COUNT	MCLK_COUNT								0x00	R
0x09 to 0x18	CHANNEL_0 to CHANNEL_15	Enable	Setup			0		AINP[4:3]		0x8001[1]	RW
		AINP[2:0]			AINM[4:0]						
0x19 to 0x20	CONFIG_0 to CONFIG_7	0				Bipolar	Burnout		REF_BUFP	0x0860	RW
		REF_BUFM	AIN_BUFP	AIN_BUFM	REF_SEL		PGA				
0x21 to 0x28	FILTER_0 to FILTER_7	Filter			REJ60	POST_FILTER			SINGLE_CYCLE	0x060180	RW
		0					FS[10:8]				
		FS[7:0]									
0x29 to 0x30	OFFSET_0 to OFFSET_7	Offset [23:16]								0x800000	RW
		Offset [15:8]									
		Offset [7:0]									
0x31 to 0x38	GAIN_0 to GAIN_7	Gain [23:16]								0x5XXXXX	RW
		Gain [15:8]									
		Gain [7:0]									

[1] CHANNEL_0 is reset to 0x8001. All other channels are reset to 0x0000.

COMMUNICATIONS REGISTER

RS[5:0] = 0, 0, 0, 0, 0, 0

The communications register is an 8-bit, write only register. All communications to the device must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place, the RS[5:0] bits selecting the register to be accessed.

For read or write operations, after the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register.

In situations where the interface sequence is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire device. Table 64 outlines the bit designations for the communications register. Bit 7 denotes the first bit of the data stream.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{WEN}}$ (0)	R/$\overline{\text{W}}$ (0)	RS[5:0] (0)					

Table 64. Communications Register Bit Descriptions

Bits	Bit Name	Description
7	$\overline{\text{WEN}}$	Write enable bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the device does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. As soon as a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits are loaded to the communications register.
6	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
5:0	RS[5:0]	Register address bits. These address bits select which registers of the ADC are being selected during this serial interface communication. See Table 63.

STATUS REGISTER

RS[5:0] = 0, 0, 0, 0, 0, 0

Power-On/Reset = 0x00

The status register is an 8-bit, read only register. To access the ADC status register, the user must write to the communications register, select the next operation to be read, and set the register address bits RS[5:0] to 0.

Table 65 outlines the bit designations for the status register. Bit 7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{RDY}}$ (0)	ERROR_FLAG (0)	0 (0)	POR_FLAG (0)	CH_ACTIVE (0)			

Table 65. Status Register Bit Descriptions

Bits	Bit Name	Description
7	$\overline{\text{RDY}}$	Ready bit for the ADC. This bit is cleared when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register is read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also set when the device is placed in power-down or standby mode. The end of a conversion is also indicated by the DOUT/$\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
6	ERROR_FLAG	ADC error bit. This bit indicates if one of the error bits has been asserted in the error register. This bit is high if one or more of the error bits in the error register has been set. This bit is cleared by a read of the error register.
5	0	This bit is set to 0.
4	POR_FLAG	Power-on reset flag. This bit indicates when a power-on reset occurs. A power-on reset occurs on power-up, when the power supply voltage goes below a threshold voltage, when a reset is performed, and when coming out of power-down mode. The status register must be read to clear the bit.

Bits	Bit Name	Description
3:0	CH_ACTIVE	These bits indicate which channel is being converted by the ADC. 0000 = Channel 0. 0001 = Channel 1. 0010 = Channel 2. 0011 = Channel 3. 0100 = Channel 4. 0101 = Channel 5. 0110 = Channel 6. 0111 = Channel 7. 1000 = Channel 8. 1001 = Channel 9. 1010 = Channel 10. 1011 = Channel 11. 1100 = Channel 12. 1101 = Channel 13. 1110 = Channel 14. 1111 = Channel 15.

ADC_CONTROL REGISTER

RS[5:0] = 0, 0, 0, 0, 0, 1

Power-On/Reset = 0x0000

Table 66 outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (0)	0 (0)	0 (0)	DOUT_RDY_DEL (0)	CONT_READ (0)	DATA_STATUS (0)	CS_EN (0)	REF_EN (0)
POWER_MODE (0)		Mode (0)				CLK_SEL (0)	

Table 66. ADC Control Register Bit Descriptions

Bits	Bit Name	Description
15:13	0	These bits must be programmed with a Logic 0 for correct operation.
12	DOUT_RDY_DEL	Controls the SCLK inactive edge to DOUT/RDY high time. When DOUT_RDY_DEL is cleared, the delay is 10 ns minimum. When DOUT_RDY_DEL is set, the delay is increased to 100 ns minimum. This function is useful when CS is tied low (the CS_EN bit is set to 0).
11	CONT_READ	Continuous read of the data register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read; that is, the contents of the data register are automatically placed on the DOUT pin when the SCLK pulses are applied after the RDY pin goes low to indicate that a conversion is complete. The communications register does not have to be written to for subsequent data reads. To enable continuous read, the CONT_READ bit is set. To disable continuous read, write a read data command while the DOUT/ RDY pin is low. While continuous read is enabled, the ADC monitors activity on the DIN line so that it can receive the instruction to disable continuous read. Additionally, a reset occurs if 64 consecutive 1s occur on DIN; therefore, hold DIN low until an instruction is written to the device.
10	DATA_STATUS	This bit enables the transmission of the status register contents after each data register read. When DATA_STATUS is set, the contents of the status register are transmitted along with each data register read. This function is useful when several channels are selected because the status register identifies the channel to which the data register value corresponds.
9	CS_EN	This bit controls when the DOUT/RDY pin transitions from being a DOUT pin to a RDY pin during data read operations. When CS_EN is cleared, the DOUT pin returns to being a RDY pin within nanoseconds of the SCLK inactive edge (the delay is determined by the DOUT_RDY_DEL bit). When set, the DOUT/ RDY pin continues to operate as a DOUT pin after the SCLK inactive edge. The pin changes function to a RDY pin when CS is taken high. CS_EN must be set to use the diagnostic functions SPI_WRITE_ERR, SPI_READ_ERR, and SPI_SCLK_CNT_ERR.

Bits	Bit Name	Description
8	REF_EN	Internal reference voltage enable. When this bit is set, the internal reference is enabled and available at the REFOUT pin. When this bit is cleared, the internal reference is disabled.
7:6	POWER_MODE	Power Mode Select. These bits select the power mode. The current consumption and output data rate ranges are dependent on the power mode. 00 = low power. 01 = mid power. 10 = full power. 11 = full power.
5:2	Mode	These bits control the mode of operation for ADC. See Table 67.
1:0	CLK_SEL	These bits select the clock source for the ADC. Either the on-chip 614.4 kHz clock can be used or an external clock can be used. The ability to use an external clock allows several AD7124-8 devices to be synchronized. Also, 50 Hz and 60 Hz rejection is improved when an accurate external clock drives the ADC. 00 = internal 614.4 kHz clock. The internal clock is not available at the CLK pin. 01 = internal 614.4 kHz clock. This clock is available at the CLK pin. 10 = external 614.4 kHz clock. 11 = external clock. The external clock is divided by 4 within the AD7124-8.

Table 67. Operating Modes

Mode Value	Description
0000	Continuous conversion mode (default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. $\overline{\text{RDY}}$ goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, a reset, or a reconfiguration of the ADC, the complete settling time of the filter is required to generate the first valid conversion. Subsequent conversions are available at the selected output data rate, which is dependent on filter choice.
0001	Single conversion mode. When single conversion mode is selected, the ADC powers up and performs a single conversion on the selected channel. The conversion requires the complete settling time of the filter. The conversion result is placed in the data register, $\overline{\text{RDY}}$ goes low, and the ADC returns to standby mode. The conversion remains in the data register and $\overline{\text{RDY}}$ remains active (low) until the data is read or another conversion is performed.
0010	Standby mode. In standby mode, all sections of the AD7124-8 can be powered down except the LDOs. The internal reference, on-chip oscillator, low-side power switch, and bias voltage generator can be enabled or disabled while in standby mode. The on-chip registers retain their contents in standby mode. Any enabled diagnostics remain active when the ADC is in idle mode. The diagnostics can be enabled/disabled while in standby mode. However, any diagnostics that require the master clock (reference detect, undervoltage/overvoltage detection, LDO trip tests, memory map CRC, and MCLK counter) must be enabled when the ADC is in continuous conversion mode or idle mode; these diagnostics do not function if enabled in standby mode.
0011	Power-down mode. In power-down mode, all the AD7124-8 circuitry is powered down, including the current sources, power switch, burnout currents, bias voltage generator, and clock circuitry. The LDOs are also powered down. In power-down mode, the on-chip registers do not retain their contents. Therefore, coming out of power-down mode, all registers must be reprogrammed.
0100	Idle mode. In idle mode, the ADC filter and modulator are held in a reset state even though the modulator clocks continue to be provided.
0101	Internal zero-scale (offset) calibration. An internal short is automatically connected to the input. $\overline{\text{RDY}}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. Select only one channel when zero-scale calibration is being performed. An internal zero-scale calibration takes a time of one settling period to be performed.
0110	Internal full-scale (gain) calibration. A full-scale input voltage is automatically connected to the selected analog input for this calibration. $\overline{\text{RDY}}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the gain register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error. Select only one channel when full-scale calibration is being performed. An internal full-scale calibration takes a time of one settling period to be performed when the gain is set to 1 and four settling periods for gains greater than one. Internal full-scale calibrations cannot be performed in the full power mode. So, if using the full-power mode, select mid or low power mode for the internal full-scale calibration. This calibration is valid in full power mode as the same reference and gain are used. When performing internal zero-scale and internal full-scale calibrations, the internal full-scale calibration must be performed before the internal zero-scale calibration. Therefore, write 0x800000 to the offset register before performing any internal full-scale calibration, which resets the offset register to its default value.

Mode Value	Description
0111	System zero-scale (offset) calibration. Connect the system zero-scale input to the channel input pins of the selected channel. $\overline{\text{RDY}}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. A system zero-scale calibration is required each time the gain of a channel is changed. Select only one channel when full-scale calibration is being performed. A system zero-scale calibration takes a time of one settling period to be performed.
1000	System full-scale (gain) calibration. Connect the system full-scale input to the channel input pins of the selected channel. $\overline{\text{RDY}}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the gain register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed. Select only one channel when full-scale calibration is being performed. A system full-scale calibration takes a time of one settling period to be performed.
1001 to1111	Reserved.

DATA REGISTER

RS[5:0] = 0, 0, 0, 0, 1, 0
Power-On/Reset = 0x000000

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the $\overline{\text{RDY}}$ bit/pin is set.

IO_CONTROL_1 REGISTER

RS[5:0] = 0, 0, 0, 0, 1, 1
Power-On/Reset = 0x000000

Table 68 outlines the bit designations for the register. Bit 23 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GPIO_DAT4 (0)	GPIO_DAT3 (0)	GPIO_DAT2 (0)	GPIO_DAT1 (0)	GPIO_CTRL4 (0)	GPIO_CTRL3 (0)	GPIO_CTRL2 (0)	GPIO_CTRL1 (0)
PDSW (0)	0 (0)	IOUT1 (0)			IOUT0 (0)		
IOUT1_CH (0)				IOUT0_CH (0)			

Table 68. IO_CONTROL_1 Register Bit Descriptions

Bits	Bit Name	Description
23	GPIO_DAT4	Digital Output P4. When GPIO_CTRL4 is set, the GPIO_DAT4 bit sets the value of the P4 general-purpose output pin. When GPIO_DAT4 is high, the P4 output pin is high. When GPIO_DAT4 is low, the P4 output pin is low. When the IO_CONTROL_1 register is read, the GPIO_DAT4 bit reflects the status of the P4 pin if GPIO_CTRL4 is set.
22	GPIO_DAT3	Digital Output P3. When GPIO_CTRL3 is set, the GPIO_DAT3 bit sets the value of the P3 general-purpose output pin. When GPIO_DAT3 is high, the P3 output pin is high. When GPIO_DAT3 is low, the P3 output pin is low. When the IO_CONTROL_1 register is read, the GPIO_DAT3 bit reflects the status of the P3 pin if GPIO_CTRL3 is set.
21	GPIO_DAT2	Digital Output P2. When GPIO_CTRL2 is set, the GPIO_DAT2 bit sets the value of the P2 general-purpose output pin. When GPIO_DAT2 is high, the P2 output pin is high. When GPIO_DAT2 is low, the P2 output pin is low. When the IO_CONTROL_1 register is read, the GPIO_DAT2 bit reflects the status of the P2 pin if GPIO_CTRL2 is set.
20	GPIO_DAT1	Digital Output P1. When GPIO_CTRL1 is set, the GPIO_DAT1 bit sets the value of the P1 general-purpose output pin. When GPIO_DAT1 is high, the P1 output pin is high. When GPIO_DAT1 is low, the P1 output pin is low. When the IO_CONTROL_1 register is read, the GPIO_DAT1 bit reflects the status of the P1 pin if GPIO_CTRL1 is set.
19	GPIO_CTRL4	Digital Output P4 enable. When GPIO_CTRL4 is set, the digital output P4 is active. When GPIO_CTRL4 is cleared, the pin functions as analog input pin AIN5.

Bits	Bit Name	Description
18	GPIO_CTRL3	Digital Output P3 enable. When GPIO_CTRL3 is set, the digital output P3 is active. When GPIO_CTRL3 is cleared, the pin functions as analog input pin AIN4.
17	GPIO_CTRL2	Digital Output P2 enable. When GPIO_CTRL2 is set, the digital output P2 is active. When GPIO_CTRL2 is cleared, the pin functions as analog input pin AIN3.
16	GPIO_CTRL1	Digital Output P1 enable. When GPIO_CTRL1 is set, the digital output P1 is active. When GPIO_CTRL1 is cleared, the pin functions as analog input pin AIN2.
15	PDSW	Bridge power-down switch control bit. Set this bit to close the bridge power-down switch PDSW to AGND. The switch can sink up to 30 mA. Clear this bit to open the bridge power-down switch. When the ADC is placed in standby mode, the bridge power-down switch remains active.
14	0	This bit must be programmed with a Logic 0 for correct operation.
13:11	IOUT1	These bits set the value of the excitation current for IOUT1. 000 = off. 001 = 50 μA. 010 = 100 μA 011 = 250 μA. 100 = 500 μA. 101 = 750 μA. 110 = 1000 μA 111 = 1000 μA.
10:8	IOUT0	These bits set the value of the excitation current for IOUT0. 000 = off. 001 = 50 μA. 010 = 100 μA 011 = 250 μA. 100 = 500 μA. 101 = 750 μA. 110 = 1000 μA 111 = 1000 μA.
7:4	IOUT1_CH	Channel select bits for the excitation current for IOUT1. 0000 = IOUT1 is available on the AIN0 pin. 0001 = IOUT1 is available on the AIN1 pin. 0010 = IOUT1 is available on the AIN2 pin. 0011 = IOUT1 is available on the AIN3 pin. 0100 = IOUT1 is available on the AIN4 pin. 0101 = IOUT1 is available on the AIN5 pin. 0110 = IOUT1 is available on the AIN6 pin. 0111 = IOUT1 is available on the AIN7 pin. 1000 = IOUT1 is available on the AIN8 pin. 1001 = IOUT1 is available on the AIN9 pin. 1010 = IOUT1 is available on the AIN10 pin. 1011 = IOUT1 is available on the AIN11 pin. 1100 = IOUT1 is available on the AIN12 pin. 1101 = IOUT1 is available on the AIN13 pin. 1110 = IOUT1 is available on the AIN14 pin. 0111 = IOUT1 is available on the AIN15 pin.

Bits	Bit Name	Description
3:0	IOUT0_CH	Channel select bits for the excitation current for IOUT0. 0000 = IOUT0 is available on the AIN0 pin. 0001 = IOUT0 is available on the AIN1 pin. 0010 = IOUT0 is available on the AIN2 pin. 0011 = IOUT0 is available on the AIN3 pin. 0100 = IOUT0 is available on the AIN4 pin. 0101 = IOUT0 is available on the AIN5 pin. 0110 = IOUT0 is available on the AIN6 pin. 0111 = IOUT0 is available on the AIN7 pin. 1000 = IOUT0 is available on the AIN8 pin. 1001 = IOUT0 is available on the AIN9 pin. 1010 = IOUT0 is available on the AIN10 pin. 1011 = IOUT0 is available on the AIN11 pin. 1100 = IOUT0 is available on the AIN12 pin. 1101 = IOUT0 is available on the AIN13 pin. 1110 = IOUT0 is available on the AIN14 pin. 1111 = IOUT0 is available on the AIN15 pin.

IO_CONTROL_2 REGISTER

RS[5:0] = 0, 0, 0, 1, 0, 0
Power-On/Reset = 0x0000

Table 69 outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. The internal bias voltage can be enabled on multiple channels.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VBIAS15 (0)	VBIAS14 (0)	VBIAS13 (0)	VBIAS12 (0)	VBIAS11 (0)	VBIAS10 (0)	VBIAS9 (0)	VBIAS8 (0)
VBIAS7 (0)	VBIAS6 (0)	VBIAS5 (0)	VBIAS4 (0)	VBIAS3 (0)	VBIAS2 (0)	VBIAS1 (0)	VBIAS0 (0)

Table 69. IO_CONTROL_2 Register Bit Descriptions

Bits	Bit Name	Description
15	VBIAS15	Enable the bias voltage on the AIN15 channel. When set, the internal bias voltage is available on AIN15.
14	VBIAS14	Enable the bias voltage on the AIN14 channel. When set, the internal bias voltage is available on AIN14.
13	VBIAS13	Enable the bias voltage on the AIN13 channel. When set, the internal bias voltage is available on AIN13.
12	VBIAS12	Enable the bias voltage on the AIN12 channel. When set, the internal bias voltage is available on AIN12.
11	VBIAS11	Enable the bias voltage on the AIN11 channel. When set, the internal bias voltage is available on AIN11.
10	VBIAS10	Enable the bias voltage on the AIN10 channel. When set, the internal bias voltage is available on AIN10.
9	VBIAS9	Enable the bias voltage on the AIN9 channel. When set, the internal bias voltage is available on AIN9.
8	VBIAS8	Enable the bias voltage on the AIN8 channel. When set, the internal bias voltage is available on AIN8.
7	VBIAS7	Enable the bias voltage on the AIN7 channel. When set, the internal bias voltage is available on AIN7.
6	VBIAS6	Enable the bias voltage on the AIN6 channel. When set, the internal bias voltage is available on AIN6.
5	VBIAS5	Enable the bias voltage on the AIN5 channel. When set, the internal bias voltage is available on AIN5.
4	VBIAS4	Enable the bias voltage on the AIN4 channel. When set, the internal bias voltage is available on AIN4.
3	VBIAS3	Enable the bias voltage on the AIN3 channel. When set, the internal bias voltage is available on AIN3.
2	VBIAS2	Enable the bias voltage on the AIN2 channel. When set, the internal bias voltage is available on AIN2.
1	VBIAS1	Enable the bias voltage on the AIN1 channel. When set, the internal bias voltage is available on AIN1.
0	VBIAS0	Enable the bias voltage on the AIN0 channel. When set, the internal bias voltage is available on AIN0.

ID REGISTER

RS[5:0] = 0, 0, 0, 1, 0, 1
Power-On/Reset = 0x12

The identification number for the AD7124-8 is stored in the ID register. This is a read only register.

ERROR REGISTER

RS[5:0] = 0, 0, 0, 1, 1, 0
Power-On/Reset = 0x000000

Diagnostics, such as checking overvoltages and checking the SPI interface, are included on the AD7124-8. The error register contains the flags for the different diagnostic functions. The functions are enabled and disabled using the ERROR_EN register.

Table 70 outlines the bit designations for the register. Bit 23 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (0)				LDO_CAP_ERR (0)	ADC_CAL_ERR (0)	ADC_CONV_ERR (0)	ADC_SAT_ERR (0)
AINP_OV_ERR (0)	AINP_UV_ERR (0)	AINM_OV_ERR (0)	AINM_UV_ERR (0)	REF_DET_ERR (0)	0 (0)	DLDO_PSM_ERR (0)	0 (0)
ALDO_PSM_ERR (0)	SPI_IGNORE_ERR (0)	SPI_SCLK_CNT_ERR (0)	SPI_READ_ERR (0)	SPI_WRITE_ERR (0)	SPI_CRC_ERR (0)	MM_CRC_ERR (0)	0 (0)

Table 70. Error Register Bit Descriptions

Bits	Bit Name	Description
23:20	0	These bits must be programmed with a Logic 0 for correct operation.
19	LDO_CAP_ERR	Analog/digital LDO decoupling capacitor check. This flag is set if the decoupling capacitors required for the analog and digital LDOs are not connected to the AD7124-8.
18	ADC_CAL_ERR	Calibration check. If a calibration is initiated but not completed, this flag is set to indicate that an error occurred during the calibration. The associated calibration register is not updated.
17	ADC_CONV_ERR	This bit indicates whether a conversion is valid. This flag is set if an error occurs during a conversion.
16	ADC_SAT_ERR	ADC saturation flag. This flag is set if the modulator is saturated during a conversion.
15	AINP_OV_ERR	Overvoltage detection on AINP.
14	AINP_UV_ERR	Undervoltage detection on AINP.
13	AINM_OV_ERR	Overvoltage detection on AINM.
12	AINM_UV_ERR	Undervoltage detection on AINM.
11	REF_DET_ERR	Reference detection. This flag indicates when the external reference being used by the ADC is open circuit or less than 0.7 V.
10	0	This bit must be programmed with a Logic 0 for correct operation.
9	DLDO_PSM_ERR	Digital LDO error. This flag is set if an error is detected with the digital LDO.
8	0	This bit must be programmed with a Logic 0 for correct operation.
7	ALDO_PSM_ERR	Analog LDO error. This flag is set if an error is detected with the analog LDO voltage.
6	SPI_IGNORE_ERR	When a CRC check of the internal registers is being performed, the on-chip registers cannot be accessed. User instructions are ignored by the ADC. This bit is set when the CRC check of the registers is occurring. The bit is cleared when the check is complete; read and write operations can only be performed then.
5	SPI_SCLK_CNT_ERR	All serial communications are some multiple of eight bits. This bit is set when the number of SCLK cycles is not a multiple of eight.
4	SPI_READ_ERR	This bit is set when an error occurs during an SPI read operation.
3	SPI_WRITE_ERR	This bit is set when an error occurs during an SPI write operation.
2	SPI_CRC_ERR	This bit is set if an error occurs in the CRC check of the serial communications.
1	MM_CRC_ERR	Memory map error. A CRC calculation is performed on the memory map each time that the registers are written to. Following this, periodic CRC checks are performed on the on-chip registers. If the register contents have changed, the MM_CRC bit is set.
0	0	This bit must be programmed with a Logic 0 for correct operation.

ERROR_EN REGISTER

RS[5:0] = 0, 0, 0, 1, 1, 1
Power-On/Reset = 0x000040

All the diagnostic functions can be enabled or disabled by setting the appropriate bits in this register.

Table 71 outlines the bit designations for the register. Bit 23 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (0)	MCLK_CNT_EN (0)	LDO_CAP_CHK_TEST_EN (0)	LDO_CAP_CHK (0)		ADC_CAL_ERR_EN (0)	ADC_CONV_ERR_EN (0)	ADC_SAT_ERR_EN (0)
AINP_OV_ERR_EN (0)	AINP_UV_ERR_EN (0)	AINM_OV_ERR_EN (0)	AINM_UV_ERR_EN (0)	REF_DET_ERR_EN (0)	DLDO_PSM_TRIP_TEST_EN (0)	DLDO_PSM_ERR_EN (0)	ALDO_PSM_TRIP_TEST_EN (0)
ALDO_PSM_ERR_EN (0)	SPI_IGNORE_ERR_EN (0)	SPI_SCLK_CNT_ERR_EN (0)	SPI_READ_ERR_EN (0)	SPI_WRITE_ERR_EN (0)	SPI_CRC_ERR_EN (0)	MM_CRC_ERR_EN (0)	0 (0)

Table 71. ERROR_EN Register Bit Descriptions

Bits	Bit Name	Description
23	0	This bit must be programmed with a Logic 0 for correct operation.
22	MCLK_CNT_EN	Master clock counter. When this bit is set, the master clock counter is enabled and the result is reported via the MCLK_COUNT register. The counter monitors the master clock being used by the ADC. If an external clock is the clock source, the MCLK counter monitors this external clock. Similarly, if the on-chip oscillator is selected as the clock source to the ADC, the MCLK counter monitors the on-chip oscillator.
21	LDO_CAP_CHK_TEST_EN	Test of analog/digital LDO decoupling capacitor check. When this bit is set, the decoupling capacitor is internally disconnected from the LDO, forcing a fault condition. This allows the user to test the circuitry that is used for the analog and digital LDO decoupling capacitor check.
20:19	LDO_CAP_CHK	Analog/digital LDO decoupling capacitor check. These bits enable the capacitor check. When a check is enabled, the ADC checks for the presence of the external decoupling capacitor on the selected supply. When the check is complete, the LDO_CAP_CHK bits are both reset to 0. 00 = check is not enabled. 01 = check the analog LDO capacitor. 10 = check the digital LDO capacitor. 11 = check is not enabled.
18	ADC_CAL_ERR_EN	When this bit is set, the calibration fail check is enabled.
17	ADC_CONV_ERR_EN	When this bit is set, the conversions are monitored and the ADC_CONV_ERR bit is set when a conversion fails.
16	ADC_SAT_ERR_EN	When this bit is set, the ADC modulator saturation check is enabled.
15	AINP_OV_ERR_EN	When this bit is set, the overvoltage monitor on all enabled AINP channels is enabled.
14	AINP_UV_ERR_EN	When this bit is set, the undervoltage monitor on all enabled AINP channels is enabled.
13	AINM_OV_ERR_EN	When this bit is set, the overvoltage monitor on all enabled AINM channels is enabled.
12	AINM_UV_ERR_EN	When this bit is set, the undervoltage monitor on all enabled AINM channels is enabled.
11	REF_DET_ERR_EN	When this bit is set, any external reference being used by the ADC is continuously monitored. An error is flagged if the external reference is open circuit or has a value of less than 0.7 V.
10	DLDO_PSM_TRIP_TEST_EN	Checks the test mechanism that monitors the digital LDO. When this bit is set, the input to the test circuit is tied to DGND instead of the LDO output. Set the DLDO_PSM_ERR bit in the error register.
9	DLDO_PSM_ERR_ERR	When this bit is set, the digital LDO voltage is continuously monitored. The DLDO_PSM_ERR bit in the error register is set if the voltage being output from the digital LDO is outside specification.
8	ALDO_PSM_TRIP_TEST_EN	Checks the test mechanism that monitors the analog LDO. When this bit is set, the input to the test circuit is tied to AV_{SS} instead of the LDO output. Set the ALDO_PSM_ERR bit in the error register.
7	ALDO_PSM_ERR_EN	When this bit is set, the analog LDO voltage is continuously monitored. The ALDO_PSM_ERR bit in the error register is set if the voltage being output from the analog LDO is outside specification.
6	SPI_IGNORE_ERR_EN	When a CRC check of the internal registers is being performed, the on-chip registers cannot be accessed. User instructions are ignored by the ADC. Set this bit so that the SPI_IGNORE_ERR bit in the error register informs the user when read and write operations must not be performed.

Bits	Bit Name	Description
5	SPI_SCLK_CNT_ERR_EN	When this bit is set, the SCLK counter is enabled. All read and write operations to the ADC are multiples of eight bits. For every serial communication, the SCLK counter counts the number of SCLK pulses. $\overline{CS}$ must be used to frame each read and write operation. If the number of SCLK pulses used during a communication is not a multiple of eight, the SPI_SCLK_CNT_ERR bit in the error register is set. For example, a glitch on the SCLK pin during a read or write operation can be interpreted as an SCLK pulse. In this case, the SPI_SCLK_CNT_ERR bit is set as there is an excessive number of SCLK pulses detected. $\overline{CS}$_EN in the ADC_CONTROL register must be set to 1 when the SCLK counter function is being used.
4	SPI_READ_ERR_EN	When this bit is set, the SPI_READ_ERR bit in the error register is set when an error occurs during a read operation. An error occurs if the user attempts to read from invalid addresses. $\overline{CS}$_EN in the ADC_CONTROL register must be set to 1 when the SPI read check function is being used.
3	SPI_WRITE_ERR_EN	When this bit is set, the SPI_WRITE_ERR bit in the error register is set when an error occurs during a write operation. An error occurs if the user attempts to write to invalid addresses or write to read-only registers. $\overline{CS}$_EN in the ADC_CONTROL register must be set to 1 when the SPI write check function is being used.
2	SPI_CRC_ERR_EN	This bit enables a CRC check of all read and write operations. The SPI_CRC_ERR bit in the error register is set if the CRC check fails. In addition, an 8-bit CRC word is appended to all data read from the AD7124-8.
1	MM_CRC_ERR_EN	When this bit is set, a CRC calculation is performed on the memory map each time that the registers are written to. Following this, periodic CRC checks are performed on the on-chip registers. If the register contents have changed, the MM_CRC bit is set.
0	0	This bit must be programmed with a Logic 0 for correct operation.

MCLK_COUNT REGISTER

RS[5:0] = 0, 0, 1, 0, 0, 0

Power-On/Reset = 0x00

The master clock frequency can be monitored using this register.

Table 72 outlines the bit designations for the register. Bit 7 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCLK_COUNT (0)							

Table 72. MCLK_COUNT Register Bit Descriptions

Bits	Bit Name	Description
7:0	MCLK_COUNT	This register allows the user to determine the frequency of the internal/external oscillator. Internally, a clock counter increments every 131 pulses of the sampling clock (614.4 kHz in full power mode, 153.6 kHz in mid power mode, and 768 kHz in low power mode). The 8-bit counter wraps around on reaching its maximum value. The counter output is read back via this register.

CHANNEL REGISTERS

RS[5:0] = 0, 0, 1, 0, 0, 1 to 0, 1, 1, 0, 0, 0

Power-On/Reset = 0x8001 for CHANNEL_0; all other channel registers are set to 0x0001

Sixteen channel registers are included on the AD7124-8, CHANNEL_0 to CHANNEL_15. The channel registers begin at Address 0x09 (CHANNEL_0) and end at Address 0x18 (CHANNEL_15). Via each register, the user can configure the channel (AINP input and AINM input), enable or disable the channel, and select the setup. The setup is selectable from eight different options defined by the user. When the ADC converts, it automatically sequences through all enabled channels. This allows the user to sample some channels multiple times in a sequence, if required. In addition, it allows the user to include diagnostic functions in a sequence also.

Table 73 outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>Enable(1)</td><td colspan="3">Setup (0)</td><td>(0)</td><td>0 (0)</td><td colspan="2">AINP[4:3] (00)</td></tr>
<tr><td colspan="3">AINP[2:0] (000)</td><td colspan="5">AINM[4:0] (00001)</td></tr>
</table>

Table 73. Channel Register Bit Descriptions

Bits	Bit Name	Description
15	Enable	Channel enable bit. Setting this bit enables the device channel for the conversion sequence. By default, only the enable bit for Channel 0 is set. The order of conversions starts with the lowest enabled channel, then cycles through successively higher channel numbers, before wrapping around to the lowest channel again. When the ADC writes a result for a particular channel, the four LSBs of the status register are set to the channel number, 0 to 15. This allows the channel the data corresponds to be identified. When the DATA_STATUS bit in the ADC_CONTROL register is set, the contents of the status register are appended to each conversion when it is read. Use this function when several channels are enabled to determine to which channel the conversion value read corresponds.
14:12	Setup	Setup select. These bits identify which of the eight setups are used to configure the ADC for this channel. A setup comprises a set of four registers: analog configuration, output data rate/filter selection, offset register, and gain register. All channels can use the same setup, in which case the same 3-bit value must be written to these bits on all active channels. Alternatively, up to eight channels can be configured differently.
11:10	0	These bits must be programmed with a Logic 0 for correct operation.
9:5	AINP[4:0]	Positive analog input AINP input select. These bits select which of the analog inputs is connected to the positive input for this channel. 00000 = AIN0 (default). 00001 = AIN1. 00010 = AIN2. 00011 = AIN3. 00100 = AIN4. 000101 = AIN5. 00110 = AIN6. 00111 = AIN7. 01000 = AIN8. 01001 = AIN9. 01010 = AIN10. 01011 = AIN11. 01100 = AIN12. 01101 = AIN13. 01110 = AIN14. 01111 = AIN15. 10000 = temperature sensor. 10001 = AV_{SS}. 10010 = internal reference. 10011 = DGND. 10100 = $(AV_{DD} – AV_{SS})/6+$. Use in conjunction with $(AV_{DD} – AV_{SS})/6–$ to monitor supply $AV_{DD} – AV_{SS}$. 10101 = $(AV_{DD} – AV_{SS})/6–$. Use in conjunction with $(AV_{DD} – AV_{SS})/6+$ to monitor supply $AV_{DD} – AV_{SS}$. 10110 = $(IOV_{DD} – DGND)/6+$. Use in conjunction with $(IOV_{DD} – DGND)/6–$ to monitor IOV_{DD} – DGND. 10111 = $(IOV_{DD} – DGND)/6–$. Use in conjunction with $(IOV_{DD} – DGND)/6+$ to monitor IOV_{DD} – DGND.

Bits	Bit Name	Description
		11000 = (ALDO − AV_{SS})/6+. Use in conjunction with (ALDO − AV_{SS})/6− to monitor the analog LDO. 11001 = (ALDO − AV_{SS})/6−. Use in conjunction with (ALDO − AV_{SS})/6+ to monitor the analog LDO. 11010 = (DLDO − DGND)/6+. Use in conjunction with (DLDO − DGND)/6− to monitor the digital LDO. 11011 = (DLDO − DGND)/6−. Use in conjunction with (DLDO − DGND)/6+ to monitor the digital LDO. 11100 = V_20MV_P. Use in conjunction with V_20MV_M to apply a 20 mV p-p signal to the ADC. 11101 = V_20MV_M. Use in conjunction with V_20MV_P to apply a 20 mV p-p signal to the ADC. 10010 = REFOUT. 10011 = DGND.
4:0	AINM[4:0]	Negative analog input AINM input select. These bits select which of the analog inputs is connected to the negative input for this channel. 00000 = AIN0 (default). 00001 = AIN1. 00010 = AIN2. 00011 = AIN3. 00100 = AIN4. 000101 = AIN5. 00110 = AIN6. 00111 = AIN7. 01000 = AIN8. 01001 = AIN9. 01010 = AIN10. 01011 = AIN11. 01100 = AIN12. 01101 = AIN13. 01110 = AIN14. 01111 = AIN15. 10000 = temperature sensor. 10001 = AV_{SS}. 10010 = internal reference. 10011 = DGND. 10100 = (AV_{DD} − AV_{SS})/6+. Use in conjunction with (AV_{DD} − AV_{SS})/6− to monitor supply AV_{DD} − AV_{SS}. 10101 = (AV_{DD} − AV_{SS})/6−. Use in conjunction with (AV_{DD} − AV_{SS})/6+ to monitor supply AV_{DD} − AV_{SS}. 10110 = (IOV_{DD} − DGND)/6+. Use in conjunction with (IOV_{DD} − DGND)/6− to monitor IOV_{DD} − DGND. 10111 = (IOV_{DD} − DGND)/6−. Use in conjunction with (IOV_{DD} − DGND)/6+ to monitor IOV_{DD} − DGND. 11000 = (ALDO − AV_{SS})/6+. Use in conjunction with (ALDO − AV_{SS})/6− to monitor the analog LDO. 11001 = (ALDO − AV_{SS})/6−. Use in conjunction with (ALDO − AV_{SS})/6+ to monitor the analog LDO. 11010 = (DLDO − DGND)/6+. Use in conjunction with (DLDO − DGND)/6− to monitor the digital LDO. 11011 = (DLDO − DGND)/6−. Use in conjunction with (DLDO − DGND)/6+ to monitor the digital LDO. 11100 = V_20MV_P. Use in conjunction with V_20MV_M to apply a 20 mV p-p signal to the ADC. 11101 = V_20MV_M. Use in conjunction with V_20MV_P to apply a 20 mV p-p signal to the ADC. 11110 = Reserved. 11111 = Reserved.

CONFIGURATION REGISTERS

RS[5:0] = 0, 1, 1, 0, 0, 1 to 1, 0, 0, 0, 0, 0

Power-On/Reset = 0x0860

The AD7124-8 has eight configuration registers, CONFIG_0 to CONFIG_7. Each configuration register is associated with a setup; CONFIG_x is associated with Setup x. In the configuration register, the reference source, polarity, reference buffers enabled or disabled are configured.

Table 74 outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td colspan="4">0 (0)</td><td>Bipolar (1)</td><td colspan="2">Burnout (0)</td><td>REF_BUFP (0)</td></tr>
<tr><td>REF_BUFM (0)</td><td>AIN_BUFP (1)</td><td>AIN_BUFM (1)</td><td colspan="2">REF_SEL (0)</td><td colspan="3">PGA (0)</td></tr>
</table>

Table 74. Configuration Register Bit Descriptions

<table>
<tr><th>Bits</th><th>Bit Name</th><th colspan="3">Description</th></tr>
<tr><td>15:12</td><td>0</td><td colspan="3">These bits must be programmed with a Logic 0 for correct operation.</td></tr>
<tr><td>11</td><td>Bipolar</td><td colspan="3">Polarity select bit. When this bit is set, bipolar operation is selected. When this bit is cleared, unipolar operation is selected.</td></tr>
<tr><td>10:9</td><td>Burnout</td><td colspan="3">These bits select the magnitude of the sensor burnout detect current source.
00 = burnout current source off (default).
01 = burnout current source on, 0.5 μA.
10 = burnout current source on, 2 μA.
11 = burnout current source on, 4 μA.</td></tr>
<tr><td>8</td><td>REF_BUFP</td><td colspan="3">Buffer enable on REFINx(+). When this bit is set, the positive reference input (internal or external) is buffered. When this bit is cleared, the positive reference input (internal or external) is unbuffered.</td></tr>
<tr><td>7</td><td>REF_BUFM</td><td colspan="3">Buffer enable on REFINx(−). When this bit is set, the negative reference input (internal or external) is buffered. When this bit is cleared, the negative reference input (internal or external) is unbuffered.</td></tr>
<tr><td>6</td><td>AIN_BUFP</td><td colspan="3">Buffer enable on AINP. When this bit is set, the selected positive analog input pin is buffered. When this bit is cleared, the selected positive analog input pin is unbuffered.</td></tr>
<tr><td>5</td><td>AIN_BUFM</td><td colspan="3">Buffer enable on AINM. When this bit is set, the selected negative analog input pin is buffered. When this bit is cleared, the selected negative analog input pin is unbuffered.</td></tr>
<tr><td>4:3</td><td>REF_SEL</td><td colspan="3">Reference source select bits. These bits select the reference source to use when converting on any channels using this configuration register.
00 = REFIN1(+)/REFIN1(−).
01 = REFIN2(+)/REFIN2(−).
10 = internal reference.
11 = AV_{DD}.</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">PGA</td><td colspan="3">Gain select bits. These bits select the gain to use when converting on any channels using this configuration register.</td></tr>
<tr><td>PGA</td><td>Gain</td><td>Input Range When V_{REF} = 2.5 V (Bipolar Mode)</td></tr>
<tr><td>000</td><td>1</td><td>±2.5 V</td></tr>
<tr><td>001</td><td>2</td><td>±1.25 V</td></tr>
<tr><td>010</td><td>4</td><td>± 625 mV</td></tr>
<tr><td>011</td><td>8</td><td>±312.5 mV</td></tr>
<tr><td>100</td><td>16</td><td>±156.25 mV</td></tr>
<tr><td>101</td><td>32</td><td>±78.125 mV</td></tr>
<tr><td>110</td><td>64</td><td>±39.06 mV</td></tr>
<tr><td>111</td><td>128</td><td>±19.53 mV</td></tr>
</table>

FILTER REGISTERS

RS[5:0] = 1, 0, 0, 0, 0, 1 to 1, 0, 1, 0, 0, 0

Power-On/Reset = 0x060180

The AD7124-8 has eight filter registers, FILTER_0 to FILTER_7. Each filter register is associated with a setup; FILTER_x is associated with Setup x. In the filter register, the filter type and output word rate are set.

Table 75 outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td colspan="3">Filter (0)</td><td>REJ60(0)</td><td colspan="3">POST_FILTER(0)</td><td>SINGLE_CYCLE(0)</td></tr>
<tr><td colspan="5">0(0)</td><td colspan="3">FS[10:8](0)</td></tr>
<tr><td colspan="8">FS[7:0](0)</td></tr>
</table>

Table 75. Filter Register Bit Descriptions

<table>
<tr><th>Bits</th><th>Bit Name</th><th colspan="3">Description</th></tr>
<tr><td>23:21</td><td>Filter</td><td colspan="3">Filter type select bits. These bits select the filter type.
000 = sinc^4 filter (default).
001 = reserved.
010 = sinc^3 filter.
011 = reserved.
100 = fast settling filter using the sinc^4 filter. The sinc^4 filter is followed by an averaging block, which results in a settling time equal to the conversion time. In full power and mid power modes, averaging by 16 occurs whereas averaging by 8 occurs in low power mode.
101 = fast settling filter using the sinc^3 filter. The sinc^3 filter is followed by an averaging block, which results in a settling time equal to the conversion time. In full power and mid power modes, averaging by 16 occurs whereas averaging by 8 occurs in low power mode.
110 = reserved.
111 = post filter enabled. The AD7124-8 includes several post filters, selectable using the POST_FILTER bits. The post filters have single cycle settling, the settling time being considerably better than a simple sinc^3/sinc^4 filter. These filters offer excellent 50 Hz and60 Hz rejection.</td></tr>
<tr><td>20</td><td>REJ60</td><td colspan="3">When this bit is set, a first order notch is placed at 60 Hz when the first notch of the sinc filter is at 50 Hz. This allows simultaneous 50 Hz and 60 Hz rejection.</td></tr>
<tr><td rowspan="10">19:17</td><td rowspan="10">POST_FILTER</td><td colspan="3">Post filter type select bits. When the filter bits are set to 1, the sinc^3 filter is followed by a post filter that offers good 50 Hz and 60 Hz rejection at output data rates that have zero latency approximately.</td></tr>
<tr><td>POST_FILTER</td><td>Output Data Rate (SPS)</td><td>Rejection at 50 Hz and 60 Hz ± 1 Hz (dB)</td></tr>
<tr><td>000</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>010</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>010</td><td>27.27</td><td>47</td></tr>
<tr><td>011</td><td>25</td><td>62</td></tr>
<tr><td>100</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>101</td><td>20</td><td>86</td></tr>
<tr><td>110</td><td>16.7</td><td>92</td></tr>
<tr><td>111</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>16</td><td>SINGLE_CYCLE</td><td colspan="3">Single cycle conversion enable bit. When this bit is set, the AD7124-8 settles in one conversion cycle so that it functions as a zero latency ADC. This bit has no effect when multiple analog input channels are enabled or when the single conversion mode is selected. When the fast filters are used, this bit has no effect.</td></tr>
<tr><td>15:11</td><td>0</td><td colspan="3">These bits must be programmed with a Logic 0 for correct operation.</td></tr>
<tr><td>10:0</td><td>FS[10:0]</td><td colspan="3">Filter output data rate select bits. These bits set the output data rate of the sinc^3 filter, sinc^4 filter, and fast settling filters. In addition, they affect the position of the first notch of the sinc filter and the cutoff frequency. In association with the gain selection, they also determine the output noise and, therefore, the effective resolution of the device (see noise tables). FS can have a value from 1 to 2047.</td></tr>
</table>

OFFSET REGISTERS

RS[5:0] = 1, 0, 1, 0, 0, 1 to 1, 1, 0, 0, 0, 0
Power-On/Reset = 0x800000

The AD7124-8 has eight offset registers, OFFSET_0 to OFFSET_7. Each offset register is associated with a setup; OFFSET_x is associated with Setup x. The offset registers are 24-bit registers and hold the offset calibration coefficient for the ADC and its power-on reset value is 0x800000. Each of these registers is a read/write register. These registers are used in conjunction with the associated gain register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The ADC must be placed in standby mode or idle mode when writing to the offset registers.

GAIN REGISTERS

RS[5:0] = 1, 1, 0, 0, 0, 1 to 1, 1, 1, 0, 0, 0
Power-On/Reset = 0x5XXXXX

The AD7124-8 has eight gain registers, GAIN_0 to GAIN_7. Each gain register is associated with a setup; GAIN_x is associated with Setup x. The gain registers are 24-bit registers and hold the full-scale calibration coefficient for the ADC. The AD7124-8 is factory calibrated to a gain of 1. The gain register contains this factory generated value on power-on and after a reset. The gain registers are read/write registers. However, when writing to the registers, the ADC must be placed in standby mode or idle mode. The default value is automatically overwritten if an internal or system full-scale calibration is initiated by the user or the full-scale registers are written to.

OUTLINE DIMENSIONS

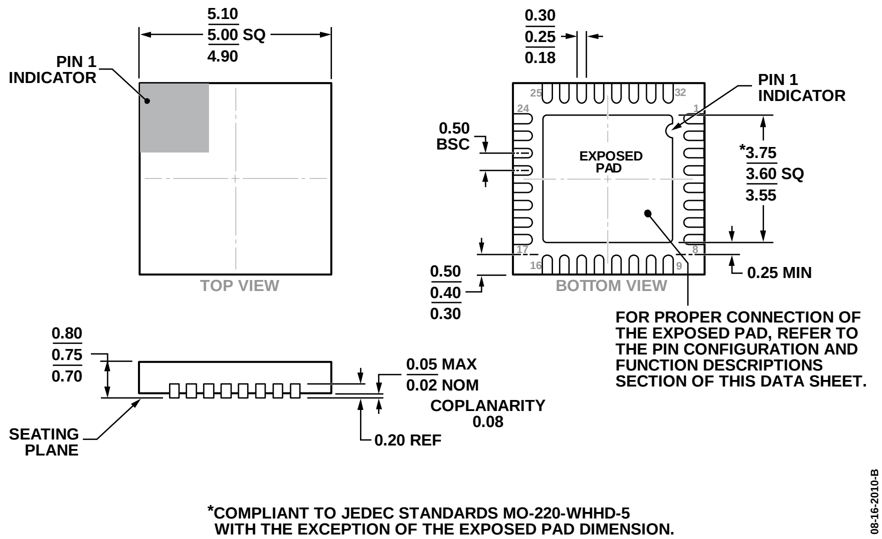


Figure 129. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm x 5 mm Body, Very, Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7124-8BCPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
AD7124-8BCPZ-RL	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
AD7124-8BCPZ-RL7	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
EVAL-AD7124-8SDZ		Evaluation Board	
EVAL-SDP-CB1Z		Evaluation Controller Board	

[1] Z = RoHS Compliant Part.