

BUK7K18-40E

Dual N-channel 40 V, 19 mΩ standard level MOSFET

10 December 2013

Product data sheet

1. General description

Dual standard level N-channel MOSFET in an LFP56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with $V_{GS(th)}$ of greater than 1 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	24.2	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	38	W
Static characteristics FET1 and FET2						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	-	15.5	19	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	-	4.3	-	nC

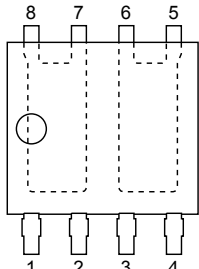
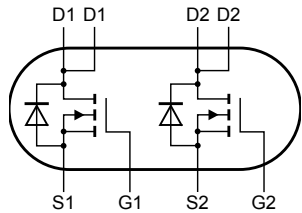


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p><i>mbk725</i></p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K18-40E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K18-40E	71840E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; DC	-20	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	24.2	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	22	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4	-	127	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	38	W

Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode FET1 and FET2					
I _S	source current	T _{mb} = 25 °C	-	24.2	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	127	A
Avalanche Ruggedness FET1 and FET2					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 24.2 A; V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; Fig. 3	[1][2]	26.3	mJ

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

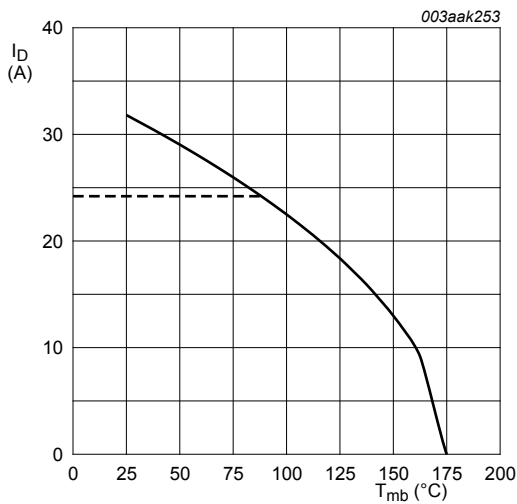


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

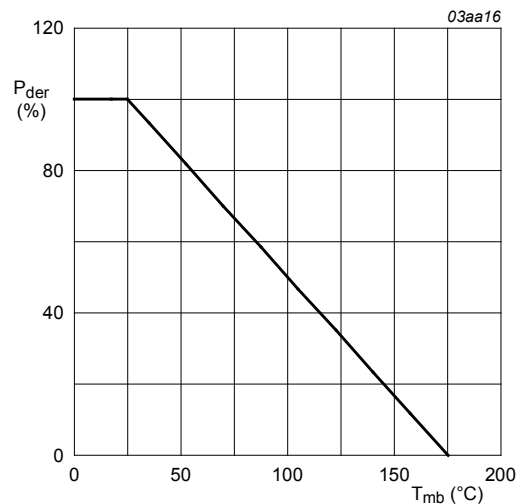


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

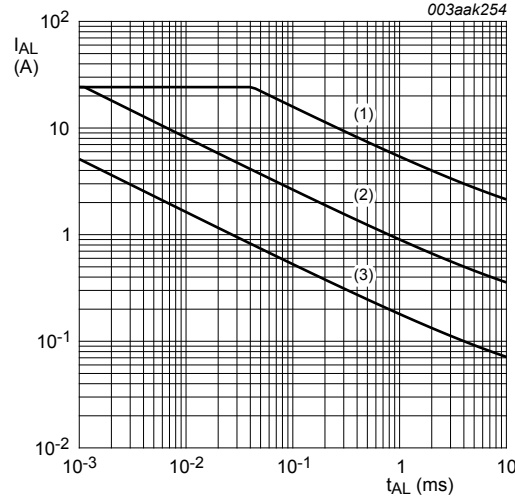


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (init)} = 25^{\circ}C$; (2) $T_{j (init)} = 150^{\circ}C$; (3) Repetitive Avalanche

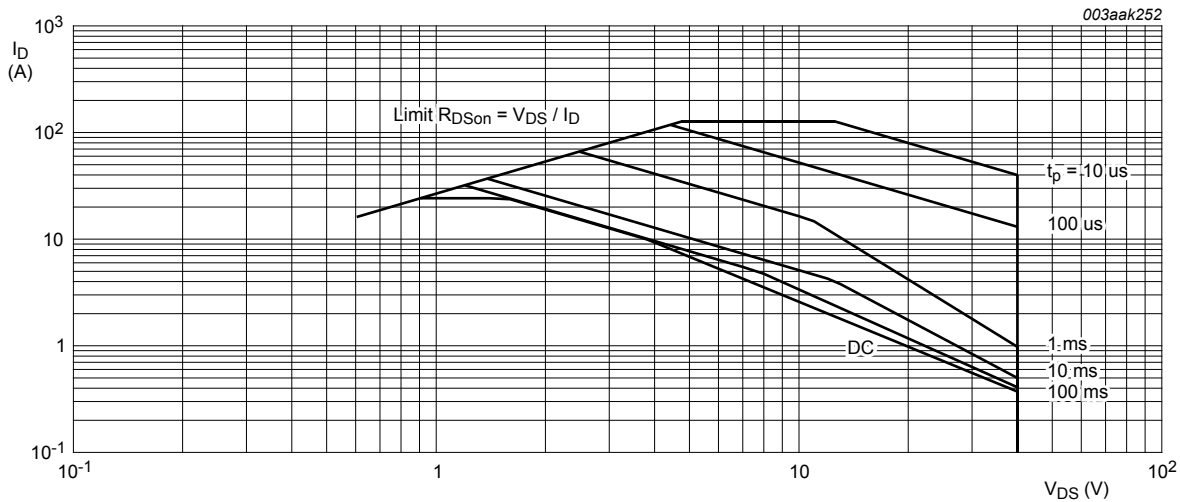


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	3.96	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

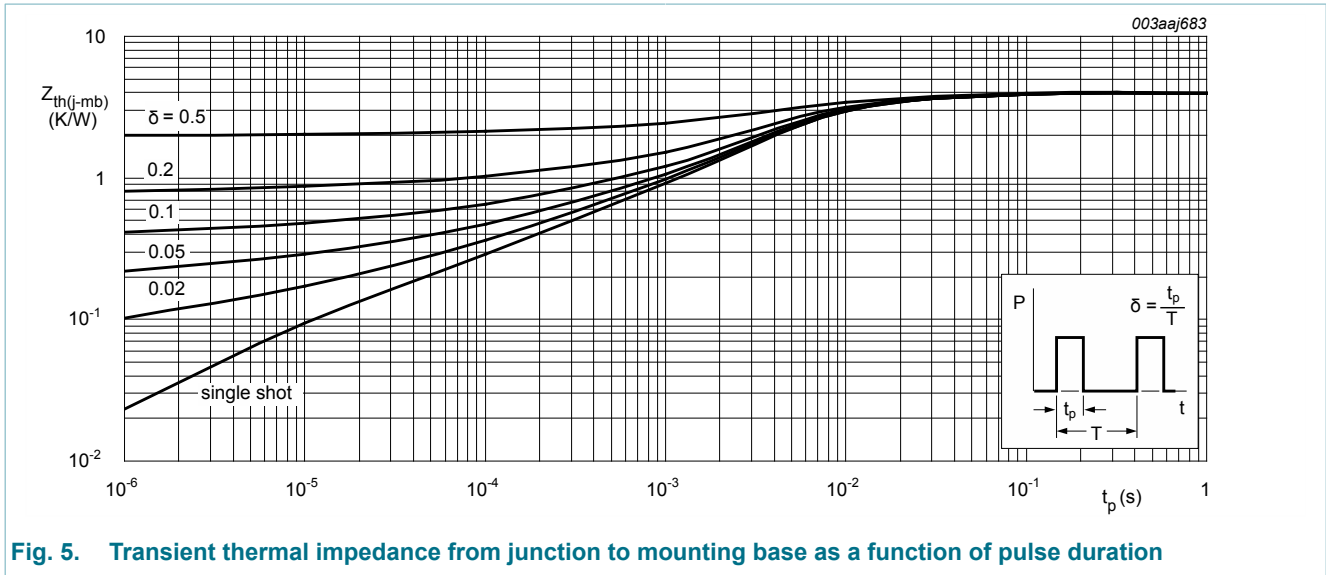


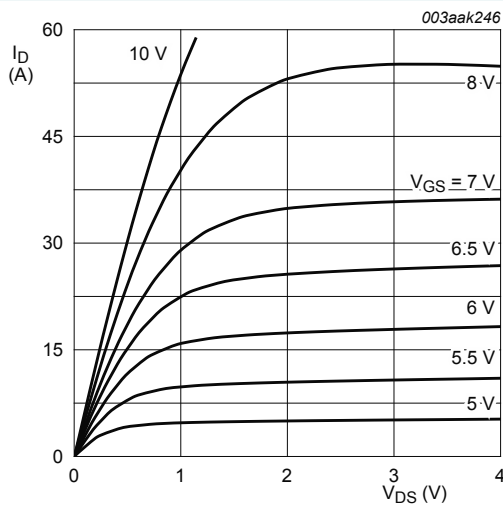
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	36	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	40	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 9; Fig. 10	2.4	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; Fig. 9; Fig. 10	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 9; Fig. 10	-	-	4.5	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _J = 25 °C	-	0.02	1	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _J = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _J = 25 °C; Fig. 11	-	15.5	19	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _J = 175 °C; Fig. 11; Fig. 12	-	30.5	37.4	mΩ
Dynamic characteristics FET1 and FET2						
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 32 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13; Fig. 14	-	11.8	-	nC
Q _{GS}	gate-source charge		-	3.6	-	nC
Q _{GD}	gate-drain charge		-	4.3	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$	-	606	808	pF
C_{oss}	output capacitance	$T_j = 25\text{ °C};$ Fig. 15	-	134	161	pF
C_{rss}	reverse transfer capacitance		-	87	119	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 32\text{ V}; R_L = 3.3\text{ }\Omega; V_{GS} = 10\text{ V};$	-	6.2	-	ns
t_r	rise time	$R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ °C}; I_D = 10\text{ A}$	-	12.7	-	ns
$t_{d(off)}$	turn-off delay time		-	7.9	-	ns
t_f	fall time		-	10	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C};$ Fig. 16	-	0.83	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	16.8	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}; T_j = 25\text{ °C}$	-	9.1	-	nC



$T_j = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

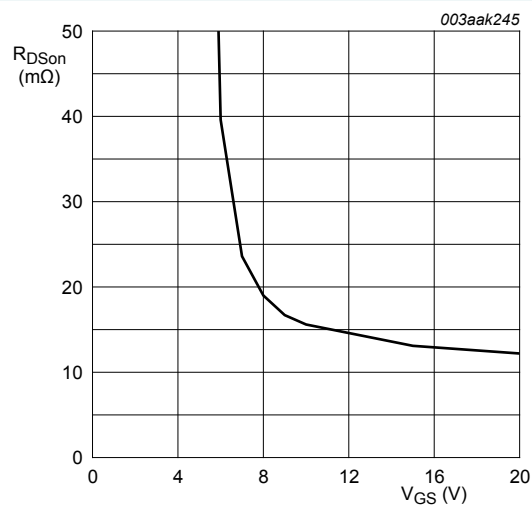


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ °C}; I_D = 10\text{ A}$

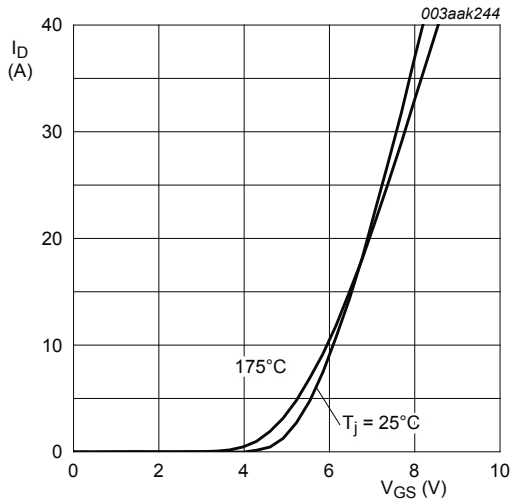


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

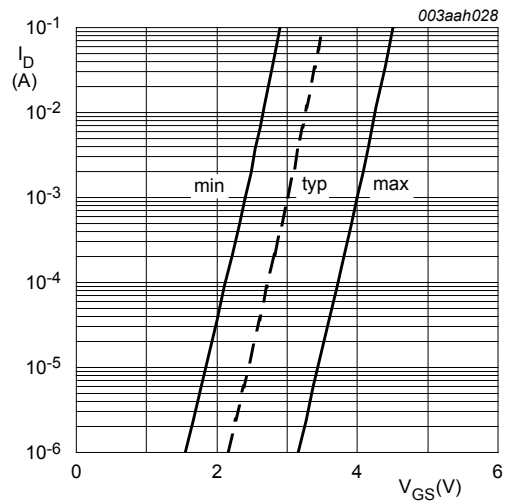


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ C; V_{DS} = 5V$

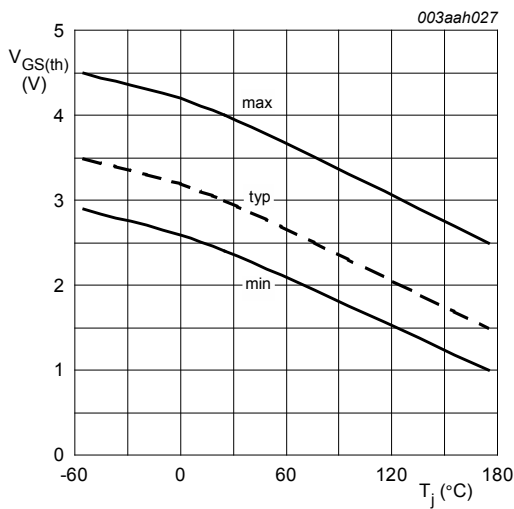
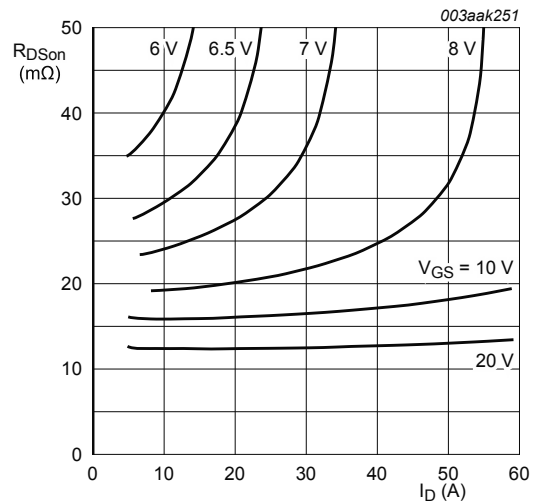


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$



$T_j = 25^\circ C; t_p = 300 \mu s$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

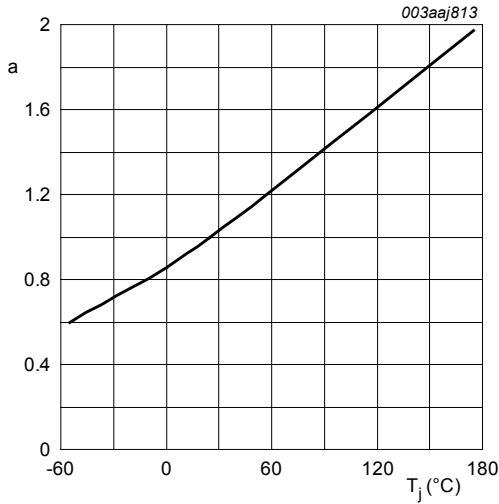


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$

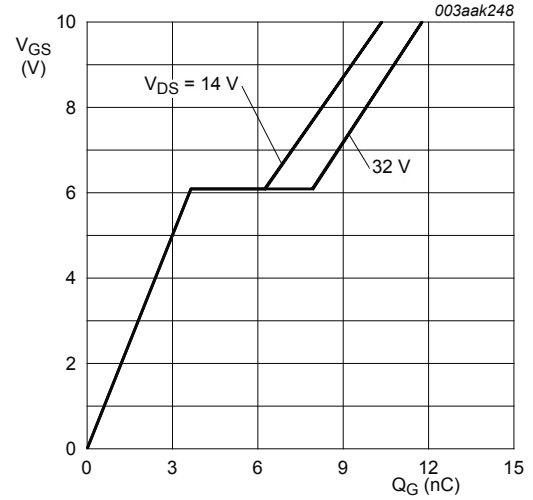


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C; I_D = 10A$



Fig. 14. Gate charge waveform definitions

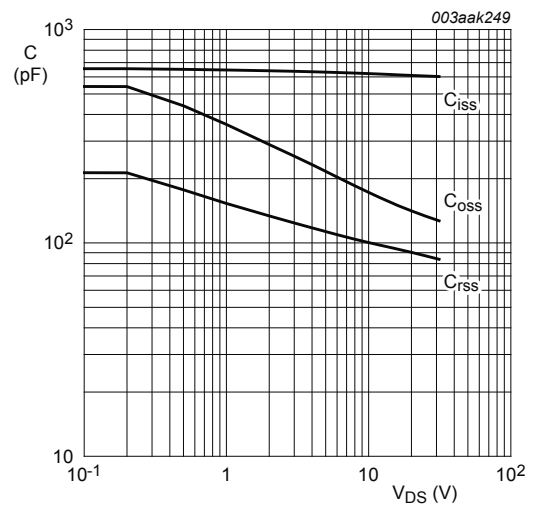


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

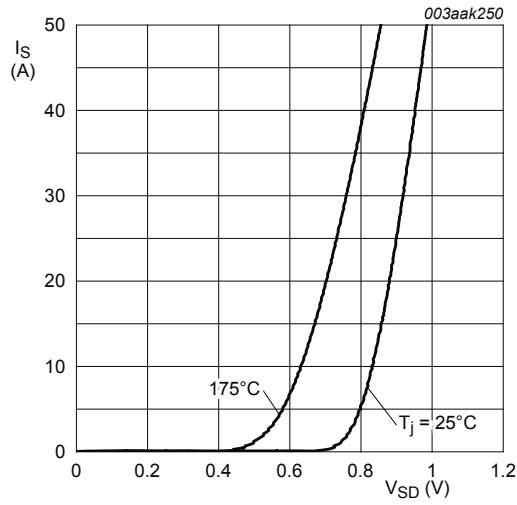
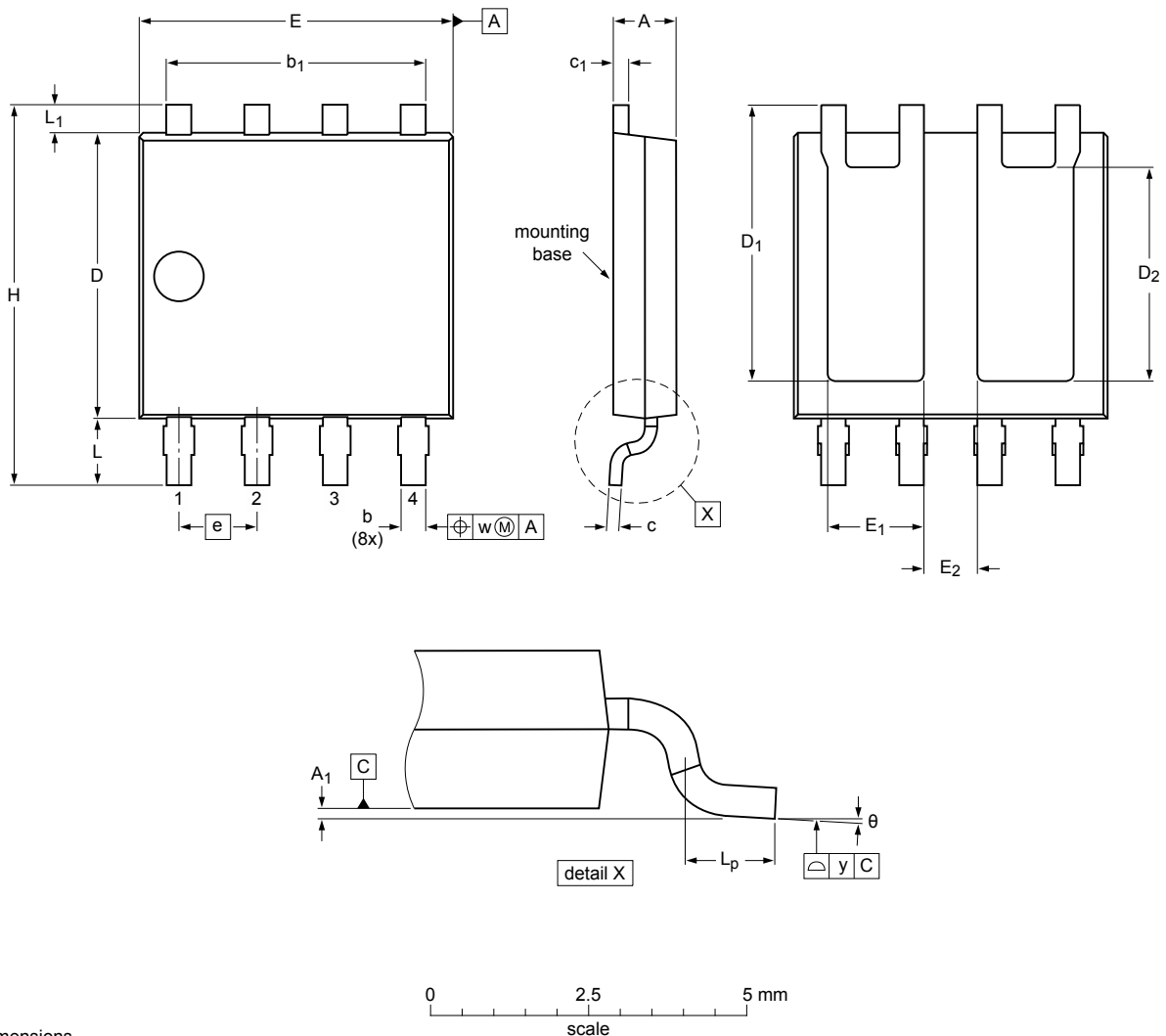


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

Plastic single ended surface mounted package (LPAK56D); 8 leads SOT1205



Dimensions

Unit	A	A ₁	b	b ₁	c	c ₁	D ⁽¹⁾	D ₁ ⁽¹⁾	D ₂ ^(ref)	E ⁽¹⁾	E ₁ ⁽¹⁾	E ₂	e	H	L	L ₁	L _p	w	y	θ	
max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.8	3.5	5.30	1.8	0.85	6.2	1.3	0.55	0.85		0.25	0.1	8°	
nom													1.27								
min		0.0	0.35	4.1	0.19	0.24	4.45			4.95	1.6		5.9	0.8	0.30	0.40				0°	

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						13-02-19 13-02-21

Fig. 17. Package outline LPAK56D (SOT1205)

12. Legal information

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(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

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ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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