NCV6323

3MHz, 2A Synchronous Buck Converter

High Efficiency, Low Ripple, Adjustable Output Voltage

The NCV6323 is a synchronous buck converter which is optimized to supply different sub systems of portable applications powered by one cell Li−ion or three cell Alkaline/NiCd/NiMH batteries. The devices are able to deliver up to 2 A on an external adjustable voltage. Operation with 3 MHz switching frequency allows employing small size inductor and capacitors. Input supply voltage feedforward control is employed to deal with wide input voltage range. Synchronous rectification offer improved system efficiency. The NCV6323 is in a space saving, low profile 2.0 x 2.0 x 0.75 mm WDFN−8 package.

Features

- 2.5 V to 5.5 V Input Voltage Range
- External Adjustable Voltage
- Up to 2 A Output Current
- 3 MHz Switching Frequency
- Synchronous Rectification
- Enable Input
- Power Good Output Option
- Soft Start
- Over Current Protection
- Active Discharge When Disabled
- Thermal Shutdown Protection
- WDFN−8, 2 x 2 mm, 0.5 mm Pitch Package
- Maximum 0.8 mm Height for Super Thin Applications
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Cellular Phones, Smart Phones, and PDAs
- Portable Media Players
- Digital Still Cameras
- Wireless and DSL Modems
- USB Powered Devices
- Point of Load
- Game and Entertainment System

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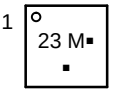
WDFN8
CASE 511BT

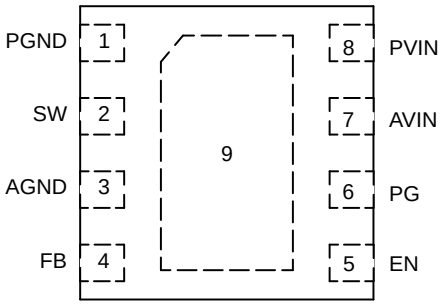
MARKING DIAGRAM



23 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

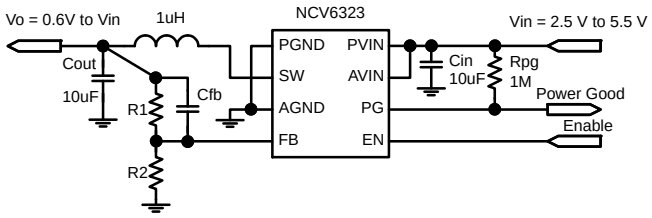
PINOUT



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.



(a) Power Good Output Option
(NCV6323)

Figure 1. Typical Application Circuit

PIN DESCRIPTION

Pin	Name	Type	Description
1	PGND	Power Ground	Power Ground for power, analog blocks. Must be connected to the system ground.
2	SW	Power Output	Switch Power pin connects power transistors to one end of the inductor.
3	AGND	Analog Ground	Analog Ground analog and digital blocks. Must be connected to the system ground.
4	FB	Analog Input	Feedback Voltage from the buck converter output. This is the input to the error amplifier. This pin is connected to the resistor divider network between the output and AGND.
5	EN	Digital Input	Enable of the IC. High level at this pin enables the device. Low level at this pin disables the device.
6	PG	Digital Output	It is open drain output. Low level at this pin indicates the device is not in power good, while high impedance at this pin indicates the device is in power good.
7	AVIN	Analog Input	Analog Supply. This pin is the analog and the digital supply of the device. An optional 1 μF or larger ceramic capacitor bypasses this input to the ground. This capacitor should be placed as close as possible to this input.
8	PVIN	Power Input	Power Supply Input. This pin is the power supply of the device. A 10 μF or larger ceramic capacitor must bypass this input to the ground. This capacitor should be placed as close a possible to this input.
9	PAD	Exposed Pad	Exposed Pad. Must be soldered to system ground to achieve power dissipation performances. This pin is internally unconnected

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV6323BMTAATBG	23	WDFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

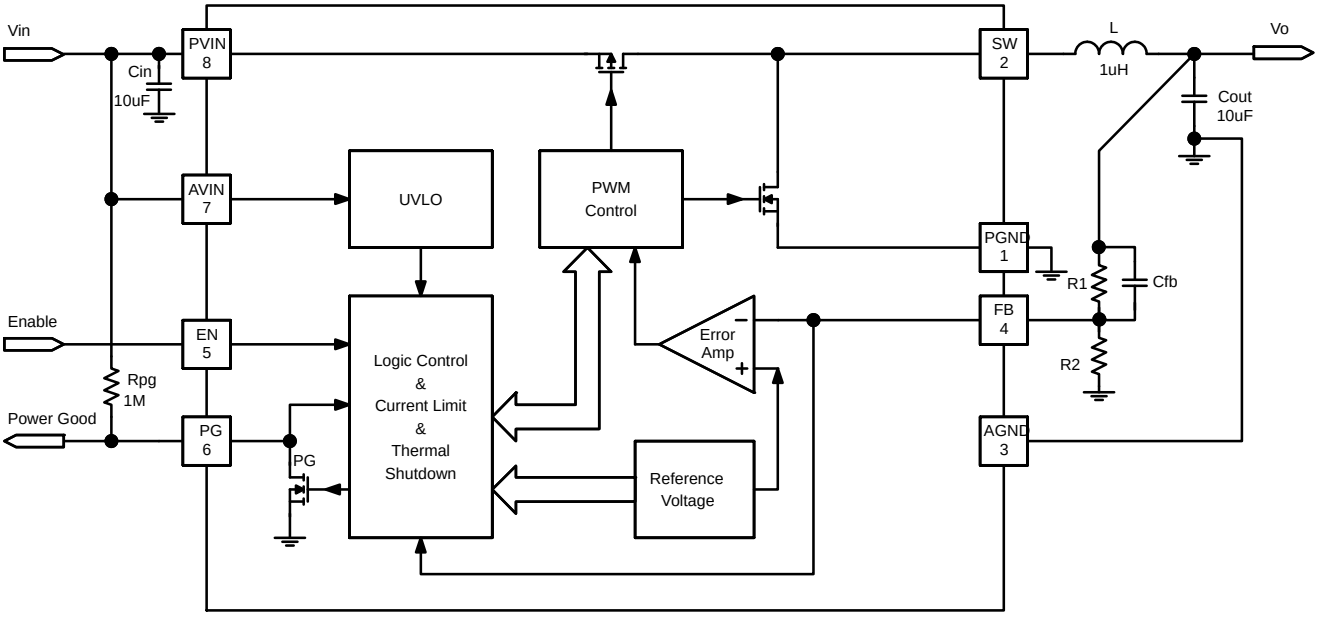


Figure 2. Functional Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Input Supply Voltage to GND	V_{PVIN}, V_{AVIN}	−0.3	7.0	V
Switch Node to GND	V_{SW}	−0.3	7.0	V
EN, PG to GND	V_{EN}, V_{PG}	−0.3	7.0	V
FB to GND	V_{FB}	−0.3	7.0	V
Human Body Model (HBM) ESD Rating are (Note 1)	ESD HBM		2000	V
Machine Model (MM) ESD Rating (Note 1)	ESD MM		200	V
Latchup Current (Note 2)	I_{LU}	−100	100	mA
Operating Junction Temperature Range (Note 3)	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	85	°C
Storage Temperature Range	T_{STG}	−55	150	°C
Thermal Resistance Junction−to−Top Case (Note 4)	$R_{\theta JC}$	12		°C/W
Thermal Resistance Junction−to−Board (Note 4)	$R_{\theta JB}$	30		°C/W
Thermal Resistance Junction−to−Ambient (Note 4)	$R_{\theta JA}$	62		°C/W
Power Dissipation (Note 5)	P_D	1.6		W
Moisture Sensitivity Level (Note 6)	MSL	1		−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
2. Latchup Current per JEDEC standard: JESD78 Class II.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
4. The thermal resistance values are dependent of the PCB heat dissipation. Board used to drive these data was an 80 x 50 mm NCP6324EVB board. It is a multilayer board with 1 once internal power and ground planes and 2−once copper traces on top and bottom of the board. If the copper trances of top and bottom are 1 once too, $R_{\theta JC}$ = 11°C/W, $R_{\theta JB}$ = 30°C/W, and $R_{\theta JA}$ = 72°C/W.
5. The maximum power dissipation (PD) is dependent on input voltage, maximum output current and external components selected.
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, L = 1 μH, C = 10 μF, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J up to 125°C, unless other noted.)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
V_{IN}	Input Voltage V_{IN} Range	(Note 7)	2.5	−	5.5	V
SUPPLY CURRENT						
I_Q	V_{IN} Quiescent Supply Current	EN high, no load, Forced PWM Mode	−	5.7	−	mA
I_{SD}	V_{IN} Shutdown Current	EN low (Note 9)	−	−	1	μA
OUTPUT VOLTAGE						
V_{OUT}	Output Voltage Range	(Note 8)	0.6	−	V_{IN}	V
V_{FB}	FB Voltage	PWM Mode	594	600	606	mV
	FB Voltage in Load Regulation	V_{IN} = 3.6 V, I_{OUT} from 200 mA to I_{OUTMAX}, PWM mode (Note 8)	−	−0.5	−	%/A
	FB Voltage in Line Regulation	I_{OUT} = 200 mA, V_{IN} from MAX (V_{NOM} + 0.5 V, 2.3 V) to 5.5 V, PWM mode (Note 8)	−	0	−	%/V
D_{MAX}	Maximum Duty Cycle	(Note 8)	−	100	−	%
OUTPUT CURRENT						
I_{OUTMAX}	Output Current Capability	(Note 8)	2.0	−	−	A
I_{LIMP}	Output Peak Current Limit P−Channel		2.3	2.8	3.3	A
I_{LIMN}	Output Peak Current Limit N−Channel			0.9		A
VOLTAGE MONITOR						
V_{INUV-}	V_{IN} UVLO Falling Threshold		−	−	2.4	V
V_{INHYS}	V_{IN} UVLO Hysteresis		60	140	200	mV
V_{PGL}	Power Good Low Threshold	V_{OUT} falls down to cross the threshold (percentage of FB voltage)	87	90	92	%
V_{PGHYS}	Power Good Hysteresis	V_{OUT} rises up to cross the threshold (percentage of Power Good Low Threshold (V_{PGL}) voltage)	0	5	7	%
Td_{PGH1}	Power Good High Delay in Start Up	From EN rising edge to PG going high.	−	1.15	−	ms
Td_{PGL1}	Power Good Low Delay in Shut Down	From EN falling edge to PG going low. (Note 8)	−	8	−	μs
Td_{PGH}	Power Good High Delay in Regulation	From V_{FB} going higher than 95% nominal level to PG going high. Not for the first time in start up. (Note 8)	−	5	−	μs
Td_{PGL}	Power Good Low Delay in Regulation	From V_{FB} going lower than 90% nominal level to PG going low. (Note 8)	−	8	−	μs
VPG_L	Power Good Pin Low Voltage	Voltage at PG pin with 5 mA sink current	−	−	0.3	V
PG_LK	Power Good Pin Leakage Current	3.6 V at PG pin when power good valid	−	−	100	nA
INTEGRATED MOSFETs						
R_{ON_H}	High−Side MOSFET ON Resistance	V_{IN} = 3.6 V (Note 9) V_{IN} = 5 V (Note 9)	−	160 130	200 −	mΩ
R_{ON_L}	Low−Side MOSFET ON Resistance	V_{IN} = 3.6 V (Note 9) V_{IN} = 5 V (Note 9)	−	110 100	140 −	mΩ
SWITCHING FREQUENCY						
F_{SW}	Normal Operation Frequency		2.7	3.0	3.3	MHz
SOFT START						
T_{SS}	Soft−Start Time	Time from EN to 90% of output voltage target	−	0.4	1	ms

7. Operation above 5.5 V input voltage for extended periods may affect device reliability. At the first power−up, input voltage must be > 2.6 V.
8. Guaranteed by design, not tested in production.
9. Maximum value applies for T_J = 85°C.

ELECTRICAL CHARACTERISTICS (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, L = 1 μH, C = 10 μF, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J up to 125°C, unless other noted.)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
CONTROL LOGIC						
V_{EN_H}	EN Input High Voltage		1.1	–	–	V
V_{EN_L}	EN Input Low Voltage		–	–	0.4	V
V_{EN_HYS}	EN Input Hysteresis		–	270	–	mV
I_{EN_BIAS}	EN Input Bias Current			0.1	1	μA
OUTPUT ACTIVE DISCHARGE						
R_DIS	Internal Output Discharge Resistance	from SW to PGND	75	500	700	Ω
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold		–	170	–	°C
T_{SD_HYS}	Thermal Shutdown Hysteresis		–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL OPERATING CHARACTERESTICS

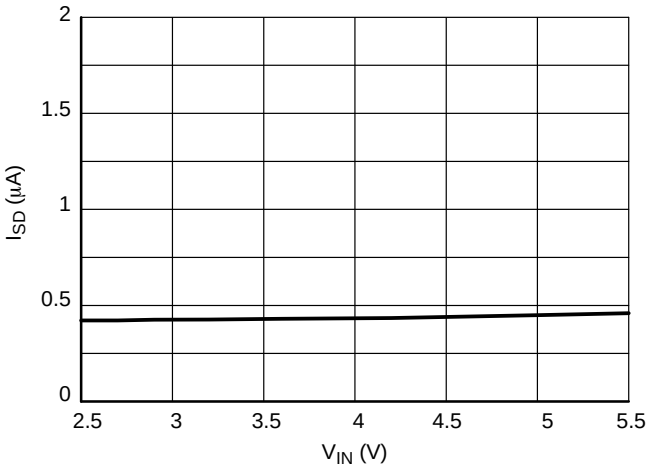


Figure 3. Shutdown Current vs. Input Voltage (EN = Low, T_A = 25°C)

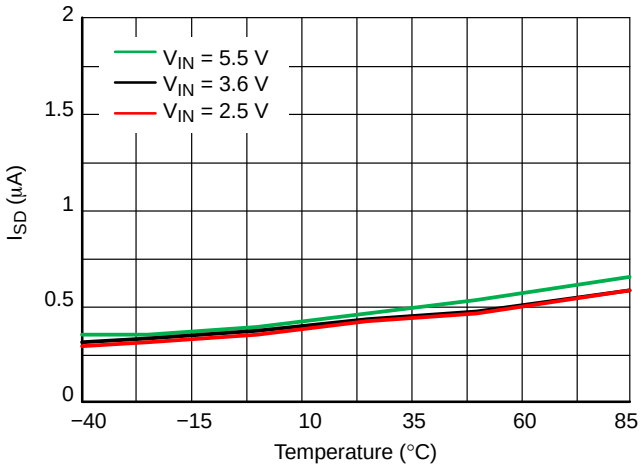


Figure 4. Shutdown Current vs. Temperature (EN = Low, V_{IN} = 3.6 V)

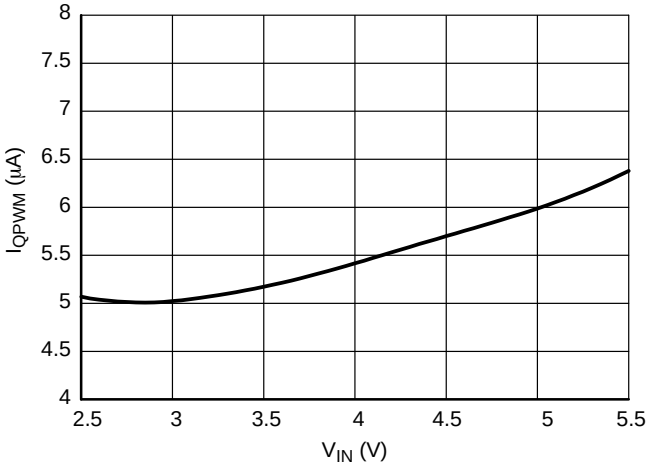


Figure 5. PWM Quiescent Current vs. Input Voltage (EN = High, Open Loop, V_{OUT} = 1.8 V, T_A = 25°C)

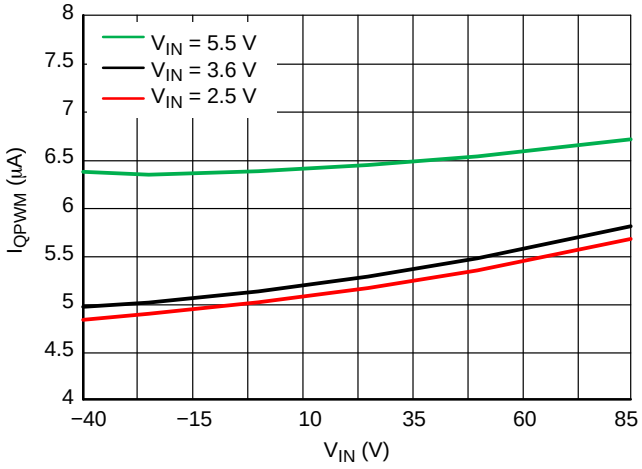


Figure 6. PWM Quiescent Current vs. Temperature (EN = High, Open Loop, V_{OUT} = 1.8 V, V_{IN} = 3.6 V)

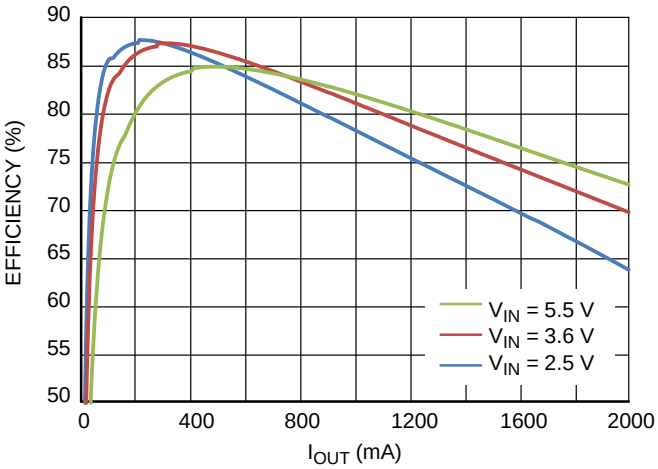


Figure 7. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.05 V, T_A = 25°C)

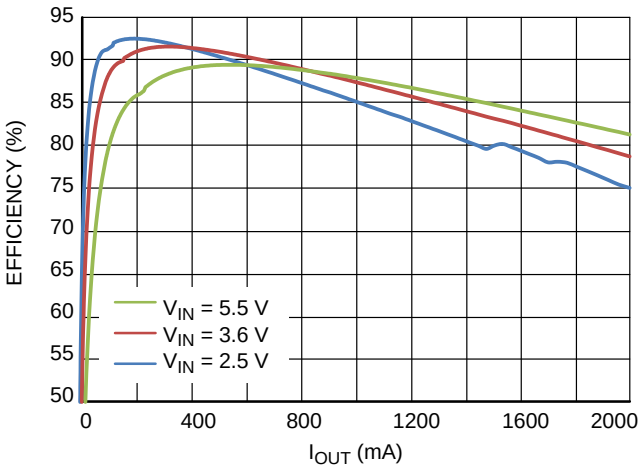


Figure 8. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.8 V, T_A = 25°C)

TYPICAL OPERATING CHARACTERESTICS

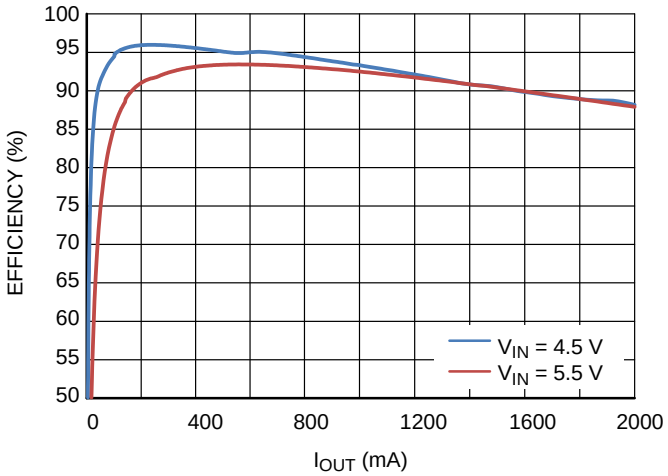


Figure 9. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 3.3 V, T_A = 25°C)

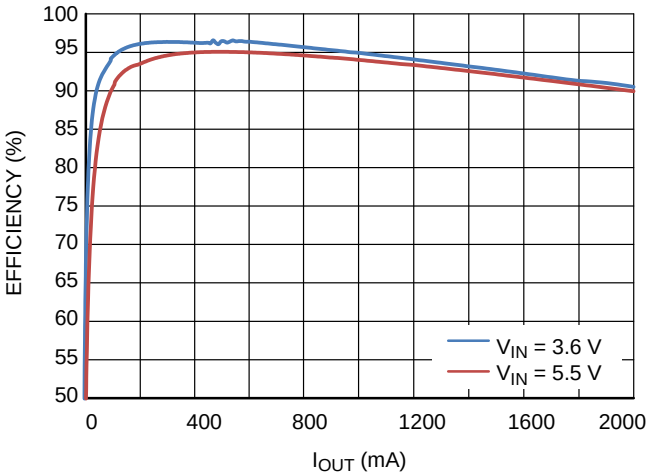


Figure 10. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 4 V , T_A = 25°C)

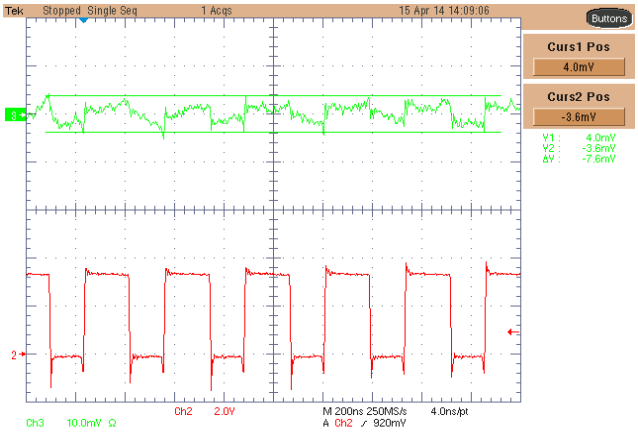


Figure 11. Output Ripple Voltage in PWM Mode (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 1 A, L=1 μH, C_{OUT} = 10 μF)

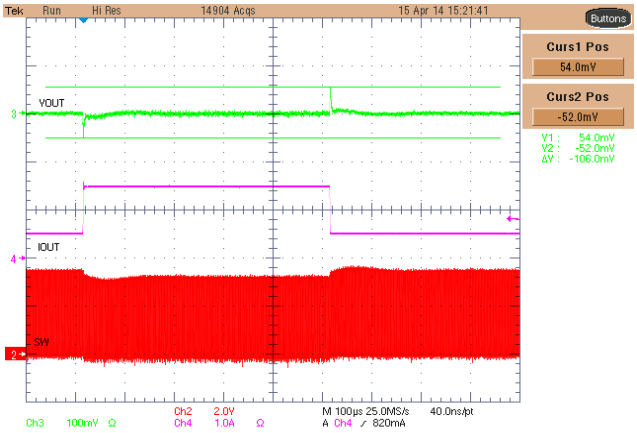


Figure 12. Load Transient Response (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA to 1500 mA, L = 1 μH, C_{OUT} = 10 μF)

TYPICAL OPERATING CHARACTERESTICS

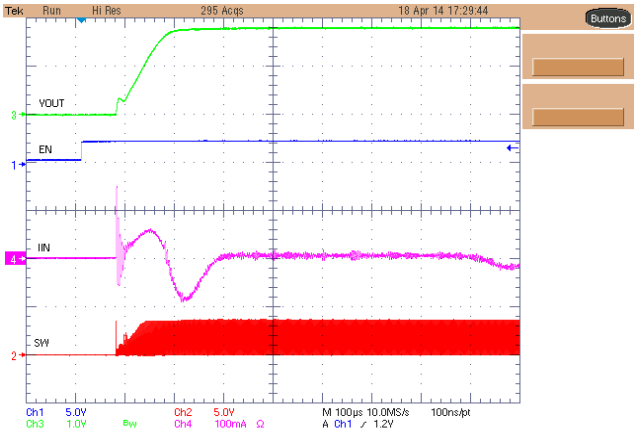


Figure 13. Power Up Sequence and Inrush Current in Input (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A, L = 1 µH, C_{OUT} = 10 µF)

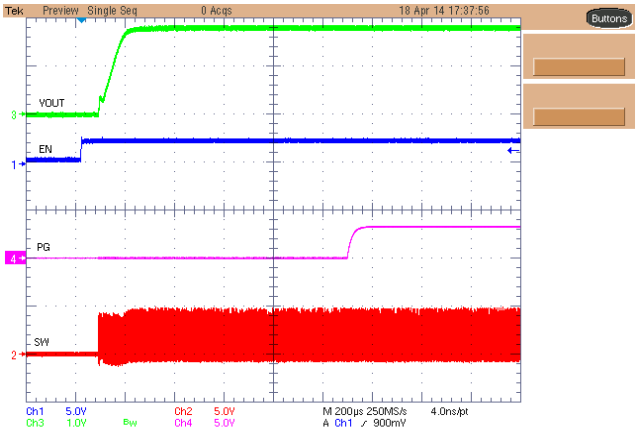


Figure 14. Power Up Sequence and Power Good (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A, L = 1 µH, C_{OUT} = 10 µF)

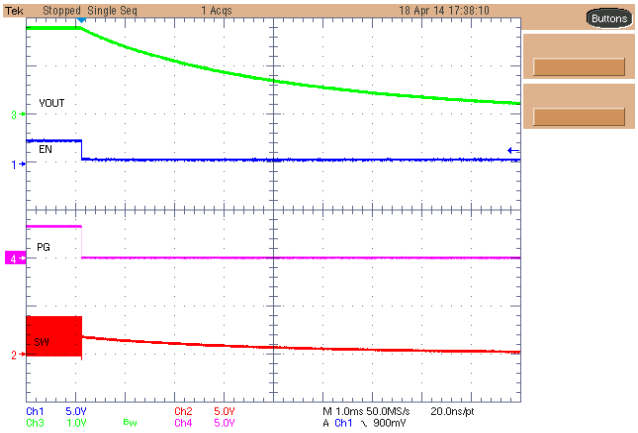


Figure 15. Power Down Sequence and Active Output Discharge (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A, L = 1 µH, C_{OUT} = 10 µF)

DETAILED DESCRIPTION

General

The NCV6323 is a synchronous buck converter which is optimized to supply different sub−systems of portable applications powered by one cell Li−ion or three cell Alkaline/NiCd/NiMH batteries. The devices are able to deliver up to 2 A on an external adjustable voltage. Operation with 3 MHz switching frequency allows employing small size inductor and capacitors. Input supply voltage feedforward control is employed to deal with wide input voltage range. Synchronous rectification offer improved system efficiency.

PWM Mode Operation

In medium and heavy load range, the inductor current is continuous and the device operates in PWM mode with fixed switching frequency, which has a typical value of 3 MHz. In this mode, the output voltage is regulated by on−time pulse width modulation of an internal P−MOSFET. An internal N−MOSFET operates as synchronous rectifier and its turn−on signal is complimentary to that of the P−MOSFET.

Undervoltage Lockout

The input voltage VIN must reach or exceed 2.5 V (typical) before the NCV6323 enables the converter output to begin the start up sequence. The UVLO threshold hysteresis is typically 100 mV.

Enable

The NCV6323 has an enable logic input pin EN. A high level (above 1.1 V) on this pin enables the device to active mode. A low level (below 0.4 V) on this pin disables the device and makes the device in shutdown mode. There is an internal filter with 5 μs time constant. The EN pin is pulled down by an internal 10 nA sink current source. In most of applications, the EN signal can be programmed independently to VIN power sequence.

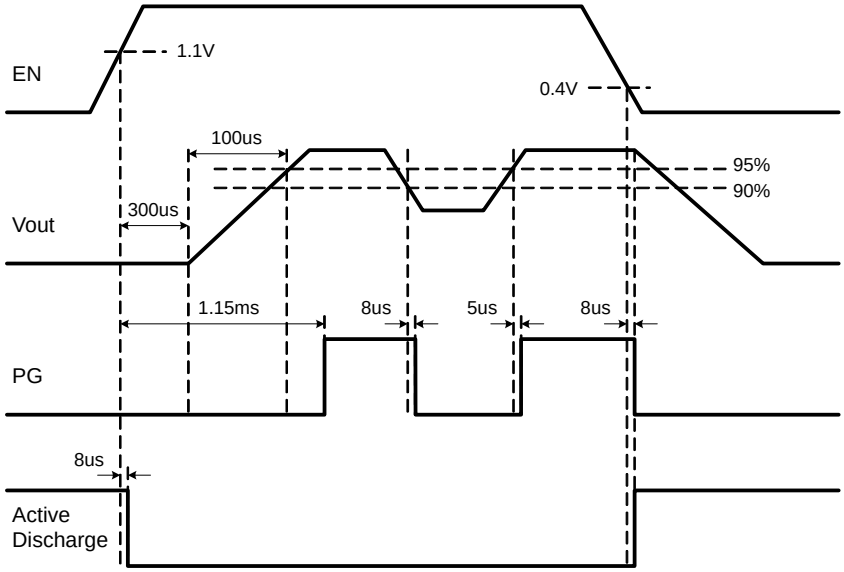


Figure 16. Power Good and Active Discharge Timing Diagram

Power Good Output

The device monitors the output voltage and provides a power good output signal at the PG pin. This pin is an open−drain output pin. To indicate the output of the converter is established, a power good signal is available. The power good signal is low when EN is high but the output voltage has not been established. Once the output voltage of the converter drops out below 90% of its regulation during operation, the power good signal is pulled low and indicates a power failure. A 5% hysteresis is required on power good comparator before signal going high again.

Soft−Start

A soft start limits inrush current when the converter is enabled. After a minimum 300 μs delay time following the enable signal, the output voltage starts to ramp up in 100 μs (for external adjustable voltage devices) or with a typical 10 V/ms slew rate (for fixed voltage devices).

Active Output Discharge

An output discharge operation is active in when EN is low. A discharge resistor (500 Ω typical) is enabled in this condition to discharge the output capacitor through SW pin.

Cycle−by−Cycle Current Limitation

The NCV6323 protects the device from over current with a fixed−value cycle−by−cycle current limitation. The typical peak current limit ILMT is 2.8 A. If inductor current exceeds the current limit threshold, the P−MOSFET will be turned off cycle−by−cycle. The maximum output current can be calculated by

$$I_{MAX} = I_{LMT} - \frac{V_{OUT} \cdot \left(V_{IN} - V_{OUT}\right)}{2 \cdot V_{IN} \cdot f_{SW} \cdot L} \quad \text{(eq. 1)}$$

where VIN is input supply voltage, VOUT is output voltage, L is inductance of the filter inductor, and f_{SW} is 3 MHz normal switching frequency.

Negative Current Protection

The NCV6323 includes a 1 A negative current protection. It helps to protect the internal NMOS in case of applications which require high output capacitor value.

Thermal Shutdown

The NCV6323 has a thermal shutdown protection to protect the device from overheating when the die temperature exceeds 170°C. After the thermal protection is triggered, the fault state can be ended by re−applying VIN and/or EN when the temperature drops down below 125°C.

APPLICATION INFORMATION

Output Filter Design Considerations

The output filter introduces a double pole in the system at a frequency of

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \quad \text{(eq. 2)}$$

The internal compensation network design of the NCV6323 is optimized for the typical output filter comprised of a 1.0 μH inductor and a 10 μF ceramic output capacitor, which has a double pole frequency at about 50 kHz. Other possible output filter combinations may have a double pole around 50 kHz to have optimum operation with the typical feedback network. Normal selection range of the inductor is from 0.47 μH to 4.7 μH, and normal selection range of the output capacitor is from 4.7 μF to 22 μF.

Inductor Selection

The inductance of the inductor is determined by given peak−to−peak ripple current IL_PP of approximately 20% to 50% of the maximum output current IOUT_MAX for a trade−off between transient response and output ripple. The inductance corresponding to the given current ripple is

$$L = \frac{\left(V_{IN} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot I_{L\_PP}} \quad \text{(eq. 3)}$$

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{I_{L\_PP}}{2} \quad \text{(eq. 4)}$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Table 1 shows some recommended inductors for high power applications and Table 2 shows some recommended inductors for low power applications.

Table 1. LIST OF RECOMMENDED INDUCTORS FOR HIGH POWER APPLICATIONS

Manufacturer	Part Number	Case Size (mm)	L (μH)	Rated Current (mA) (Inductance Drop)	Structure
MURATA	LQH44PN2R2MP0	4.0 x 4.0 x 1.8	2.2	2500 (−30%)	Wire Wound
MURATA	LQH44PN1R0NP0	4.0 x 4.0 x 1.8	1.0	2950 (−30%)	Wire Wound
MURATA	LQH32PNR47NNP0	3.0 x 2.5 x 1.7	0.47	3400 (−30%)	Wire Wound

Table 2. LIST OF RECOMMENDED INDUCTORS FOR LOW POWER APPLICATIONS

Manufacturer	Part Number	Case Size (mm)	L (μH)	Rated Current (mA) (Inductance Drop)	Structure
MURATA	LQH44PN2R2MJ0	4.0 x 4.0 x 1.1	2.2	1320 (−30%)	Wire Wound
MURATA	LQH44PN1R0NJ0	4.0 x 4.0 x 1.1	1.0	2000 (−30%)	Wire Wound
TDK	VLS201612ET−2R2	2.0 x 1.6 x 1.2	2.2	1150 (−30%)	Wire Wound
TDK	VLS201612ET−1R0	2.0 x 1.6 x 1.2	1.0	1650 (−30%)	Wire Wound

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For a given peak−to−peak ripple current IL_PP in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three ripple components as below.

$$V_{OUT\_PP} \approx V_{OUT\_PP(C)} + V_{OUT\_PP(ESR)} + V_{OUT\_PP(ESL)} \quad \text{(eq. 5)}$$

where VOUT_PP(C) is a ripple component by an equivalent total capacitance of the output capacitors, VOUT_PP(ESR) is a ripple component by an equivalent ESR of the output capacitors, and VOUT_PP(ESL) is a ripple component by an equivalent ESL of the output capacitors. In PWM operation mode, the three ripple components can be obtained by

$$V_{OUT\_PP(C)} = \frac{I_{L\_PP}}{8 \cdot C \cdot f_{SW}} \quad \text{(eq. 6)}$$

$$V_{OUT\_PP(ESR)} = I_{L\_PP} \cdot ESR \quad \text{(eq. 7)}$$

$$V_{OUT\_PP(ESL)} = \frac{ESL}{ESL + L} \cdot V_{IN} \quad \text{(eq. 8)}$$

and the peak−to−peak ripple current is

$$I_{L\_PP} = \frac{\left(V_{IN} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot L} \quad \text{(eq. 9)}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is VOUT_PP(C). So that the minimum output capacitance can be calculated regarding to a given output ripple requirement VOUT_PP in PWM operation mode.

$$C_{MIN} = \frac{I_{L\_PP}}{8 \cdot V_{OUT\_PP} \cdot f_{SW}} \quad \text{(eq. 10)}$$

Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance regarding to the input ripple voltage VIN_PP is

$$C_{IN\_MIN} = \frac{I_{OUT\_MAX} \cdot (D - D^2)}{V_{IN\_PP} \cdot f_{SW}} \quad \text{(eq. 11)}$$

where

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 12)}$$

In addition, the input capacitor needs to be able to absorb the input current, which has a RMS value of

$$I_{IN\_RMS} = I_{OUT\_MAX} \cdot \sqrt{D - D^2} \quad \text{(eq. 13)}$$

The input capacitor also needs to be sufficient to protect the device from over voltage spike, and normally at least a 4.7 μF capacitor is required. The input capacitor should be located as close as possible to the IC on PCB.

Table 3. LIST OF RECOMMENDED INPUT CAPACITORS AND OUTPUT CAPACITORS

Manufacturer	Part Number	Case Size	Height Max (mm)	C (μF)	Rated Voltage (V)	Structure
MURATA	GRM21BR60J226ME39, X5R	0805	1.4	22	6.3	MLCC
TDK	C2012X5R0J226M, X5R	0805	1.25	22	6.3	MLCC
MURATA	GRM21BR61A106KE19, X5R	0805	1.35	10	10	MLCC
TDK	C2012X5R1A106M, X5R	0805	1.25	10	10	MLCC
MURATA	GRM188R60J106ME47, X5R	0603	0.9	10	6.3	MLCC
TDK	C1608X5R0J106M, X5R	0603	0.8	10	6.3	MLCC
MURATA	GRM188R60J475KE19, X5R	0603	0.87	4.7	6.3	MLCC
Murata	GRM21BR70J106KE76, X7R	0805	1.4	10	6.3	MLCC
TDK	C2012X7R0J106K125AB, X7R	0805	1.45	10	6.3	MLCC
Murata	GRM21BR71A106KE51, X7R	0805	1.4	10	6.3	MLCC
TDK	C2012X7R1A106K125AC, X7R	0805	1.45	10	6.3	MLCC

Design of Feedback Network

The output voltage is programmed by an external resistor divider connected from V_{OUT} to FB and then to AGND, as shown in the typical application schematic Figure 1(a). The programmed output voltage is

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) \quad \text{(eq. 14)}$$

where V_{FB} is equal to the internal reference voltage 0.6 V, R1 is the resistance from V_{OUT} to FB, which has a normal value range from 50 kΩ to 1 MΩ and a typical value of 220 kΩ for applications with the typical output filter. R2 is the resistance from FB to AGND, which is used to program the output voltage according to equation (14) once the value of R1 has been selected. A capacitor Cfb needs to be employed between the V_{OUT} and FB in order to provide feedforward function to achieve optimum transient response. Normal value range of Cfb is from 0 to 100 pF, and a typical value is 15 pF for applications with the typical output filter and R1 = 220 kΩ.

Table 4 provides reference values of R1 and Cfb in case of different output filter combinations. The final design may need to be fine tuned regarding to application specifications.

Table 4. REFERENCE VALUES OF FEEDBACK NETWORKS (R1 AND CFB) FOR OUTPUT FILTER COMBINATIONS (L and C)

R1 (kΩ)		L (μH)					
Cfb (pF)		0.47	0.68	1	2.2	3.3	4.7
C (μF)	4.7	220	220	220	220	330	330
		3	5	8	15	15	22
	10	220	220	220	220	330	330
		8	10	15	27	27	39
	22	220	220	220	220	330	330
		15	22	27	39	47	56

LAYOUT CONSIDERATIONS

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Use wide and short traces for power paths (such as PVIN, VOUT, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW node should be a large copper pour, but compact because it is also a noise source.
- It would be good to have separated ground planes for PGND and AGND and connect the two planes at one point. Directly connect AGND pin to the exposed pad and then connect to AGND ground plane through vias. Try best to avoid overlap of input ground loop and output ground loop to prevent noise impact on output regulation.
- Arrange a “quiet” path for output voltage sense and feedback network, and make it surrounded by a ground plane.

Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pad must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and/or underneath the exposed pad to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

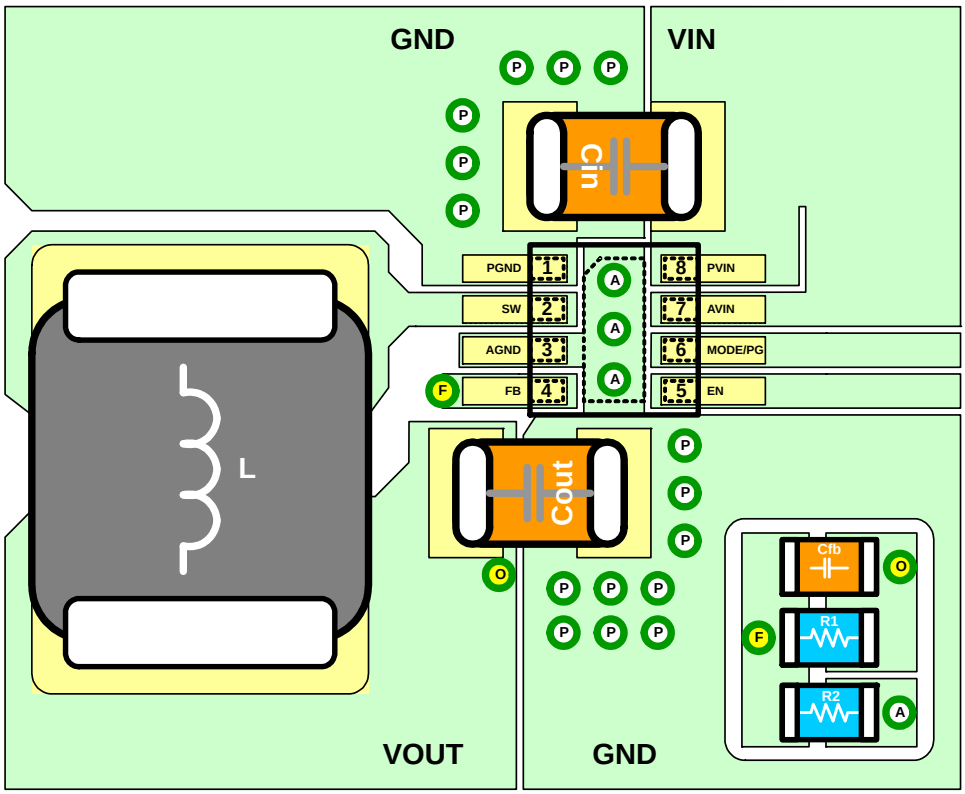
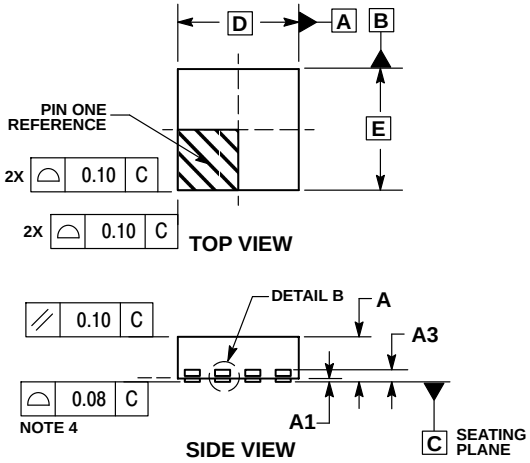
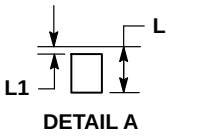


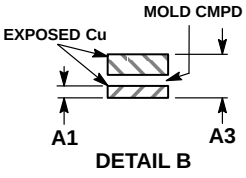
Figure 17. Recommended PCB Layout for Application Boards

PACKAGE DIMENSIONS

WDFN8 2x2, 0.5P
CASE 511BT
ISSUE O

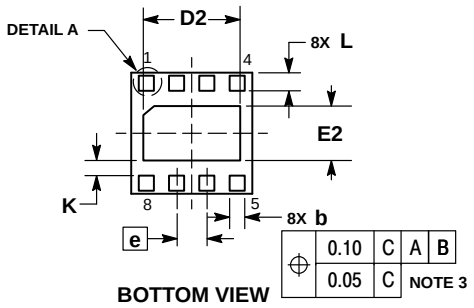




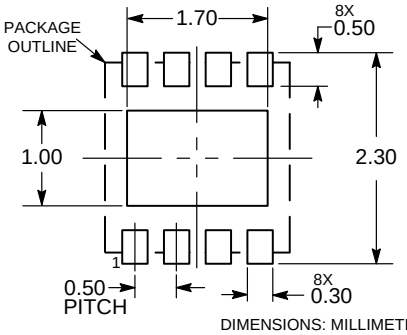


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
K	0.25 REF	
L	0.20	0.40
L1	−−−	0.15



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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