NXP Semiconductors
Technical Data

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RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 56 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 to 2200 MHz.

2100 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.6 Vdc, P_{out} = 56 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	16.4	52.0	7.7	–29.3
2140 MHz	16.6	51.7	7.6	–30.2
2170 MHz	16.7	50.7	7.3	–30.7
2200 MHz	16.5	49.6	7.2	–31.1

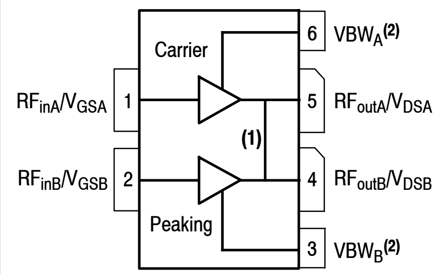
Features

- Advanced high performance in-package Doherty
- Designed for wide instantaneous bandwidth applications
- Greater negative gate-source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for digital predistortion error correction systems

A3T21H360W23SR6

2110–2200 MHz, 56 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR

ACP-1230S-4L2S



(Top View)

Figure 1. Pin Connections

1. Pin connections 4 and 5 are DC coupled and RF independent.
2. Device can operate with V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C when DC current is fed through pin 3 and pin 6 Derate above 25°C	CW	156 0.9	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 56 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.6 Vdc, 2155 MHz	$R_{\theta JC}$	0.21	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C3

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 120 μAdc)	$V_{GS(th)}$	1.4	1.8	2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 600 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.3	2.7	3.1	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.2 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 240 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.4 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Side A and Side B are tied together for these measurements.

(continued)

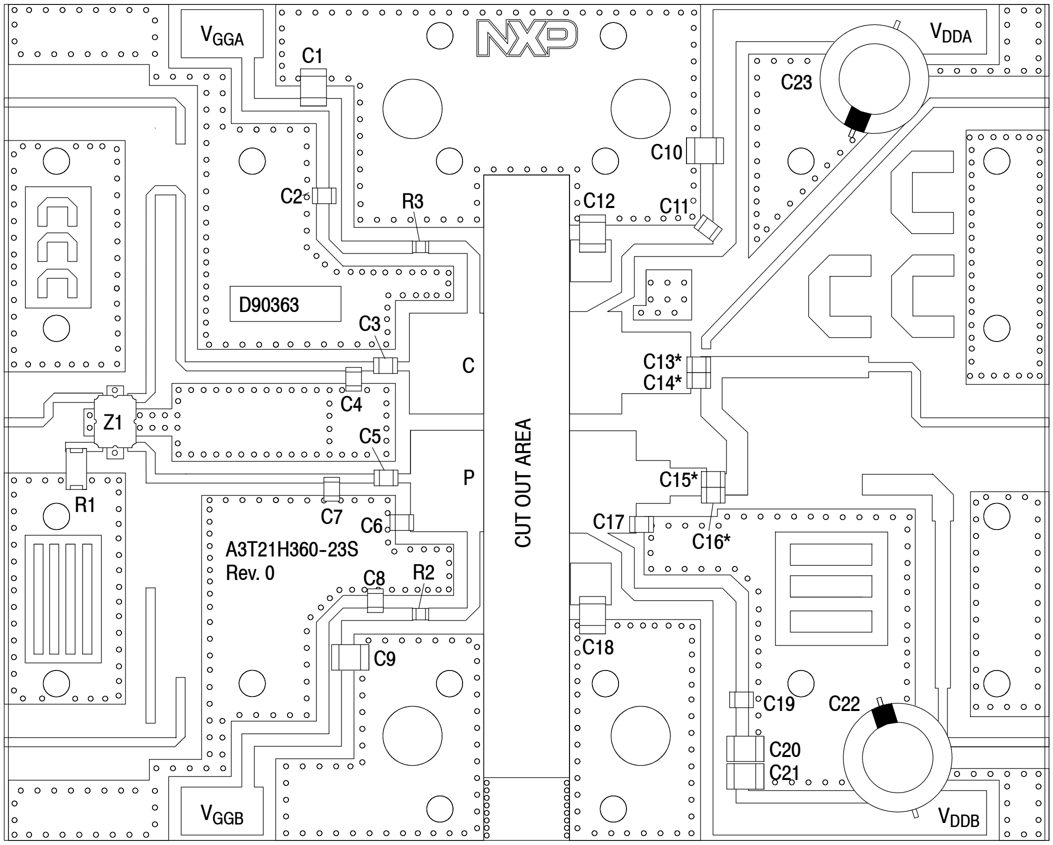
Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2,3] (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.6 Vdc, P_{out} = 56 W Avg., f = 2110 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	15.7	16.4	18.7	dB
Drain Efficiency	η_D	49.0	52.0	—	%
P_{out} @ 3 dB Compression Point, CW	P3dB	54.7	55.3	—	dBm
Adjacent Channel Power Ratio	ACPR	—	–29.3	–27.0	dBc
Load Mismatch [3] (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 600 mA, V_{GSB} = 0.6 Vdc, f = 2140 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 308 W Pulsed CW Output Power (3 dB Input Overdrive from 206 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance [3] (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.6 Vdc, 2110–2200 MHz Bandwidth					
P_{out} @ 3 dB Compression Point [4]	P3dB	—	348	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2200 MHz bandwidth)	Φ	—	–32	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	125	—	MHz
Gain Flatness in 90 MHz Bandwidth @ P_{out} = 56 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.005	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A3T21H360W23SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	ACP-1230S-4L2S

1. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurements made with device in an asymmetrical Doherty configuration.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



*C13, C14, C15, and C16 are mounted vertically.

Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. A3T21H360W23SR6 Test Circuit Component Layout

Table 6. A3T21H360W23SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C10, C12, C18, C20, C21	10 μF Chip Capacitor	GRM32ER61H106KA12L	Murata
C2, C8	9.1 pF Chip Capacitor	GQM2195C2E9R1BB12D	Murata
C3, C5	27 pF Chip Capacitor	ATC600F270JT250XT	ATC
C4, C17	0.8 pF Chip Capacitor	ATC600F0R8BT250XT	ATC
C6, C7	1 pF Chip Capacitor	ATC600F1R0BT250XT	ATC
C11, C19	12 pF Chip Capacitor	GQM2195C2E120FB12D	Murata
C13, C14	2.2 pF Chip Capacitor	GQM2195C2E2R2BB12D	Murata
C15, C16	2 pF Chip Capacitor	GQM2195C2E2R0BB12D	Murata
C22, C23	220 μF, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
R1	50 Ω, 4 W Termination Chip Resistor	ATCCW12010T0050GBK	ATC
R2, R3	2.2 Ω, 1/4 W Chip Resistor	CRCW12062R20JNEA	Vishay
Z1	2000-2300 MHz Band, 90°, 5 dB Directional Coupler	X3C21P1-05S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D90363	MTL

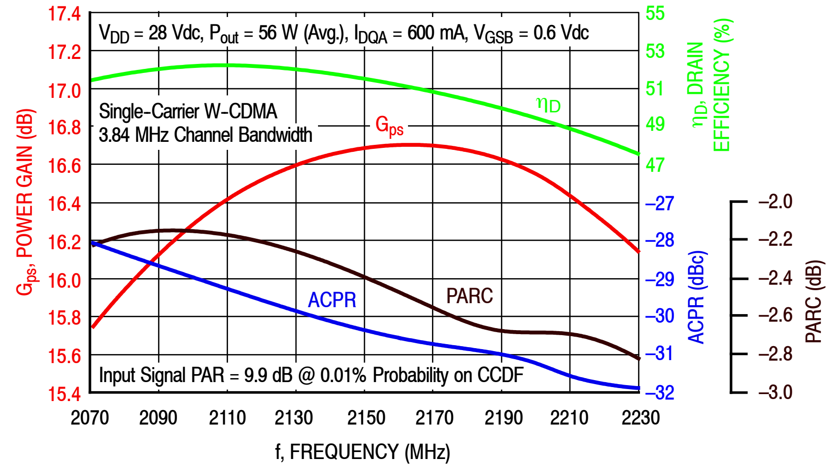


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 56 Watts Avg.

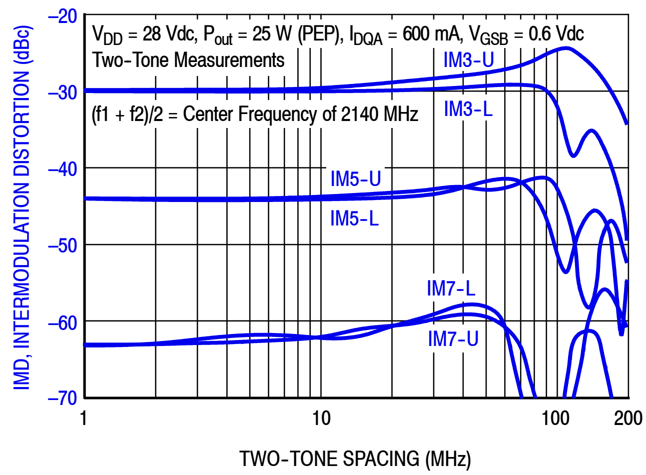


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

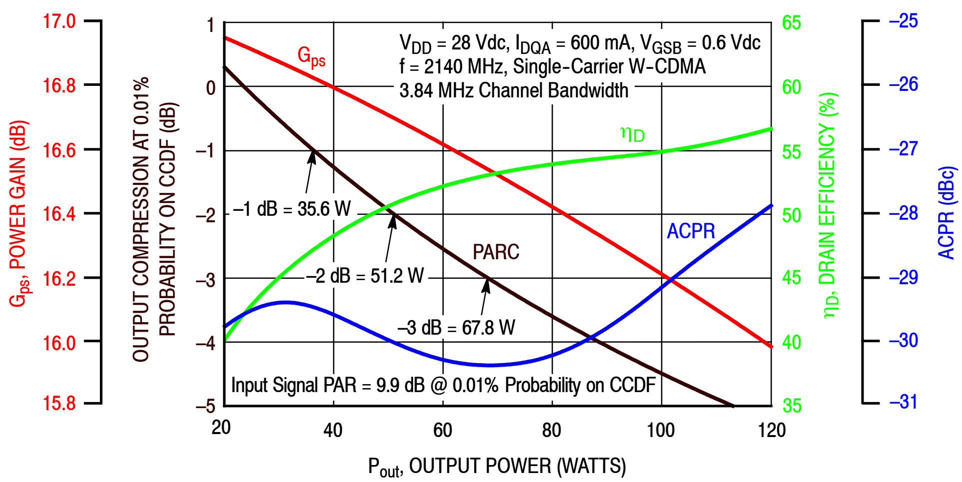


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

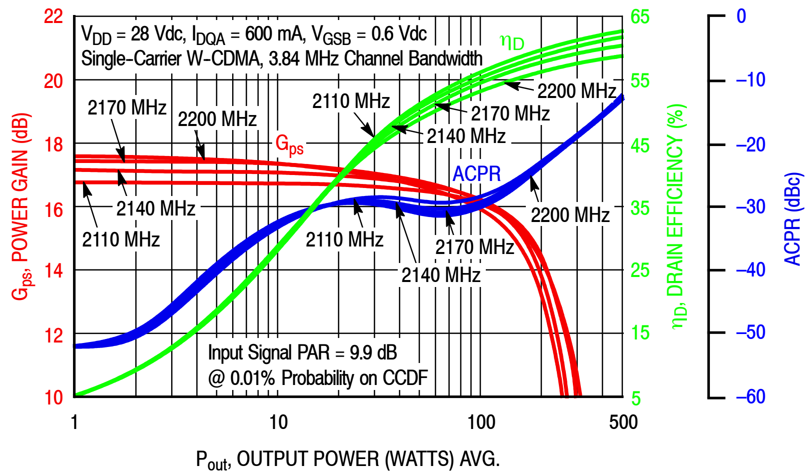


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

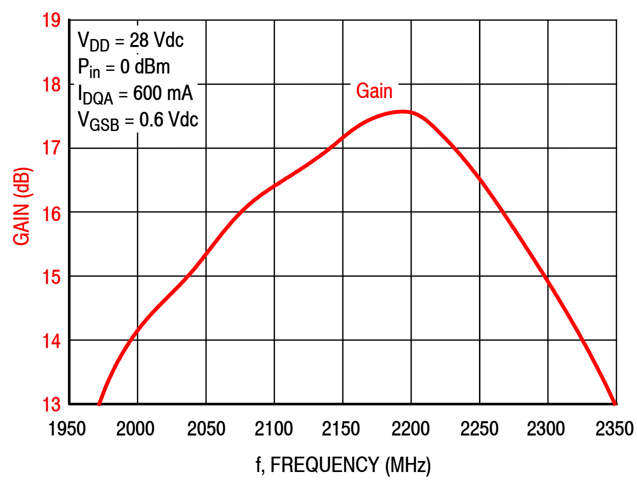


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 604 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.00 – j9.46	3.69 + j8.52	2.65 – j6.39	17.9	51.7	148	59.3	–13
2140	5.01 – j9.50	4.30 + j8.67	2.62 – j6.38	18.1	51.6	146	59.0	–13
2170	6.30 – j9.09	5.01 + j8.70	2.52 – j6.21	18.4	51.6	144	58.5	–15
2200	8.01 – j7.71	6.12 + j8.17	2.38 – j6.20	18.5	51.6	145	58.2	–13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.00 – j9.46	3.60 + j9.13	2.68 – j6.73	15.7	52.4	174	60.3	–18
2140	5.01 – j9.50	4.33 + j9.40	2.62 – j6.63	16.0	52.3	172	59.9	–18
2170	6.30 – j9.09	5.31 + j9.49	2.53 – j6.61	16.1	52.3	169	58.8	–19
2200	8.01 – j7.71	6.79 + j8.94	2.47 – j6.56	16.3	52.3	170	59.2	–18

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 604 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.00 – j9.46	3.57 + j8.75	4.75 – j3.46	20.8	49.7	94	71.0	–23
2140	5.01 – j9.50	4.21 + j8.90	4.49 – j3.31	21.1	49.5	90	70.0	–24
2170	6.30 – j9.09	5.00 + j8.90	4.14 – j3.68	21.1	49.7	94	69.0	–22
2200	8.01 – j7.71	6.22 + j8.35	3.82 – j3.57	21.3	49.6	91	69.0	–22

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.00 – j9.46	3.39 + j9.20	4.66 – j3.64	18.7	50.4	110	71.6	–30
2140	5.01 – j9.50	4.10 + j9.49	4.23 – j3.73	18.8	50.4	111	70.5	–30
2170	6.30 – j9.09	5.12 + j9.63	4.02 – j3.88	18.9	50.5	112	69.5	–29
2200	8.01 – j7.71	6.64 + j9.14	3.57 – j4.50	18.6	51.0	127	69.6	–26

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

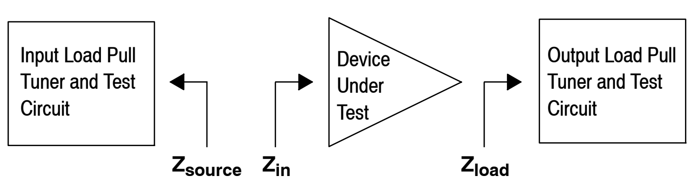


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.5 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.10 – j7.99	3.33 + j8.00	2.22 – j5.00	16.9	55.2	328	59.1	–30
2140	5.10 – j7.80	4.11 + j8.17	2.21 – j4.94	17.2	55.1	327	59.6	–31
2170	6.30 – j6.90	5.21 + j8.06	2.17 – j4.98	17.3	55.1	321	58.4	–32
2200	7.30 – j5.00	6.72 + j7.19	2.15 – j4.88	17.5	55.1	323	59.5	–31

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.10 – j7.99	3.65 + j8.53	2.19 – j5.39	14.6	55.8	381	58.7	–36
2140	5.10 – j7.80	4.67 + j8.73	2.25 – j5.25	15.0	55.8	380	60.1	–38
2170	6.30 – j6.90	6.15 + j8.47	2.20 – j5.20	15.1	55.7	374	59.2	–39
2200	7.30 – j5.00	8.03 + j7.02	2.24 – j5.17	15.3	55.7	374	59.9	–39

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

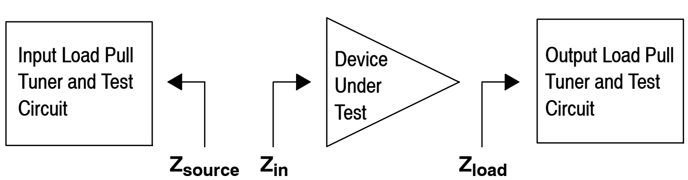
Table 10. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.5 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.10 – j7.99	3.08 + j7.95	4.17 – j3.64	18.3	53.9	244	68.3	–36
2140	5.10 – j7.80	3.75 + j8.13	4.08 – j3.16	18.7	53.6	230	68.8	–38
2170	6.30 – j6.90	4.71 + j8.12	3.79 – j2.66	18.9	53.3	213	69.1	–41
2200	7.30 – j5.00	6.12 + j7.45	3.39 – j2.70	19.0	53.4	217	69.4	–40

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.10 – j7.99	3.43 + j8.48	4.18 – j4.58	16.0	54.8	302	67.1	–41
2140	5.10 – j7.80	4.35 + j8.69	4.17 – j4.07	16.3	54.6	289	67.7	–43
2170	6.30 – j6.90	5.69 + j8.53	4.06 – j3.60	16.6	54.4	275	67.6	–46
2200	7.30 – j5.00	7.55 + j7.32	3.56 – j3.70	16.6	54.6	290	68.3	–44

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

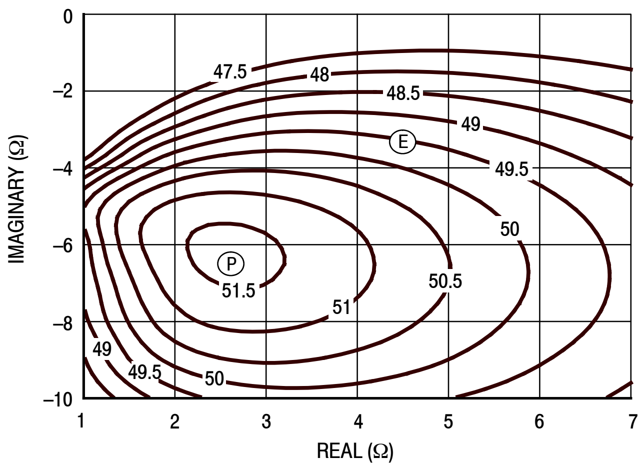


Figure 8. P1dB Load Pull Output Power Contours (dBm)

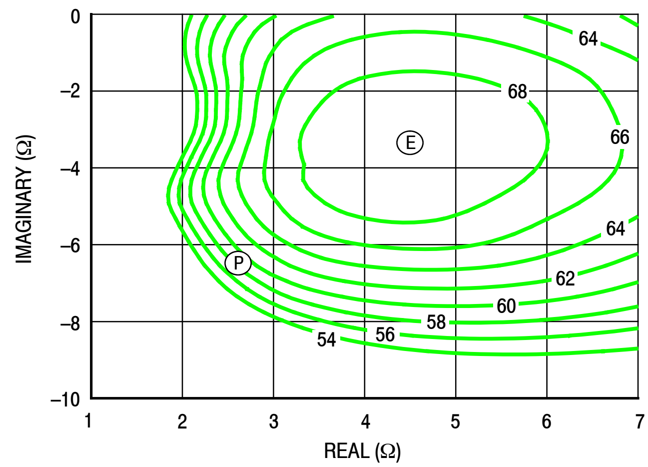


Figure 9. P1dB Load Pull Efficiency Contours (%)

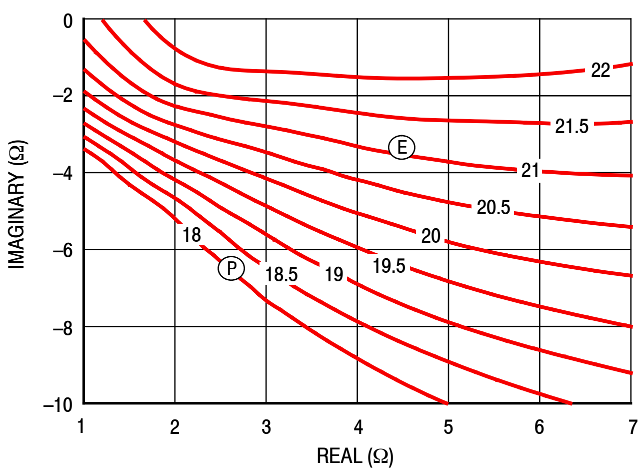


Figure 10. P1dB Load Pull Gain Contours (dB)

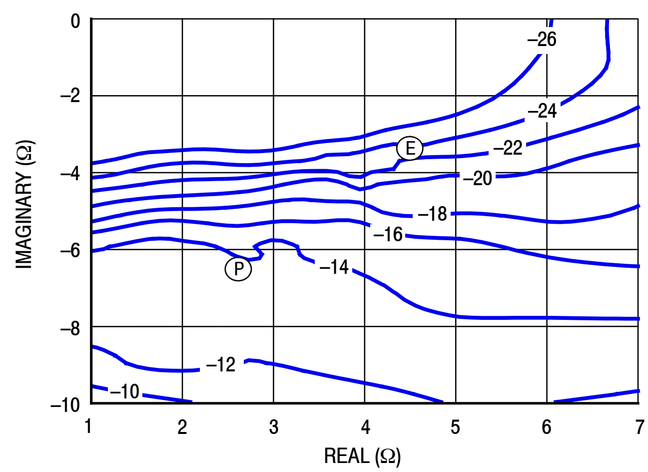


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power
E = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

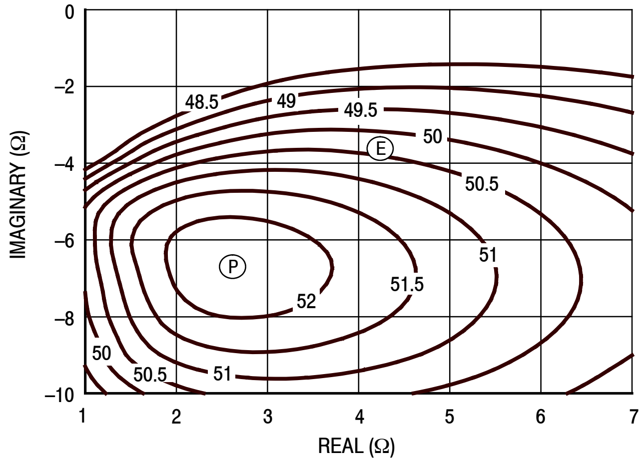


Figure 12. P3dB Load Pull Output Power Contours (dBm)

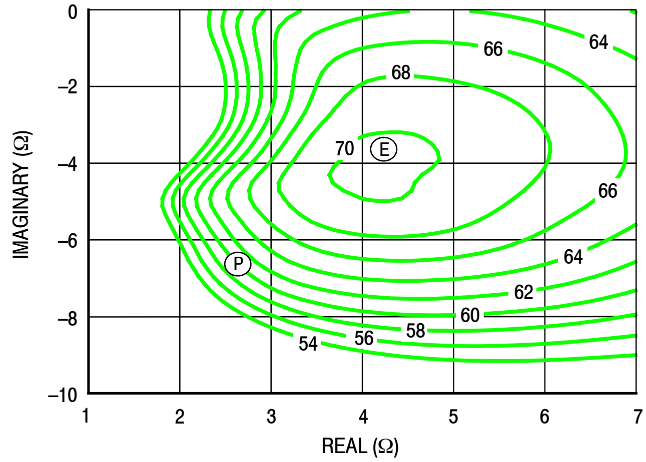


Figure 13. P3dB Load Pull Efficiency Contours (%)

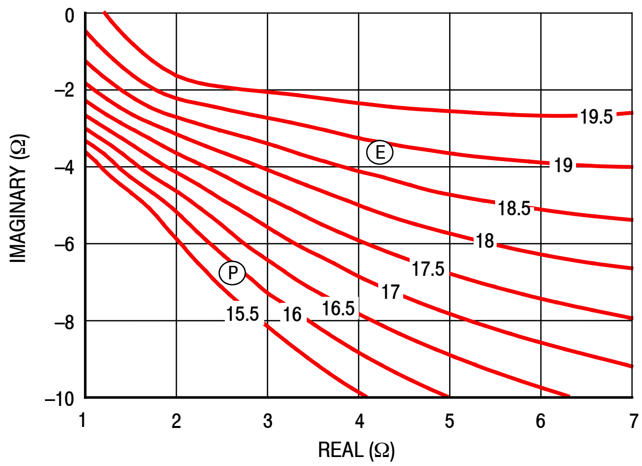


Figure 14. P3dB Load Pull Gain Contours (dB)

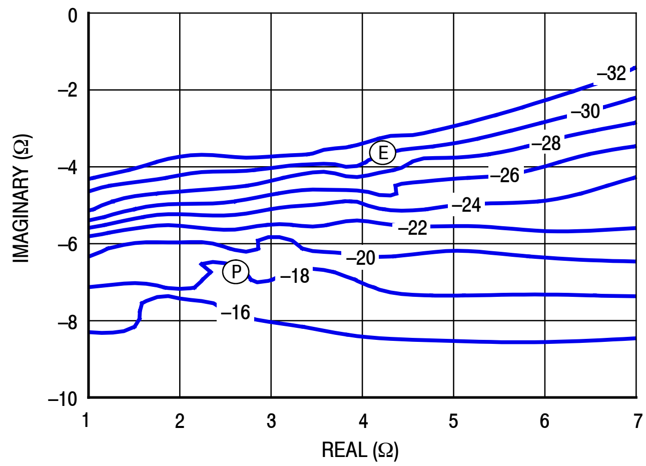


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

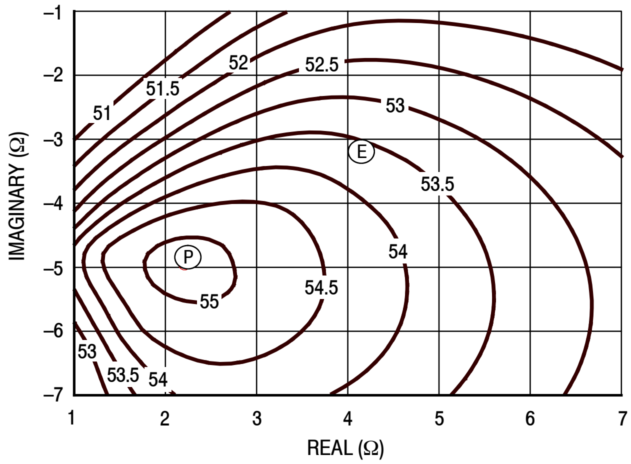


Figure 16. P1dB Load Pull Output Power Contours (dBm)

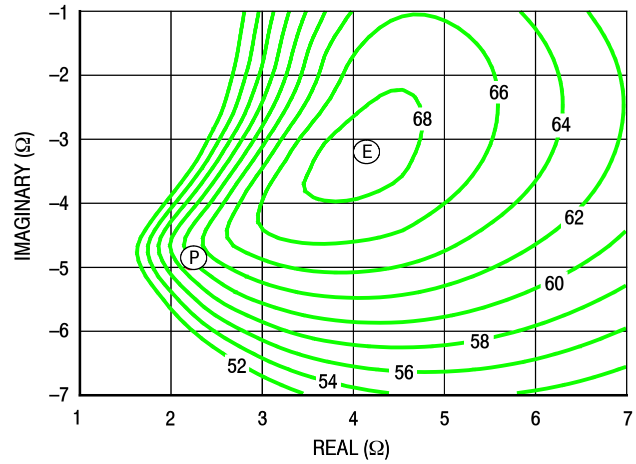


Figure 17. P1dB Load Pull Efficiency Contours (%)

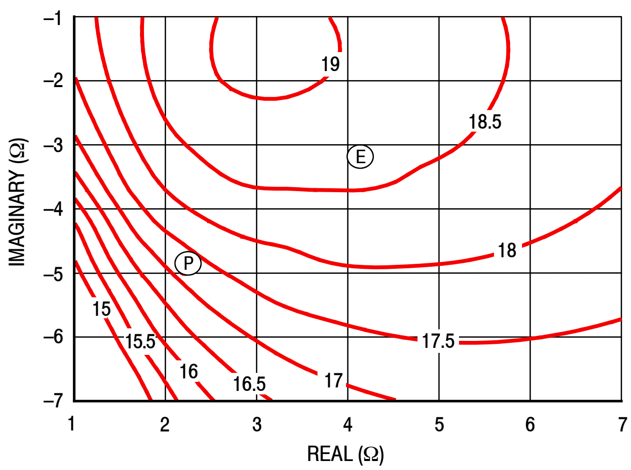


Figure 18. P1dB Load Pull Gain Contours (dB)

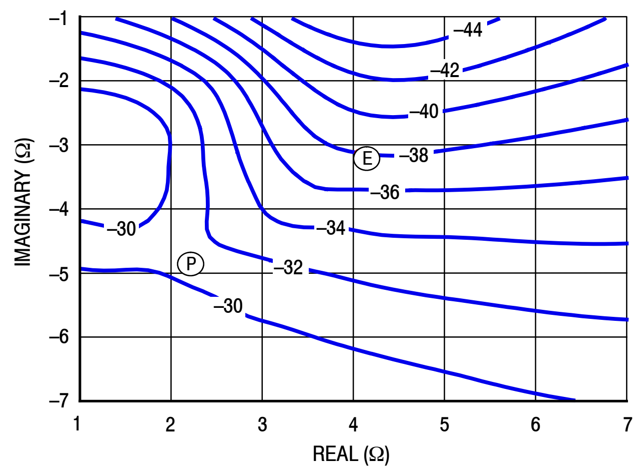


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power

E = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

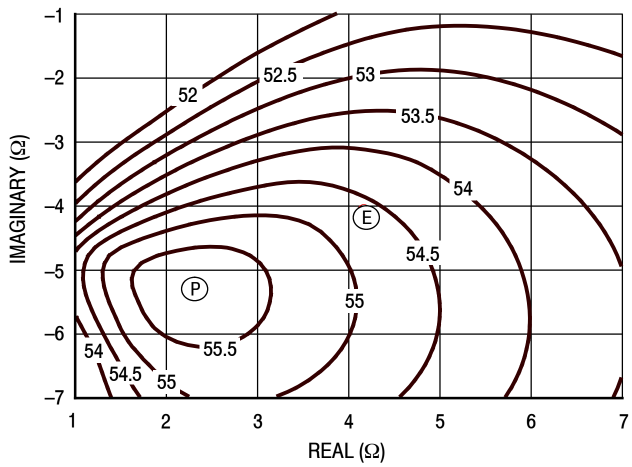


Figure 20. P3dB Load Pull Output Power Contours (dBm)

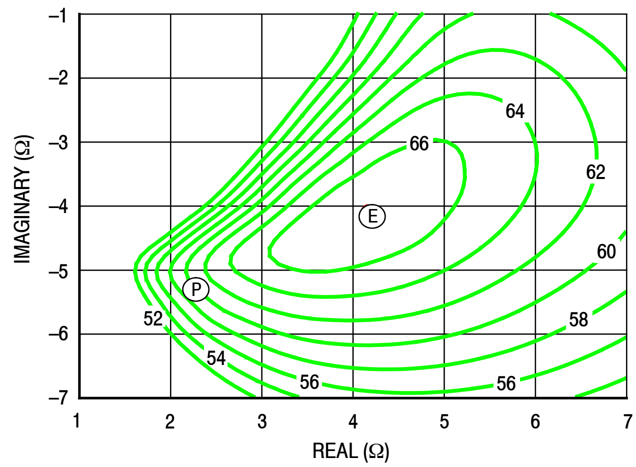


Figure 21. P3dB Load Pull Efficiency Contours (%)

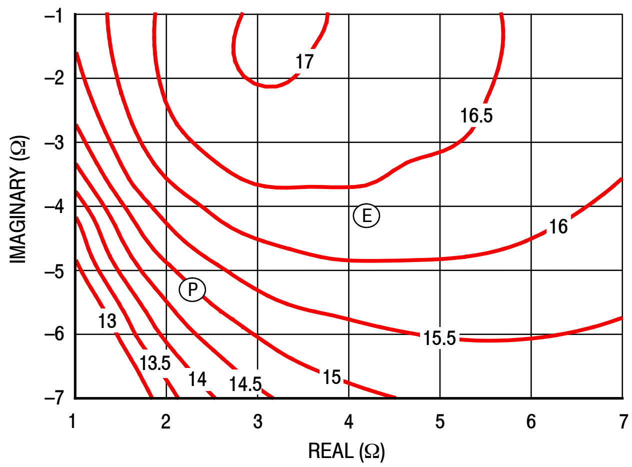


Figure 22. P3dB Load Pull Gain Contours (dB)

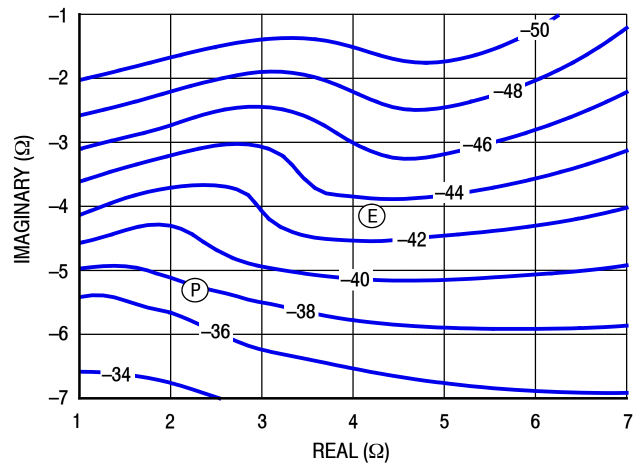


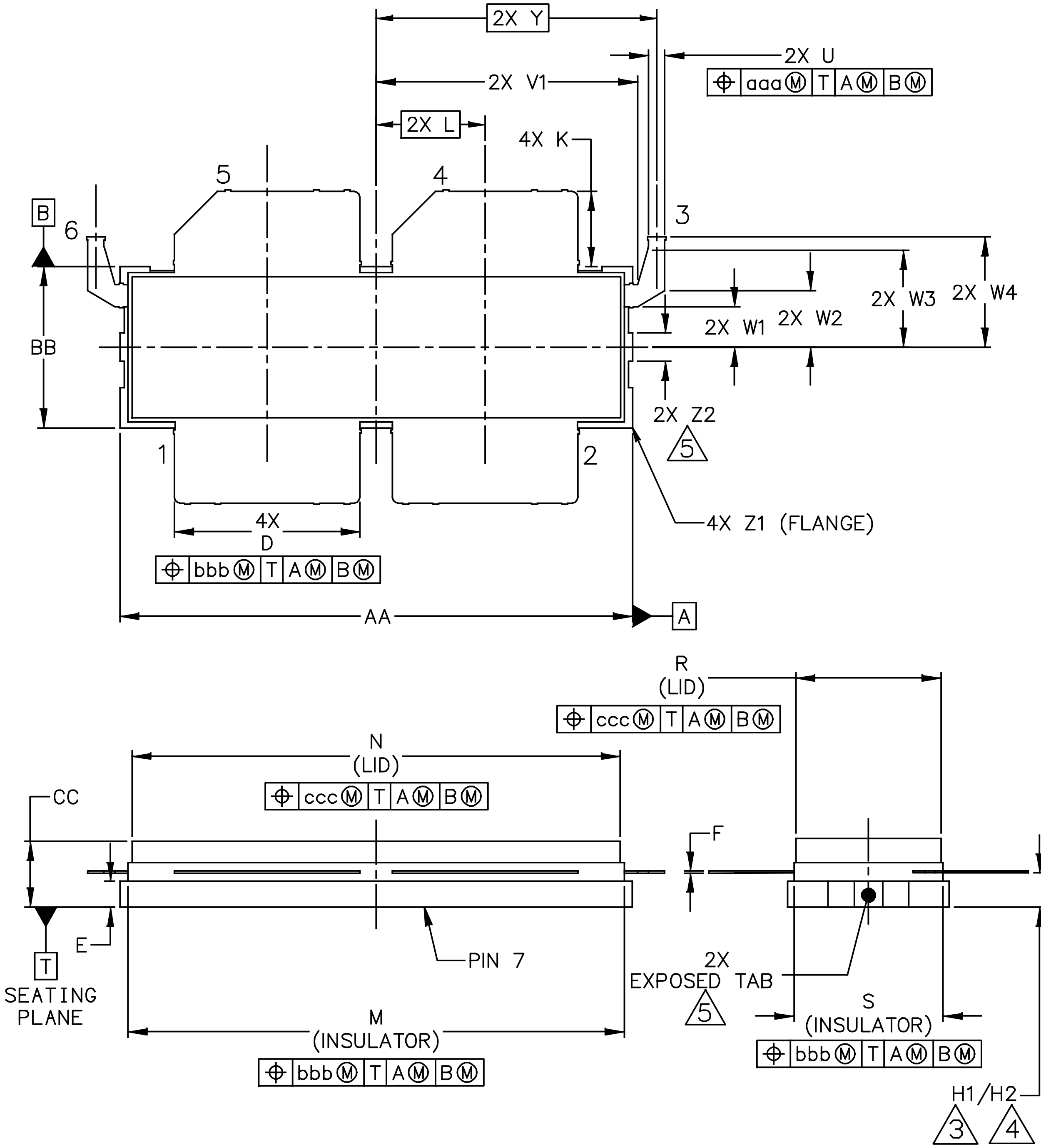
Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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	STANDARD: NON−JEDEC	
	SOT1800−4	21 JUN 2017

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

5. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

6. DATUM H IS LOCATED AT THE BOTTOM OF THE LEAD FRAME AND IS COINCIDENT WITH THE LEAD WHERE THE LEADS EXIT THE PLASTIC BODY.

7. DIMENSIONS M AND S DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .012 INCH (0.30 MM) PER SIDE. DIMENSIONS M AND S DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

8. DIMENSIONS D, U AND K DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .010 INCH (0.25 MM) TOTAL IN EXCESS OF THE D, U AND K DIMENSION AT MAXIMUM MATERIAL CONDITION.

9. DATUM A AND B TO BE DETERMINED AT DATUM T.

	INCHES		MILLIMETERS			INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	S	.365	.375	9.27	9.53
BB	.395	.405	10.03	10.29	U	.035	.045	0.89	1.14
CC	.160	.190	4.06	4.83	V1	.640	.655	16.26	16.64
D	.455	.465	11.56	11.81	W1	.105	.115	2.67	2.92
E	.062	.069	1.57	1.75	W2	.135	.145	3.43	3.68
F	.004	.007	0.10	0.18	W3	.245	.255	6.22	6.48
H1	.082	.090	2.08	2.29	W4	.265	.281	6.73	7.14
H2	.078	.094	1.98	2.39	Y	0.695 BSC		17.65 BSC	
K	.175	.195	4.45	4.95	Z1	R.000	R.040	R0.00	R1.02
L	0.270 BSC		6.86 BSC		Z2	.060	.100	1.52	2.54
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
N	1.218	1.242	30.94	31.55	bbb	.010		0.25	
R	.365	.375	9.27	9.53	ccc	.020		0.51	

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	SOT1800–4 21 JUN 2017

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2017	• Initial release of data sheet

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Rev. 0, 08/2017

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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