

FEATURES

Rail-to-rail input/output
Low power: 625 μ A typical
Gain bandwidth product: 15.9 MHz at $A_v = 100$ typical
Unity-gain crossover: 9.9 MHz typical
-3 dB closed-loop bandwidth: 13.9 MHz typical at ± 15 V
Low offset voltage: 100 μ V maximum (SOIC)
Unity-gain stable
High slew rate: 4.6 V/ μ s typical
Low noise: 3.9 nV/ $\sqrt{\text{Hz}}$ typical at 1 kHz

APPLICATIONS

Battery-powered instrumentation
Power supply control and protection
Telecommunications
DAC output amplifier
ADC input buffer

GENERAL DESCRIPTION

The [ADA4084-2](#) is a dual, single-supply, 10 MHz bandwidth amplifier featuring rail-to-rail inputs and outputs. It is guaranteed to operate from 3 V to 30 V (or ± 1.5 V to ± 15 V).

These amplifiers are well suited for single-supply applications requiring both ac and precision dc performance. The combination of wide bandwidth, low noise, and precision makes the [ADA4084-2](#) useful in a wide variety of applications, including filters and instrumentation.

Other applications for these amplifiers include portable telecommunications equipment, power supply control and protection, and use as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezoelectric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The [ADA4084-2](#) is specified over the industrial temperature range of -40°C to $+125^\circ\text{C}$. The dual [ADA4084-2](#) is available in the 8-lead SOIC, MSOP, and LFCSP surface-mount packages.

PIN CONFIGURATION



NOTES
 1. FOR THE LFSCSP PACKAGE THE EXPOSED PAD MUST BE CONNECTED TO V-.

Figure 1. 8-Lead MSOP (RM)
 8-Lead SOIC (R)
 8-Lead LFCSP (CP)

The [ADA4084-2](#) is a member of a growing series of high voltage, low noise op amps offered by Analog Devices, Inc., (see Table 1).

For a more complete selection table of low input voltage noise amplifiers, see the [AN-940](#) Application Note, *Low Noise Amplifier Selection Guide for Optimal Noise Performance*, available at www.analog.com.

Table 1. Low Noise Op Amps

Voltage Noise	Single	Dual	Quad
1.1 nV/Hz	AD8597	AD8599	
1.8 nV/Hz	ADA4004-1	ADA4004-2	ADA4004-4
2.8 nV/Hz RRO ¹	AD8675	AD8676	
2.8 nV/Hz	AD8671	AD8672	AD8674
3.2 nV/Hz	OP27/OP37		
3.9 nV/Hz RRIO ²		ADA4084-2	

¹ Rail-to-rail output.

² Rail-to-rail input/output.

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REVISION HISTORY

4/13—Rev. B to Rev. C

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Updated Outline Dimensions 25

6/12—Rev. A to Rev. B

Added LFCSP Package Universal

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2/12—Rev. 0 to Rev. A

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10/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_{SY} = 3\text{ V}$, $V_{CM} = 1.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package			100	μV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			200	μV
		MSOP package			130	μV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			250	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	LFCSP package			200	μV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			300	μV
Offset Voltage Matching		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.5	1.75	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	Channel A vs. Channel B, $T_A = 25^\circ\text{C}$			150	μV
Input Offset Current	I_{OS}			140	300	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			450	nA
Input Voltage Range	CMRR		0		3	V
		Common-Mode Rejection Ratio	$V_{CM} = 0\text{ V to } 3\text{ V}$	64	80	
Large Signal Voltage Gain	A_{VO}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	60			dB
		$R_L = 2\text{ k}\Omega$, $0.5\text{ V} \leq V_O \leq 2.5\text{ V}$	100	104		dB
Input Impedance, Differential		$R_L = 2\text{ k}\Omega$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	97			dB
				100 1.1		k Ω pF
Input Impedance, Common-Mode				80 2.9		M Ω pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$ to V_{CM}	2.85	2.95		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.8			V
		$R_L = 2\text{ k}\Omega$ to V_{CM}	2.8	2.9		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.7			V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to V_{CM}		10	20	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			40	mV
		$R_L = 2\text{ k}\Omega$ to V_{CM}			50	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			75	mV
Short-Circuit Current	I_{SC}			-17/+10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 1.25\text{ V to } \pm 1.75\text{ V}$	100	110		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	90			dB
Supply Current/Amplifier	I_{SY}	$I_O = 0\text{ mA}$		565	650	μA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			950	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$	2.0	2.6		V/ μs
Gain Bandwidth Product	GBP	$V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 100$		15.4		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$		8.08		MHz
Phase Margin	Φ_M			86		Degrees
-3 dB Closed-Loop Bandwidth	-3 dB	$A_V = 1$, $V_{IN} = 5\text{ mV p-p}$		12.3		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.14		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		3.9		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.55		pA/ $\sqrt{\text{Hz}}$

$V_{SY} = \pm 5.0\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			100	μV
		MSOP package $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			250	μV
		LFCSP package $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			130	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.5	300	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Matching		Channel A vs. Channel B, $T_A = 25^\circ\text{C}$			150	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		140	300	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			450	nA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-5		50	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 4\text{ V}$	106	124	+5	V
		$V_{CM} = \pm 5\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	76			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $-4\text{ V} \leq V_O \leq 4\text{ V}$	108	112		dB
		$R_L = 2\text{ k}\Omega$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	103			dB
Input Impedance, Differential				100 1.1		$\text{k}\Omega \text{pF}$
Input Impedance, Common-Mode				200 2.5		$\text{M}\Omega \text{pF}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$ to V_{CM} $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.9	4.95		V
		$R_L = 2\text{ k}\Omega$ to V_{CM} $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.8	4.85		V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to V_{CM} $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-4.95	-4.9	V
		$R_L = 2\text{ k}\Omega$ to V_{CM} $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-4.95	-4.8	V
Short Circuit Current	I_{SC}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-24/+17	-4.7	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 2\text{ V}$ to $\pm 18\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	120		dB
Supply Current/Amplifier	I_{SY}	$I_O = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105	595	700	dB
					1000	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ to V_{CM}	2.4	3.7		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP	$V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 100$		15.9		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$		9.6		MHz
Phase Margin	Φ_M			85		Degrees
-3 dB Closed-Loop Bandwidth	-3 dB	$A_V = 1$, $V_{IN} = 5\text{ mV p-p}$		13.9		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.14		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		3.9		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.55		$\text{pA}/\sqrt{\text{Hz}}$

$V_{SY} = \pm 15.0\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package			100	μV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			200	μV
		MSOP package			130	μV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			250	μV
		LFCSP package			200	μV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			300	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Channel A vs. Channel B, $T_A = 25^\circ\text{C}$		0.5	1.75	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Matching					150	μV
Input Bias Current	I_B			140	300	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			450	nA
Input Offset Current	I_{OS}				25	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			50	nA
Input Voltage Range			-15		+15	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 14\text{ V}$	106	124		dB
		$V_{CM} = \pm 15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	85			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $-13.5\text{ V} \leq V_O \leq +13.5\text{ V}$	110	117		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105			dB
Input Impedance, Differential				100 1.1		k Ω pF
Input Impedance, Common-Mode				200 2.5		M Ω pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$ to V_{CM}	14.8	14.9		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	14.8			V
		$R_L = 2\text{ k}\Omega$ to V_{CM}	14.5	14.6		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	14.0			V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to V_{CM}		-14.95	-14.9	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			-14.8	V
		$R_L = 2\text{ k}\Omega$ to V_{CM}		-14.9	-14.8	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			-14.7	V
Short Circuit Current	I_{SC}			± 30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 2\text{ V}$ to $\pm 18\text{ V}$	110	120		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105			dB
Supply Current/Amplifier	I_{SY}	$I_O = 0\text{ mA}$		625	750	μA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			1050	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$	2.4	4.6		V/ μs
Gain Bandwidth Product	GBP	$V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 100$		15.9		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 5\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$		9.9		MHz
Phase Margin	Φ_M			86		Degrees
-3 dB Closed-Loop Bandwidth	-3 dB	$A_V = 1$, $V_{IN} = 5\text{ mV p-p}$		13.9		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.1		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		3.9		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.55		pA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$V- \leq V_{IN} \leq V+$
Differential Input Voltage ¹	±0.6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

¹ For input differential voltages greater than 0.6 V, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	121	43	°C/W
8-Lead MSOP	142	45	°C/W
8-Lead LFCSP ¹	55	6	°C/W

¹ Numbers are based on 4-layer JEDEC thermal boards with the exposed pad soldered to the PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



Figure 2. Simplified Schematic

08237-002

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

$\pm 1.5\text{ V}$ CHARACTERISTICS



Figure 3. Input Offset Voltage Distribution, SOIC



Figure 6. TCV_{OS} Distribution, SOIC and MSOP



Figure 4. Input Offset Voltage Distribution, MSOP



Figure 7. TCV_{OS} Distribution, LFCSP



Figure 5. Input Offset Voltage Distribution, LFCSP



Figure 8. Input Offset Voltage vs. Common-Mode Voltage



Figure 9. Input Bias Current vs. Temperature

08237-007

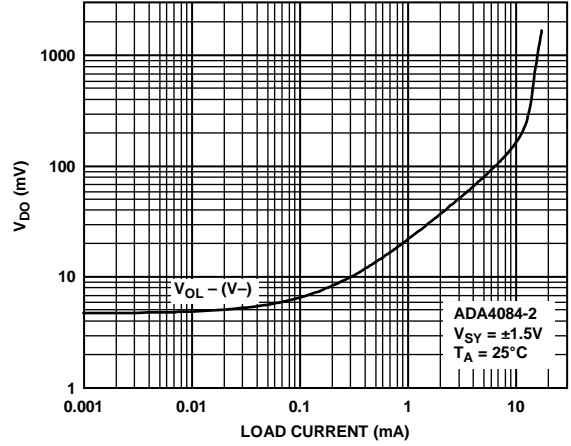


Figure 12. Dropout Voltage vs. Sink Current

08237-010

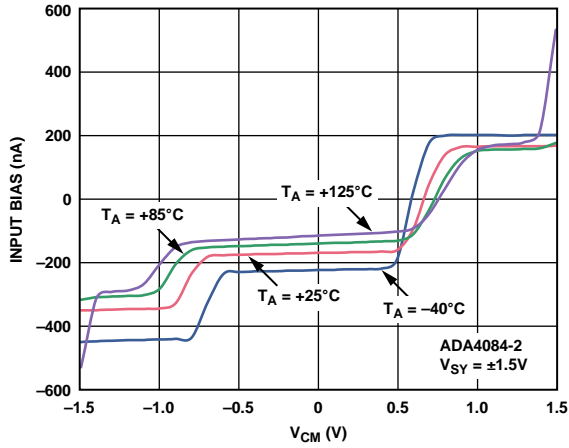


Figure 10. Input Bias Current vs. V_{CM} and Temperature

08237-008



Figure 13. Open-Loop Gain and Phase vs. Frequency

08237-011

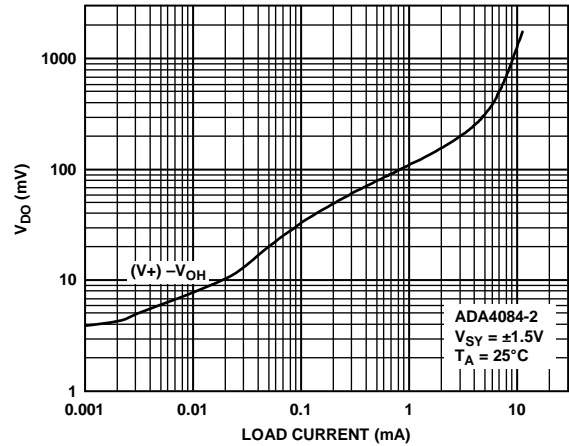


Figure 11. Dropout Voltage vs. Source Current

08237-009



Figure 14. Closed-Loop Gain vs. Frequency

08237-012



Figure 15. Output Impedance vs. Frequency

08237-013



Figure 18. Large Signal Transient Response

08237-016



Figure 16. PSRR vs. Frequency

08237-014



Figure 19. Small Signal Transient Response

08237-017



Figure 17. CMRR vs. Frequency

08237-015

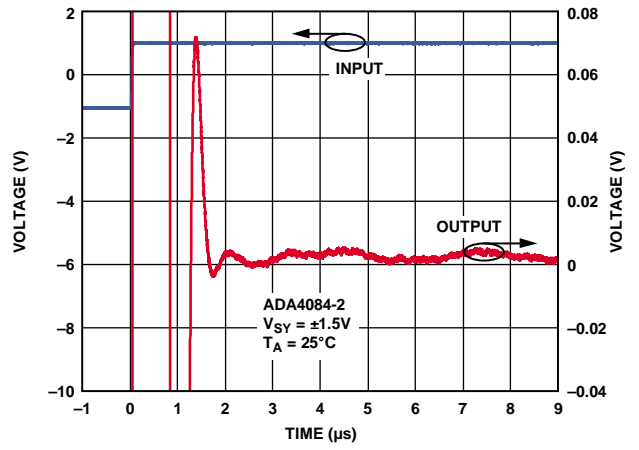


Figure 20. Settling Time

08237-018



Figure 21. Voltage Noise Density

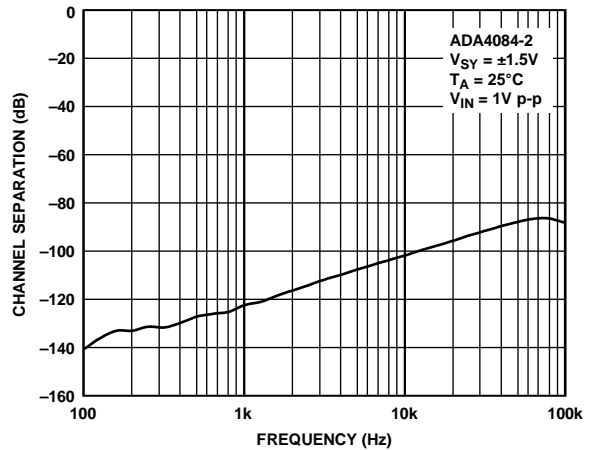


Figure 24. Channel Separation



Figure 22. Overshoot vs. Capacitance



Figure 25. THD + N vs. Amplitude



Figure 23. Voltage Noise 0.1 Hz to 10 Hz



Figure 26. THD + N vs. Frequency



Figure 27. No Phase Reversal

±5 V CHARACTERISTICS



Figure 28. Input Offset Voltage Distribution SOIC

08237-026



Figure 31. TCV_{os} Distribution, SOIC and MSOP

08237-028



Figure 29. Input Offset Voltage Distribution MSOP

08237-027



Figure 32. TCV_{os} Distribution, LFCSP

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Figure 30. Input Offset Voltage Distribution, LFCSP

08237-080



Figure 33. Input Offset Voltage vs. Common-Mode Voltage

08237-029



Figure 34. Input Bias Current vs. Temperature

08237-030



Figure 37. Dropout Voltage vs. Sink Current

08237-033



Figure 35. Input Bias Current vs. V_{CM} and Temperature

08237-031

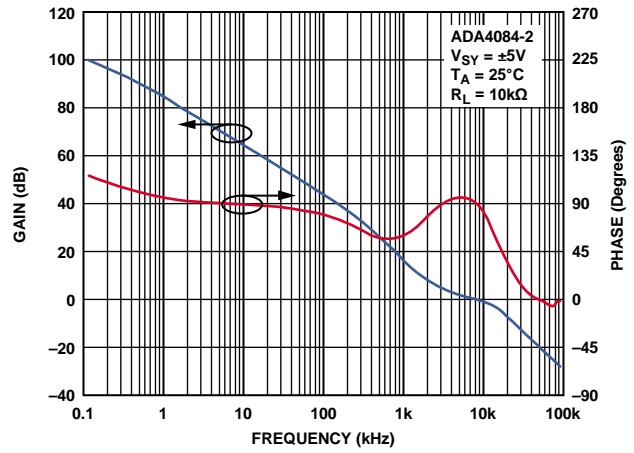


Figure 38. Open-Loop Gain and Phase vs. Frequency

08237-034



Figure 36. Dropout Voltage vs. Source Current

08237-032

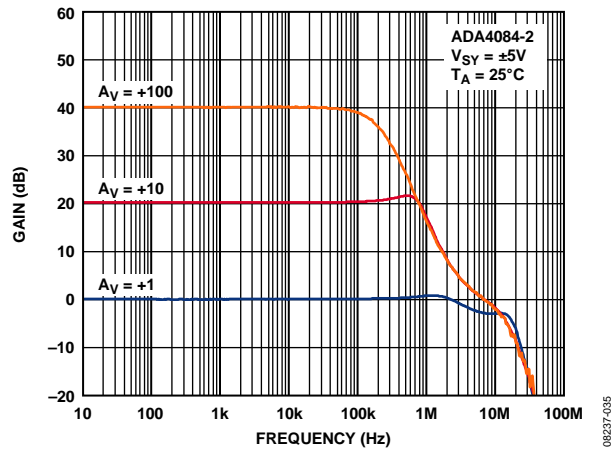


Figure 39. Closed-Loop Gain vs. Frequency

08237-035

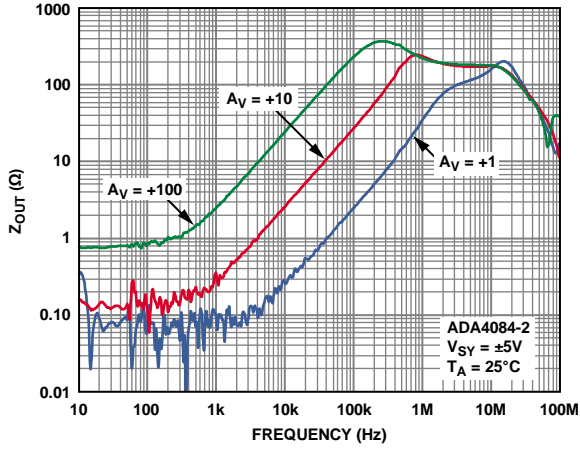


Figure 40. Output Impedance vs. Frequency



Figure 43. Large Signal Transient Response

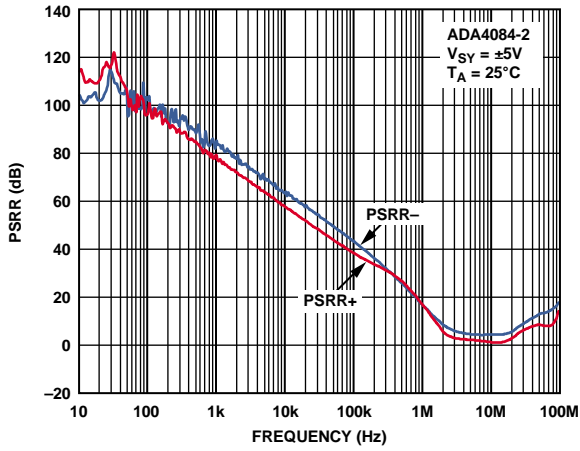


Figure 41. PSRR vs. Frequency



Figure 44. Small Signal Transient Response

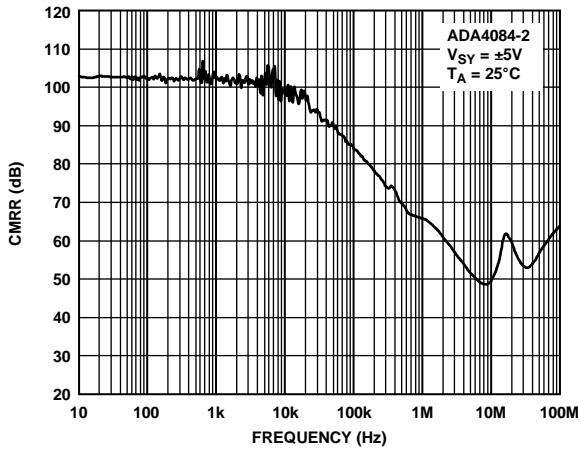


Figure 42. CMRR vs. Frequency



Figure 45. Settling Time

08237-038

08237-039

08237-037

08237-040

08237-038

08237-041



Figure 46. Voltage Noise Density

08237-042



Figure 49. Channel Separation

08237-045



Figure 47. Overshoot vs. Load Capacitance

08237-043



Figure 50. THD + N vs. Amplitude

08237-046

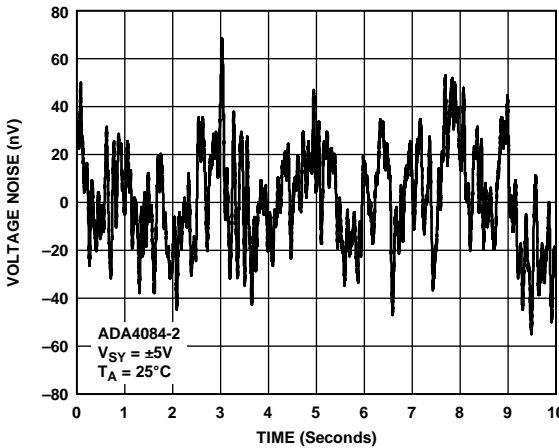


Figure 48. Voltage Noise 0.1 Hz to 10 Hz

08237-044



Figure 51. THD + N vs. Frequency

08237-047



Figure 52. No Phase Reversal

±15 V CHARACTERISTICS



Figure 53. Input Offset Voltage Distribution, SOIC

08237-049



Figure 56. TCVos Distribution, SOIC and MSOP

08237-051

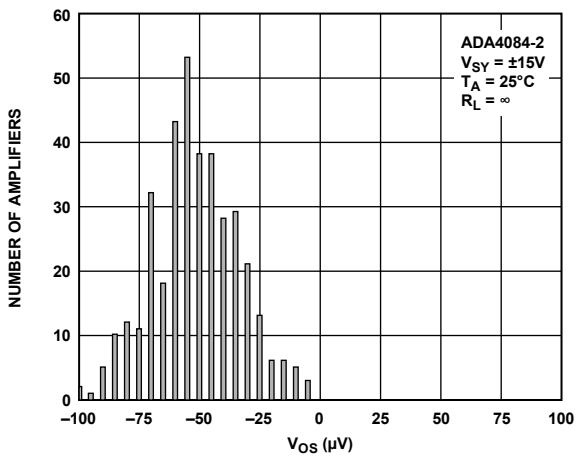


Figure 54. Input Offset Voltage Distribution, MSOP

08237-050



Figure 57. TCVos Distribution, LFCSP

08237-055



Figure 55. Input Offset Voltage Distribution, LFCSP

08237-079



Figure 58. Input Offset Voltage vs. Common-Mode Voltage

08237-052



Figure 59. Input Bias Current vs. Temperature

08237-053



Figure 62. Dropout Voltage vs. Sink Current

08237-056



Figure 60. Input Bias Current vs. V_{CM} and Temperature

08237-054



Figure 63. Open-Loop Gain and Phase vs. Frequency

08237-057

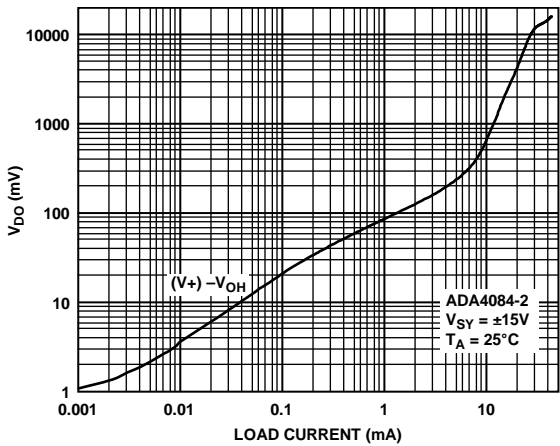


Figure 61. Dropout Voltage vs. Source Current

08237-055



Figure 64. Closed-Loop Gain vs. Frequency

08237-058



Figure 65. Output Impedance vs. Frequency

08237-059



Figure 68. Large Signal Transient Response

08237-062



Figure 66. PSRR vs. Frequency

08237-060

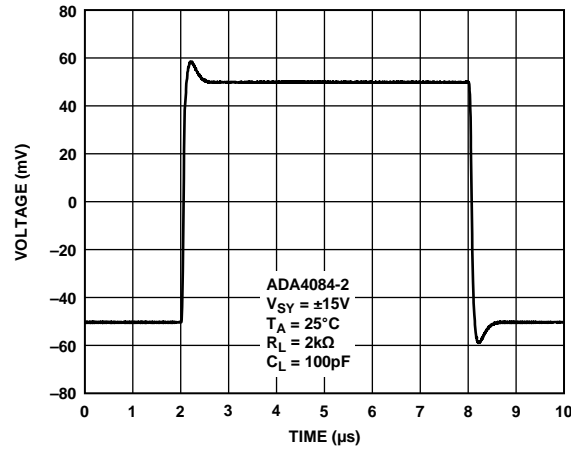


Figure 69. Small Signal Transient Response

08237-063



Figure 67. CMRR vs. Frequency

08237-061



Figure 70. Settling Time

08237-064

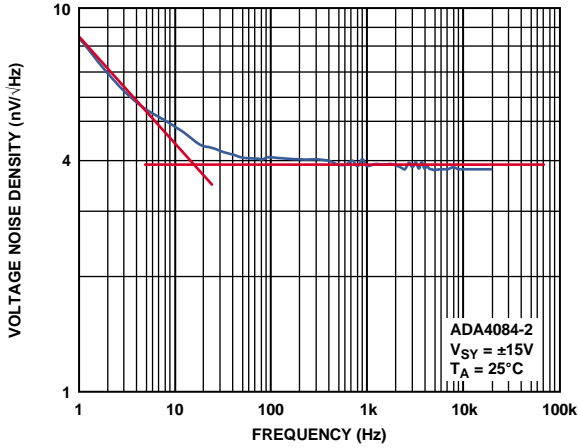


Figure 71. Voltage Noise Density

08237-065

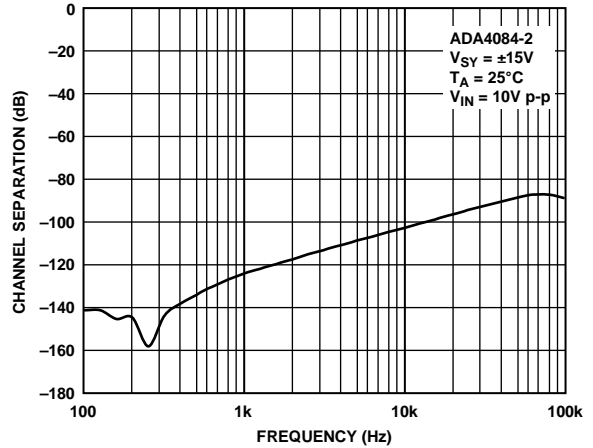


Figure 74. Channel Separation

08237-066

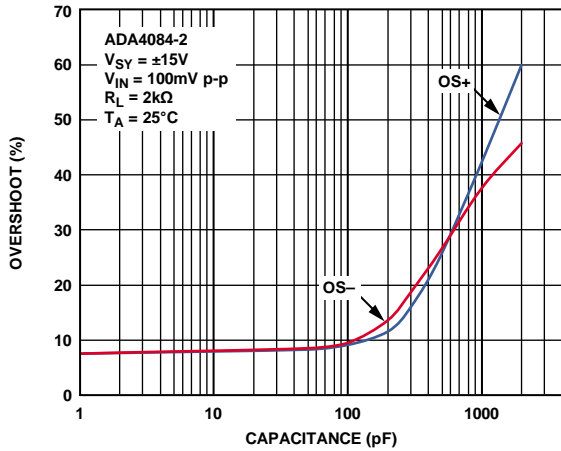


Figure 72. Overshoot vs. Load Capacitance

08237-066

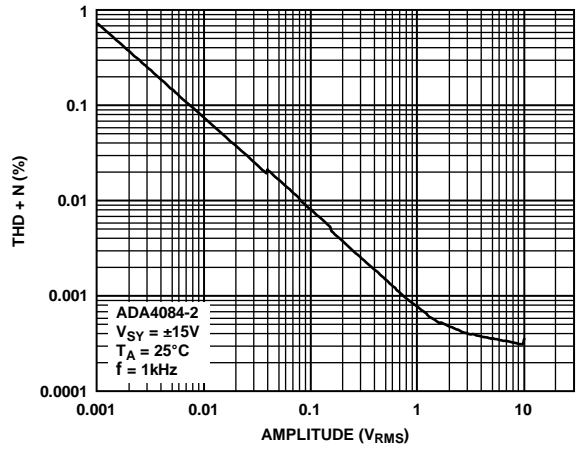


Figure 75. THD + N vs. Amplitude

08237-069

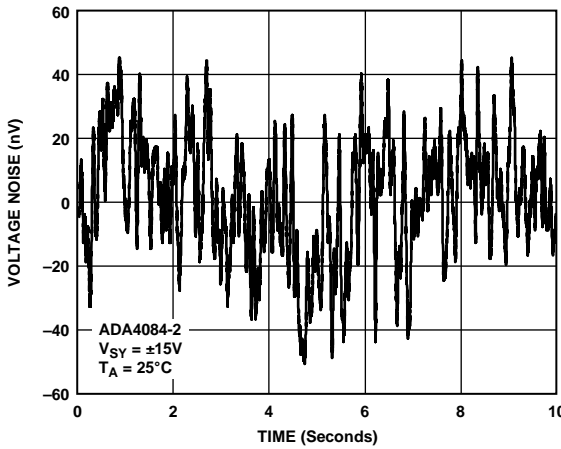


Figure 73. Voltage Noise 0.1 Hz to 10 Hz

08237-067

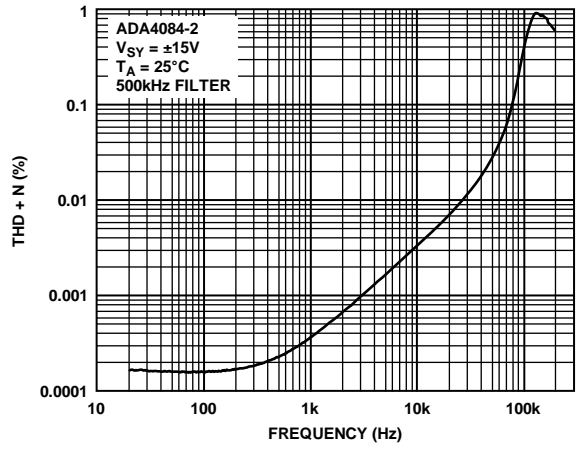


Figure 76. THD + N vs. Frequency

08237-070



Figure 77. No Phase Reversal

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The ADA4084-2 is a precision single-supply, rail-to-rail operational amplifier. Intended for portable instrumentation, the ADA4084-2 combines the attributes of precision, wide bandwidth, and low noise to make it an ideal choice in single-supply applications that require both ac and precision dc performance. Other low supply voltage applications for which the ADA4084-2 is well suited are active filters, audio microphone preamplifiers, power supply control, and telecommunications. To combine all of these attributes with rail-to-rail input/output operation, novel circuit design techniques are used.



Figure 78. ADA4084-2 Equivalent Input Circuit

For example, Figure 78 illustrates a simplified equivalent circuit for the input stage of the ADA4084-2. It comprises a PNP differential pair, Q1 and Q2, and an NPN differential pair, Q3 and Q4, operating concurrently. Diode D100 and Diode D101 serve to clamp the applied differential input voltage to the ADA4084-2, thereby protecting the input transistors against Zener breakdown of the emitter-base junctions. Input stage voltage gains are kept low for input rail-to-rail operation. The two pairs of differential output voltages are connected to the second stage of the ADA4084-2, which is a modified compound folded cascade gain stage. It is also in the second gain stage, where the two pairs of differential output voltages are combined into a single-ended output signal voltage used to drive the output stage.

A key issue in the input stage is the behavior of the input bias currents over the input common-mode voltage range. Input bias currents in the ADA4084-2 are the arithmetic sum of the base currents in Q1 and Q4 and in Q2 and Q3. As a result of this design approach, the input bias currents in the ADA4084-2 not only exhibit different amplitudes; they also exhibit different polarities. This effect is best illustrated by Figure 9, Figure 10, Figure 34, Figure 35, Figure 59, and Figure 60. It is therefore important that the effective source impedances connected to the ADA4084-2 inputs be balanced for optimum dc and ac performance.

To achieve rail-to-rail output, the ADA4084-2 output stage design employs a unique topology for both sourcing and sinking current. This circuit topology is illustrated in Figure 79. The output stage is voltage-driven from the second gain stage. The signal path through the output stage is inverting; that is, for positive input signals, Q13 provides the base current drive to Q19 so that it conducts (sinks) current. For negative input signals, the signal path via Q18 → mirror → Q24 provides the base current drive for Q23 to conduct (source) current. Both transistors provide output current until they are forced into saturation.



Figure 79. ADA4084-2 Equivalent Output Circuit

Thus, the saturation voltage of the output transistors sets the limit on the ADA4084-2 maximum output voltage swing. Output short-circuit current limiting is determined by the maximum signal current into the base of Q13 from the second gain stage. The output stage also exhibits voltage gain. This is accomplished by the use of common-emitter amplifiers, and, as a result, the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a dependence on the total load resistance at the output of the ADA4084-2.

STARTUP CHARACTERISTICS

The ADA4084-2 is specified to operate from 3 V to 30 V (± 1.5 V to ± 15 V) under nominal power supplies. During power up as the supply voltage increases from 0 V to the nominal power supply voltage, the supply current (I_{SY}) increases as well to the point at which it stabilizes and the amplifier is ready to operate. The stabilization varies with temperature, as shown in Figure 80, below such that at -40°C it takes a higher voltage and stabilizes at a lower supply current than at hot temperatures where it takes a lower voltage but stabilizes at a higher current. In all cases, the ADA4084-2 is specified to start up and operate at a minimum of 3 V under all temperature conditions.

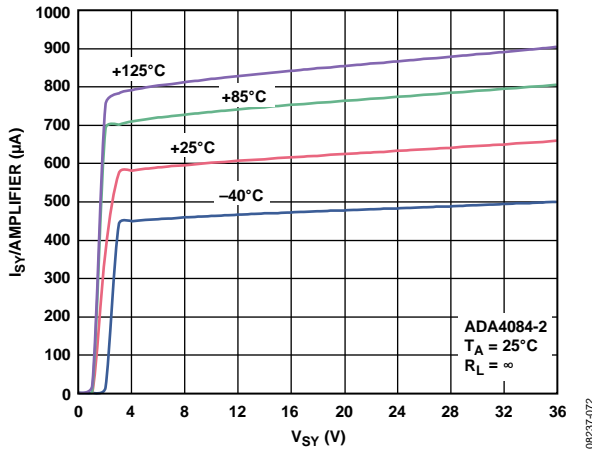


Figure 80. Supply Current vs. Supply Voltage

INPUT PROTECTION

As with any semiconductor device, if conditions exist where the applied input voltages to the device exceed either supply voltage, the input overvoltage I-to-V characteristic of the device must be considered. When an overvoltage occurs, the amplifier may be damaged, depending on the magnitude of the applied voltage and the magnitude of the fault current.

The D1, D2, D4, and D5 diodes conduct when the input common-mode voltage exceeds either supply pin by a diode drop. This varies with temperature and is in the range of 0.3 V to 0.8 V. As illustrated in the simplified equivalent circuit shown in Figure 78, the ADA4084-2 does not have any internal current limiting resistors; thus, fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device, provided that it is limited to 5 mA or less. If a fault condition causes more than 5 mA to flow, an external series resistor should be added at the expense of additional thermal noise. Figure 81 illustrates a typical noninverting configuration for an overvoltage-protected amplifier where the series resistance, R_s , is chosen, such that

$$R_s = \frac{V_{IN(MAX)} - V_{SUPPLY}}{5 \text{ mA}}$$

For example, a 1 k Ω resistor protects the ADA4084-2 against input signals up to 5 V above and below the supplies. Note that the thermal noise of a 1 k Ω resistor at room temperature is 4 nV/ $\sqrt{\text{Hz}}$, which exceeds the voltage noise of the ADA4084-2. For other configurations where both inputs are used, each input should be protected against abuse with a series resistor. Again, to ensure optimum dc and ac performance, it is recommended that source impedance levels be balanced.

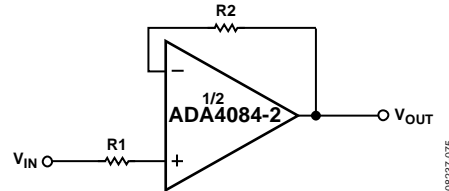


Figure 81. Resistance in Series with Input Limits Overvoltage Currents to Safe Values

To protect Q1-Q2 and Q3-Q4 from large differential voltages that may result in Zener breakdown of the emitter-base junction, D100 and D101 are connected between the two inputs. This precludes operation as a comparator. For a more complete description, see the MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*; the MT-083 Tutorial, *Comparators*, the MT-084 Tutorial, *Using Op Amps As Comparators*; and the AN-849 Application Note, *Using Op Amps as Comparators*, at www.analog.com.

OUTPUT PHASE REVERSAL

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically, for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes, with the anode connected to ground and the cathode to the inputs, prevent input signal excursions from exceeding the negative supply of the device (that is, GND), preventing a condition that causes the output voltage to change phase. JFET input amplifiers can also exhibit phase reversal, and, if so, a series input resistor is usually required to prevent it.

The ADA4084-2 is free from reasonable input voltage range restrictions, provided that input voltages no greater than the supply voltages are applied (see Figure 27, Figure 52, and Figure 77).

Although device output does not change phase, large currents can flow through the input protection diodes. Therefore, the technique recommended in the Input Protection section should be applied to those applications where the likelihood of input voltages exceeding the supply voltages is high.

DESIGNING LOW NOISE CIRCUITS IN SINGLE-SUPPLY APPLICATIONS

In single-supply applications, devices like the ADA4084-2 extend the dynamic range of the application through the use of rail-to-rail operation. Referring to the op amp noise model circuit configuration illustrated in Figure 82, the expression for an amplifier's total equivalent input noise voltage for a source resistance level, R_s , is given by

$$e_{nT} = \sqrt{2[(e_{nR})^2 + (i_{nOA} \times R_s)^2] + (e_{nOA})^2}, \text{ units in } \frac{V}{\sqrt{Hz}}$$

where:

- $R_s = 2R$, the effective, or equivalent, circuit source resistance.
- $(e_{nR})^2$ is the source resistance thermal noise voltage power ($4kTR$).
- k is the Boltzmann's constant, 1.38×10^{-23} J/K.
- T is the ambient temperature in Kelvin of the circuit, $273.15 + T_A$ ($^{\circ}C$).
- $(i_{nOA})^2$ is the op amp equivalent input noise current spectral power (1 Hz bandwidth).
- $(e_{nOA})^2$ is the op amp equivalent input noise voltage spectral power (1 Hz bandwidth).



Figure 82. Op Amp Noise Circuit Model Used to Determine Total Circuit Equivalent Input Noise Voltage and Noise Figure

As a design aid, Figure 83 shows the total equivalent input noise of the ADA4084-2 and the total thermal noise of a resistor for comparison. Note that for source resistance less than 1 k Ω , the equivalent input noise voltage of the ADA4084-2 is dominant.



Figure 83. ADA4084-2 Equivalent Thermal Noise vs. Total Source Resistance

Because circuit SNR is the critical parameter in the final analysis, the noise behavior of a circuit is sometimes expressed in terms of its noise figure, NF. The noise figure is defined as the ratio of a circuit's output signal-to-noise to its input signal-to-noise.

Noise figure is generally used for RF and microwave circuit analysis in a 50 Ω system. This is not very useful for op amp circuits where the input and output impedances can vary greatly. For a more complete description of noise figure, see the MT-052 Tutorial, *Op Amp Noise Figure: Don't be Mislead*, available at www.analog.com.

Signal levels in the application invariably increase to maximize circuit SNR, which is not an option in low voltage, single-supply applications.

Therefore, to achieve optimum circuit SNR in single-supply applications, it is recommended that an operational amplifier with the lowest equivalent input noise voltage be chosen, along with source resistance levels that are consistent with maintaining low total circuit noise.

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp can be used as a comparator; however, this is not recommended for any rail-to-rail output op amps. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the part operating open loop, the second stage increases the current drive to the ratioed mirror to close the loop. However, it cannot, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 84). An unused section should be configured as a voltage follower with the noninverting input connected to a voltage within the input voltage range. The ADA4084-2 has unique second stage and output stage designs that greatly reduce the excess supply current when the op amp is operating open loop.



Figure 84. Supply Current vs. Supply Voltage

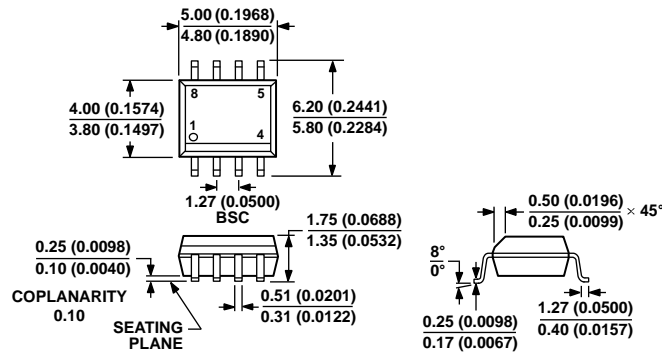
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 85. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 86. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 87. 8-Lead Lead Frame Chip Scale Package [LFCS-P_WD]
 3 x 3 mm Body, Very Very Thin, Dual Lead
 (CP-8-12)
 Dimensions shown in millimeters

02-05-2013-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADA4084-2ARMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARMZ-R7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARMZ-RL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-2ARZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-2ARZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-2ACPZ-R7	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCS-P_WD]	CP-8-12	A2Q
ADA4084-2ACPZ-RL	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCS-P_WD]	CP-8-12	A2Q

¹ Z = RoHS Compliant Part.

NOTES

NOTES

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