DATASHEET

Ultra Low Power Programmable Main Clock for VIA VX900 Chipset

ICS9UM709B

Recommended Application:

Ultra low power main clock for VIA VX900 chipset

Output Features:

- 2 - pairs 0.7V differential push-pull CPU outputs
- 4 - pairs 0.7V differential push-pull PCIEX outputs
- 1 - pair 0.7V differential push-pull MCLK output
- 1 - pair 0.7V differential push-pull CPU/PCIEX selectable output
- 1 - SATA 100MHz single-ended 3.3V output
- 2 - USB 48MHz single-ended 3.3V output
- 1 - AGP 66.66MHz single-ended 3.3V outputs
- 1 - GFX 27MHz single-ended 3.3V outputs
- 3 - PCI 33.33MHz single-ended 3.3V outputs
- 1 - REF 14.318181MHz single-ended 3.3V outputs

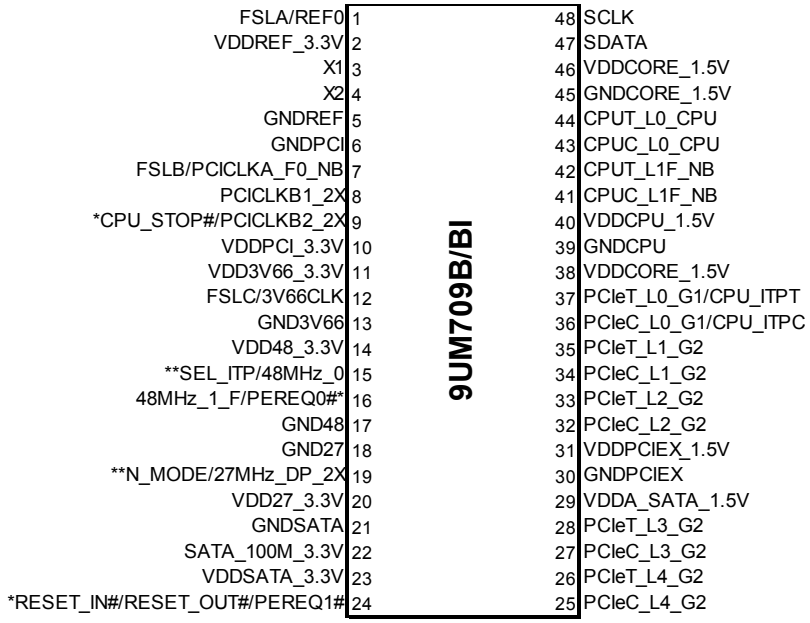
Features/Benefits:

- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Low power differential clock outputs (No 50Ω resistor to GND needed)
- Programmable output skew
- Programmable watchdog safe frequency
- Integrated 33ohm series resistor on all differential outputs
- Low power supply voltage support for differential outputs
- Meets PCIEX Gen2 specifications
- Uses 1.5V core voltage for ultra low power design
- Output programmable slew rate controls

Key Specifications:

- CPU output cycle-cycle jitter < 85ps
- PCIEX output cycle-cycle jitter < 125ps
- +/- 100ppm frequency accuracy for all output clocks
- CPU-AGP skew ~ 1.1ns typical
- AGP-PCIA skew ~ 1.06ns typical
- AGP-PCIB skew ~ 1.46ns typical
- CPU1-PCIA skew ~ 2.16ns typical
- CPU1-PCIB skew ~ 2.46ns typical

Pin Configuration



48-TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	FSLA/REF0	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values / Fixed 3.3V single-ended 14.318 MHz reference clock.
2	VDDREF_3.3V	PWR	Ref, crystal power supply, nominal 3.3V.
3	X1	IN	Crystal input, nominally 14.318MHz.
4	X2	OUT	Crystal output, nominally 14.318MHz.
5	GNDREF	PWR	Ground pin for reference clock output.
6	GNDPCI	PWR	Ground pin for PCI outputs.
7	FSLB/PCICLKA_F0_NB	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values / 3.3V free-running 33.33MHz PCI clock output for North Bridge.
8	PCICLKB1_2X	OUT	3.3V single-ended 33.33MHz PCI clock output default at 2x drive.
9	*CPU_STOP#/PCICLKB2_2X	I/O	Stops all CPU clocks at logic 0 level when low, except those set to be free-running clocks / 3.3V single-ended 33.33MHz PCI clock output default at 2x drive.
10	VDDPCI_3.3V	PWR	Power supply pin for PCI outputs, nominal 3.3V.
11	VDD3V66_3.3V	PWR	Power supply pin for 3V66 outputs, nominal 3.3V.
12	FSLC/3V66CLK	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values / Fixed single-ended 3V66.
13	GND3V66	PWR	Ground pin for 3V66 outputs.
14	VDD48_3.3V	PWR	Ground pin for 48MHz outputs.
15	**SEL_ITP/48MHz_0	I/O	ITP_EN: latched input to select pin functionality 0 (default) = PCIEX0 pair, 1 = CPU_ITP pair / 3.3V single-ended 48MHz output.
16	48MHz_1_F/PEREQ0#*	I/O	3.3V single-ended 48MHz output / Real-time input pin that controls PCIEX0 or PCIEX2 outputs that are selected through the I2C. 1 = disabled, 0 = enabled.
17	GND48	PWR	Ground pin for 48MHz outputs.
18	GND27	PWR	Ground pin for 27MHz outputs.
19	**N_MODE/27MHz_DP_2X	I/O	Input latch pin to select chip to operate in Desktop or Notebook mode. 0 (default) = Notebook, 1=Desktop / 3.3V single-ended 27MHz output, default at 2x drive.
20	VDD27_3.3V	PWR	Power supply pin for 27M outputs, nominal 3.3V.
21	GNDSATA	PWR	Ground pin for single-ended 3.3V SATACLK.
22	SATA_100M_3.3V	OUT	3.3V single-ended 3.3V 100MHz SATACLK.
23	VDDSATA_3.3V	PWR	Power supply pin for single-ended 3.3V SATACLK, nominal 3.3V.
24	*RESET_IN#/RESET_OUT#/PEREQ1#	I/O	Real time active low input. When active, SMBus is reset to power up default / Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low / Real-time input pin that controls PCIEX3 or PCIEX4 outputs that are selected through the I2C. 1 = disabled, 0 = enabled.

Pin Description (continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
25	PCIeC_L4_G2	OUT	Complement clock of 0.7V differential push-pull PCI_Express pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
26	PCIeT_L4_G2	OUT	True clock of 0.7V differential push-pull PCI_Express pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
27	PCIeC_L3_G2	OUT	Complement clock of 0.7V differential push-pull PCI_Express pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
28	PCIeT_L3_G2	OUT	True clock of 0.7V differential push-pull PCI_Express pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
29	VDDA_SATA_1.5V	PWR	Analog power supply for SATA PLL, typically 1.5V.
30	GNDPCIEX	PWR	Ground pin for PCIEX outputs.
31	VDDPCIEX_1.5V	PWR	Low voltage power supply pin for differential PCIEX outputs, nominal 1.5V.
32	PCIeC_L2_G2	OUT	Complement clock of 0.7V differential push-pull PCI_Express pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
33	PCIeT_L2_G2	OUT	True clock of 0.7V differential push-pull PCI_Express pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
34	PCIeC_L1_G2	OUT	Complement clock of 0.7V differential push-pull PCI_Express pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
35	PCIeT_L1_G2	OUT	True clock of 0.7V differential push-pull PCI_Express pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
36	PCIeC_L0_G1/CPU_ITPC	OUT	Complementary clock of differential pair 0.7V push-pull CPU or PCIEX Gen1 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
37	PCIeT_L0_G1/CPU_ITPT	OUT	True clock of differential pair 0.8V push-pull CPU or PCIEX Gen1 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
38	VDDCORE_1.5V	PWR	Power supply pin for core PLL, nominal 1.5V.
39	GNDCPU	PWR	Ground pin for CPU outputs.
40	VDDCPU_1.5V	PWR	Low voltage power supply pin for differential CPU outputs, nominal 1.5V.
41	CPUC_L1F_NB	OUT	Complement clock of 0.7V differential push-pull CPU output for NorthBridge with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
42	CPUT_L1F_NB	OUT	True clock of 0.7V differential push-pull CPU output for NorthBridge with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
43	CPUC_L0_CPU	OUT	Complement clock of 0.7V differential push-pull CPU output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
44	CPUT_L0_CPU	OUT	True clock of 0.7V differential push-pull CPU output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
45	GNDCORE_1.5V	PWR	Ground pin for low voltage core PLL.
46	VDDCORE_1.5V	PWR	Power supply pin for low voltage core PLL, nominal 1.5V.
47	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
48	SCLK	IN	Clock pin of SMBus circuitry, 3.3V tolerant.

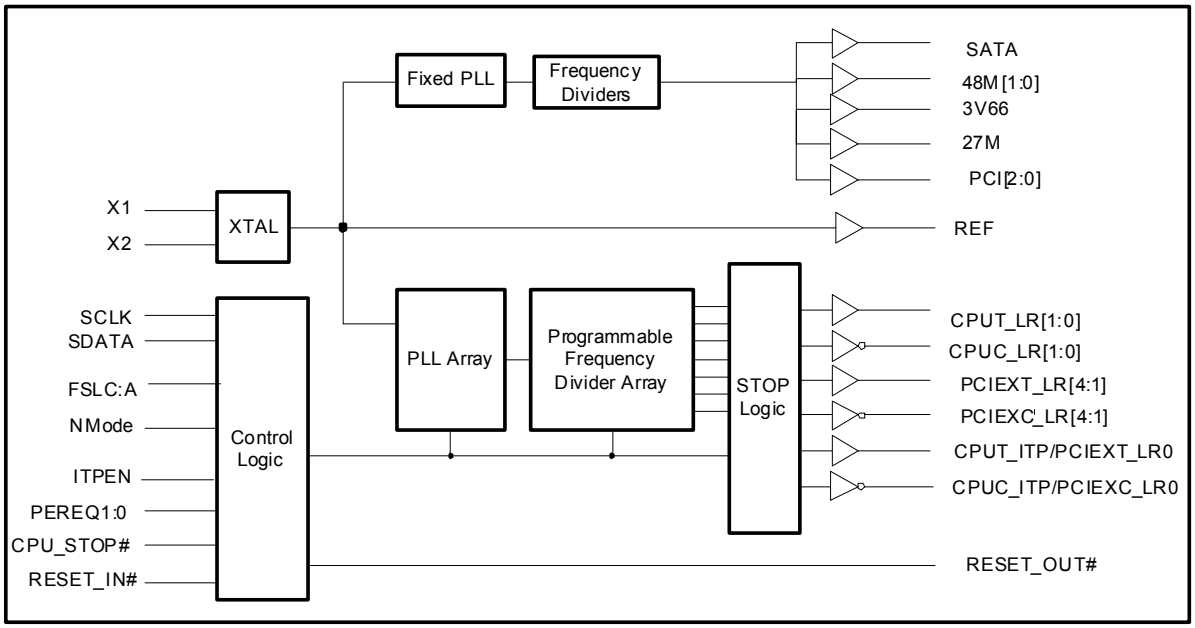
Power Distribution Table:

VDD Pin#	GND pin#	VDD Connection Description
2	5	REF clock output
10	6	PCI clock output
11	13	3V66 clock output
14	17	48M clock output; 48M PLL analog
20	18	27M clock output; 27M PLL analog
23	21	SATA clock output
29	30	SATA PLL analog
31	30	SRC clock output; PCIEX PLL analog
38	13	3V66 core circuit
38	6	PCI core circuit
40	39	CPU clock output
46	45	All PLL digital; Crystal; REF core

General Description

ICS9UM709B is a ultra low power main clock for VIA VX900 chipset. **ICS9UM709B** is driven with a 14.318MHz crystal. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support.

Block Diagram



Transmission lines to load do not share series resistors.
Desktop (Zo=50Ω) and mobile (Zo=55Ω) have the same drive strength.

	Number of Loads to Drive	Match Point for N & P Voltage / Current (mA)	Number of Loads Actually Driven.		
			1 Load Rs =	2 Loads Rs=	3 Loads Rs =
D.C.Drive Strength	1	0.56 / 33 (17Ω)	33Ω [39Ω]	-	-
	2	0.92 / 66 (14Ω)	39Ω [43Ω]	22Ω [27Ω]	-
	3	1.15 / 99 (11.6Ω)	43Ω [43Ω]	27Ω [33Ω]	15Ω [22Ω]

CPU PLL Table1: Frequency Selection Table

B0b4	B0b3	B0b2	B0b1	B0b0	CPU	3V66	PCI33	Spread
FS4	FS3	FSLC	FSLB	FSLA	MHz	MHz	MHz	%
0	0	0	0	0	266.66	66.66	33.33	-0.5% Down
0	0	0	0	1	133.33	66.66	33.33	-0.5% Down
0	0	0	1	0	200.00	66.66	33.33	-0.5% Down
0	0	0	1	1	166.66	66.66	33.33	-0.5% Down
0	0	1	0	0	Reserved			
0	0	1	0	1	100.00	66.66	33.33	-0.5% Down
0	0	1	1	0	Reserved			
0	0	1	1	1	Reserved			
0	1	0	0	0	266.66	66.66	33.33	+/-0.25% Center
0	1	0	0	1	133.33	66.66	33.33	+/-0.25% Center
0	1	0	1	0	200.00	66.66	33.33	+/-0.25% Center
0	1	0	1	1	166.66	66.66	33.33	+/-0.25% Center
0	1	1	0	0	Reserved			
0	1	1	0	1	100.00	66.66	33.33	+/-0.25% Center
0	1	1	1	0	Reserved			
0	1	1	1	1	Reserved			
1	0	0	0	0	293.33	73.33	36.66	-0.5% Down
1	0	0	0	1	146.66	73.33	36.66	-0.5% Down
1	0	0	1	0	220.00	73.33	36.66	-0.5% Down
1	0	0	1	1	183.33	73.33	36.66	-0.5% Down
1	0	1	0	0	Reserved			
1	0	1	0	1	110.00	73.33	36.66	-0.5% Down
1	0	1	1	0	Reserved			
1	0	1	1	1	Reserved			
1	1	0	0	0	239.99	59.99	30.00	-0.5% Down
1	1	0	0	1	120.00	59.99	30.00	-0.5% Down
1	1	0	1	0	180.00	59.99	30.00	-0.5% Down
1	1	0	1	1	149.99	59.99	30.00	-0.5% Down
1	1	1	0	0	Reserved			
1	1	1	0	1	90.00	59.99	30.00	-0.5% Down
1	1	1	1	0	Reserved			
1	1	1	1	1	Reserved			

PCIEX PLL Table2: Frequency Selection Table

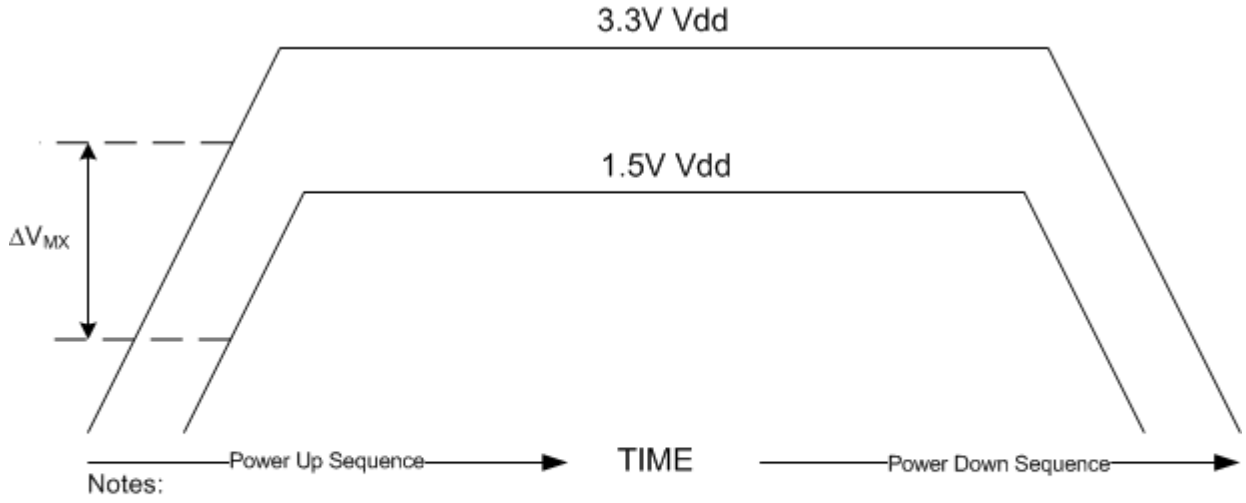
B19b4	B19b3	B19b2	B19b1	B19b0	PCIEX	3V66	PCI33	SATA	Spread
FS4	FS3	FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz	%
0	0	0	0	0	100.00	66.66	33.33	100.00	-0.5% Down
0	0	0	0	1	100.00	66.66	33.33	100.00	-0.5% Down
0	0	0	1	0	100.00	66.66	33.33	100.00	-0.5% Down
0	0	0	1	1	100.00	66.66	33.33	100.00	-0.5% Down
0	0	1	0	0	100.00	66.66	33.33	100.00	-0.5% Down
0	0	1	0	1	100.00	66.66	33.33	100.00	-0.5% Down
0	0	1	1	0	100.00	66.66	33.33	100.00	-0.5% Down
0	0	1	1	1	100.00	66.66	33.33	100.00	-0.5% Down
0	1	0	0	0	100.00	66.66	33.33	100.00	+/-0.25% Center
0	1	0	0	1	100.00	66.66	33.33	100.00	+/-0.25% Center
0	1	0	1	0	100.00	66.66	33.33	100.00	+/-0.25% Center
0	1	0	1	1	100.00	66.66	33.33	100.00	+/-0.25% Center
0	1	1	0	0	100.00	66.66	33.33	100.00	+/-0.25% Center
0	1	1	0	1	100.00	66.66	33.33	100.00	+/-0.25% Center
0	1	1	1	0	100.00	66.66	33.33	100.00	+/-0.25% Center
0	1	1	1	1	100.00	66.66	33.33	100.00	+/-0.25% Center
1	0	0	0	0	110.00	73.33	36.67	110	-0.5% Down
1	0	0	0	1	110.00	73.33	36.67	110	-0.5% Down
1	0	0	1	0	110.00	73.33	36.67	110	-0.5% Down
1	0	0	1	1	110.00	73.33	36.67	110	-0.5% Down
1	0	1	0	0	110.00	73.33	36.67	110	-0.5% Down
1	0	1	0	1	110.00	73.33	36.67	110	-0.5% Down
1	0	1	1	0	110.00	73.33	36.67	110	-0.5% Down
1	0	1	1	1	110.00	73.33	36.67	110	-0.5% Down
1	1	0	0	0	90.00	59.99	30.00	90	-0.5% Down
1	1	0	0	1	90.00	59.99	30.00	90	-0.5% Down
1	1	0	1	0	90.00	59.99	30.00	90	-0.5% Down
1	1	0	1	1	90.00	59.99	30.00	90	-0.5% Down
1	1	1	0	0	90.00	59.99	30.00	90	-0.5% Down
1	1	1	0	1	90.00	59.99	30.00	90	-0.5% Down
1	1	1	1	0	90.00	59.99	30.00	90	-0.5% Down
1	1	1	1	1	90.00	59.99	30.00	90	-0.5% Down

IO_Vout Selection Table

b2	b1	b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	**0**	**0**	**0.7V**
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

***Bold is default**

Power-Up Sequence Requirement



Notes:

1. 3.3V power rail should always come up before 1.5V power rail(s).
2. There are no timing requirements between the higher and lower voltages if the higher voltages power up first.
3. The maximum difference (ΔV_{MX}) between any two voltages is 0.7V if the lower power supply is powered up first.

Differential Power Management Table

CPU_STOP#	PEREQ#	SMBus Register OE	CPU[1:0]T/C		CPU2_ITPT/C (SEL_ITP=1)	
			CPU Stoppable	CPU Free-Running	CPU Stoppable	CPU Free-Running
1	X	Enable	Running/Running	Running/Running	Running/Running	Running/Running
0	X	Enable	High/Low	Running/Running	High/Low	Running/Running
X	X	**Disable**	Low/Low	Low/Low	Low/Low	Low/Low

CPU_STOP#	PEREQ#	SMBus Register OE	PCIEX[4,3,2,0]T/C		PCIEX1T/C
			PEREQ# Controlled	PEREQ# Not Controlled	-
X	0	Enable	Running/Running	Running/Running	Running/Running
X	1	Enable	Low/Low	Running/Running	Running/Running
X	X	**Disable**	Low/Low	Low/Low	Low/Low

Singled-Ended Power Management Table

CPU_STOP#	PEREQ#	SMBus Register OE	PCI[2:0]	REF	27M	48M[1:0]	3V66	SATA
			-	-	-	-	-	-
X	X	Enable	Running	Running	Running	Running	Running	Running
X	X	**Disable**	Low	Low	Low	Low	Low	Low

PEREQ# Control Table:

PEREQ#	PCIEX
0	0,2
1	3,4

Commercial Temperature Specifications

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
3.3V Logic Input Supply Voltage	VDD_In	Logic Supply	GND - 0.5	V_{DD} + 0.5V	V	1,2,3
3.3V Supply Voltage	VDD_3.3	Core Supply	GND - 0.5	V_{DD} + 0.5V	V	1,2
1.5V Supply Voltage	VDDx_1.5	Low Voltage Differential Core/Logic Supply	GND - 0.5	V_{DD} + 0.3V	V	1,2
VDDIO Supply Voltage	VDDx_IO	Low Voltage Differential I/O Supply	GND - 0.5	V_{DD} + 0.3V	V	1,2
Storage Temperature	Ts	-	-65	150	°C	1,2
Case Temperature	Tcase	-		115	°C	1,2

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied, nor guaranteed.

[3] Maximum input voltage is not to exceed maximum VDD

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	70	°C	
3.3V Supply Voltage	VDDxxx_3.3	3.3V +/- 5%	3.135	3.465	V	1
1.5V Supply Voltage	VDDxxx_1.5	1.5V +/- 5%	1.425	1.575	V	1
3.3V Input High Voltage	$V_{IHSE3.3}$		2	$V_{DDxx\_3.3}$ + 0.3	V	1,4
3.3V Input Low Voltage	$V_{ILSE3.3}$		V_{SS} - 0.3	0.8	V	1,4
1.5V Input High Voltage	$V_{IHSE1.5}$		0.8	$V_{DDxxx\_1.5}$ + 0.3	V	1
1.5V Input Low Voltage	$V_{ILSE1.5}$		V_{SS} - 0.3	0.6	V	1
Low Threshold Input-High Voltage	$V_{IH\_FS\_3.3}$	3.3 V +/-5%	0.7	V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	$V_{IL\_FS\_3.3}$	3.3 V +/-5%	V_{SS} - 0.3	0.35	V	1
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	1,3
Input Leakage Current	I_{INRES}	Inputs with pull or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200	200	uA	1
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4		V	1,2
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA		0.4	V	1,2
Operating Current	$I_{DD3.3OP}$	All outputs driven, Full Active		39	mA	1
	$I_{DD1.5OP}$			58	mA	1
	$I_{DDIO\_1.5OP}$			6	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		15	MHz	1
Pin Inductance	L_{pin}			7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	1
	C_{OUT}	Output pin capacitance		6	pF	1
	C_{INX}	X1 & X2 pins		6	pF	1
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	33	kHz	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3V/1.5V +/-5%

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] Signal is required to be monotonic in this region.

[3] Input leakage current does not include inputs with pull-up or pull-down resistors

[4] 3.3V referenced inputs are: SCLK, SDATA, CPU_STOP#, SEL_ITP, N_MODE, RESET_IN# and PEREQ1/0.

Electrical Characteristics - SMBus Interface

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	V_{DD}		2.7	3.6	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}		0.4	V	1
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4		mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	1
Maximum SMBus Operating Frequency	F_{SMBUS}	Block Mode		100	kHz	1

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

AC Electrical Characteristics - Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	T_{STAB}	From 70% VDD (VDD3.3, VDD1.5, VDDIO) to clock output	4	6.5	ms	1
Tdrive_CPU	T_{DRSRC}	CPU output enable after CPU_STOP# de-assertion		10	ns	1
Tfall_PD#	T_{FALL}	Fall/Rise time of CPU_STOP# inputs		5	ns	1
Trise_PD#	T_{RISE}			5	ns	1

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - AGP66MHz (3V66) Clock Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2,6
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Rise Time	t_{r1}	Measured from 0.8 to 2.0 V	0.3		1.2	ns	1,3
Fall Time	t_{f1}	Measured from 2.0 to 0.8 V	0.3		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		275	500	ps	1,4
Group to Group Skew	$t_{CPU-AGP\ skew}$	V_T = 1.5 V		1.1		ns	1,4
	$t_{AGP-PCIA\ skew}$	V_T = 1.5 V		1.06		ns	1,4
	$t_{AGP-PCIB\ skew}$	V_T = 1.5 V		1.46		ns	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

AC Electrical Characteristics - CPUCLK (0.7V Push-Pull) Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	11
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	2.5	8	V/ns	1,3,4
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	2.5	8	V/ns	1,3,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1,2,7
Average Maximum Output Voltage	$V_{HIGH-TYP}$	Average High	660	850	mV	1,2
Average Minimum Output Voltage	$V_{LOW-TYP}$	Average Low	-150		mV	1,2
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1,2,8
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1,2,9
Differential Voltage Swing	V_{SWING}	Differential Measurement	300		mV	1,3
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,2,5,6
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,2,5,10
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%	1,3
CPU[2:0] Skew	$t_{CPU\ skew}$	Single-ended Measurement		100	ps	1,2

*TA = 0 - 70°C; Supply Voltage VDD = 1.5 V +/-5%, Rs=0ohm, CL=2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2]Measurement taken for single ended waveform on a component test board (not in system)

[3] Measurement taken from differential waveform on a component test board. (not in system)

[4] Slew rate emastured through V_swing voltage range centered about differential zero

[5] Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

[6] Only applies to the differential rising edge (Clock rising, Clock# falling)

[7] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage.

[8] The max voltage including overshoot.

[9] The min voltage including undershoot.

[10] The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross induced modulation by setting C_cross_delta to be smaller than V_Cross

[11] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

AC Electrical Characteristics - PCIEX (0.7V Push-Pull) Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	11
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	0.6	4	V/ns	1,3,4
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	0.6	4	V/ns	1,3,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1,2,7
Average Maximum Output Voltage	$V_{HIGH-TYP}$	Average High	660	850	mV	1,2
Average Minimum Output Voltage	$V_{LOW-TYP}$	Average Low	-150		mV	1,2
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1,2,8
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1,2,9
Differential Voltage Swing	V_{SWING}	Differential Measurement	300		mV	1,3
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,2,5,6
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,2,5,10
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%	1,3
PCIEX[4:0] Skew	$t_{PCIEX\ skew}$	Single-ended Measurement		100	ps	1,2

*TA = 0 - 70°C; Supply Voltage VDD = 1.5 V +/-5%, Rs=0ohm, CL=2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2]Measurement taken for single ended waveform on a component test board (not in system)

[3] Measurement taken from differential waveform on a component test board. (not in system)

[4] Slew rate emastured through V_swing voltage range centered about differential zero

[5] Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

[6] Only applies to the differential rising edge (Clock rising, Clock# falling)

[7] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage.

[8] The max voltage including overshoot.

[9] The min voltage including undershoot.

[10] The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross induced modulation by setting C_cross_delta to be smaller than V_Cross absolute.

[11] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - PCICLK Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2,6
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Rise Time	t_{r1}	Measured from 0.8 to 2.0 V	0.3		1.2	ns	1,3
Fall Time	t_{f1}	Measured from 2.0 to 0.8 V	0.3		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
PCI[B:A] Skew	t_{skew}	V_T = 1.5 V		400		ps	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		250	500	ps	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm (for PCICLKA), Rs=39ohm (for PCICLKB), CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Electrical Characteristics - 48M Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2,6
Clock period	T_{period}	48.00MHz output nominal	20.83130		20.83540	ns	1,4,5
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		2	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		2	V/ns	1,3
Risetime	t_R	V_{OH}=2.0V, V_{OL}=0.8V	0.6		1.2	ns	1,3
Falltime	t_F	V_{OH}=2.0V, V_{OL}=0.8V	0.6		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		150	350	ps	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Electrical Characteristics - 27MHz GFX Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-30		30	ppm	1,2,6
Clock period	T_{period}	27.000MHz output nominal	37.0365		37.0376	ns	1,4,5
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Rise Time	t_{r1}	Measured from 0.8 to 2.0 V	0.3		1.2	ns	1,3
Fall Time	t_{f1}	Measured from 2.0 to 0.8 V	0.3		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter	t_{ltj}	Long Term (10us), V_T = 1.5 V			500	ps	1,4
	$t_{jcyc-cyc}$	Cycle to Cycle, V_T = 1.5 V		250	500	ps	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=39ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-30		30	ppm	1,2,6
Clock period	T_{period}	14.318MHz output nominal	69.827		69.855	ns	1,4,5
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-33		-33	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	30		38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Rise Time	t_{r1}	Measured from 0.8 to 2.0 V	0.3		1.2	ns	1,3
Fall Time	t_{f1}	Measured from 2.0 to 0.8 V	0.3		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		600	1000	ps	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Electrical Characteristics - 100MHz SATA Clock Output

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-30		30	ppm	1,2,6
Clock period	T_{period}	25.00MHz output nominal	9.9999		10.0001	ns	1,4,5
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1,3
		V_{OL} @ MAX = 0.4 V			27	mA	1,3
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter	$t_{jcyc-cyc}$	Cycle to Cycle, V_T = 1.5 V, source from PCIEX spread PLL		350	700	ps	1,4
	t_{ltj}	Long Term (10us), V_T = 1.5 V, source from SATA non-spread PLL		1000	1500	ps	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Clock Jitter Specifications - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		85	ps	1,2
PCIEX Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		125	ps	1,2
PCIEX Phase Jitter	$t_{jphasePLL}$	PCIe Gen 1		86	ps (p-p)	1,2
	$t_{jphaseLo}$	PCIe Gen 2 10kHz < f < 1.5MHz		3.0	ps (RMS)	1,3,4
	$t_{jphaseHigh}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)		3.1	ps (RMS)	1,3,4

*TA = 0 - 70°C; Supply Voltage VDD = 1.5V +/- 5%, Rs=0ohm, CL=2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2]JItter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the receiver jitter specs as measured in a real system.

[3] Phase jitter requirement: The designated Gen2 outputs will meet the reference clock jitter requiremernts from the PCI Express Gen2 Base Spec. The test is performed on a componnet test board under quiet conditttions with all outputs on.

[4]See http://www.pcisig.com for complete specs

Industrial Temperature Specifications

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
3.3V Logic Input Supply Voltage	VDD_In	Logic Supply	GND - 0.5	V_{DD} + 0.5V	V	1,2,3
3.3V Supply Voltage	VDD_3.3	Core Supply	GND - 0.5	V_{DD} + 0.5V	V	1,2
1.5V Supply Voltage	VDDx_1.5	Low Voltage Differential Core/Logic Supply	GND - 0.5	V_{DD} + 0.3V	V	1,2
Storage Temperature	Ts	-	-65	150	°C	1,2
Case Temperature	Tcase	-		115	°C	1,2

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied, nor guaranteed.

[3] Maximum input voltage is not to exceed maximum VDD

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	-40	85	°C	
3.3V Supply Voltage	VDDxxx_3.3	3.3V +/- 5%	3.135	3.465	V	1
1.5V Supply Voltage	VDDxxx_1.5	1.5V +/- 5%	1.425	1.575	V	1
3.3V Input High Voltage	$V_{IHSE3.3}$		2	$V_{DDxx\_3.3}$ + 0.3	V	1,4
3.3V Input Low Voltage	$V_{ILSE3.3}$		V_{SS} - 0.3	0.8	V	1,4
1.5V Input High Voltage	$V_{IHSE1.5}$		0.8	$V_{DDxxx\_1.5}$ + 0.3	V	1
1.5V Input Low Voltage	$V_{ILSE1.5}$		V_{SS} - 0.3	0.6	V	1
Low Threshold Input-High Voltage	$V_{IH\_FS\_3.3}$	3.3 V +/-5%	0.7	V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	$V_{IL\_FS\_3.3}$	3.3 V +/-5%	V_{SS} - 0.3	0.35	V	1
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	1,3
Input Leakage Current	I_{INRES}	Inputs with pull or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200	200	uA	1
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4		V	1,2
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA		0.4	V	1,2
Operating Current	$I_{DD3.3OP}$	All outputs driven, Full Active		39	mA	1
	$I_{DD1.5OP}$			58	mA	1
	$I_{DDIO\_1.5OP}$			6	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		15	MHz	1
Pin Inductance	L_{pin}			7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	1
	C_{OUT}	Output pin capacitance		6	pF	1
	C_{INX}	X1 & X2 pins		6	pF	1
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	33	kHz	1

*TA = -40°C ~ 85°C; Supply Voltage VDD = 3.3V/1.5V +/-5%

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] Signal is required to be monotonic in this region.

[3] Input leakage current does not include inputs with pull-up or pull-down resistors

[4] 3.3V referenced inputs are: SCLK, SDATA, CPU_STOP#, SEL_ITP, N_MODE, RESET_IN# and PEREQ1/0.

Electrical Characteristics - SMBus Interface

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	V_{DD}		2.7	3.6	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}		0.4	V	1
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4		mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	1
Maximum SMBus Operating Frequency	F_{SMBUS}	Block Mode		100	kHz	1

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

AC Electrical Characteristics - Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	T_{STAB}	From 70% VDD (VDD3.3, VDD1.5, VDDIO) to clock output	4	6.5	ms	1
Tdrive_CPU	T_{DRSRC}	CPU output enable after CPU_STOP# de-assertion		10	ns	1
Tfall_PD#	T_{FALL}	Fall/Rise time of CPU_STOP# inputs		5	ns	1
Trise_PD#	T_{RISE}			5	ns	1

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - AGP66MHz (3V66) Clock Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2,6
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Rise Time	t_{r1}	Measured from 0.8 to 2.0 V	0.3		1.2	ns	1,3
Fall Time	t_{f1}	Measured from 2.0 to 0.8 V	0.3		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		275	500	ps	1,4
Group to Group Skew	$t_{CPU-AGP\ skew}$	V_T = 1.5 V		1.1		ns	1,4
	$t_{AGP-PCIA\ skew}$	V_T = 1.5 V		1.06		ns	1,4
	$t_{AGP-PCIB\ skew}$	V_T = 1.5 V		1.46		ns	1,4

*TA = -40°C ~ 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

AC Electrical Characteristics - CPUCLK (0.7V Push-Pull) Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	11
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	2.5	8	V/ns	1,3,4
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	2.5	8	V/ns	1,3,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1,2,7
Average Maximum Output Voltage	$V_{HIGH-TYP}$	Average High	660	850	mV	1,2
Average Minimum Output Voltage	$V_{LOW-TYP}$	Average Low	-150		mV	1,2
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1,2,8
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1,2,9
Differential Voltage Swing	V_{SWING}	Differential Measurement	300		mV	1,3
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,2,5,6
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,2,5,10
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%	1,3
CPU[2:0] Skew	$t_{CPU\ skew}$	Single-ended Measurement		100	ps	1,2

*TA = -40°C ~ 85°C; Supply Voltage VDD = 1.5 V +/-5%, Rs=0ohm, CL=2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2]Measurement taken for single ended waveform on a component test board (not in system)

[3] Measurement taken from differential waveform on a component test board. (not in system)

[4] Slew rate emastured through V_swing voltage range centered about differential zero

[5] Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

[6] Only applies to the differential rising edge (Clock rising, Clock# falling)

[7] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage.

[8] The max voltage including overshoot.

[9] The min voltage including undershoot.

[10] The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross induced modulation by setting C_cross_delta to be smaller than V_Cross absolute.

[11] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

AC Electrical Characteristics - PCIEX (0.7V Push-Pull) Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	11
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	0.6	4	V/ns	1,3,4
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	0.6	4	V/ns	1,3,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1,2,7
Average Maximum Output Voltage	$V_{HIGH-TYP}$	Average High	660	850	mV	1,2
Average Minimum Output Voltage	$V_{LOW-TYP}$	Average Low	-150		mV	1,2
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1,2,8
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1,2,9
Differential Voltage Swing	V_{SWING}	Differential Measurement	300		mV	1,3
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,2,5,6
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,2,5,10
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%	1,3
PCIEX[4:0] Skew	$t_{PCIEX\ skew}$	Single-ended Measurement		100	ps	1,2

*TA = -40°C ~ 85°C; Supply Voltage VDD = 1.5 V +/-5%, Rs=0ohm, CL=2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2]Measurement taken for single ended waveform on a component test board (not in system)

[3] Measurement taken from differential waveform on a component test board. (not in system)

[4] Slew rate emastured through V_swing voltage range centered about differential zero

[5] Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

[6] Only applies to the differential rising edge (Clock rising, Clock# falling)

[7] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage.

[8] The max voltage including overshoot.

[9] The min voltage including undershoot.

[10] The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross induced modulation by setting C_cross_delta to be smaller than V_Cross absolute.

[11] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - PCICLK Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2,6
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Rise Time	t_{r1}	Measured from 0.8 to 2.0 V	0.3		1.2	ns	1,3
Fall Time	t_{f1}	Measured from 2.0 to 0.8 V	0.3		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
PCI[B:A] Skew	t_{skew}	V_T = 1.5 V		400		ps	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		250	500	ps	1,4

*TA = -40°C ~ 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm (for PCICLKA), Rs=39ohm (for PCICLKB), CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Electrical Characteristics - 48M Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2,6
Clock period	T_{period}	48.00MHz output nominal	20.83130		20.83540	ns	1,4,5
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		2	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		2	V/ns	1,3
Risetime	t_R	V_{OH}=2.0V, V_{OL}=0.8V	0.6		1.2	ns	1,3
Falltime	t_F	V_{OH}=2.0V, V_{OL}=0.8V	0.6		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		150	350	ps	1,4

*TA = -40°C ~ 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Electrical Characteristics - 27MHz GFX Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-30		30	ppm	1,2,6
Clock period	T_{period}	27.000MHz output nominal	37.0365		37.0376	ns	1,4,5
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Rise Time	t_{r1}	Measured from 0.8 to 2.0 V	0.3		1.2	ns	1,3
Fall Time	t_{f1}	Measured from 2.0 to 0.8 V	0.3		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter	t_{ltj}	Long Term (10us), V_T = 1.5 V			500	ps	1,4
	$t_{jcyc-cyc}$	Cycle to Cycle, V_T = 1.5 V		250	500	ps	1,4

*TA = -40°C ~ 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=39ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-30		30	ppm	1,2,6
Clock period	T_{period}	14.318MHz output nominal	69.827		69.855	ns	1,4,5
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-33		-33	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	30		38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Rise Time	t_{r1}	Measured from 0.8 to 2.0 V	0.3		1.2	ns	1,3
Fall Time	t_{f1}	Measured from 2.0 to 0.8 V	0.3		1.2	ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		600	1000	ps	1,4

*TA = -40°C ~ 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Electrical Characteristics - 100MHz SATA Clock Output

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-30		30	ppm	1,2,6
Clock period	T_{period}	25.00MHz output nominal	9.9999		10.0001	ns	1,4,5
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1,3
		V_{OL} @ MAX = 0.4 V			27	mA	1,3
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1		4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1		4	V/ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,4
Jitter	$t_{jcyc-cyc}$	Cycle to Cycle, V_T = 1.5 V, source from PCIEX spread PLL		350	700	ps	1,4
	t_{ltj}	Long Term (10us), V_T = 1.5 V, source from SATA non-spread PLL		1000	1500	ps	1,4

*TA = -40°C ~ 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 27.000000MHz, 33.333333MHz, 48.000000MHz, 66.666666MHz and 100.000000MHz.

Clock Jitter Specifications - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		85	ps	1,2
PCIEX Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		125	ps	1,2
PCIEX Phase Jitter	$t_{jphasePLL}$	PCIe Gen 1		86	ps (p-p)	1,2
	$t_{jphaseLo}$	PCIe Gen 2 10kHz < f < 1.5MHz		3.0	ps (RMS)	1,3,4
	$t_{jphaseHigh}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)		3.1	ps (RMS)	1,3,4

*TA = -40°C ~ 85°C; Supply Voltage VDD = 1.5V +/- 5%, Rs=0ohm, CL=2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2]JItter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the receiver jitter specs as measured in a real system.

[3] Phase jitter requirement: The designated Gen2 outputs will meet the reference clock jitter requiremernts from the PCI Express Gen2 Base Spec. The test is performed on a componnet test board under quiet conditttions with all outputs on.

[4]See http://www.pcisig.com for complete specs

General SMBus serial interface information for the ICS9UM709B

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBUS Table: CPU PLL Frequency Select Register

Byte 0	Name	Control Function	Type	0	1	PWD
Bit 7	ROD	Reset On Demand	RW	Disable	Enable	0
Bit 6	SS_EN1	PCIEX PLL Spread Enable	RW	OFF	ON	1
Bit 5	SS_EN2	CPU PLL Spread Enable	RW	OFF	ON	1
Bit 4	FS4	Freq Select Bit 4	RW	See Table 1: CPU PLL Frequency Selection Table		0
Bit 3	FS3	Freq Select Bit 3	RW			0
Bit 2	FSLC	Freq Select Bit 2	RW			Latch
Bit 1	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	FSLA	Freq Select Bit 0	RW			Latch

SMBUS Table: Input Select Control Register

Byte 1	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	CPU PLL MNEN	CPU PLL M/N Enable	RW	Disable	Enable	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	PCIEX PLL MNEN	PCIEX PLL M/N Enable	RW	Disable	Enable	0
Bit 2	RESET_EN	RESET pin enable bit (enables pin to be active)	RW	Disable	Enable	0
Bit 1	**ITPEN	Select CPUITP or PCIEX0	R	PCIEX0	CPUITP	Latch
Bit 0	**NMode	Select Desktop or Mobile Mode	R	Mobile	Desktop	Latch

* Default power-up state of Pin24 is PEREQ1#, following Byte1 bit 2

SMBUS Table: Output Control Register

Byte 2	Name	Control Function	Type	0	1	PWD
Bit 7	REF	Output Control	RW	Disable	Enable	1
Bit 6	48M_0	Output Control	RW	Disable	Enable	1
Bit 5	48M_1	Output Control	RW	Disable	Enable	1
Bit 4	27M_DP	Output Control	RW	Disable	Enable	1
Bit 3	AGP_3V66	Output Control	RW	Disable	Enable	1
Bit 2	PCICLKA0	Output Control	RW	Disable	Enable	1
Bit 1	PCICLKB1	Output Control	RW	Disable	Enable	1
Bit 0	PCICLKB2	Output Control	RW	Disable	Enable	1

SMBUS Table: Output Control Register

Byte 3	Name	Control Function	Type	0	1	PWD
Bit 7	SATA_100M	Output Control	RW	Disable	Enable	1
Bit 6	CPUCLK_0	Output Control	RW	Disable	Enable	1
Bit 5	CPUCLK_1	Output Control	RW	Disable	Enable	1
Bit 4	CPUCLK_2_ITP	Output Control	RW	Disable	Enable	1
Bit 3	PCIEXT/C0	Output Control	RW	Disable	Enable	1
Bit 2	PCIEXT/C1	Output Control	RW	Disable	Enable	1
Bit 1	PCIEXT/C2	Output Control	RW	Disable	Enable	1
Bit 0	PCIEXT/C3	Output Control	RW	Disable	Enable	1

SMBUS Table: Output Control Register

Byte 4	Name	Control Function		0	1	PWD
Bit 7	PCIEXT/C4	Output Control	RW	Disable	Enable	1
Bit 6	PCICLKA0	PCICLKA0 Strength Control	RW	1x	2x	0
Bit 5	PCICLKB1	PCICLKB1 Strength Control	RW	1x	2x	1
Bit 4	PCICLKB2	PCICLKB2 Strength Control	RW	1x	2x	1
Bit 3	REF	REF Strength Control	RW	1x	2x	0
Bit 2	48M_0	48M_0 Strength Control	RW	1x	2x	0
Bit 1	48M_1	48M_1 Strength Control	RW	1x	2x	0
Bit 0	27M_DP	27M_DP Strength Control	RW	1x	2x	1

SMBUS Table: Output Control Register

Byte 5	Name	Control Function	Type	0	1	PWD
Bit 7	AGP_3V66	3V66 Strength Control	RW	1x	2x	0
Bit 6	SATA_100M	SATA Strength Control	RW	1x	2x	0
Bit 5	CPU_SR	CPU Group Programmable Slew Rate Control	RW	0 = 2.5V/ns	1 = 4V/ns	1
Bit 4	CPUCLK_0	Free running control (during CPU_STOP#)	RW	Free-running	Stoppable	0
Bit 3	CPUCLK_1	Free running control (during CPU_STOP#)	RW	Free-running	Stoppable	0
Bit 2	CPUCLK_2_ITP	Free running control (during CPU_STOP#)	RW	Free-running	Stoppable	0
Bit 1	PCIEX_SR	PCIEX Group Programmable Slew Rate Control	RW	0 = 2.5V/ns	1 = 4V/ns	1
Bit 0	Load Control	IIC Load control/RAM read back select	RW	Load/ RB from Active RAM	Do not Load/ RB from Shadow RAM	0

SMBUS Table: Output Control Register

Byte 6	Name	Control Function	Type	0	1	PWD
Bit 7	CPU IO_VOUT2	CPU IO Output Voltage Select (Most Significant Bit)	RW	See Table 4: V_IO Selection (Default is 0.7V)		1
Bit 6	CPU IO_VOUT1	CPU IO Output Voltage Select	RW			0
Bit 5	CPU IO_VOUT0	CPU IO Output Voltage Select (Least Significant Bit)	RW			0
Bit 4	PCIEX IO_VOUT2	PCIEX IO Output Voltage Select (Most Significant Bit)	RW	See Table 4: V_IO Selection (Default is 0.7V)		1
Bit 3	PCIEX IO_VOUT1	PCIEX IO Output Voltage Select	RW			0
Bit 2	PCIEX IO_VOUT0	PCIEX IO Output Voltage Select (Least Significant Bit)	RW			0
Bit 1	PEREQ0# Control	PCIEX0 is controlled	RW	Not Controlled	Controlled	0
Bit 0	PEREQ0# Control	PCIEX2 is controlled	RW	Not Controlled	Controlled	0

SMBUS Table: Revision and Vendor ID Register

Byte 7	Name	Control Function	Type	0	1	PWD
Bit 7	RID3	Revision ID	R	-	-	0
Bit 6	RID2		R	-	-	0
Bit 5	RID1		R	-	-	0
Bit 4	RID0		R	-	-	1
Bit 3	VID3	VENDOR ID	R	-	-	0
Bit 2	VID2		R	-	-	0
Bit 1	VID1		R	001 = ICS	-	0
Bit 0	VID0		R	-	-	1

SMBUS Table: Byte Count Register

Byte 8	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	R	-	-	0
Bit 6	Reserved	Reserved	R	-	-	0
Bit 5	Reserved	Reserved	R	-	-	0
Bit 4	Reserved	Reserved	R	-	-	0
Bit 3	BC3	Byte Count Programming b(3:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		1
Bit 2	BC2		RW			1
Bit 1	BC1		RW			1
Bit 0	BC0		RW			1

SMBUS Table: Watch Dog Timer Control Register

Byte 9	Name	Control Function	Type	0	1	PWD
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable	Enable	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	HWD5	WD Hard Alarm Timer Bit 5	RW	These bits represent X*290ms (or 1.16s) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s. Combined with B10b<7:5>		0
Bit 1	HWD4	WD Hard Alarm Timer Bit 4	RW			0
Bit 0	HWD3	WD Hard Alarm Timer Bit 3	RW			0

SMBUS Table: WD Safe Frequency Control Register

Byte 10	Name	Control Function	Type	0	1	PWD
Bit 7	HWD2	WD Hard Alarm Timer Bit 2	RW	These bits represent X*290ms (or 1.16s) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s. Combined with B9b<2:0>		1
Bit 6	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 5	HWD0	WD Hard Alarm Timer Bit 0	RW			1
Bit 4	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte10 bit (4:0).		0
Bit 3	WD SF3		RW			0
Bit 2	WD SF2		RW			Latch
Bit 1	WD SF1		RW			Latch
Bit 0	WD SF0		RW			Latch

SMBUS Table: CPU PLL Frequency Control Register

Byte 11	Name	Control Function	Type	0	1	PWD
Bit 7	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x Ndiv(9:0)/Mdiv(5:0)		X
Bit 6	N Div9	N Divider Prog bit 9	RW			X
Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

SMBUS Table: CPU PLL Frequency Control Register

Byte 12	Name	Control Function	Type	0	1	PWD
Bit 7	N Div7	N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x Ndiv(9:0)/Mdiv(5:0)		X
Bit 6	N Div6		RW			X
Bit 5	N Div5		RW			X
Bit 4	N Div4		RW			X
Bit 3	N Div3		RW			X
Bit 2	N Div2		RW			X
Bit 1	N Div1		RW			X
Bit 0	N Div0		RW			X

SMBUS Table: CPU PLL Spread Spectrum Control Register

Byte 13	Name	Control Function	Type	0	1	PWD
Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of CPU PLL		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

SMBUS Table: CPU PLL Spread Spectrum Control Register

Byte 14	Name	Control Function	Type	0	1	PWD
Bit 7	SSP15	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of CPU PLL		X
Bit 6	SSP14		RW			X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

SMBUS Table: PCIEX PLL Frequency Control Register

Byte 15	Name	Control Function	Type	0	1	PWD
Bit 7	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divider in Byte 15 and 16 will configure the PCIEX PLL VCO frequency. Default at power up = latch-in or Byte 19 Rom table. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div9	N Divider Prog bit 9	RW			X
Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

SMBUS Table: PCIEX PLL Frequency Control Register

Byte 16	Name	Control Function	Type	0	1	PWD
Bit 7	N Div7	N Divider Programming Byte16 bit(7:0) and Byte15 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 15 and 16 will configure the PCIEX PLL VCO frequency. Default at power up = latch-in or Byte 19 Rom table. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div6		RW			X
Bit 5	N Div5		RW			X
Bit 4	N Div4		RW			X
Bit 3	N Div3		RW			X
Bit 2	N Div2		RW			X
Bit 1	N Div1		RW			X
Bit 0	N Div0		RW			X

SMBUS Table: PCIEX PLL Spread Spectrum Control Register

Byte 17	Name	Control Function	Type	0	1	PWD
Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of PCIEX PLL		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

SMBUS Table: PCIEX PLL Spread Spectrum Control Register

Byte 18	Name	Control Function	Type	0	1	PWD
Bit 7	SSP15	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of PCIEX PLL		X
Bit 6	SSP14		RW			X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

SMBUS Table: PCIEX Frequency Select Register

Byte 19	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	FS4	Freq Select Bit 4	RW	See Table 1: PCIEX PLL Frequency Selection Table		0
Bit 3	FS3	Freq Select Bit 3	RW			0
Bit 2	FSLC	Freq Select Bit 2	RW			Latch
Bit 1	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	FSLA	Freq Select Bit 0	RW			Latch

SMBUS Table: Output Control Register

Byte 20	Name	Control Function	Type	0	1	PWD
Bit 7	PCICLKA0	PCICLKA0 Programmable	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 6	PCICLKA0	Slew Rate Control	RW	10=2.0V/ns	11=2.5V/ns	1
Bit 5	PCICLKB1	PCICLKB1 Programmable	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 4	PCICLKB1	Slew Rate Control	RW	10=2.0V/ns	11=2.5V/ns	1
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	PEREQ1# Control	PCIEX3 is controlled	RW	Not Controlled	Controlled	0
Bit 1	PEREQ1# Control	PCIEX4 is controlled	RW	Not Controlled	Controlled	0
Bit 0	RESET Sync	Reset Synchronization upon Reset (Byte 21)	RW	Disable	Enable	0

SMBUS Table: Synchronization Control Register

Byte 21	Name	Control Function	Type	0	1	PWD
Bit 7	PCI33 Source	PCI Source	RW	CPU PLL	PCIEX PLL	0
Bit 6	3V66 Source	AGP 3V66 Source	RW	CPU PLL	PCIEX PLL	0
Bit 5	SATA Source	SATA Source	RW	PCIEX PLL	SATA PLL	1
Bit 4	PCIEX Source	PCIEX Source	RW	PCIEX PLL	SATA PLL	0
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Reserved	Reserved	RW	-	-	0

SMBUS Table: Output Control Register

Byte 22	Name	Control Function	Type	0	1	PWD
Bit 7	27M_DP	27M_DP Programmable	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 6	27M_DP	Slew Rate Control	RW	10=2.0V/ns	11=2.5V/ns	1
Bit 5	48M_0	48M_1 Programmable	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 4	48M_0	Slew Rate Control	RW	10=2.0V/ns	11=2.5V/ns	1
Bit 3	48M_1	48M_1 Programmable	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 2	48M_1	Slew Rate Control	RW	10=2.0V/ns	11=2.5V/ns	1
Bit 1	PCICLKB2	PCICLKB2 Programmable	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 0	PCICLKB2	Slew Rate Control	RW	10=2.0V/ns	11=2.5V/ns	1

Byte 23 ~ 24 Reserved Registers

SMBUS Table: Output Skew programming Register

Byte 25	Name	Control Function	Type	0		1		PWD
Bit 7	CPU0/2-CPU1Skw3	CPU0/2-CPU1 Programmable Skew Control (ps)	RW	0000: -800	0100: -400	1000 = 0	1100: +400	1
Bit 6	CPU0/2-CPU1Skw2		RW	0001: -700	0101: -300	1001: +100	1101: +500	0
Bit 5	CPU0/2-CPU1Skw1		RW	0010: -600	0110: -200	1010: +200	1110: +600	0
Bit 4	CPU0/2-CPU1Skw0		RW	0011: -500	0111: -100	1011: +300	1111: +700	0
Bit 3	CPU-3V66 Skw3	CPU-3V66 Programmable Skew Control (ps)	RW	0000: -800	0100: -400	1000 = 0	1100: +400	1
Bit 2	CPU-3V66 Skw2		RW	0001: -700	0101: -300	1001: +100	1101: +500	0
Bit 1	CPU-3V66 Skw1		RW	0010: -600	0110: -200	1010: +200	1110: +600	0
Bit 0	CPU-3V66 Skw0		RW	0011: -500	0111: -100	1011: +300	1111: +700	0

SMBus Table: Output Skew Programming Register

Byte 26	Name	Control Function	Type	0		1		PWD
Bit 7	CPU-PCIA Skw3	CPU-PCICLKA Programmable Skew Control (ps)	RW	0000: -800	0100: -400	1000 = 0	1100: +400	1
Bit 6	CPU-PCIA Skw2		RW	0001: -700	0101: -300	1001: +100	1101: +500	0
Bit 5	CPU-PCIA Skw1		RW	0010: -600	0110: -200	1010: +200	1110: +600	0
Bit 4	CPU-PCIA Skw0		RW	0011: -500	0111: -100	1011: +300	1111: +700	0
Bit 3	PCIA-PCIB1/2 Skw3	PCICLKA-PCICLKB1/2 Programmable Skew Control (ps)	RW	0000: -800	0100: -400	1000 = 0	1100: +400	1
Bit 2	PCIA-PCIB1/2 Skw2		RW	0001: -700	0101: -300	1001: +100	1101: +500	0
Bit 1	PCIA-PCIB1/2 Skw1		RW	0010: -600	0110: -200	1010: +200	1110: +600	0
Bit 0	PCIA-PCIB1/2 Skw0		RW	0011: -500	0111: -100	1011: +300	1111: +700	0

SMBUS Table: Output Control Register

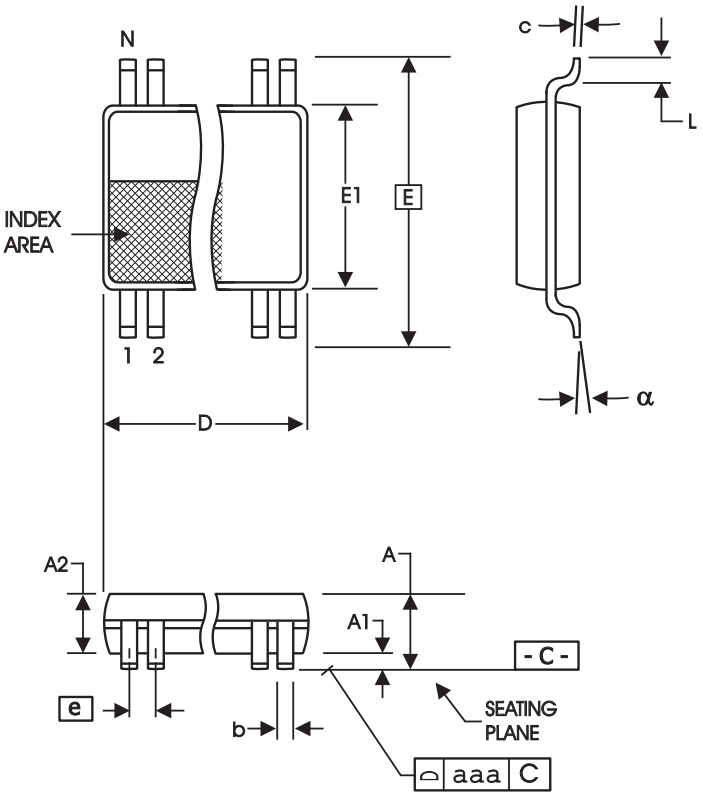
Byte 27	Name	Control Function	Type	0	1	PWD
Bit 7	AGP_3V66	AGP_3V66 Programmable Slew Rate Control	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 6	AGP_3V66		RW	10=2.0V/ns	11=2.5V/ns	1
Bit 5	REF	REF Programmable Slew Rate Control	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 4	REF		RW	10=2.0V/ns	11=2.5V/ns	1
Bit 3	SATA_100M	SATA_100M Programmable Slew Rate Control	RW	00=1.0V/ns	01=1.5V/ns	0
Bit 2	SATA_100M		RW	10=2.0V/ns	11=2.5V/ns	1
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Reserved	Reserved	RW	-	-	0

I2C Table: CPU PLL Frequency Control Register

Byte 28	Name	Control Function	Type	0	1	PWD
Bit 7	N Div11	CPU NDiv11:10	RW	Dividers used with Byte 11 and 12 to configure the CPU PLL VCO frequency.		X
Bit 6	N Div10		RW			X
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	Reserved	Reserved	RW	-	-	X
Bit 3	Reserved	Reserved	RW	-	-	X
Bit 2	Reserved	Reserved	RW	-	-	X
Bit 1	Reserved	Reserved	RW	-	-	X
Bit 0	Reserved	Reserved	RW	-	-	X

I2C Table: PCIEX PLL Frequency Control Register

Byte 29	Name	Control Function	Type	0	1	PWD
Bit 7	N Div11	PCIEX NDiv11:10	RW	Dividers used with Byte 15 and 16 to configure the PCIEX PLL VCO frequency.		X
Bit 6	N Div10		RW			X
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	Reserved	Reserved	RW	-	-	X
Bit 3	Reserved	Reserved	RW	-	-	X
Bit 2	Reserved	Reserved	RW	-	-	X
Bit 1	Reserved	Reserved	RW	-	-	X
Bit 0	Reserved	Reserved	RW	-	-	X



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9UM709BGLF	Tubes	48-pin TSSOP	0 to +70°C
9UM709BGLFT	Tape and Reel	48-pin TSSOP	0 to +70°C
9UM709BGILF	Tubes	48-pin TSSOP	-40 to +85°C
9UM709BGILFT	Tape and Reel	48-pin TSSOP	-40 to +85°C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.
"B" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	Description	Page #
0.1	1/4/2010	Initial Release	-
0.2	12/20/2010	Added I-temp specifications	Various
0.3	11/16/2011	Updated Byte 1.	
A	1/28/2014	Moved to final per characterization data.	

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