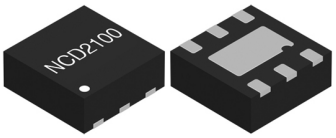
IXYS
INTEGRATED CIRCUITS DIVISION



NCD2100
Non-volatile Digital Programmable Capacitor

Features
- Wide capacitance range of 6.6pF to 37.553pF
- Small step size: 0.063pF
- Digitally select up to 1024 capacitance values.
- Operating supply voltage range of 2.5V to 5.5V
- Minimal current draw: I_{DD} = 1 µA (Typical)
- Industrial temperature range -40°C to +85°C
- Very small size
  DFN: 2 mm x 2 mm (0.079 in x 0.079 in)
  TSOT: 2.9 mm x 2.8 mm (0.114 in x 0.110 in)
- Moisture Sensitivity Level 1

Applications
- VCXOs
- Crystal Oscillators
- Tunable RF Stages
- Filter Tuning
- RFID Tags
- Industrial Wireless Controls
- Capacitive Sensor Trimming

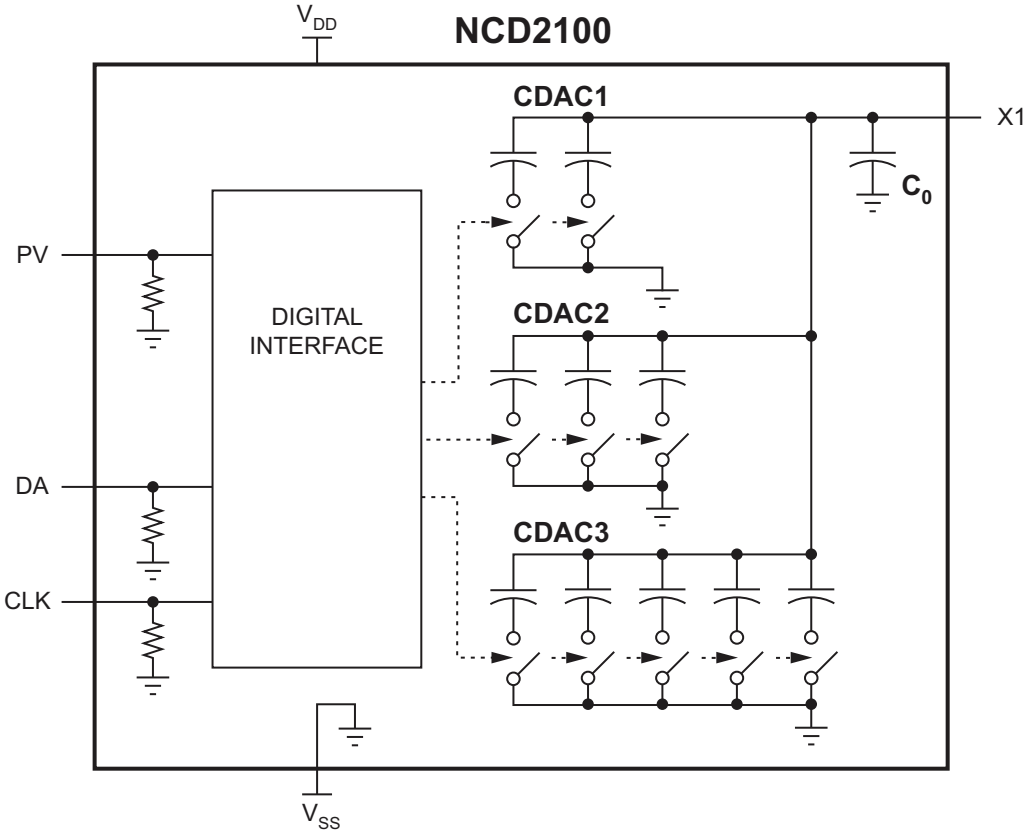
Description
The NCD2100 is an EEPROM based digitally programmable variable capacitor that provides capacitive offset trimming for capacitance sensitive circuits. Programming the non-volatile EEPROM register value or implementing on demand capacitance value changes are easily accomplished by means of the simple two-wire serial bus.

Providing 1024 discrete capacitance values over a nominal value range of 6.6pF to 37.553pF with step sizes of 0.063pF, the NCD2100 is well suited to ensure proper operation of capacitive critical circuits. Additionally, to ensure interoperability over a broad array of design environments, the NCD2100 is rated for operation with supply voltages of 2.5V to 5.5V across the temperature range of -40°C to +85°C.

Ordering Information

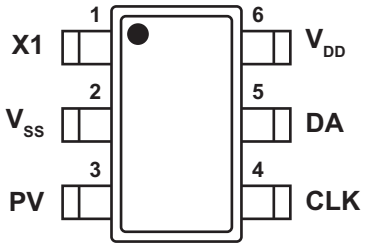
Part #	Description
NCD2100MTR	NCD2100 DFN-6 in T&R (3000/Reel)
NCD2100TTR	NCD2100 TSOT-6 in T&R (3000/Reel)

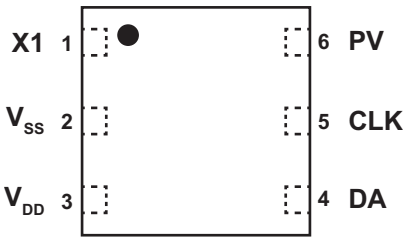
Figure 1. NCD2100 Block Diagram



1. Specifications

1.1 Package Pinout





1.2 Pin Descriptions

Pin	Name	Description
TSOT-6 Package		
1	X1	CDAC Output
2	V_{SS}	Power Supply Ground
3	PV	Programming and Verification I/O
4	CLK	Serial Bus Clock Input
5	DA	Serial Bus Data Input
6	V_{DD}	Power Supply Voltage
DFN-6 Package		
1	X1	CDAC Output
2	V_{SS}	Power Supply Ground
3	V_{DD}	Power Supply Voltage
4	DA	Serial Bus Data Input
5	CLK	Serial Bus Clock Input
6	PV	Programming and Verification I/O

Note: CLK and DA pins have a Schmitt trigger input.

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}-V_{SS}	-0.3	+ 6	V
Pins DA, CLK, and X1 Voltage	V_{SS} -0.3	V_{DD} + 0.3	V
Pin PV Voltage	V_{SS} -0.3	7.5	V
PV Pulse Width, t_{PV}	-	80	ms
Operating Temperature, T_A	-40	+85	°C
Storage temperature, T_{STG}	-55	+150	°C

Absolute maximum electrical ratings are over the operating temperature range.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DD}	2.5	3.3	5.5	V
X1 Voltage	V_{X1}	-	-	3.6	V
PV Voltage [1]	V_{PV}	6	6.5	7	V
PV Pulse Width	t_{PV}	40	50	80	ms
Operating Temperature					
Normal Operation and Shift Register Mode	T_A	-40	-	+85	°C
Programming Modes		+20	-	+30	

[1] V_{PV} applied only when programming the EEPROM.

1.5 ESD Ratings

Parameter	Symbol	Conditions	Rating	Unit
Human Body Model	HBM	EIA/JESD22-A114-D		
		All pins except X1	±2	kV
		Pin X1	±1	
Charged Device Model	CDM	EIA/JESD22-C101-C		
		All pins except X1	±500	V
		Pin X1	±250	

1.6 General Conditions for Electrical Characteristics

Typical values are characteristic of the device and are the result of engineering evaluations. They are provided for informational purposes only, and are not guaranteed by production testing.

Unless otherwise specified: Specifications cover the operating temperature range T_A = -40°C to +85°C, the supply voltage range V_{DD} = 2.5V to 5.5V and V_{PV} = 0V (or pin PV is open circuit). For testing purposes V_{DD} = 5V, the logic low input voltage is $0V_{DC}$ and the logic high input voltage is $5V_{DC}$.

1.7 Capacitor Electrical Characteristics (Pin X1)

Parameters measured at the Nominal Operating Temperature of 25±5°C, unless otherwise noted.

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Operational Frequency Range [1]	-	f_{X1}	0.2	-	250	MHz
Variation of Capacitance vs. V_{DD} [2]	Code=0 [3,5], f=50MHz	dC/dV				ppm/V
	V_{DD}=3.3V		-2635	-2790	-2800	
	V_{DD}=5V		-4305	-4785	-4795	
	Code=1023 [4,5], f=50MHz					
	V_{DD}=3.3V		-390	-455	-505	
	V_{DD}=5V		-555	-705	-785	
Temperature Drift [2]	Code=0 [3,5], f=50MHz	dC/dT				ppm/°C
	V_{DD}=3.3V		-	+207	-	
	V_{DD}=5V		-	+204.4	-	
	Code=1023 [4,5], f=50MHz					
	V_{DD}=3.3V		-	+41.4	-	
	V_{DD}=5V		-	+40.8	-	
Variation of Capacitance vs. process [2]	-	-	-25	-	+25	%

Notes:
[1] Contact the factory for operational capabilities beyond 250MHz.
[2] Simulation results (not measurements).
[3] Code=0 corresponds to “00000000000” as seen in the shift register (no additional capacitance).
[4] Code=1023 corresponds to “11111111110” as seen in the shift register (maximum additional capacitance). CHK = 0.
[5] The CHK bit is not used to determine the Code’s decimal value.
[6] Capacitance variations due to temperature are always smaller than 180fF between the nominal temperature (25°C) and maximum or minimum operating temperature.

1.8 Power Supply

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Normal Operation and Shift Register Mode					
Supply Voltage	V_{DD}	2.5	3.3	5.5	V
Supply Current	I_{DD}	-	1	50	µA
PV Voltage [1]	V_{PV}	-	0	-	V
Power Dissipation	-	-	-	100	mW
Programming Modes					
Supply Voltage	V_{DD}	4.75	5	5.25	V
Programming Voltage [2]	V_{PV}	6	6.5	7	V
Programming Current	I_{PV}	-	-	4	mA
Programming Verification					
Supply Voltage	V_{DD}	4.75	5	5.25	V

Notes:
[1] Set V_{PV}=0V or leave pin PV open circuit.
[2] V_{PV}=6.5V only when programming the EEPROM.

1.9 Digital Interface Electrical Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input Voltage						
Logic 1 Threshold	CLK and DA	V_{IH}	-	-	V_{DD}-0.5	V
Logic 0 Threshold	CLK, DA and PV	V_{IL}	0.5	-	-	
Hysteresis	CLK and DA	V_{IH} - V_{IL}	-	0.2	-	
Output Voltage	Pin PV with a 68kΩ Pull-up to V_{DD}					
Logic 1		V_{OH}	0.6 V_{DD}			V
Logic 0		V_{OL}			0.4 V_{DD}	
Pull-Down Resistors						
Pins CLK and DA	T_A = +25°C	R_{CLK}, R_{DA}	118	135	150	kΩ
	T_A = 25 ±5°C		116		154	
	-40°C ≤ T_A ≤ +85°C		101		184	
Pin PV	T_A = +25°C	R_{PV}	157	180	203	kΩ
	T_A = 25 ±5°C		155		205	
	-40°C ≤ T_A ≤ +85°C		135		245	
Input Capacitance	CLK and DA	C_{CLK}, C_{DA}	-	-	1.2	pF

1.10 Digital Interface AC Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Serial Clock						
Frequency	-	f_{CLK}	-	-	120	kHz
Duty Cycle		D_{CLK}	40	50	60	%
Serial Data						
Setup time	-	t_{setup}	1	-	-	us
Hold time		t_{hold}	1	-	-	us
Shift Register Mode						
X1 Valid delay	CLK = 1	t_{d_X1}	-	-	1	us
Programming Mode	V_{DD} = 5V, T_A = 25 ± 5°C					
PV Rising Edge delay	CLK = 1	t_{d_PV}	4	-	-	us
PV Pulse Width	V_{PV} = 6.5V	t_{PV}	40	-	80	us
CLK Falling Edge delay	PV = 0	t_{d_CLK}	0	-	-	us
X1 Valid delay	CLK = 0	t_{d_M-X1}	-	-	15	us
Programming Verification	V_{DD} = 5V, Only one input bit = logic 0					
PV Output Voltage Valid delay	CLK = 1	$t_{d\_PV\_out}$	-	-	4	us
Power Up Delay: Time before sending the first command after power supply reaches 95% of its value.	-	t_{SC}	500	-	-	µs

Figure 1: Shift Register Mode Timing Diagram

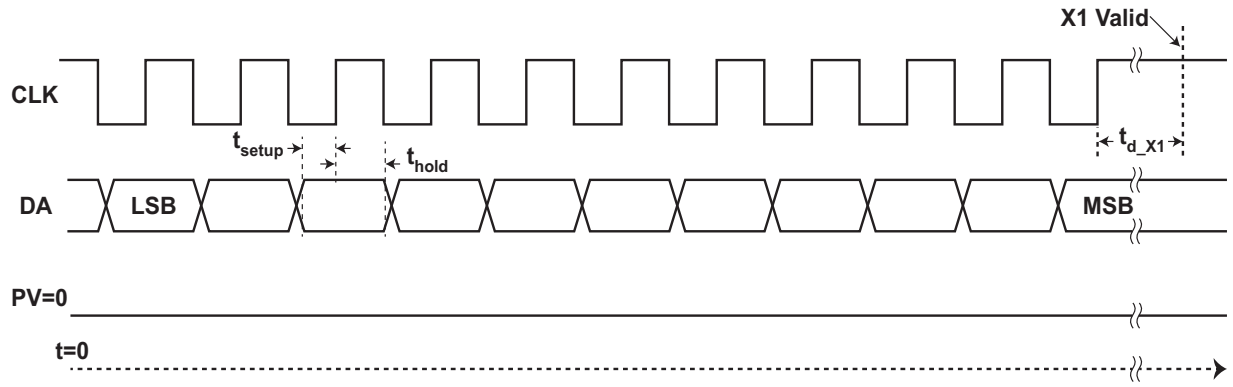


Figure 2: Programming Mode Timing Diagram

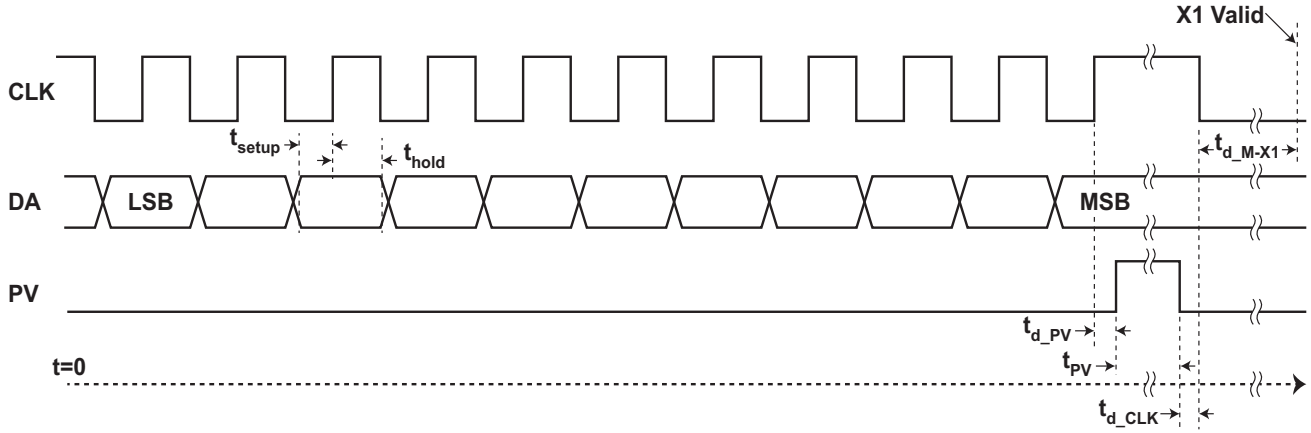
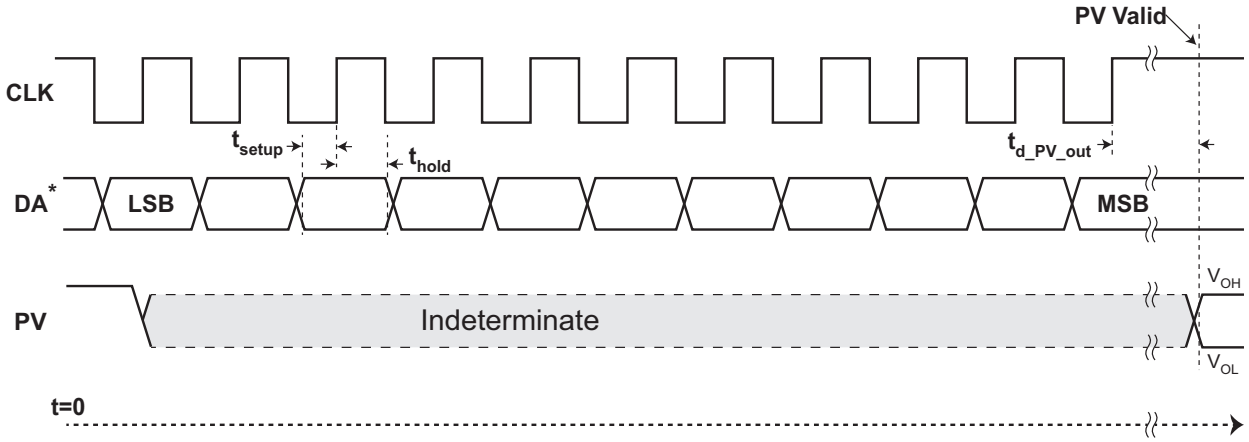
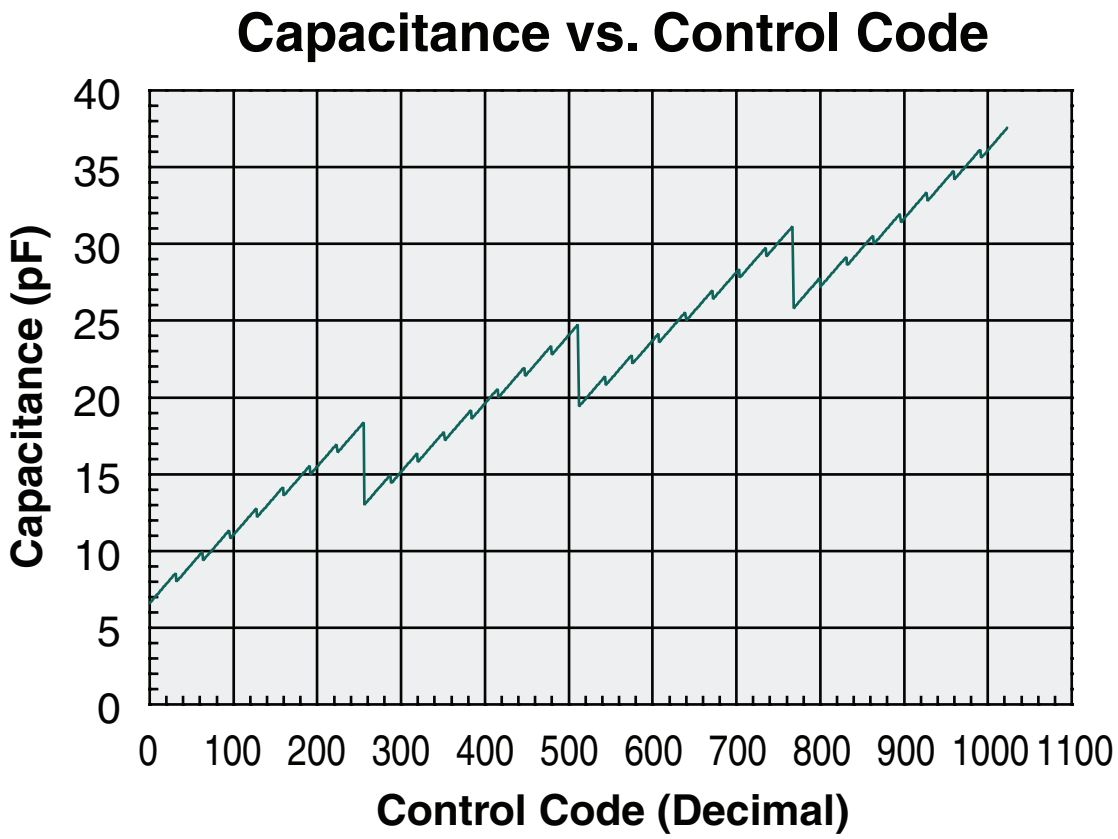


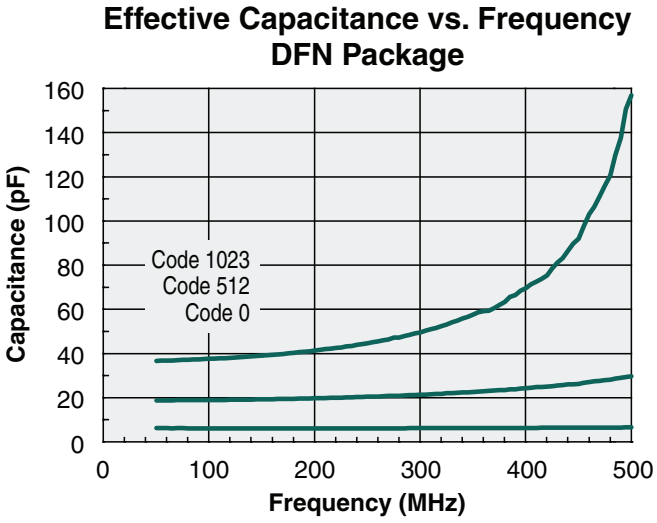
Figure 3: Programming Verification Timing Diagram

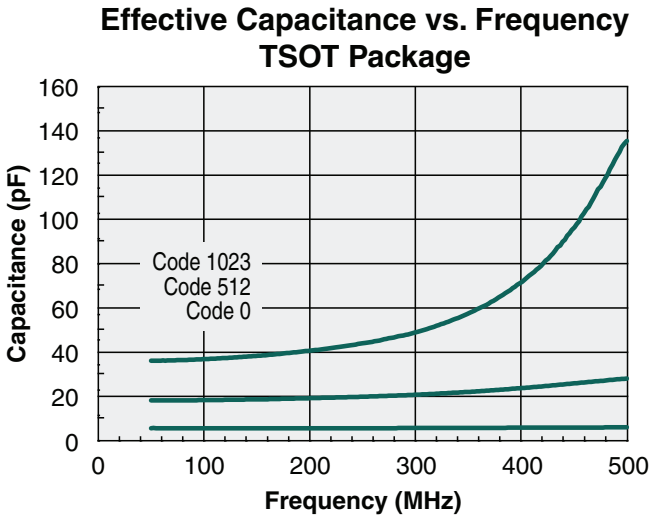


*** Only one data bit can be set to logic 0.**

2. Performance Data

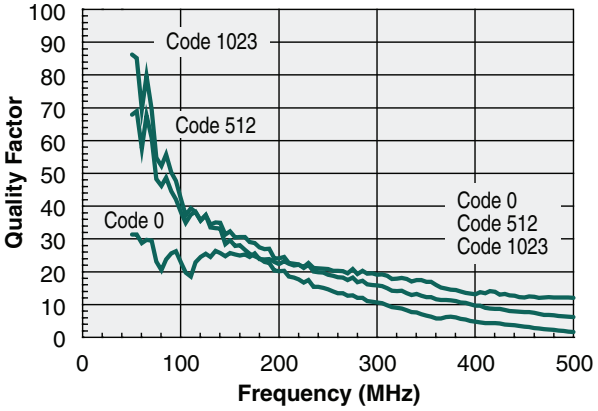




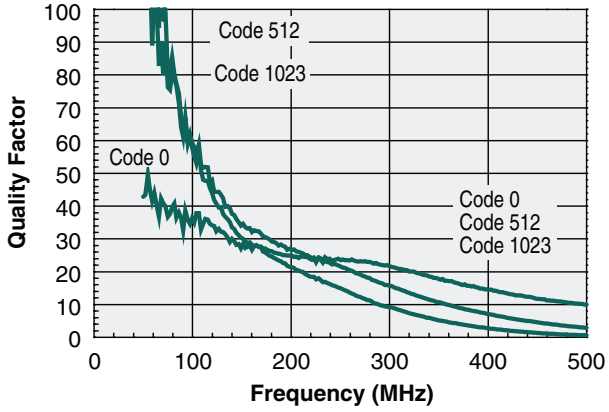


Note: The performance data shown in the graphs above is typical of device performance.

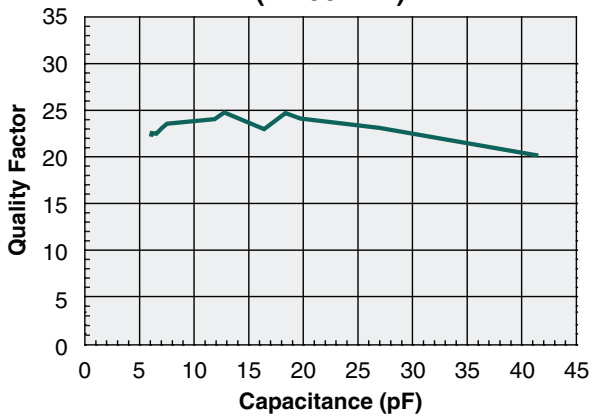
Quality Factor vs. Frequency
DFN Package



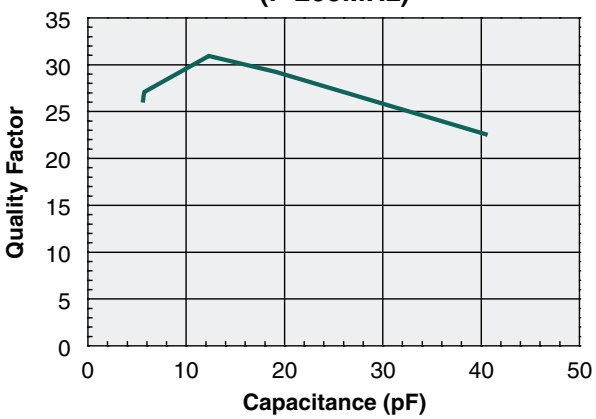
Quality Factor vs. Frequency
TSOT Package



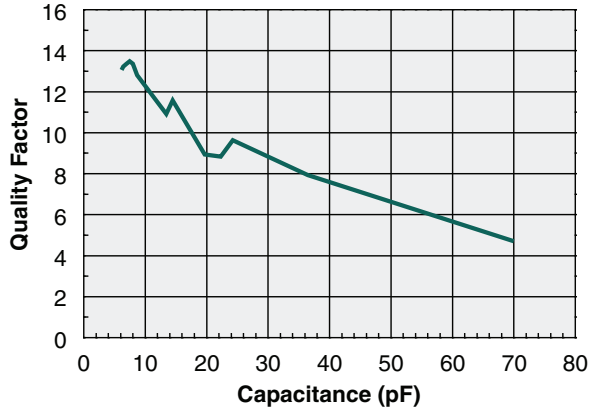
Quality Factor vs. Capacitance
DFN Package
(f=200MHz)



Quality Factor vs. Capacitance
TSOT Package
(f=200MHz)



Quality Factor vs. Capacitance
DFN Package
(f=400MHz)



Note: The performance data shown in the graphs above is typical of device performance.

3. Functional Description

3.1 Introduction

The NCD2100 provides a digitally controlled variable capacitance between its X1 pin and V_{SS}. The output capacitance is set by either the content of the shift register or by the content stored in the non-volatile memory.

By default, the value of the capacitance at X1 is based on the digital value stored in memory, but can be controlled directly with the content of the input shift register, depending on the operating mode. The memory and shift register are 11 bits wide, and are organized as follows:

Control Data Organization										
CDAC1		CDAC2			CDAC3					CHK
Bit 2	Bit 1	Bit 3	Bit 2	Bit 1	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	
10	9	8	7	6	5	4	3	2	1	0
(MSB)	<— 11-Bit Shift Register —>									(LSB)

The load capacitance presented by the NCD2100 at pin X1 is defined by:

$$C_{LOAD} = C_0 + C_1 + C_2 + C_3$$

Where:

- C_0 is the base load capacitance with a nominal value of 6.6pF, varying ±25% due to IC fabrication process variations.
- C_1 is the first coarse tuning capacitance.
- C_2 is the second coarse tuning capacitance.
- C_3 is the fine tuning capacitance.

The NCD2100 has two operating modes:

- Shift Register Mode (CLK=1): the Control Data value loaded into the shift register determines the load capacitance.
- Memory Mode (CLK=0): the Control Data value stored in the EEPROM determines the load capacitance.

In Shift Register Mode the Control Data value must be shifted in after the device powers up and can be changed as needed.

In Memory Mode, the default mode, the Control Data value is determined by the content of the internal memory that was programmed earlier. Memory mode is applicable to situations in which the required output capacitance is unlikely to change and the control data must be retained across periods of no power.

The NCD2100 has two programming modes to set the value stored in the non-volatile memory, they are:

- All-Bits Programming Mode: program all bits of the non-volatile memory simultaneously (CHK=1).
- Single-Bit Programming Mode: program a single memory bit to a logic 1 (CHK=0). In this mode the memory bits can only be set to logic 1 and only one bit at a time.

Programming methods and the tuning capacitance components are discussed below.

3.2 CDAC1: Capacitor Segment 1 (10:9)

The two bits in the first Capacitive Digital to Analog Converter (CDAC1) constitute the control bits of the first capacitance tuning segment. This CDAC is the first of two coarse capacitive tuning segments. Values of C_1 increment in nominal steps of 6.4pF, varying ±25% due to process variations.

Bit 2	Bit 1	C_1 Value
0	0	0 pF
0	1	6.4 pF
1	0	12.8 pF
1	1	19.2 pF

3.3 CDAC2: Capacitor Segment 2 (8:6)

The three bits of CDAC2 comprise the control bits of the second coarse tuning capacitance segment. These C_2 values increment in nominal steps of 1.4pF, varying ±25% due to process variations.

Bit 3	Bit 2	Bit 1	C_2 Value
0	0	0	0 pF
0	0	1	1.4 pF
0	1	0	2.8 pF
0	1	1	4.2 pF
1	0	0	5.6 pF
1	0	1	7.0 pF
1	1	0	8.4 pF
1	1	1	9.8 pF

3.4 CDAC3: Capacitor Segment 3 (5:1)

The five bits of CDAC3 comprise the control bits of the fine tuning capacitance segment. Values of C_3 increment in steps of 0.063pF, varying ±25% due to process variations.

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	C_3 Value
0	0	0	0	0	0 pF
0	0	0	0	1	0.063 pF
0	0	0	1	0	0.126 pF
0	0	0	1	1	0.189 pF
0	0	1	0	0	0.252 pF
0	0	1	0	1	0.315 pF
0	0	1	1	0	0.378 pF
0	0	1	1	1	0.441 pF
0	1	0	0	0	0.504 pF
0	1	0	0	1	0.567 pF
0	1	0	1	0	0.630 pF
0	1	0	1	1	0.693 pF
0	1	1	0	0	0.756 pF
0	1	1	0	1	0.819 pF
0	1	1	1	0	0.882 pF
0	1	1	1	1	0.945 pF
1	0	0	0	0	1.008 pF
1	0	0	0	1	1.071 pF
1	0	0	1	0	1.134 pF
1	0	0	1	1	1.197 pF
1	0	1	0	0	1.260 pF
1	0	1	0	1	1.323 pF
1	0	1	1	0	1.386 pF
1	0	1	1	1	1.449 pF
1	1	0	0	0	1.512 pF
1	1	0	0	1	1.575 pF
1	1	0	1	0	1.638 pF
1	1	0	1	1	1.701 pF
1	1	1	0	0	1.764 pF
1	1	1	0	1	1.827 pF
1	1	1	1	0	1.890 pF
1	1	1	1	1	1.953 pF

3.5 Operating Modes

The NCD2100 functions in one of two different operating modes. The load capacitance presented at pin X1 can be controlled by the value loaded into the NCD2100 shift register, or by reading the value stored in the device's internal non-volatile memory.

By default the NCD2100 operates in Memory Mode so that in most end-user applications the capacitance value corresponds to the calibration information programmed in the memory.

Whether shift register or memory mode is in use is determined by the logical state at the CLK input.

- CLK = 1: Shift Register Mode
- CLK = 0: Memory Mode

3.5.1 Shift Register Mode

Shift Register Mode provides the means to alter the load capacitance at any time. This mode varies from the Memory Mode in that the value loaded into the shift register is volatile and will be lost whenever power to the device is removed.

Because Shift Register Mode is functional over the entire operational range of the NCD2100, the capacitance presented at pin X1 can be modified under all allowable operating conditions.

Modifying the capacitance is easily accomplished by loading the 11 bit control code into pin DA using the clock (CLK), with pin PV held low or left open. When pin PV is open circuit, an internal pull down resistor having a nominal value of 180kΩ will satisfy the logic 0 requirement.

The NCD2100 utilizes a first-in first-out shift register so it is necessary to ensure only 11 rising edges of the clock are applied to the device when entering data. The least significant bit (LSB) of the serial data is the first bit entered into the shift register. This bit is CHK and does not affect the value of the capacitance. As such, bit CHK is a "Don't Care" in Shift Register Mode and may be set to either a logic 0 or a logic 1.

When the last bit is entered into the shift register, the CLK input must remain at a logic 1 for the control data in the shift register to regulate the capacitor value. Should the clock return to zero and then be pulled back up to a logic 1, the value on DA when CLK transitions to a logic 1 will be loaded into the MSB of the shift register causing the contents in bits 11:1 to shift into locations 10:0. generally resulting in an incorrect control code.

3.5.2 Memory Mode

Memory Mode is the default mode of operation as this is the most likely in-service condition for a typical application in a finished product. This operational mode uses the value stored in the non-volatile memory to configure the capacitor to the proper value.

To facilitate Memory Mode as the default mode, an internal pull down resistor at the CLK pin with a nominal value of 135kΩ. provides the required logic 0 state.

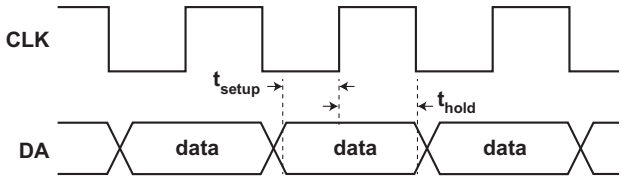
In addition to the internal pull down resistor at the CLK pin there are pull down resistors at the DA and PV pins to maintain inert logic 0 states at these inputs ensuring stable and predictable behavior without the need for supplementary external discrete components. The nominal value of the pull down resistor at the DA input is 135kΩ and the nominal value at PV is 180kΩ.

To use Memory Mode, the non-volatile memory within the NCD2100 must be programmed with the appropriate digital code to create the desired capacitive value at the X1 pin.

3.6 Serial Data Interface

Central to the NCD2100 digitally controlled variable capacitor is the serial interface. This simple two-wire interface is used to modify the output capacitance in Shift Register Mode, program the EEPROM (Programming Mode), and verify the memory contents. This interface requires only a clock (CLK) and a data line (DA) to load control data into the shift register.

With this implementation, data is latched in with the rising edge of the clock. In an application with a typical host, data change onto the bus is synchronized with the falling edge of the clock. This way, the time from when data is asserted onto the bus until the data is latched in by the rising edge of the clock is maximized. Assuming relatively equal propagation delays for both the clock and data, this configuration will maximize both the setup and hold times as shown in the waveform below.



3.7 Programming the Non-Volatile Memory

To take advantage of the default operating mode, the non-volatile memory must be programmed with a control code that provides the desired capacitance at pin X1. Two programming modes are available to the user. One mode allows for writing the entire contents of the control code into memory with a single programming sequence while the other mode restricts writing the control code to a single bit at a time and only allows changing the control bit value held in memory from a logic 0 to a logic 1. Selection of the programming mode is done with the CHK control bit.

Programming Mode Selection:

- CHK = 1: All-Bits Programming Mode
- CHK = 0: Single-Bit Programming Mode

The electrical and timing conditions that must be followed for reliable programming is the same for both programming modes.

3.7.1 Memory Programming Conditions

The NCD2100 should be programmed under the following conditions:

- T_A = +25°C±5°C
- V_{DD} = +5V±0.5V.
- CLK: f_{CLK_MAX} = 120kHz
- CLK: D_{CLK} = 50% ±10%.
- PV: Programming pulse voltage V_{PV} = +6.5V ±0.5V.
- PV: Programming pulse width 40ms ≤ t_{PV} ≤ 80ms with a 4µs delay from the last rising edge of CLK to the rising edge of the PV pulse.
- PV voltage source with minimum current compliance of 4mA.

3.7.2 Programming Control Data into Memory

The data sequence used to program the memory follows the same structure as used in Shift Register Mode with the LSB being the first bit loaded into the shift register followed by the CDAC control bits. Although the data sequence for programming the memory is the same as the Shift Register Mode, the data itself is not.

When programming the memory, the control data is not entered directly into the shift register. Rather, the bit address of a control bit to be programmed with a logic 1 is selected with a logic 0. Put another way, invert the control bit values used in Shift Register Mode and enter the inverted value into the shift register when programming the memory. This also applies to the CHK bit. For the memory circuits to recognize the All-Bits Programming Mode (CHK = 1) a logic 0 must be entered into the shift register least significant bit location. An example of this is shown in **Section 4.2.1 Figure 5 on page 15**.

3.8 Verification of Memory Contents

Once the EEPROM has been programed, the contents can be queried using the two-wire serial bus and properly configuring the PV for data retrieval.

To read the memory data output at the PV pin, it must be pulled up to V_{DD} by a 68kΩ resistor. V_{DD} and CLK must comply with the conditions specified above for programming the memory. Memory contents are read one bit at a time by loading the shift register with a logic 1 in all locations except for the bit to be queried who's location must contain a logic 0.

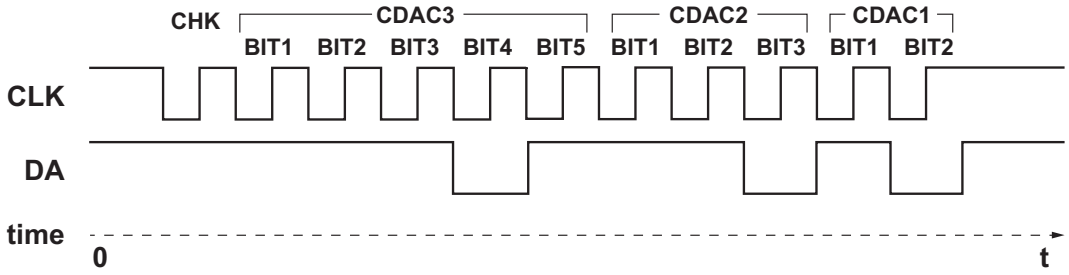
An example is shown in **Section 4.3 "Programming Verification" on page 17**.

4. Load Capacitance Programming Procedure

Determining the proper control code for the desired load capacitance and then programming the control data (trim code) into the non-volatile memory has three phases:

- Capacitance Trim Code Determination: the desired capacitance is found by loading different trim codes into the shift register using the Shift Register Mode.
- Programming the memory
- Verification of the programming

Figure 4: Trim Code Loading Sequence (Shift Register Mode)



4.1 Capacitance Trim Code Determination

In this phase, Shift Register Mode is used to find the correct capacitance value. It is determined by sweeping the CDAC1, CDAC2, and CDAC3 values. The shift register value is loaded using pins DA and CLK as explained in **"Serial Data Interface" on page 13**. Shown in **Figure 4** is an example of loading a trim code into the shift register using Shift Register Mode. The level of the signals is 0V to V_{DD}.

In this example (see **Figure 4**), the control data trim code = 375 {01011101111} (MSB ... LSB) will be entered into the shift register for a nominal output capacitance of 18.649pF. Data loaded into the shift register is LSB (CHK bit) first.

This load capacitance value is synthesized by adding the additional capacitance from CDAC1, CDAC2 and CDAC3 to the base capacitance. In this case, the capacitance value is generated as shown in the following equation:

C_{LOAD}=6.6pF+6.4pF+4.2 pF+1.449pF=18.649pF

The bits to be loaded for this configuration are:

CDAC1
- BIT2 = 0
- BIT1 = 1

CDAC2
- BIT3 = 0
- BIT2 = 1
- BIT1 = 1

CDAC3
- BIT5 = 1
- BIT4 = 0
- BIT3 = 1
- BIT2 = 1
- BIT1 = 1

CHK*
- BIT1 = 1

* In shift register mode the value of CHK is a "Don't Care," and can therefore be set to logic 1 or logic 0.

All 11 bits **(see the Control Data Organization table)** in **"Introduction" on page 10**) have to be loaded into the shift register. The host program used to load the shift register must ensure this condition is satisfied and that no additional CLK pulses be applied.

4.2 Programming the Memory

After the correct trim code is found, it should be programmed into the non-volatile EEPROM memory. There are two ways to program the memory, the selection of which is through the value of the CHK bit in the programming sequence. In the following examples, the Code = 66 (0001000010x) has been determined by means of the Shift Register Mode to provide the optimal capacitance value. Each programming mode will be explained in the following sections.

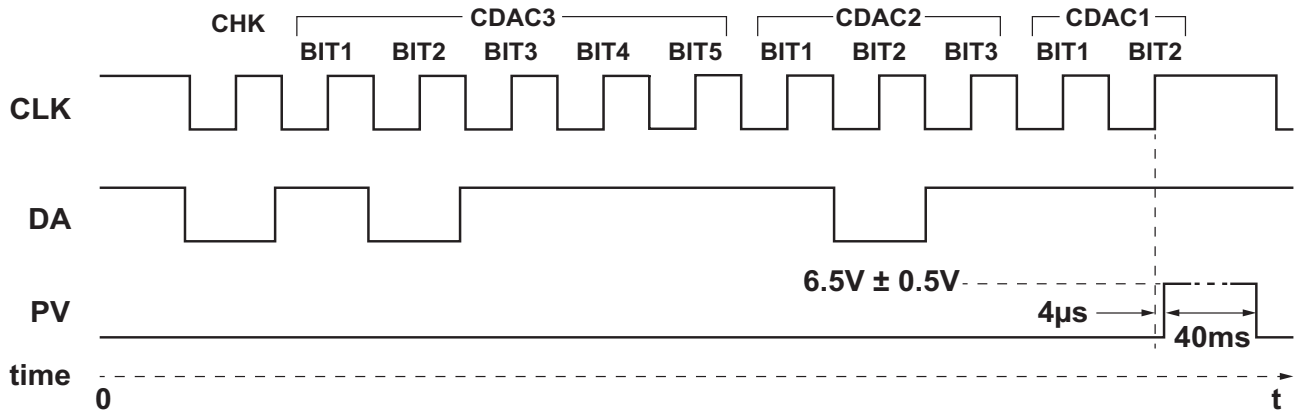
4.2.1 All-Bits Programming Mode (CHK=1)

In this programming mode, all of the bits are programmed simultaneously. The All-Bits Programming Mode has the advantage of modifying all of the memory bits with a single write and also provides the vehicle for modifying a memory bit from a logic 1 to a logic 0.

Programming the memory with the binary code 00010000101 using the All-Bits Programming Mode requires loading the shift register with the binary code 11101111010.

In order to program the memory to code = 66, the sequence shown in **Figure 5**, has to be followed. In this example, CDAC3 BIT2, CDAC2 BIT2, and CHK are being programmed to logic 1 while all the other control bits are being programmed to logic 0. Selection of which bits in memory are provisioned to logic 1 is by setting a logic 0 in that bit's address during programming.

Figure 5: All-Bits Programming Sequence



The programming steps are as follows:

1. Determine the desired capacitor value.
2. Apply the programming conditions listed in **Section 3.7.1 "Memory Programming Conditions" on page 13**.
3. Send the programming sequence shown in **Figure 5**.
4. After a 4µs delay from the rising edge of CLK for CDAC1 BIT2 the voltage at PV must be set to 6.5V±0.5V for a duration of 40ms to 80ms.
5. Return CLK to a logic 0 concurrent with or after the voltage at PV returns to a logic 0. The contents in memory set the capacitance at X1 whenever CLK = 0.
6. Verify the memory content, see **"Programming Verification" on page 17**

   Note: The 'CHK' bit is always read as logic 1 in the verification of the programming (see **"Programming Verification" on page 17**)

4.2.2 Single-Bit Programming Mode (CHK=0)

In Single-Bit Programming Mode, the memory functions as a fuse. This means that once the memory bits have programmed to a logic 1 they can not be cleared using this programming mode.

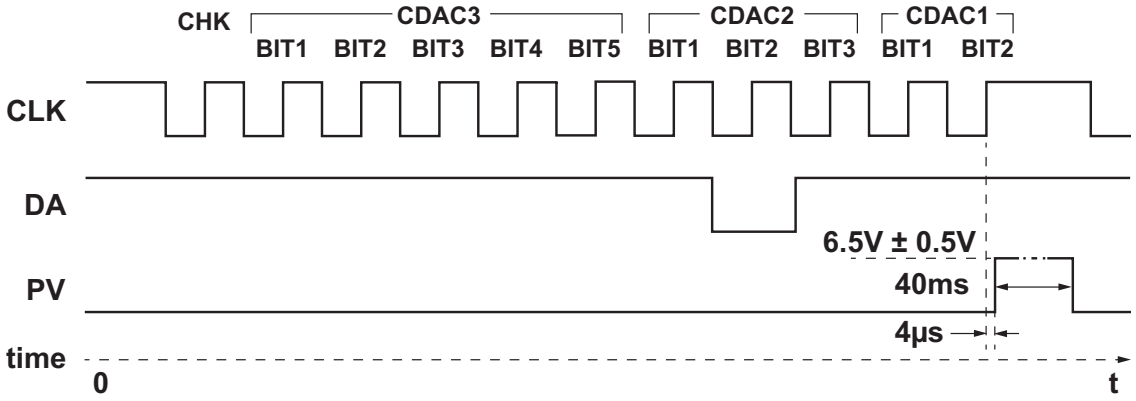
The detailed sequence for single-bit programming of the memory is:

1. Determine the desired capacitance value.
2. Apply the programming conditions listed in **Section 3.7.1 "Memory Programming Conditions" on page 13**.
3. Erase the memory content if it is not already erased (see **"Erasing the Memory" on page 17**).
4. Verify the memory content (see **"Programming Verification" on page 17**).
5. Send the programming sequence to program one bit (see example depicted in **Figure 6**).
6. After a 4µs delay, the voltage at PV pin must be set to +6.5V±0.5V for between 40ms and 80ms.
7. Repeat steps 5 & 6 for each additional memory bit that needs be set to a logic 1.
8. Verify the memory content (see **"Programming Verification" on page 17**).
   The CHK bit is always read as logic 1 during program verification.

For this example, CDAC2 BIT2 needs to be set to a logic 1. Depicted in **Figure 6** CDAC2 BIT2 is being programmed to a logic 1 in memory by loading a logic 0 into that bit's address in the shift register while all of the remaining bits in the shift register are set to logic 1. CLK loads the entire sequence of these bits into the shift register and when the last bit is loaded CLK must remain high. After a minimum wait of 4µs, set the PV pin to +6.5V±0.5V for between 40ms and 80ms to store a logic 1 into the selected EEPROM bit (in this example CDAC2 BIT2).

Should one or more memory bits need to be returned to a logic 0 the other programming mode, All-Bits Mode, can be used to make the changes.

Figure 6: Single-Bit Programming Sequence



4.3 Programming Verification

It is possible to verify the contents of the memory ONE BIT AT A TIME. The supply voltage in the verification process must be +5V±0.5V.

With an external 68kΩ pull-up resistor to V_{DD} on the PV pin, a CDAC memory bit programmed to a logic 0 will produce a voltage $\leq 0.4*V_{DD}$ on PV while a memory bit programmed to a logic 1 will produce a voltage $\geq 0.6*V_{DD}$. Reading the CHK bit will only return the logic 1 voltage of $0.6*V_{DD}$ or greater at the PV pin.

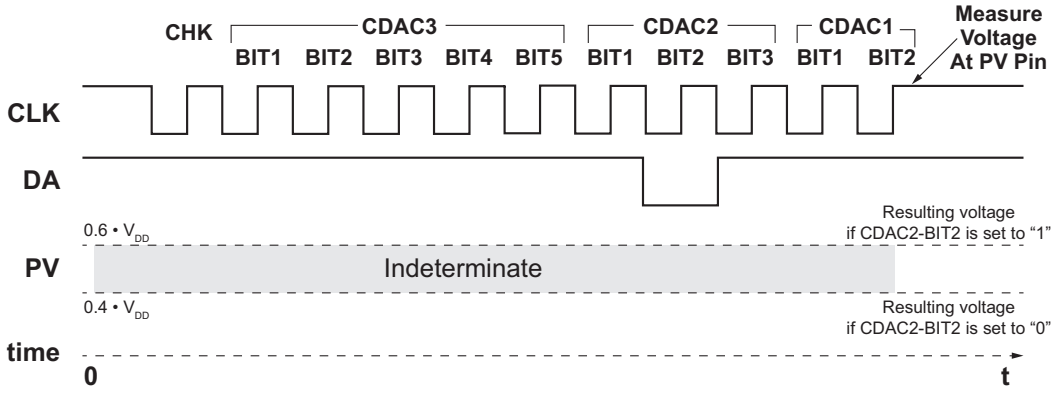
The steps that must be followed for verification are:

1. Connect a 68kΩ resistor from the V_{DD} supply to the PV pin.
2. Select the bit to be verified by setting it to logic 0 in the shift register with all the other ten bits set to a logic 1 as shown in **Figure 7**. Hold CLK = 1 after the last bit is clocked in for the duration of the measurement.
   If more than one bit is selected (set to a logic 0), the verification procedure will fail.
3. Measure the voltage at the PV pin.

Repeat steps 2-3 to verify the other bits (CDAC3 BIT5, CDAC3 BIT4, etc...)

An example of how to verify the value of the CDAC2-BIT2 bit is provided in **Figure 7**.

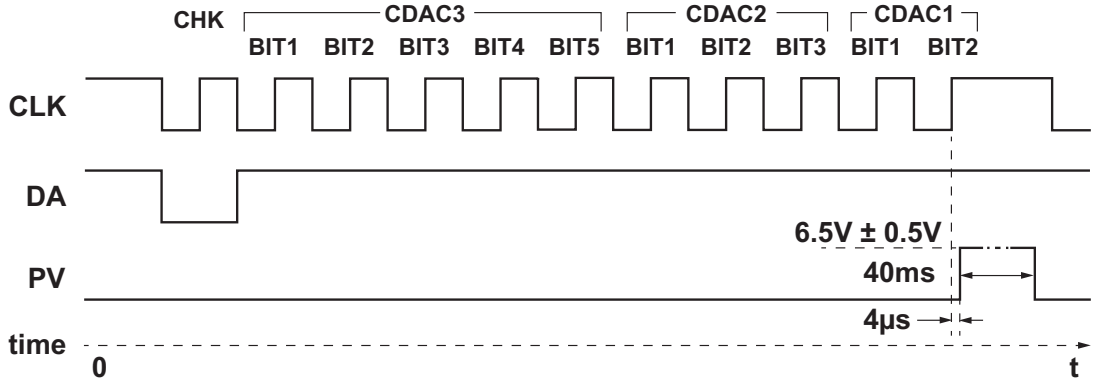
Figure 7: Sequence for Verifying the Programmed Bits



4.4 Erasing the Memory

Restoring the memory to it's initial factory default Code = 0 value is easily accomplished. The memory can be erased using a particular case of the All-Bits Programming Sequence by writing Code = 0 with CHK = 1 (00000000001). This sequence, depicted in **Figure 8**, will cause all of the EEPROM CDAC bits to clear.

Figure 8: Memory Erase Sequence



5. Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
NCD2100 All Versions	MSL 1

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

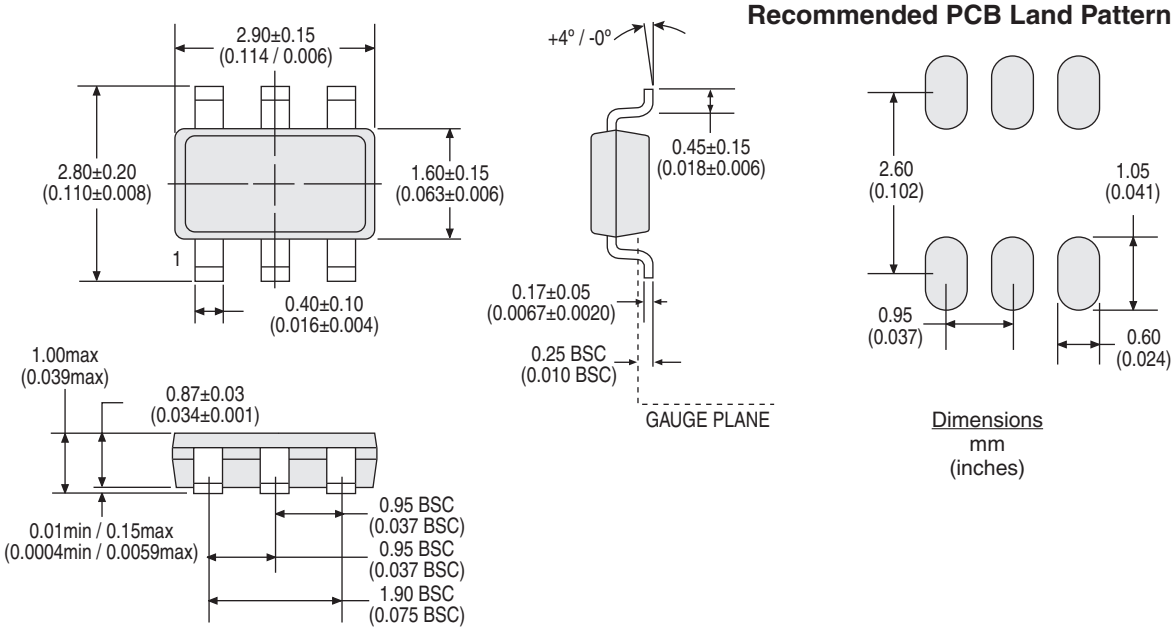
Device	Maximum Temperature and Duration	Maximum Reflow Cycles
NCD2100 All Versions	260°C for 30 seconds	3

5.4 Board Wash

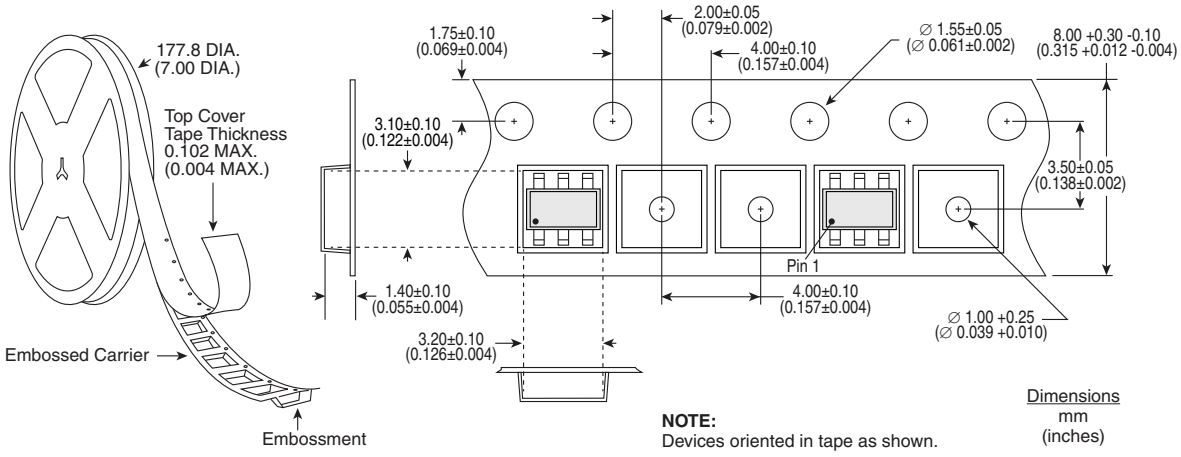
IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

5.5 Mechanical Dimensions

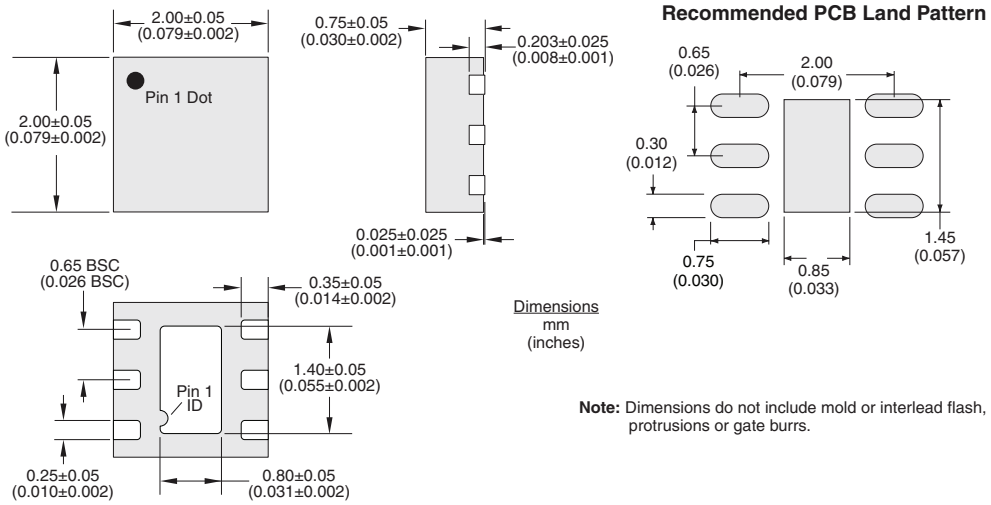
5.5.1 NCD2100T TSOT-6 Package Dimensions



5.5.2 NCD2100TTR TSOT-6 Tape & Reel Specification

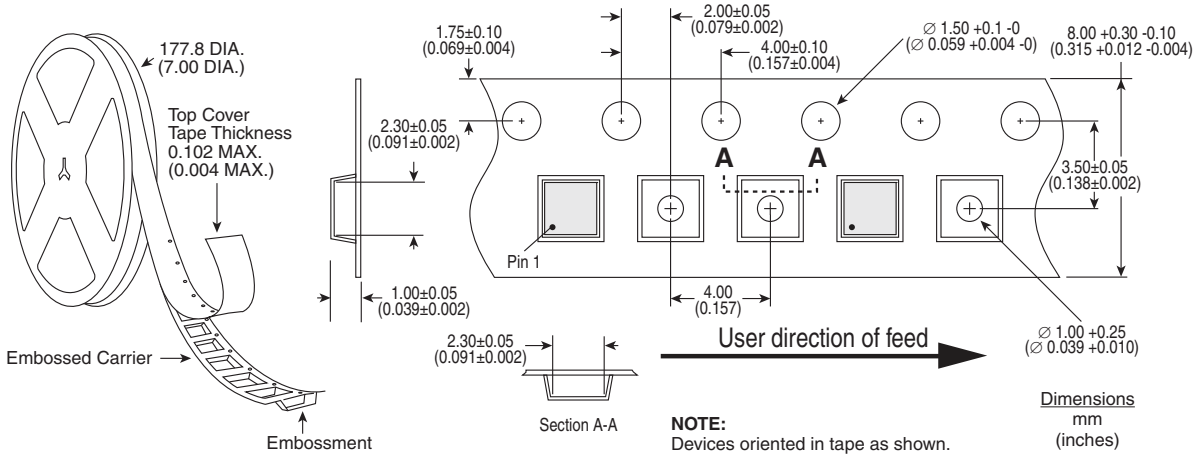


5.5.3 NCD2100M DFN-6 Package Dimensions



Note: Dimensions do not include mold or interlead flash, protrusions or gate burrs.

5.5.4 NCD2100MTR DFN-6 Tape & Reel Specification



NOTE:
Devices oriented in tape as shown.

For additional information please visit www.ixysic.com

Specifications: DS-NCD2100-R02

10/17/2014

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