SEMTECH

POWER MANAGEMENT

Description

The SC2516 is a fully integrated, Three-in-One DDR Controller supplying power to the VDDQ, VTT and GMCH rails. Two synchronous buck controller provide the VDDQ and GMCH at high efficiency, while an internal linear regulator supplies the termination voltage with 1.8A(min) Source/Sink capability.

The SC2516 uses the Intel® defined Latched BF_Cut signal to comply with motherboard state transitions. The regulator uses the 5VDUAL rail to supply VDDQ under all motherboard states, via the VDDQ switcher. The GMCH regulator is slaved off the 5V main regulator, using a separate UVLO on that rail. Additional logic and supervisory circuitry complete the functionality of this single chip DDR power solution in compliance with ACPI requirements.

The MLP package with a copper pad provides excellent thermal impedance while keeping small footprint. VDDQ short circuit protection along with VTT current limit as well as two independent thermal shutdown circuits assure safe operation under all fault conditions.

Features

◆ Uses Latched BF_Cut from Intel Glue Chip to control regulators
◆ External VDDQ divider allows DDRI or DDRII Compatibility
◆ High efficiency VDDQ switcher
◆ External GMCH divider allows 1.5V or 1.25V programming
◆ High efficiency GMCH switcher supplies programmed output from the 5V or 3.3V rail
◆ Single chip solution complies fully with ACPI power sequencing specifications
◆ 1.8A (min) VTT Source/Sink capability
◆ High current 1Amp gate driver for VDDQ switcher
◆ Independent thermal shutdown for VTT
◆ Fast transient response
◆ Space saving 22-pin MLP package with copper thermal pad for heatsinking to PC Board

Applications

◆ Power Solution for DDR memory per Intel motherboard specification
◆ High speed data line termination

Typical Application Circuit
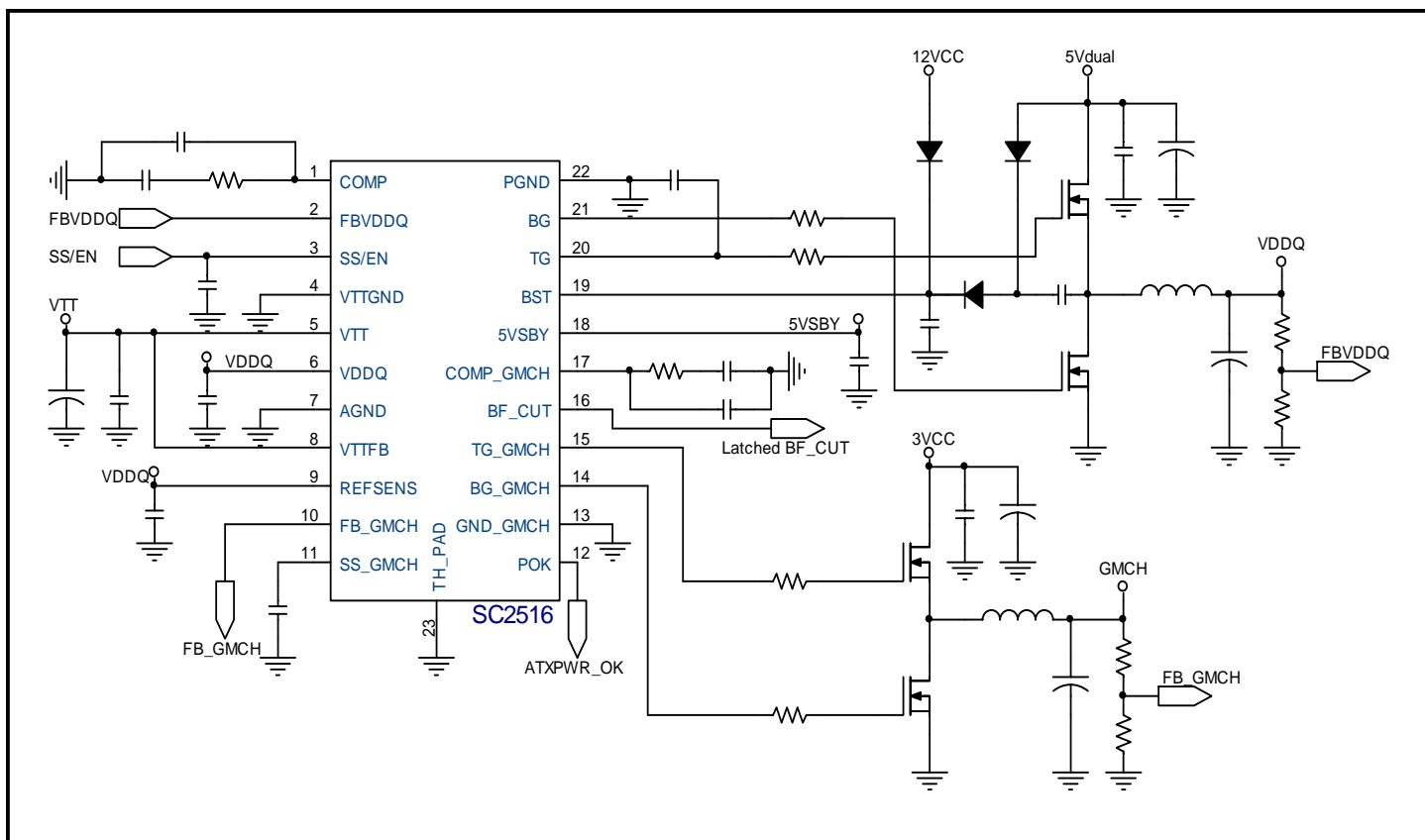
POWER MANAGEMENT

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage, BST to AGND	V_{BST}	20	V
Standby Input Voltage	V_{5VSBY}	7	V
Inputs	I/O	5VSTBY +0.3, AGND -0.3	V
AGND to PGND or LGND		0.3	V
VTT Output Current	$I_{O(VTT)}$	+/- 2	A
Operating Ambient Temperature Range	T_A	0 to 70	^{o}C
Operating Junction Temperature	T_J	125	^{o}C
Thermal Resistance Junction to Ambient	θ_{JA}	25	^{o}C/W
Thermal Resistance Junction to Case	θ_{JC}	4	^{o}C/W
Storage Temperature Range	T_{STG}	-65 to 150	^{o}C
TG/BG/TG_GMCH/BG_GMCH DC Voltage		BST + 0.3, PGND -0.3	V
TG/BG/TG_GMCH/BG_GMCH AC Voltage		BST + 1.0, PGND -4.0 t < 100 nS (measured from 50% to 50%)	V
ESD Rating (Human Body Model)	ESD	2	KV

Electrical Characteristics

Unless specified: T_A = 25 ^{o}C , 5VSBY = 5V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
5VSBY Voltage	V_{5VSBY}		4.5	5	5.5	V
Quiescent Current	$I_{Q(5VSBY)}$	BF_CUT low		12	16	mA
		BF_CUT High		8	10	
BF_CUT Threshold			0.8	TTL	2.4	V
P_OK Threshold			0.8	TTL	2.4	V
5VSBY Under Voltage Lockout	$UVLO_{5VSBY}$		2.4	2.7	3	V
VDDQ Feedback Reference	V_{REF}		1.238	1.25	1.263	V
VDDQ Feedback Current	I_{FB}	V_{FB} = 1.25V	-2			u A
SS/EN Shutdown Threshold	$V_{EN(TH)}$	VDDQ/VTT @ Shutdown	0.3	0.5		V
Thermal Shutdown	T_{J-SHDN}			150		^{o}C
Thermal Shutdown Hysteresis	T_{J-HYST}			10		^{o}C

POWER MANAGEMENT
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Switcher						
Load Regulation		I_{VDDQ} = 0A to 10A		0.2		%
Oscillator Frequency	f_{OSC}		225	250	275	KHz
Soft Start Current	I_{SS}	V_{SS} = 800mV	20	25	30	u A
Maximum Duty Cycle				75	80	%
Overcurrent Trip Voltage	V_{TRIP}	% of VDDQ Setpoint	70	75	80	%
Top Gate Rise Time	TG_R	Gate capacitance = 4000pF		25		nS
Top Gate Fall Time	TG_F	Gate capacitance = 4000pF		25		nS
Bottom Gate Rise Time	BG_R	Gate capacitance = 4000pF		35		nS
Bottom Gate Fall Time	BG_F	Gate capacitance = 4000pF		35		nS
Dead Time	t_d		20	50	80	nS
Error Amplifier Transconductance	G_m		0.8	1	1.2	mS
Error Amplifier Gain @ DC	A_{EA}	R_{COMP} = open		38		dB
Error Amplifier Bandwidth	G_{BW}			5		MHz
Error Amplifier Source Current		FB = 0 , COMP = 1V	55	70	85	u A
Error Amplifier Sink Current		FB = 1.5V , COMP = 1V	70	90	110	u A
Internal Ramp	V_{RAMP}	Peak - to - Peak		0.55		V
VTT LDO						
Output Voltage	VTT	V_{VDDQ} = 2.500V	1.235	1.250	1.265	V
Source and Sink Currents	I_{VTT}	V_{VDDQ} = 2.500V	-1.8		+1.8	A
Source and Sink Currents	I_{VTT}	V_{VDDQ} = 1.500V	-1.4		+1.4	A
Load Regulation	$\Delta VTT/ \Delta I$	I_{VTT} =+1.8A to -1.8A	-1		+1	%
Error Amplifier Gain	A_{EA_VTT}			75		dB
Current Limit	VTT_{ILIM}	BF_CUT = low		3		A

POWER MANAGEMENT

Electrical Characteristics (Cont.)

Unless specified: $T_A = 25^oC$, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
GMCH Switcher						
GMCH Feedback Reference	V_{REF_GMCH}		1.238	1.25	1.263	V
GMCH Feedback current	I_{FB_GMCH}	V_{FB_GMCH} = 1.25V	-2			uA
Load Regulation		I_{GMCH} = 0A to 5A		0.2		%
Oscillator Frequency	f_{OSC}		225	250	275	KHz
Soft start current	I_{SS_GMCH}	V_{SS} = 200mV	8	10	12	u A
Maximum Duty Cycle				75	80	%
Top Gate Rise Time	TG_R	Gate capacitance = 2000pF		40		nS
Top Gate Fall Time	TG_F	Gate capacitance = 2000pF		40		nS
Bottom Gate Rise Time	BG_R	Gate capacitance = 2000pF		40		nS
Bottom Gate Fall Time	BG_F	Gate capacitance = 2000pF		40		nS
Dead Time	t_d		50	85	120	nS
Error Amplifier Transconductance	G_m		0.8	1	1.2	mS
Error Amplifier Gain @ DC	A_{EA}			38		dB
Error Amplifier Bandwidth	G_{BW}			1		MHz
Error Amplifier Sink/Source Current		V_{FB_GMCH} = 0 - 1.5V, COMP = 1V	60	75	90	uA
Internal Ramp	V_{RAMP}	Peak - to - Peak		0.55		V

Pin Configuration

TOP VIEW

```
        COMP  [ 1      22 ]  PGND
       FBVDDQ [ 2      21 ]  BG
         SS/EN [ 3      20 ]  TG
       VTTGND [ 4      19 ]  BST
          VTT [ 5      18 ]  5VSBY
         VDDQ [ 6      17 ]  COMP_GMCH
         AGND [ 7      16 ]  BF_CUT
        VTTFB [ 8      15 ]  TG_GMCH
      REFSENS [ 9      14 ]  BG_GMCH
      FB_GMCH [ 10     13 ]  GND_GMCH
      SS_GMCH [ 11     12 ]  POK
```

SC2516

Note: Pin 23 is the thermal Pad on the bottom of the device
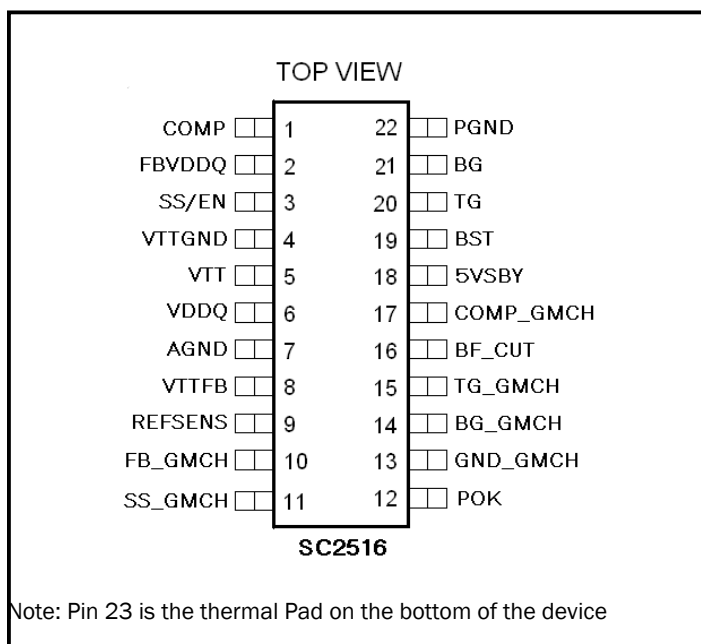
Ordering Information

| Part Numbers	Package
SC2516MLTR[1]	MLP-22
SC2516MLTRT[1],[2]	MLP-22

Notes:
(1) Only available in tape and reel packaging.
    A reel contains 3000 devices.
(2) Lead free package. Device is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	COMP	Compensation pin for the PWM transconductance amplifier for the VDDQ Switcher.
2	FBVDDQ	Feedback for the VDDQ regulator. Connect to the VDDQ sense at the point of load.
3	SS/EN	Soft start capacitor to GND. Pull low to disable controller.
4	VTTGND	VTT return. Connect to copper plane carrying VTT return current. The trace connecting to this pin must be able to carry 2 Amps.
5	VTT	VTT Regulator output. Regulates to 1/2 VDDQ. Sources or sinks 1.8 Amps. The trace connecting to this pin must be able to carry 2 Amps.
6	VDDQ	VDDQ power input to VTT LDO. The trace connecting to this pin must be able to carry 2 Amps.
7	AGND	Analog ground. Compensation components and the Soft Start Capacitor connect to this ground.
8	VTTFB	Sense input for the VTT regulator. Connect to Point of Load for the VTT rail.
9	REFSNS	Sense input for the VDDQ rail. VTT will be regulated to 1/2 of its voltage. Connect to Point of Load, where the VREF for the memory is generated.
10	FB_GMCH	Sense input for the GMCH. Connect to Point of Load for the GMCH rail.
11	SS_GMCH	Soft start for GMCH switcher . Connect a capacitor to GND.
12	POK	Connect to power OK signal from ATX power.
13	GND_GMCH	Gate Drive return Ground for the GMCH regulator. Connect to Source of bottom FET.
14	BG_GMCH	Bottom FET Gate drive for the GMCH regulator.
15	TG_GMCH	Top FET Gate drive for the GMCH regulator.
16	BF_CUT	Latched BF_CUT input from Glue Chip.
17	COMP_GMCH	Compensation pin for the PWM transconductance amplifier for the GMCH Switcher
18	5VSBY	Connect to 5VSTBY input.
19	BST	The Top and Bottom Gate drive bus.Generated using bootstrap diode/capacitor. An additional diode is also required to trap the peak Bootstrap voltage for the BG drive. (see typical application circuit)
20	TG	Top FET gate drive.
21	BG	Bottom FET gate drive.
22	PGND	Gate drive return. Keep this pin close to bottom FET source.
23	TH_PAD	Copper pad on bottom of chip used for heatsinking. It must be connected to ground plane under IC.
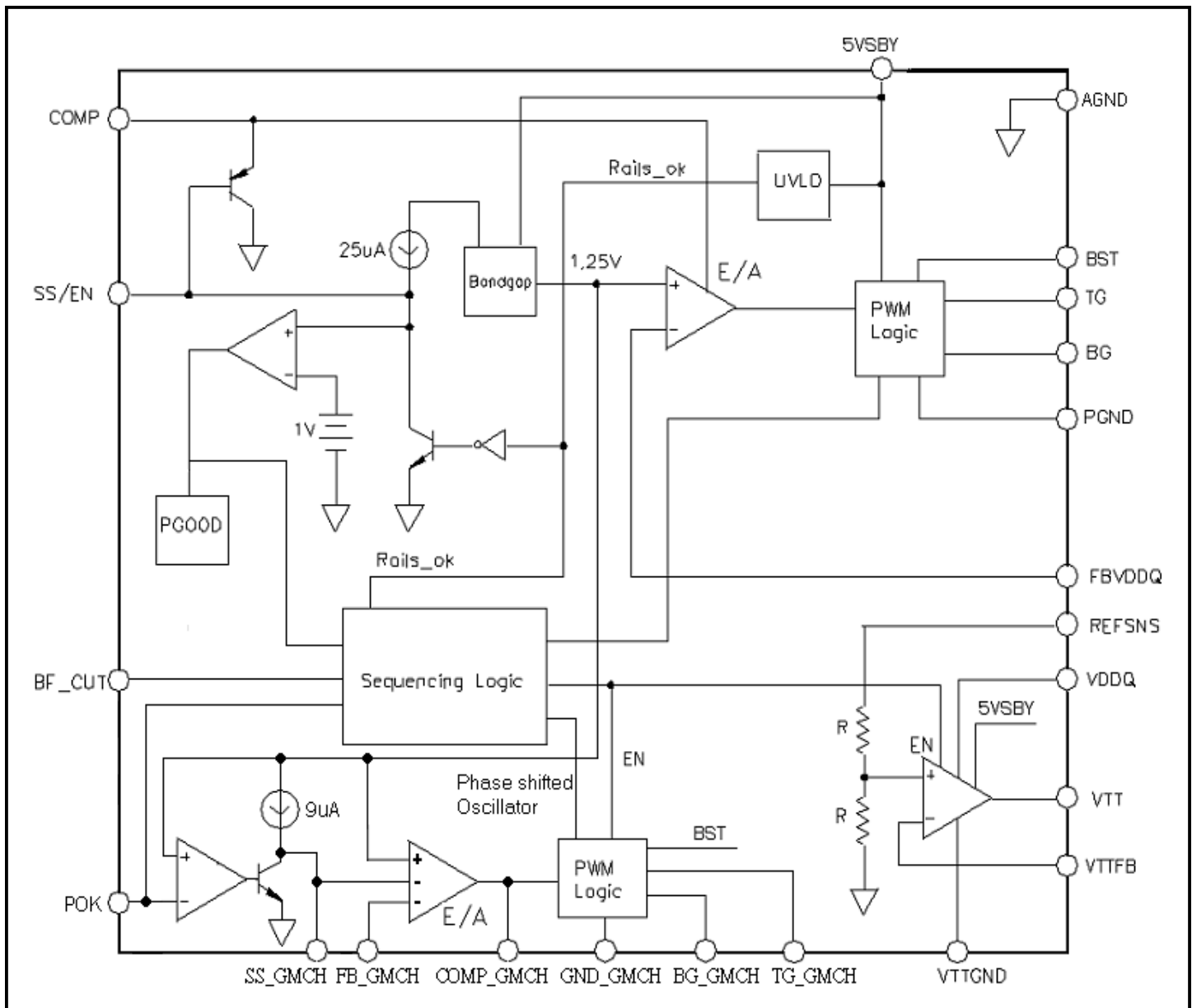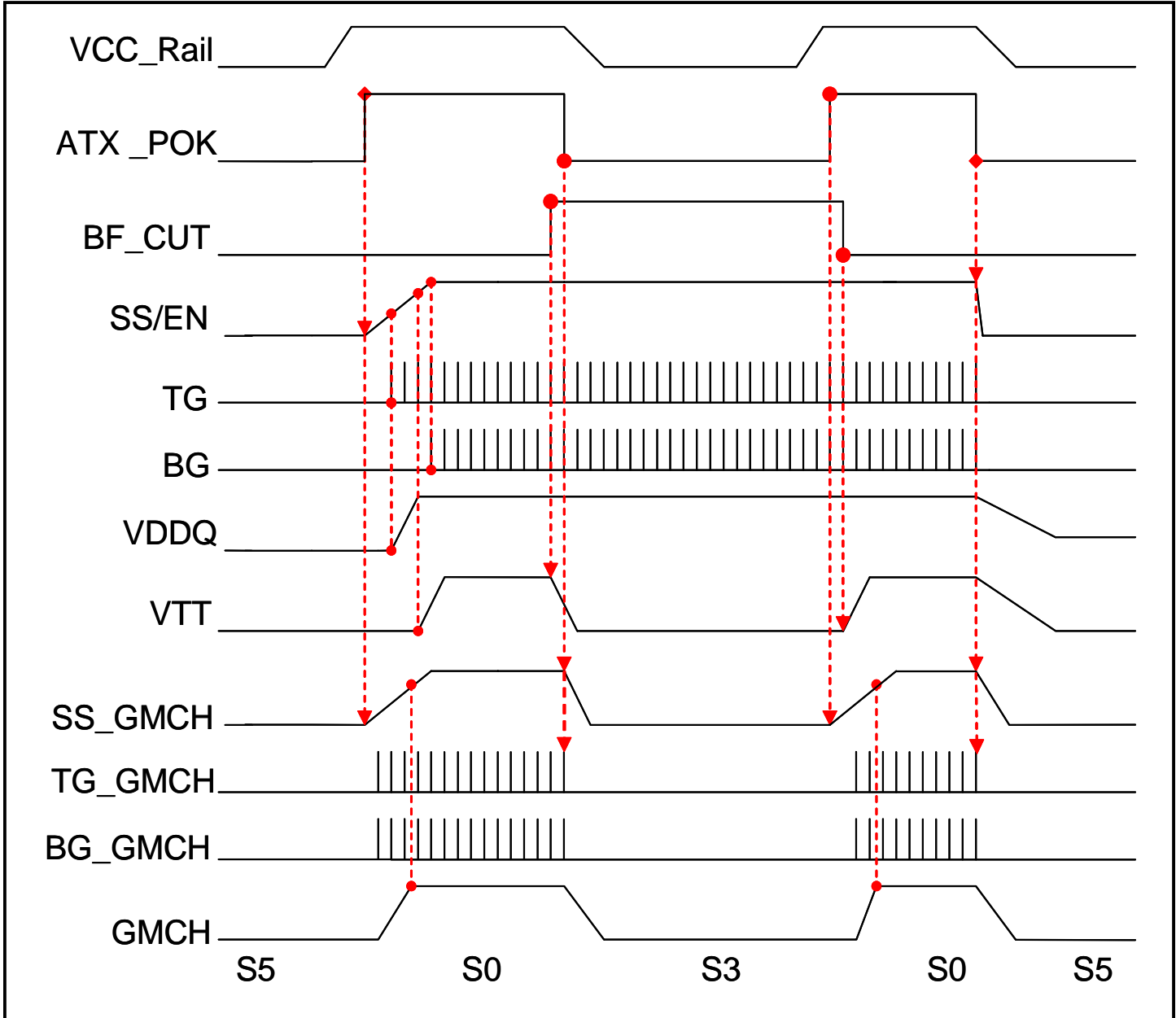
Application information

Description

The SEMTECH SC2516 DDR power supply controller is the latest and most complete, Three in One switching and linear regulator controller, providing the necessary functions to comply with S3 and S5 sleep state signals generated by the Desktop Computer Motherboards. The SC2516 uses the Latched BF_CUT input signal which is generated externally on Intel[R] P4 Motherboard glue chip to comply with the power sequencing requirements. Logically, the BF_CUT signal can be represented as:

$$BF\_CUT = \overline{\overline{S3} \bullet P\_OK}$$

(For details of the Latched BF_CUT signal definition, refer to Intel documentation).

Where S3 is the input to the Silver-box Supply for Suspend to RAM, (S3=1 for Suspend to RAM) and P_OK is a signal generated by the Silver-box supply, indicating that all rails are within specification.

S3 and S5 States

During S3 and S5 sleep states, The operation of the VDDQ and VTT is governed by the intel[R] specifications with regards to the BF_CUT signal. The timing diagram demonstrates the state of the controller and each of the VDDQ, VTT and GMCH supplies during S3 and S5 transitions

VDDQ Power Section

SC2516 architecture eliminates the need for the Back-Feed Cut MOSFET, since the VDDQ is always supplied from the same input voltage bus (5V dual). The SC2516 is capable of driving a 4000pf capacitor in 25ns (typical, top gate). This drive capability allows 15-20A DC load on the VDDQ supply from the 5V main input rail.

Power Sequencing

Once BF_CUT signal low and P_OK signal goes high, The VDDQ supply will be activated with S0 as well. The SS/EN pin voltage is charged by internal constant current source. When SS/EN voltage reaches to 0.3V (typical), High side driver begins chopping and main power is activated as an asynchronous Buck converter. When SS/EN voltage reaches to 1.25V (typical), Low side driver begins chopping and main power is activated as a synchronous Buck converter.

When BF_CUT signal goes high (S3 state), the VDDQ switcher is always on and is sourced by 5VSTBY rail during this time.

When both BF_CUT and P_OK signals are low, The VDDQ supply be disabled with S5 as well. Both high side and low side drivers are pulled low.

Short Circuit Protection

Short circuit protection is implemented by sensing the VDDQ output voltage. If it falls to 75% (typical) of its nominal voltage, as sensed by the FB pin, the TG and BG pins are latched off and the VDDQ switcher is shutdown. It will shutdown the VTT also, since the VTT regulator is fed from the VDDQ bus. To recover from the short circuit protection mode, either the 5VSBY rail has to be recycled, or the SS/EN pin must be pulled below 0.3V and released to restart VDDQ switcher operation.

GMCH Power Section

The SC2516 Switching controller supplies a 1.5V or 1.25V GMCH (Graphic Memory Control Hub) voltage via a standard synchronous BUCK converter typically connected to the 5VCC or 3.3VCC power rail from Silver-box supply. Base on the basic advantage of switching mode controller, The GMCH output current can support up to 20A.

Power Sequencing

Since the Chip-Set supply should come up before the Active Memory cycle, the GMCH supply is sequenced with the rising edge of the P_OK signal from Sliver-box supply. Thus the GMCH regulator drivers are on when P_OK signal is greater than its respective threshold. The external MOSFET gates are pulled low when P_OK signal is lower than its threshold. Thus the GMCH is disabled during S3 and S5 (See timing diagram).

VTT Rail

The VTT termination voltage is supplied via an internal sink/source linear regulator when BF_CUT is low, and the P_OK signal has met its threshold voltage and SS/EN voltage reaches to 1V. When BF_CUT is high, the VTT termination voltage is not needed and is thus tri-stated. The VTT linear regulator is capable of sourcing and sinking 1.8 Amps (Minimum). It is recommended that one should use at least 470uF low ESR capacitor and 1uF ceramic capacitor (from VTT pin to Ground with short distance) to ensure the stable operation.

Short Circuit Protection

The VTT regulator has two internal current limit circuits, one for the sink and one for the source regulators. Both current limits are set at 3Amp (typical). If maintained at current limit, the internal regulators act like constant current sources, and supply the max current until the device temperature raises above thermal shutdown thresholds, at which point that regulator shuts down.
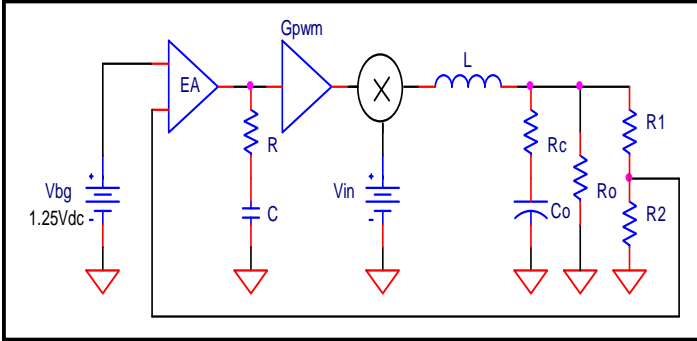
Applications Information (Cont.)

Fig. 1. SC2516 small signal model.

Compensation design of the VDDQ Channel

The control model of SC2516 VDDQ and GMCH section can be depicted in Fig. 1. This model can also be used in Spice kind of simulator to generate loop gain Bode plots. The bandgap reference is 1.25 V and trimmed to +/-1% accuracy. The desired output voltage can be achieved by setting the resistive divider network, R1 and R2.

The error amplifier is transconductance type with fixed gain of:

$$G_m := \frac{0.001 \cdot A}{V}$$

The compensation network includes a resistor and a capacitor in series, which terminates from the output of the error amplifier to the ground. The PWM gain is inversion of the ramp amplitude, and this gain is given by:

$$G_{pwm} := \frac{1}{V_{ramp}}$$

where the ramp amplitude (peak-to-peak) is 0.55 volts .

The total control loop-gain can then be derived as follows:

$$T(s) = T_o \cdot \left(\frac{1 + s \cdot R \cdot C}{s \cdot R \cdot C} \right) \cdot \frac{1 + s \cdot R_c \cdot C_o}{1 + s \cdot \left(R_c \cdot C_o + \frac{L}{R_o} \right) + s^2 \cdot L \cdot C_o \cdot \left(1 + \frac{R_c}{R_o} \right)}$$

where

$$T_o := G_m \cdot G_{pwm} \cdot V_{in} \cdot R \cdot \left(\frac{V_{bg}}{V_o} \right)$$

The task here is to properly choose the compensation network for a nicely shaped loop-gain Bode plot. The following design procedures are recommended to accomplish the goal:

(1) Calculate the corner frequency of the output filter:

$$F_o := \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_o}}$$

(2) Calculate the ESR zero frequency of the output filter capacitor:

$$F_{esr} := \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o}$$

(3) Check that the ESR zero frequency is not too high.

$$F_{esr} < \frac{F_{sw}}{5}$$

If this condition is not met, the compensation structure may not provide loop stability. The solution is to add some electrolytic capacitors to the output capacitor bank to correct the output filter corner frequency and the ESR zero frequency. In some cases, the filter inductance may also need to be adjusted to shift the filter corner frequency. It is not recommended to use only high frequency multi-layer ceramic capacitors for output filter.

(4) Choose the loop gain cross over frequency (0 dB frequency). It is recommended that the crossover frequency is always less than one fifth of the switching frequency :

$$F_{x\_over} \leq \frac{F_{sw}}{5}$$

If the transient specification is not stringent, it is better to choose a crossover frequency that is less than one tenth of the switching frequency for good noise immunity. The resistor in the compensation network can then be calculated as:

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_m} \cdot \left(\frac{F_{esr}}{F_o} \right)^2 \cdot \left(\frac{F_{x\_over}}{F_{esr}} \right) \cdot \left(\frac{V_o}{V_{bg}} \right)$$

when

$$F_o < F_{esr} < F_{x\_over}$$

POWER MANAGEMENT

Applications Information (Cont.)

or

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_m} \cdot \left(\frac{F_o}{F_{esr}}\right)^2 \cdot \left(\frac{F_{x\_over}}{F_o}\right) \cdot \left(\frac{V_o}{V_{bg}}\right)$$

when

$$F_{esr} < F_o < F_{x\_over}$$

(5) The compensation capacitor is determined by choosing the compensator zero to be about one fifth of the output filter corner frequency:

$$F_{zero} := \frac{F_o}{5}$$

$$C := \frac{1}{2 \cdot \pi \cdot R \cdot F_{zero}}$$

(6) The final step is to generate the Bode plot, either by using the simulation model in Fig. 1 or using the equations provided here with Mathcad. The phase margin can then be checked using the Bode plot. Usually, this design procedure ensures a healthy phase margin.

(7) An additional capacitor should be reserved at the compensation pin to ground to have another high frequency pole.

An example is given below to demonstrate the procedure introduced above. The parameters of the power supply (typical for VDDQ section) are given as :

$$V_{in} := 5 \cdot V$$

$$V_o := 2.5 \cdot V$$

$$I_o := 20 \cdot A$$

$$F_{sw} := 250 \cdot KHz$$

$$L := 2.2 \cdot \mu H$$

$$C_o := 4500 \cdot \mu F$$

$$R_c := 0.01 \cdot \Omega$$

$$V_{bg} := 1.25 \cdot V$$

$$V_{ramp} := 0.55 \cdot V$$

$$G_m := \frac{0.001 \cdot A}{V}$$

Step 1. Output filter corner frequency

$$F_o = 1.6 \text{ KHz}$$

Step 2. ESR zero frequency:

$$F_{esr} = 3.537 \text{ KHz}$$

Step 3. Check the following condition:

$$F_{esr} < \frac{F_{sw}}{5}$$

Which is satisfied in this case.

Step 4. Choose crossover frequency and calculate compensator R:

$$F_{x\_over} = 50 \text{ KHz}$$

$$R = 15 \text{ K}\Omega$$

Step 5. Calculate the compensator C:

$$C = 33 \text{ nF}$$

Step 6. Generate Bode plot and check the phase margin. In this case, the phase margin is about 85°C that ensures the loop stability. Fig. 2 shows the Bode plot of the loop.

Compensation design of the GMCH Channel

The configuration of the PWM comparator of GMCH channel is such that its inverter input is connected to Comp_GMCH and the non-inverter input is connected to the internal ramp. The peak voltage of the internal ramp is 1.1V and the valley voltage is 0.55V. When COMP_GMCH voltage is below 0.55V, the maximum duty cycle will be generated by PWM comparator. If COMP_GMCH voltage is over 1.1V then the minimum duty cycle will be generated.

To ensure proper soft start function of the GMCH channel, COMP_GMCH voltage must rise above 1.1V at the beginning of soft start period quickly. So a higher compensation gain is required. The following example shows that by choosing the compensation parameters as 15kOhm and 27nF for a typical output filter with 1~2uH inductor and 2000uF capacitor (ESR of 8~12 mOhm), the circuit will yield smooth soft start, stable control loop, and satisfactory transient response. The measured Bode plot of the loop gain is shown in Figure 3.
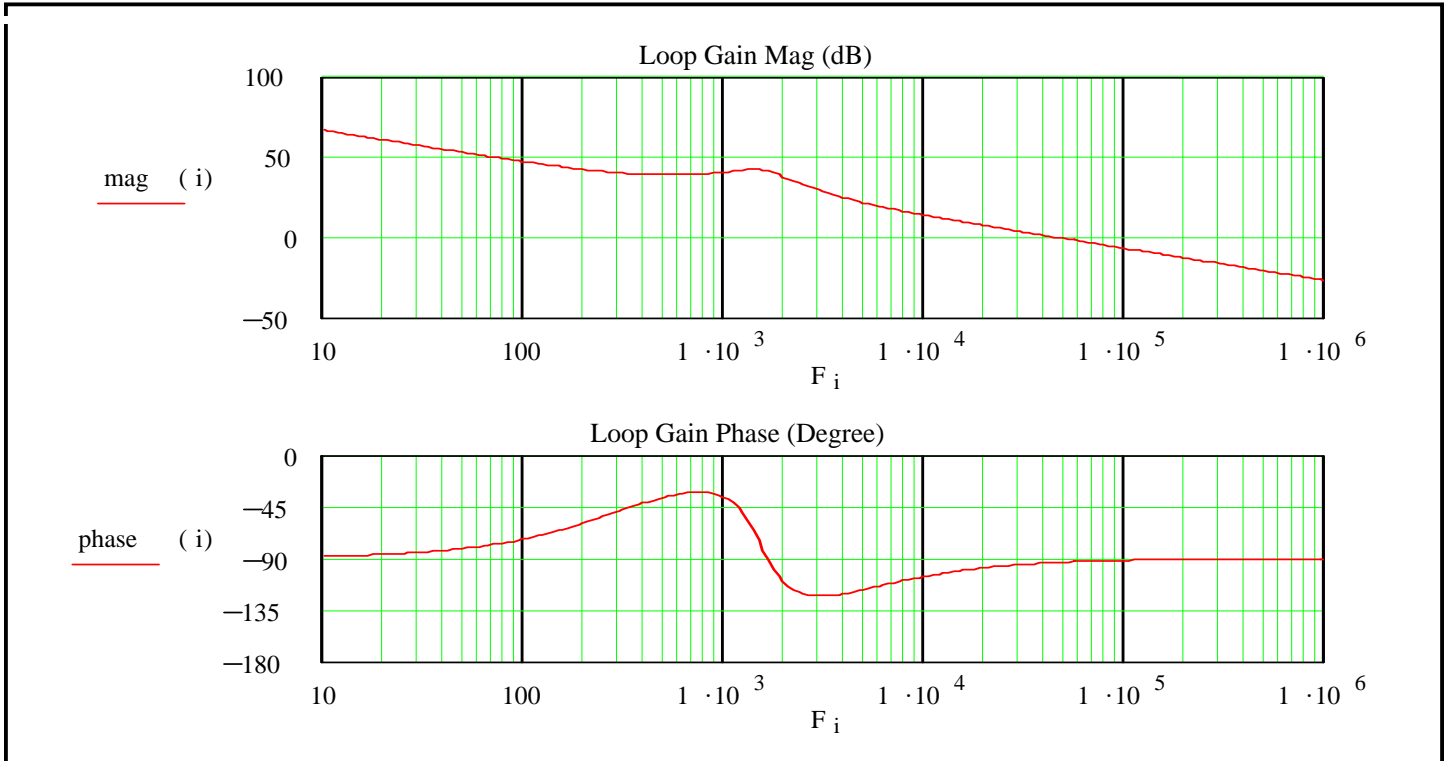
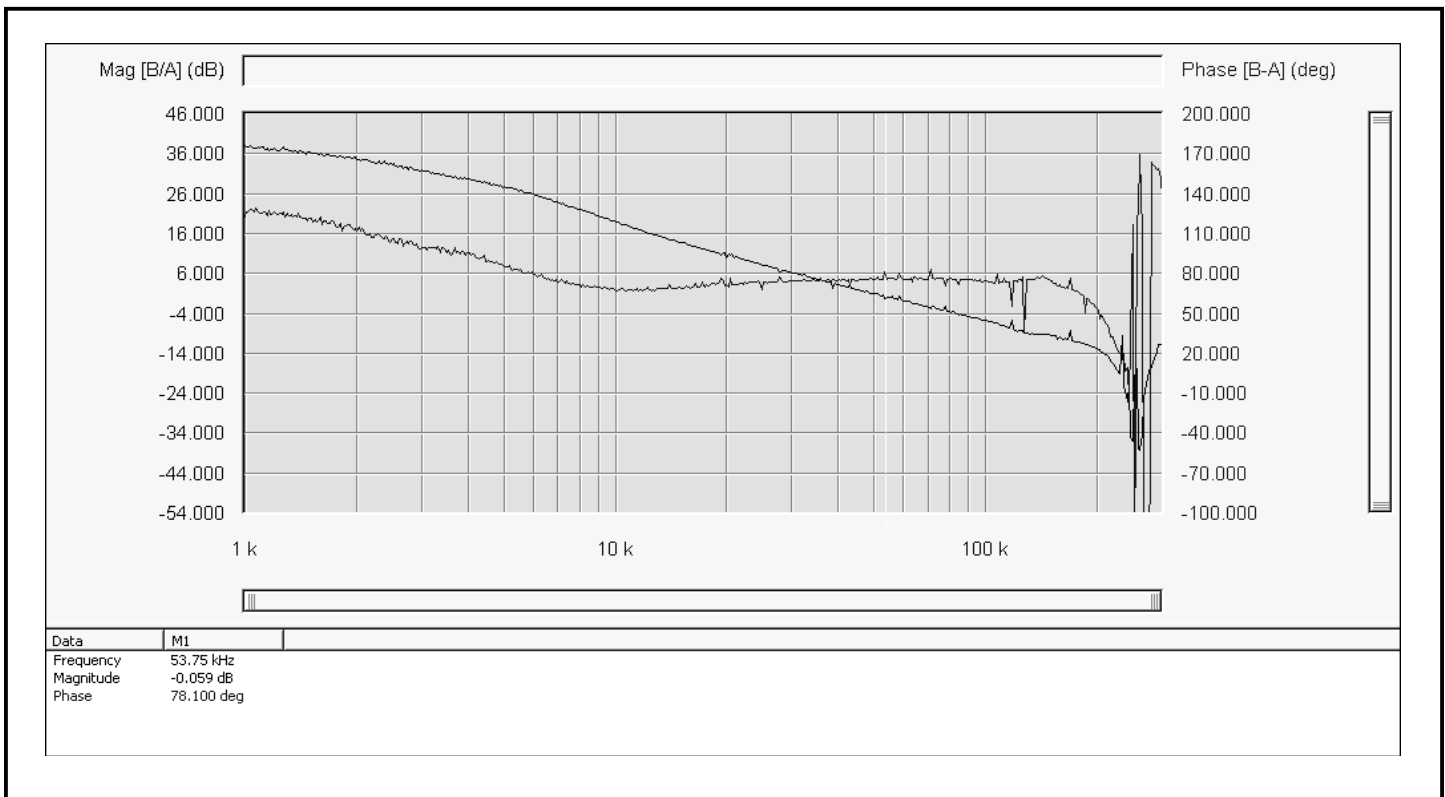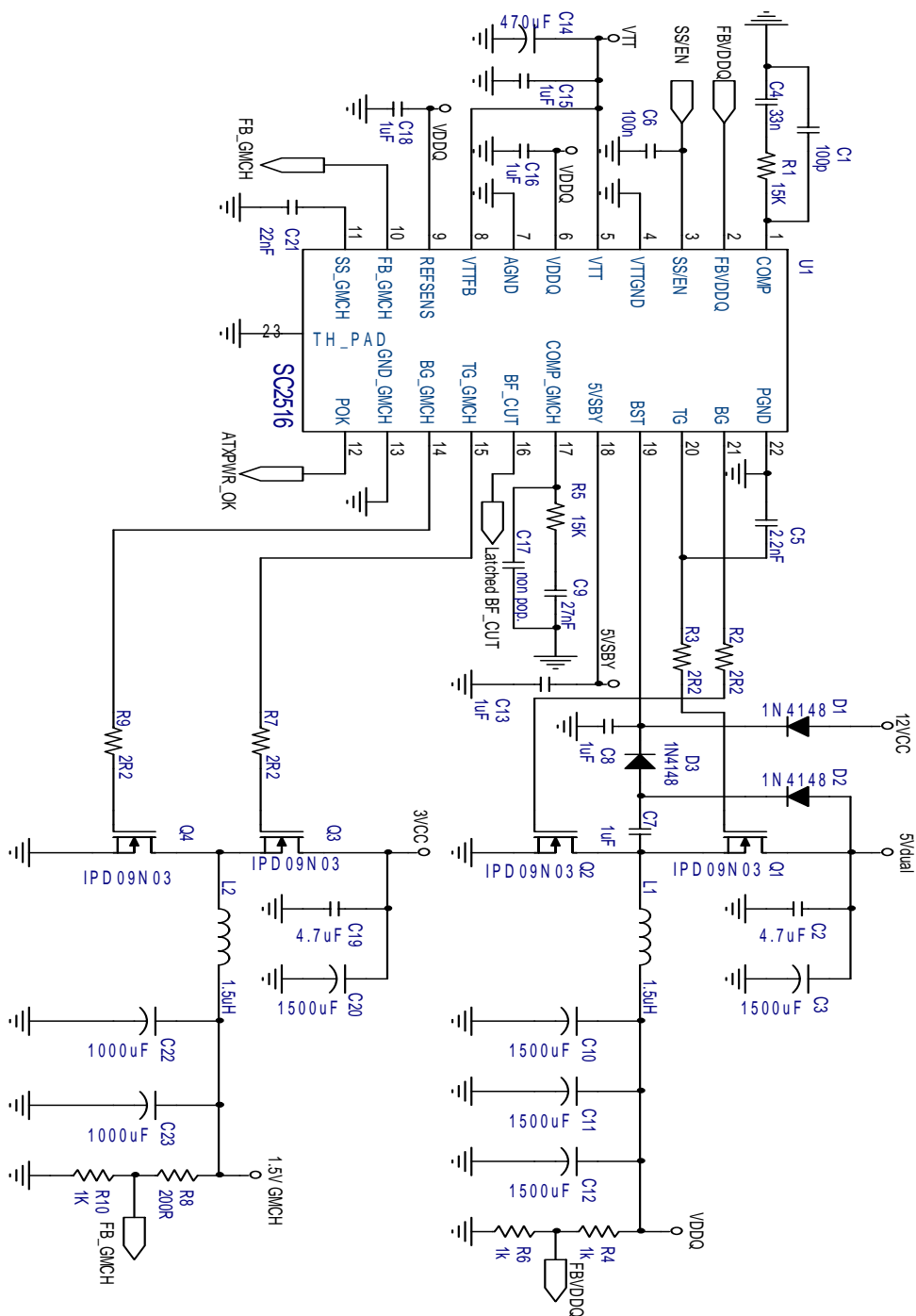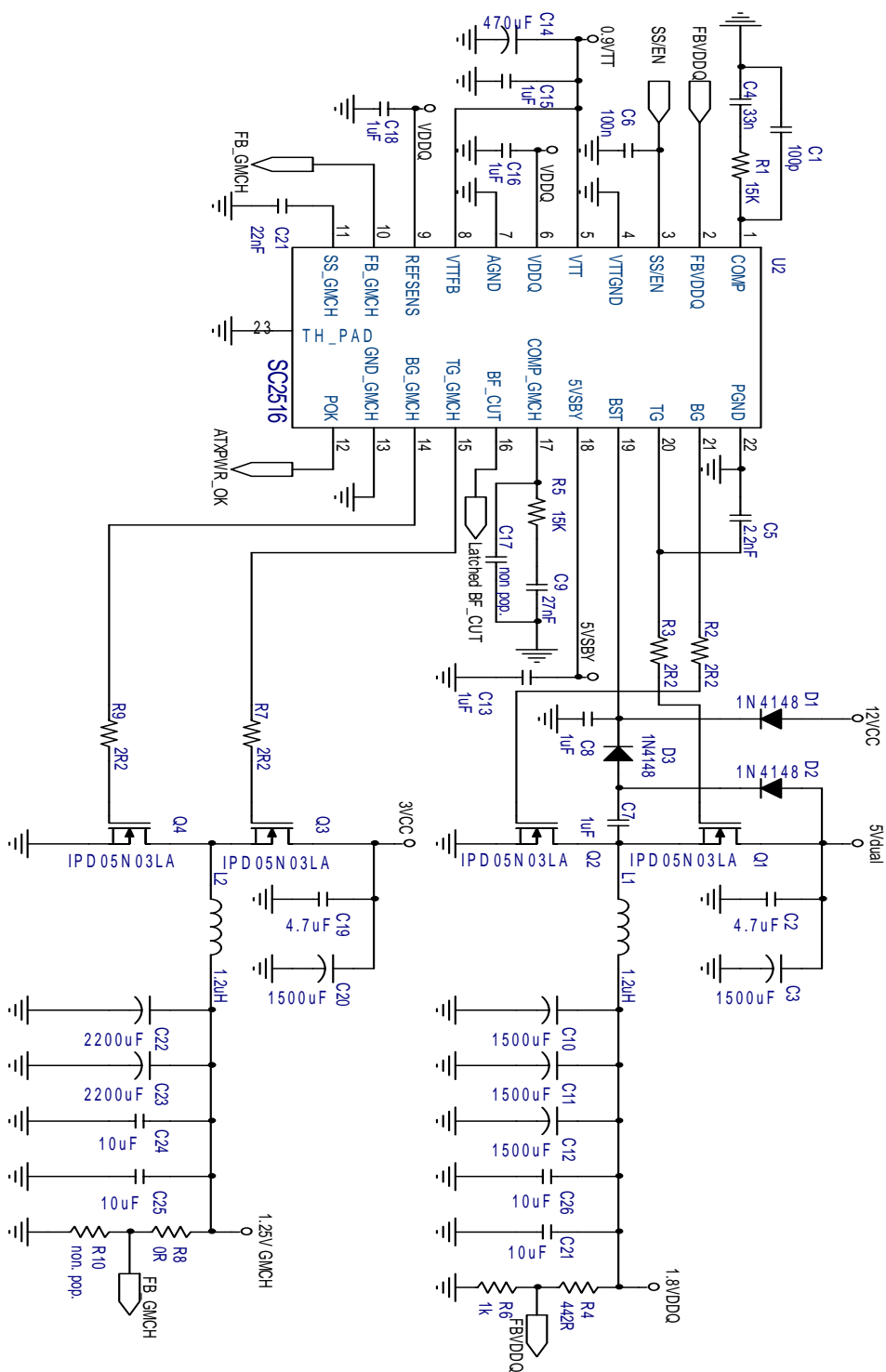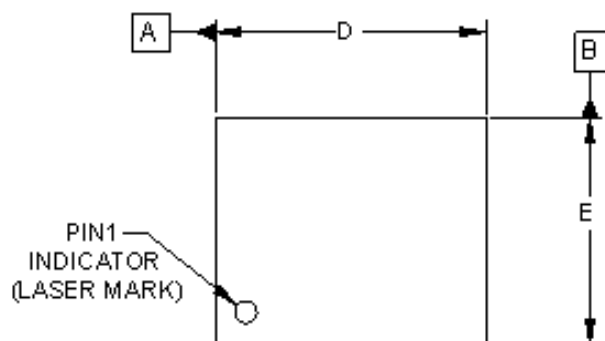Fig. 2. Bode plot of the VDDQ Channel

Fig. 3. Bode plot of the GMCH Channel

Typical application Schematic

# Application Schematic for Intel Broadwater platform

SEMTECH

Outline Drawing - MLP-22

DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.040	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.232	.236	.240	5.90	6.00	6.10
D1	.190	.196	.200	4.85	5.00	5.10
E	.192	.196	.200	4.90	5.00	5.10
E1	.118	.124	.127	3.00	3.15	3.25
e	.021 BSC			0.50 BSC		
L	.017	.021	.025	0.45	0.55	0.65
N	22			22		
aaa	.003			0.08		
bbb	.004			0.10		
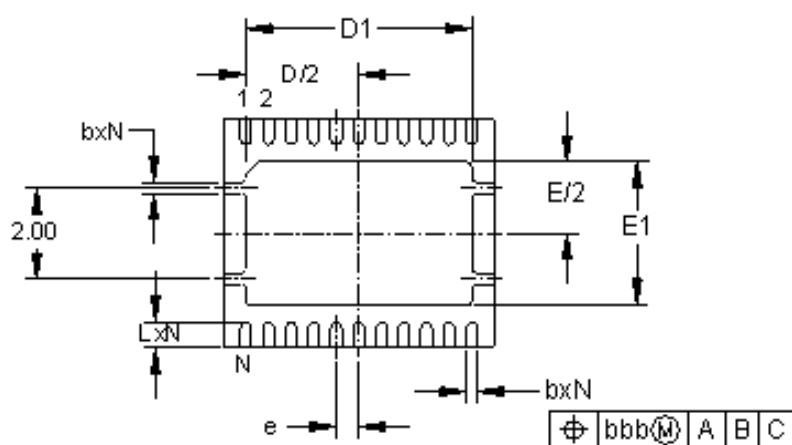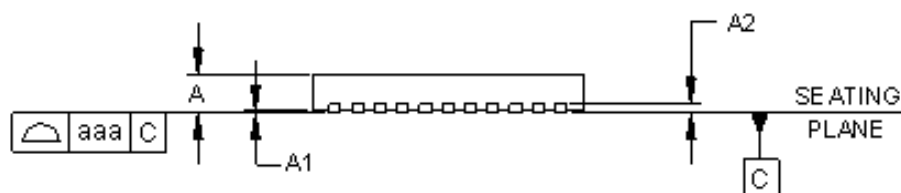
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

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Land Pattern- MLP-22
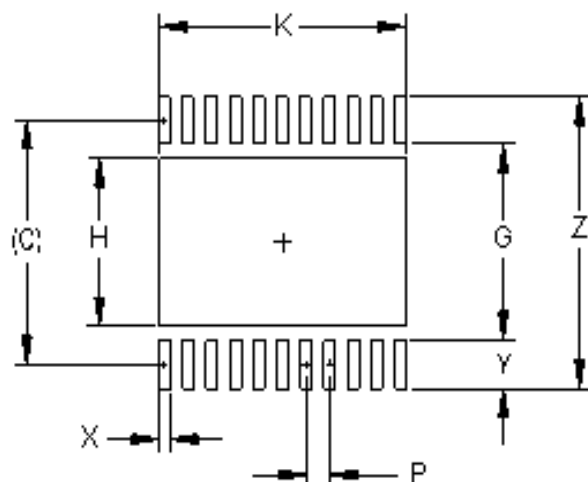
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.190)	(4.85)
G	.153	3.90
H	.131	3.35
K	.204	5.20
P	.020	0.50
X	.012	0.30
Y	.037	0.95
Z	.228	5.80

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

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