

1-Mbit (128 K × 8) Static RAM

Features

- Pin- and function-compatible with CY7C109B/CY7C1009B
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 80 \text{ mA}$ at 10 ns
- Low CMOS standby power
 - $I_{SB2} = 3 \text{ mA}$
- 2.0 V Data Retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} options
- CY7C109D available in Pb-free 32-pin 400-Mil wide Molded SOJ and 32-pin TSOP I packages. CY7C1009D available in Pb-free 32-pin 300-Mil wide Molded SOJ package

Functional Description [1]

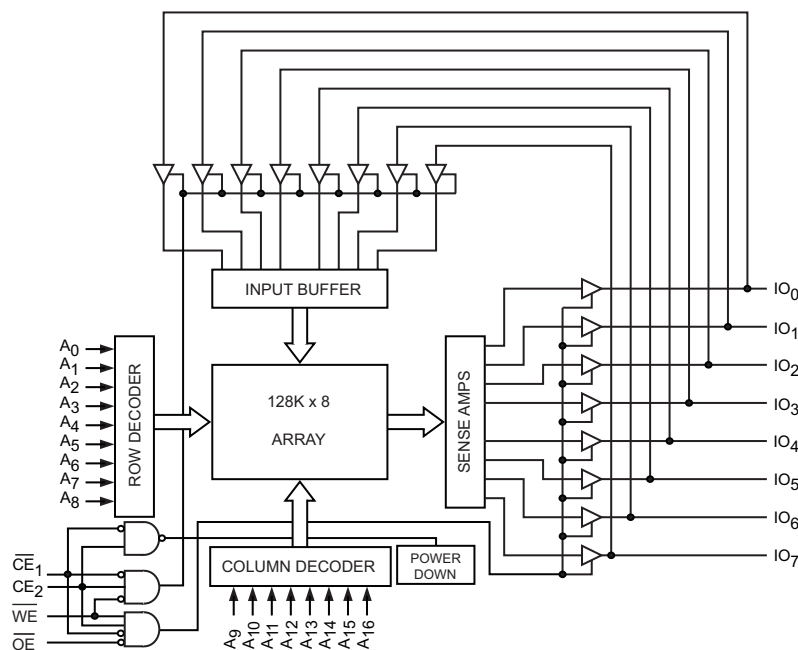
The CY7C109D/CY7C1009D is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}_1), an active HIGH Chip Enable (CE_2), an active LOW Output Enable (\overline{OE}), and tri-state drivers. The eight input and output pins (I/O_0 through I/O_7) are placed in a high-impedance state when:

- Deselected (\overline{CE}_1 HIGH or CE_2 LOW),
- Outputs are disabled (\overline{OE} HIGH),
- When the write operation is active (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW)

Write to the device by taking Chip Enable One (\overline{CE}_1) and Write Enable (\overline{WE}) inputs LOW and Chip Enable Two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Read from the device by taking Chip Enable One (\overline{CE}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the I/O pins.

Logic Block Diagram



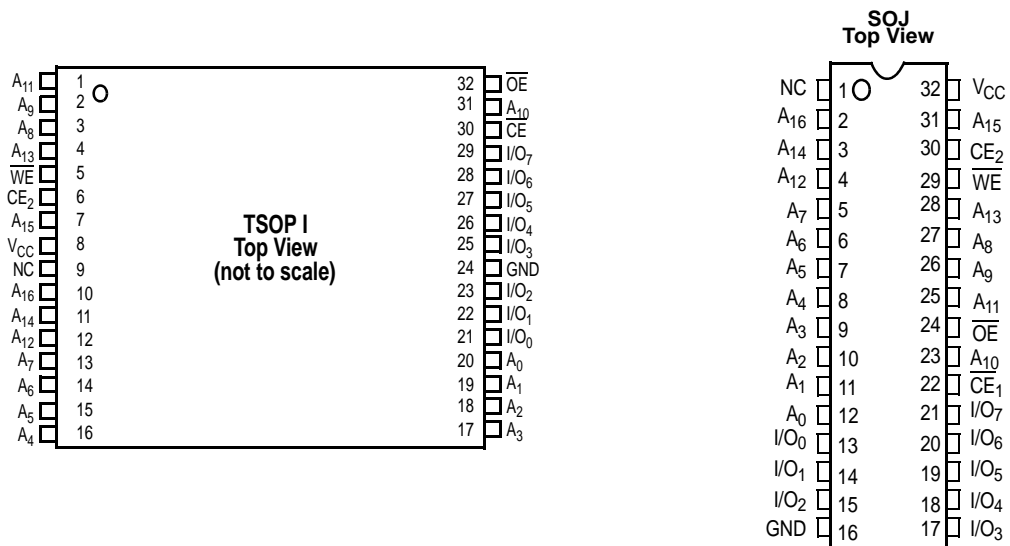
Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Contents

Pin Configuration	3	Switching Waveforms	7
Selection Guide	3	Truth Table	9
Maximum Ratings	4	Ordering Information	10
Operating Range	4	Ordering Code Definitions	10
Electrical Characteristics (Over the Operating Range) ...	4	Package Diagrams	11
Capacitance	5	Acronyms	12
Thermal Resistance	5	Document Conventions	12
AC Test Loads and Waveforms	5	Units of Measure	12
Switching Characteristics (Over the Operating Range) ..	6	Document History Page	13
Data Retention Characteristics		Sales, Solutions, and Legal Information	14
(Over the Operating Range)	7	Worldwide Sales and Design Support	14
Data Retention Waveform	7	Products	14

Pin Configuration [2]



Selection Guide

	CY7C109D-10 CY7C1009D-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	3	mA

Note
2. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND ^[3]...-0.5 V to +6.0 V
 DC Voltage Applied to Outputs in High-Z State ^[3].....-0.5 V to V_{CC} + 0.5 V

DC Input Voltage ^[3] -0.5 V to V_{CC} + 0.5 V
 Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001 V (per MIL-STD-883, Method 3015)
 Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}	Speed
Industrial	-40°C to +85°C	5 V ± 0.5 V	10 ns

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	7C109D-10 7C1009D-10		Unit
			Min	Max	
V _{OH}	Output HIGH Voltage	I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.5	V
V _{IL}	Input LOW Voltage ^[3]		-0.5	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{max} = 1/t _{RC}	100 MHz	80	mA
			83 MHz	72	mA
			66 MHz	58	mA
			40 MHz	37	mA
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{max}		10	mA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max V _{CC} , CE ₁ ≥ V _{CC} - 0.3 V, or CE ₂ ≤ 0.3 V, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0		3	mA

Note

3. V_{IL} (min) = -2.0 V and V_{IH}(max) = V_{CC} + 1 V for pulse durations of less than 5 ns.

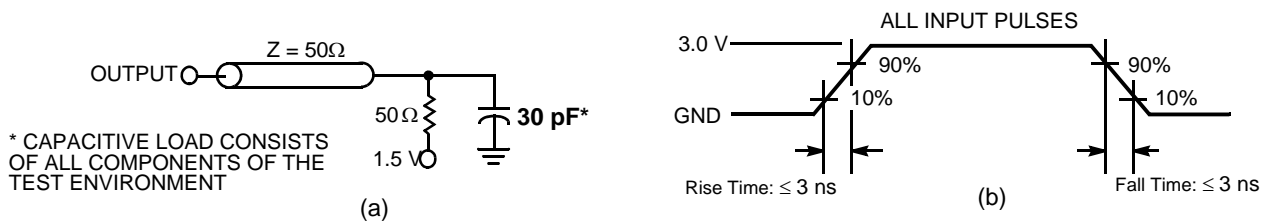
Capacitance ^[4]

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0 V	8	pF
C _{OUT}	Output Capacitance		8	pF

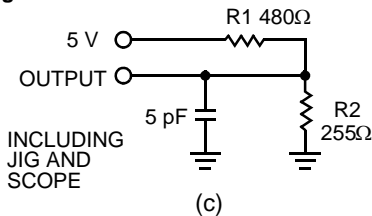
Thermal Resistance ^[4]

Parameter	Description	Test Conditions	300-Mil Wide SOJ	400-Mil Wide SOJ	TSOP I	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.61	56.29	50.72	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		40.53	38.14	16.21	°C/W

AC Test Loads and Waveforms ^[5]



High-Z characteristics:



Notes

4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

Switching Characteristics (Over the Operating Range) ^[6]

Parameter	Description	7C109D-10 7C1009D-10		Unit
		Min	Max	
Read Cycle				
$t_{power}^{[7]}$	V_{CC} (typical) to the first access	100		μ s
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	\overline{CE}_1 LOW to Data Valid, CE_2 HIGH to Data Valid		10	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[8, 9]		5	ns
t_{LZCE}	\overline{CE}_1 LOW to Low Z, CE_2 HIGH to Low Z ^[9]	3		ns
t_{HZCE}	\overline{CE}_1 HIGH to High Z, CE_2 LOW to High Z ^[8, 9]		5	ns
$t_{PU}^{[10]}$	\overline{CE}_1 LOW to Power-Up, CE_2 HIGH to Power-Up	0		ns
$t_{PD}^{[10]}$	\overline{CE}_1 HIGH to Power-Down, CE_2 LOW to Power-Down		10	ns
Write Cycle ^[11, 12]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	\overline{CE}_1 LOW to Write End, CE_2 HIGH to Write End	7		ns
t_{AW}	Address Set-Up to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	7		ns
t_{SD}	Data Set-Up to Write End	6		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[9]	3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[8, 9]		5	ns

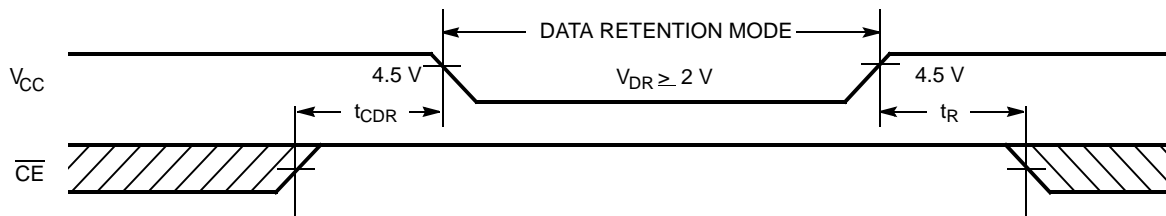
Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed
8. t_{HZOE} , t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of "AC Test Loads and Waveforms ^[5]" on page 5. Transition is measured when the outputs enter a high impedance state.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
10. This parameter is guaranteed by design and is not tested.
11. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = V_{DR} = 2.0\text{ V}$,	2.0		V
I_{CCDR}	Data Retention Current	$CE_1 \geq V_{CC} - 0.3\text{ V}$ or $CE_2 \leq 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$		3	mA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[13]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform



Switching Waveforms

Figure 1. Read Cycle No. 1 (Address Transition Controlled) [14, 15]

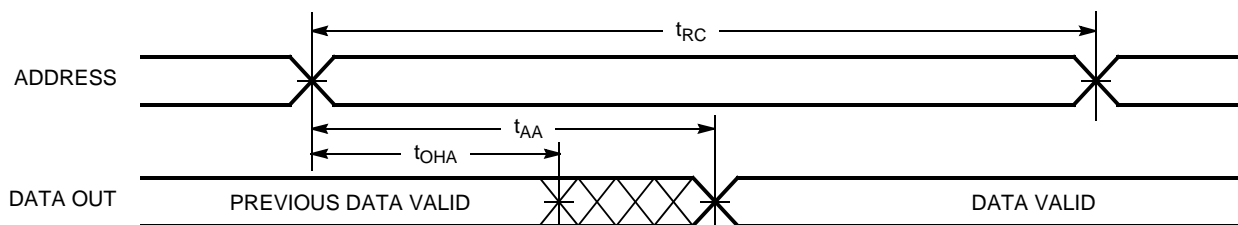
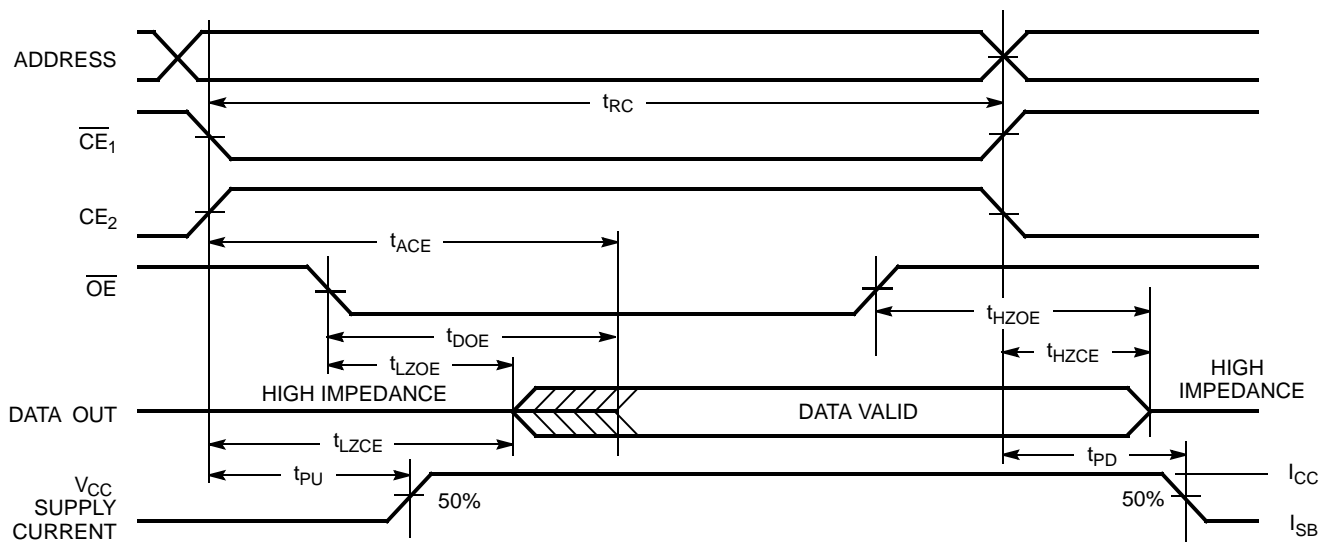


Figure 2. Read Cycle No. 2 (\overline{OE} Controlled) [15, 16]



Notes

13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50\ \mu\text{s}$ or stable at $V_{CC(min)} \geq 50\ \mu\text{s}$.
14. Device is continuously selected. \overline{OE} , $CE_1 = V_{IL}$, $CE_2 = V_{IH}$.
15. \overline{WE} is HIGH for read cycle.
16. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 3. Write Cycle No. 1 (\overline{CE}_1 or CE_2 Controlled) [17, 18]

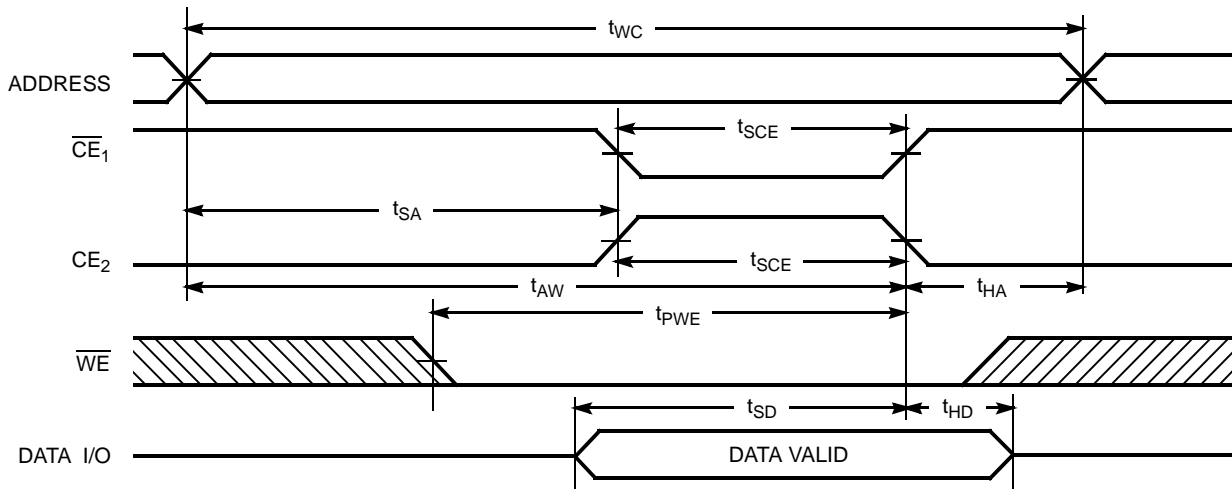
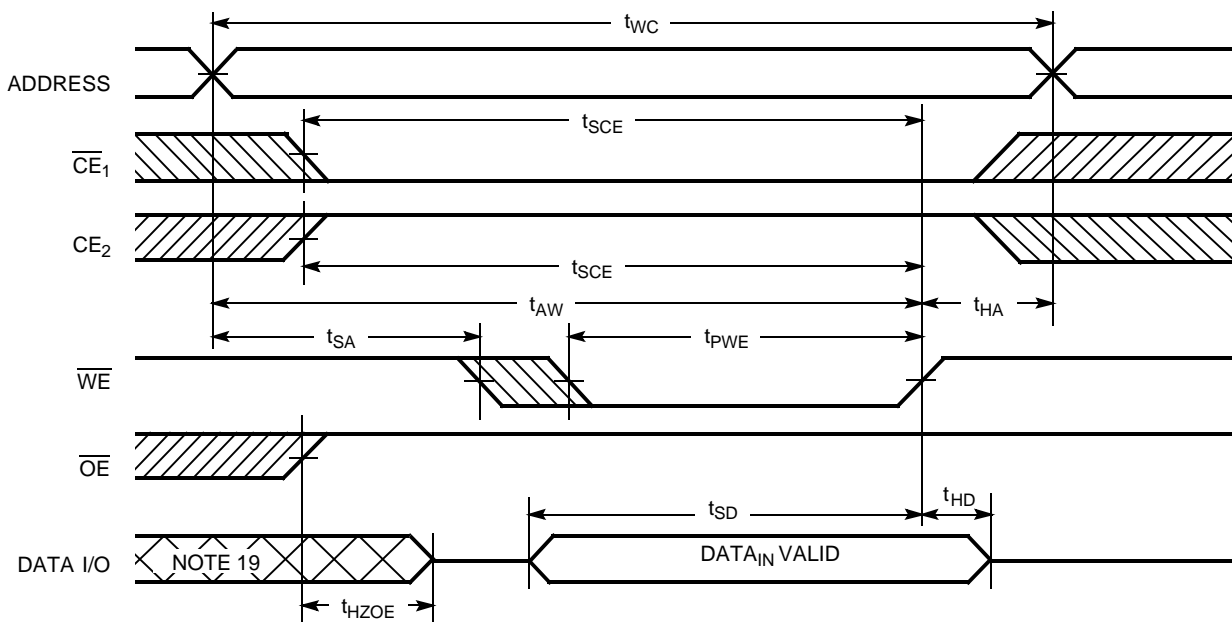


Figure 4. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [17, 18]

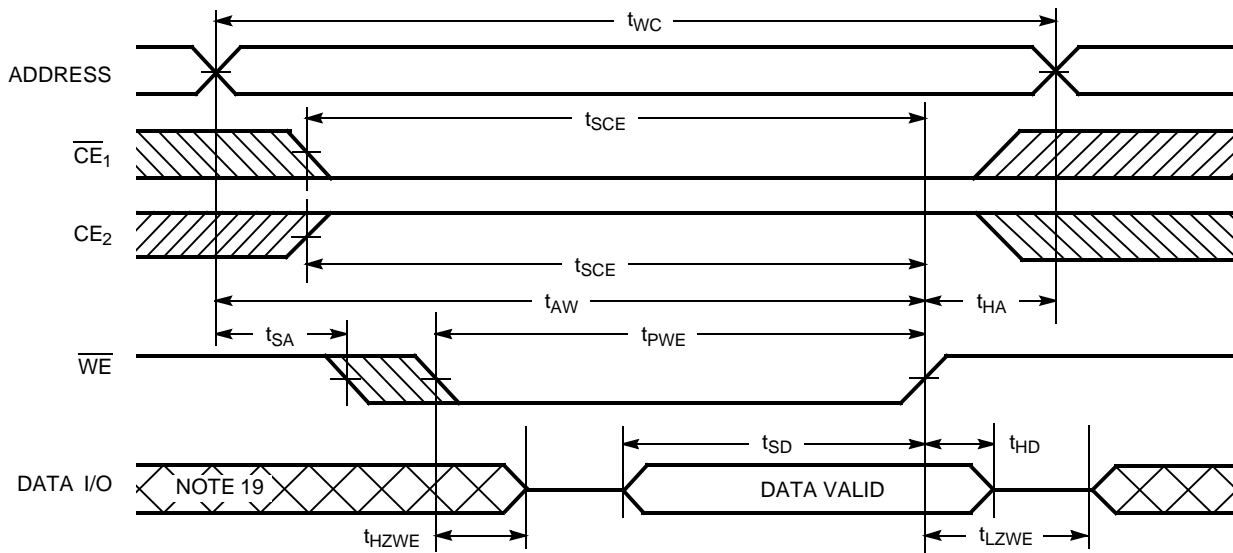


Notes

- 17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 18. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
- 19. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [12, 18]



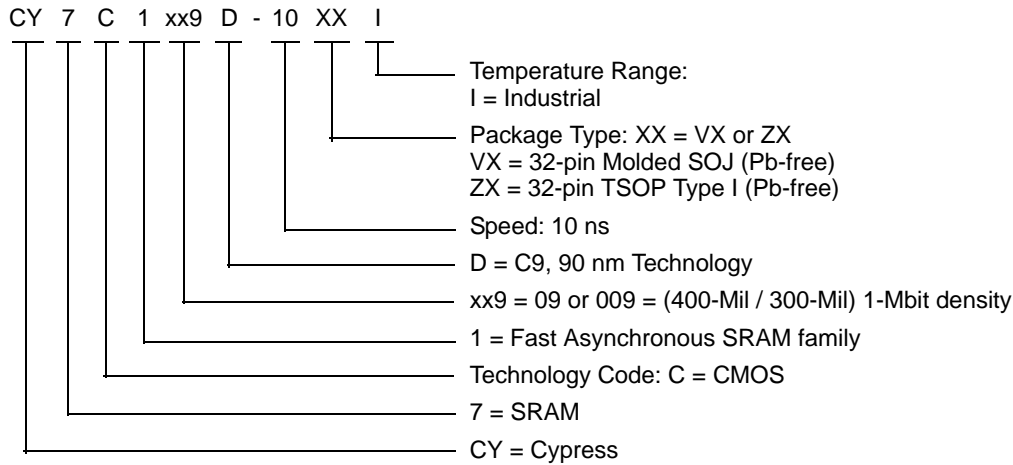
Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I_{SB})
X	L	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C109D-10VXI	51-85033	32-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C109D-10ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
	CY7C1009D-10VXI	51-85041	32-pin (300-Mil) Molded SOJ (Pb-free)	

Ordering Code Definitions



Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

Figure 6. 32-pin (300-Mil) Molded SOJ, 51-85041

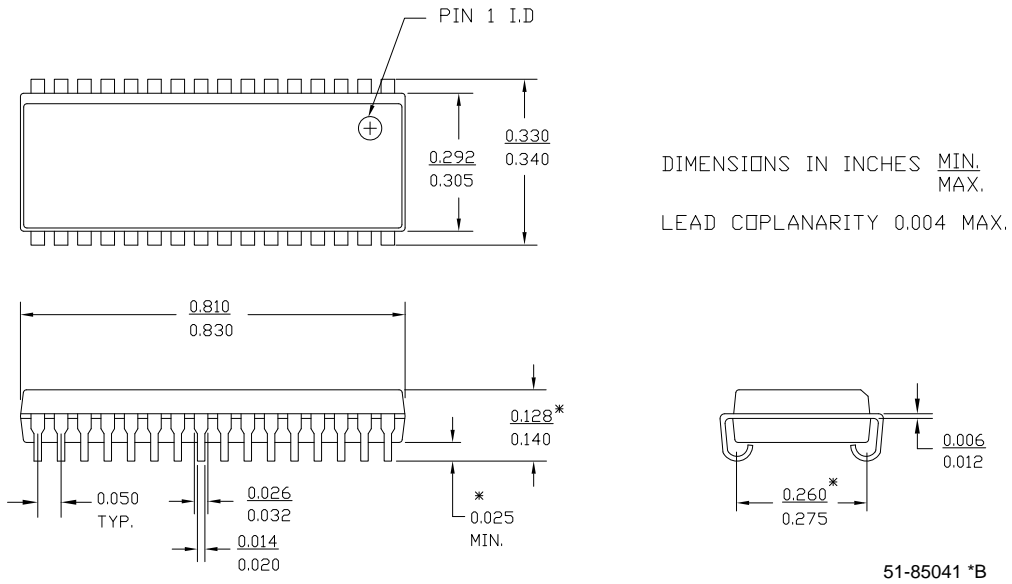
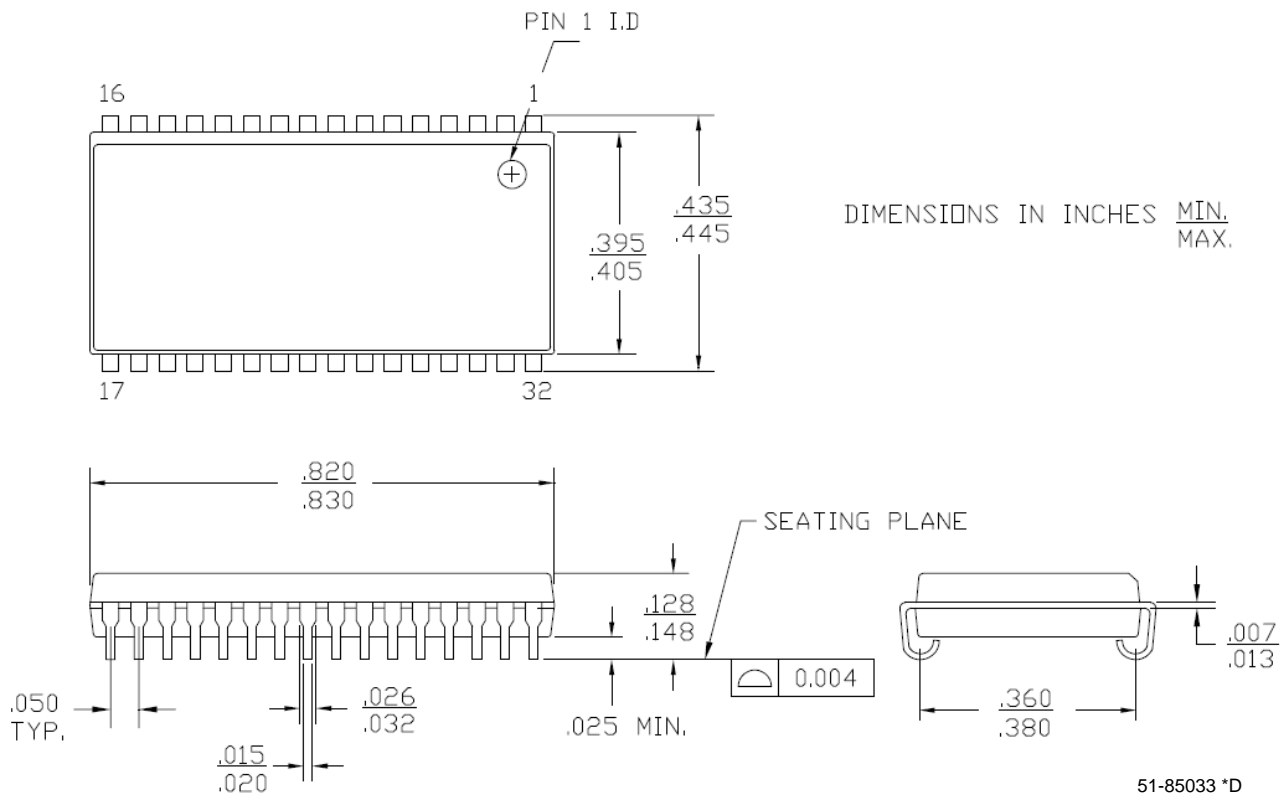
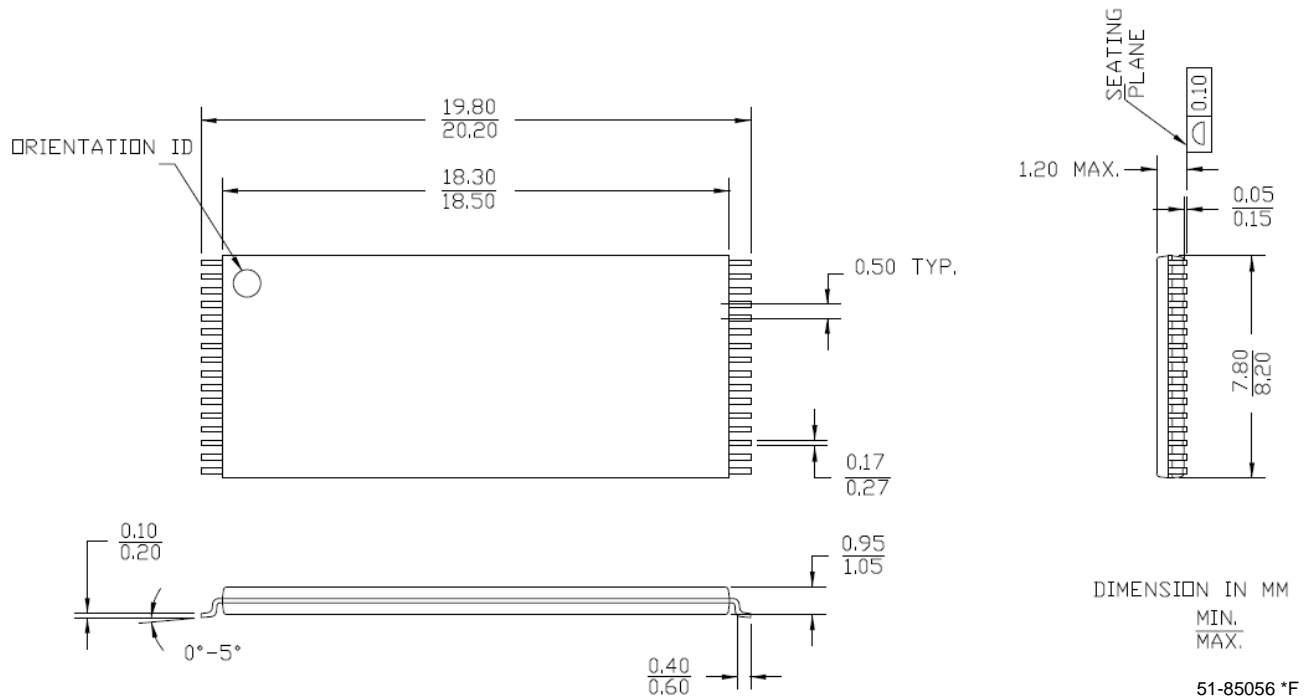


Figure 7. 32-pin (400-Mil) Molded SOJ, 51-85033



Package Diagrams (continued)

Figure 8. 32-pin Thin Small Outline Package Type I (8 × 20 mm), 51-85056



Acronyms

Acronym	Description
CE	chip enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	output enable
SRAM	Static random access memory
SOJ	Small Outline J-Lead
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts

Document History Page

Document Title: CY7C109D/CY7C1009D, 1-Mbit (128 K × 8) Static RAM				
Document Number: 38-05468				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in Ordering Information
*B	262950	See ECN	RKF	Added Data Retention Characteristics table Added T _{power} Spec in Switching Characteristics Table Shaded Ordering Information
*C	See ECN	See ECN	RKF	Reduced Speed bins to -10 and -12 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V _{CC} +2 V to V _{CC} +1 V in footnote #3
*E	802877	See ECN	VKN	Changed I _{CC} spec from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	3104943	12/08/2010	AJU	Added Ordering Code Definitions . Updated Package Diagrams .
*G	3220123	04/08/2011	PRAS	Updated template and styles as per current Cypress standards. Added Acronyms and units of measure. Updated package diagrams: 51-85033 to *D 51-85056 to *F

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2004-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».



JONHON

«**JONHON**» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«**FORSTAR**» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А