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October 2013

FDB075N15A_F085

N-Channel Power Trench® MOSFET

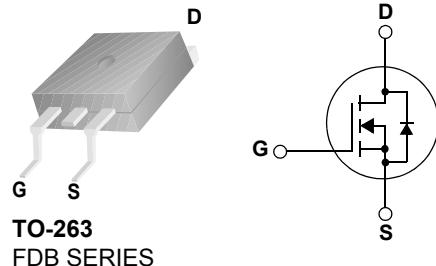
150V, 110A, 7.5mΩ

Features

- Typ $r_{DS(on)} = 5.5\text{m}\Omega$ at $V_{GS} = 10\text{V}$, $I_D = 80\text{A}$
- Typ $Q_{g(\text{tot})} = 80\text{nC}$ at $V_{GS} = 10\text{V}$, $I_D = 80\text{A}$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Integrated Starter/alternator
- Primary Switch for 12V Systems



MOSFET Maximum Ratings $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (<i>Note 1</i>)	110	A
	Pulsed Drain Current	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy	502	mJ
P_D	Power Dissipation	333	W
	Derate above 25°C	2.22	$\text{W}/^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.45	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient	(<i>Note 3</i>)	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB075N15A	FDB075N15A_F085	D2-PAK(TO-263)	330mm	24mm	800 units

Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 0.24\text{mH}$, $I_{AS} = 64\text{A}$, $V_{DD} = 100\text{V}$ during inductor charging and $V_{DD} = 0\text{V}$ during time in avalanche
- 3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	150	-	-	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 150\text{V}, T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	-	1	mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	3.0	4.0	V
$r_{DS(\text{on})}$	Drain to Source On Resistance	$I_D = 80\text{A}, T_J = 25^\circ\text{C}$	-	5.5	7.5	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	14.2	20	$\text{m}\Omega$

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	5595	-	pF
C_{oss}	Output Capacitance		-	513	-	pF
C_{rss}	Reverse Transfer Capacitance		-	16	-	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	-	2.4	-	Ω
$Q_{g(\text{ToT})}$	Total Gate Charge at 10V	$V_{GS} = 0 \text{ to } 10\text{V}$	-	80	95	nC
$Q_{g(\text{th})}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2\text{V}$	-	11	13	nC
Q_{gs}	Gate to Source Gate Charge	$I_D = 80\text{A}$	-	26.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	14	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 75\text{V}, I_D = 80\text{A}, V_{GS} = 10\text{V}, R_{\text{GEN}} = 6\Omega$	-	-	100	ns
$t_{d(on)}$	Turn-On Delay Time		-	33	-	ns
t_r	Rise Time		-	46	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	76	-	ns
t_f	Fall Time		-	25	-	ns
t_{off}	Turn-Off Time		-	-	138	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}, V_{GS} = 0\text{V}$	-	-	1.25	V
		$I_{SD} = 40\text{A}, V_{GS} = 0\text{V}$	-	-	1.2	V
T_{rr}	Reverse Recovery Time	$I_F = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}, V_{DD} = 120\text{V}$	-	118	132	ns
			-	341	494	nC

Notes:

4: The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

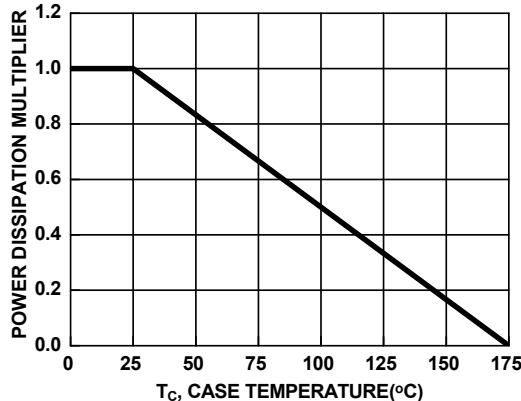


Figure 1. Normalized Power Dissipation vs Case Temperature

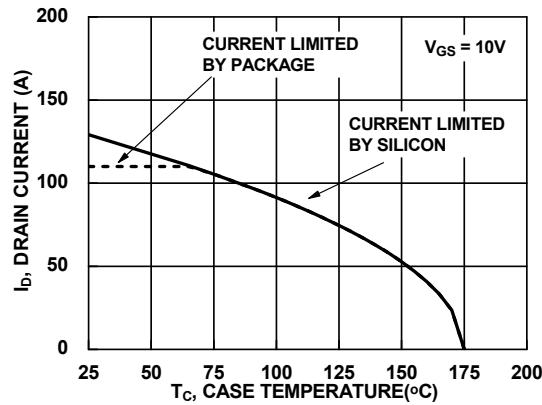


Figure 2. Maximum Continuous Drain Current vs Case Temperature

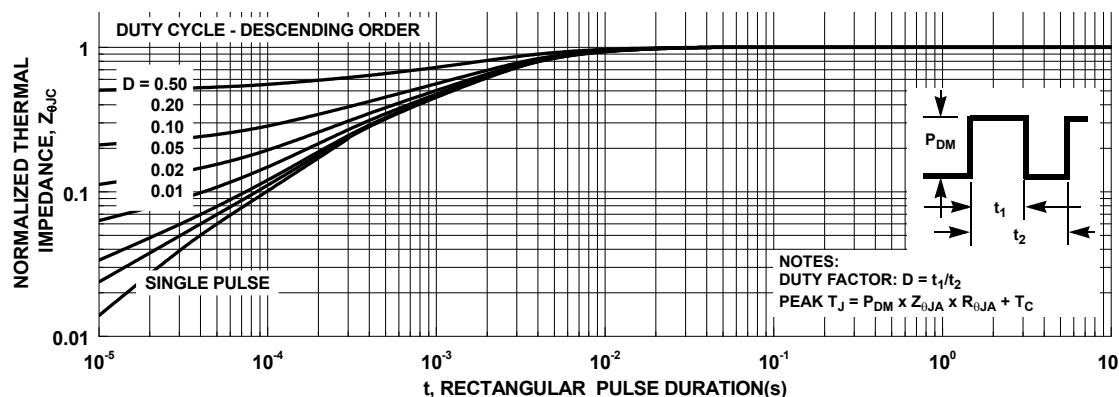


Figure 3. Normalized Maximum Transient Thermal Impedance

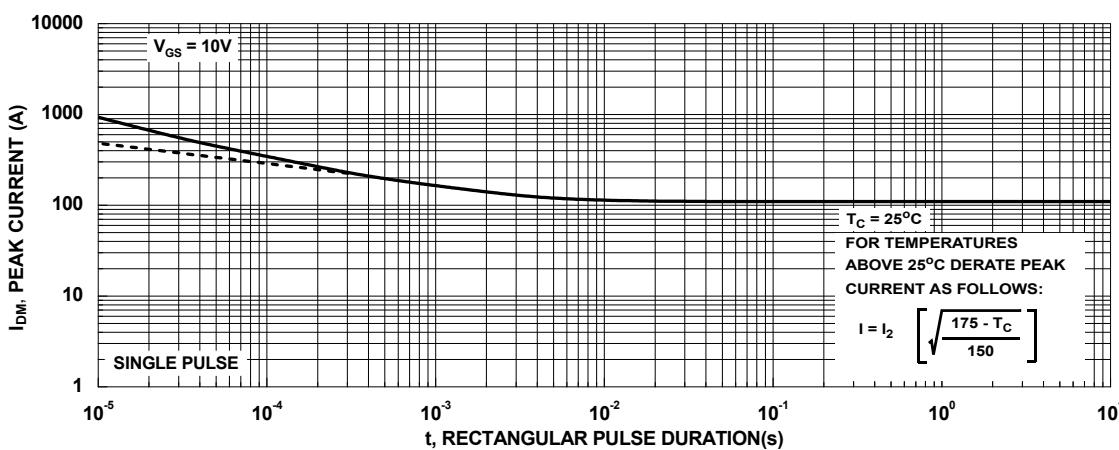


Figure 4. Peak Current Capability

Typical Characteristics

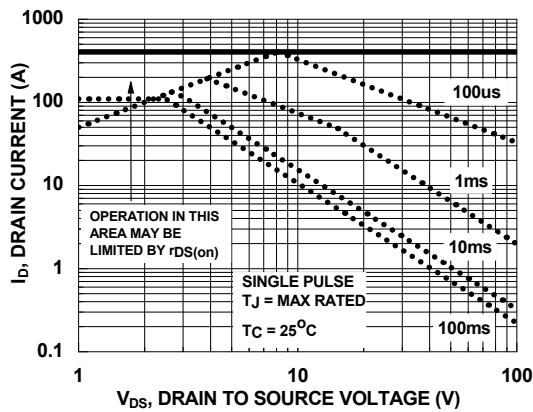
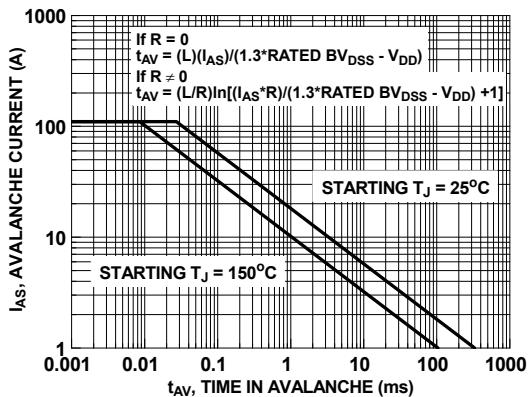


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

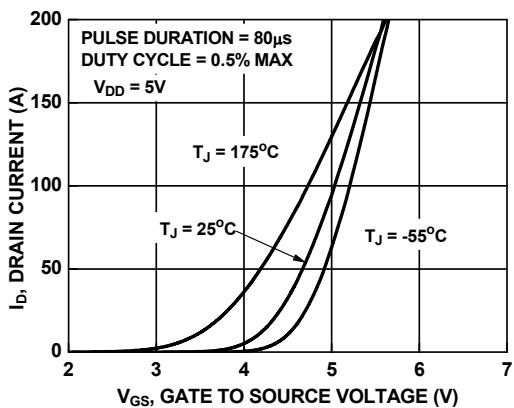


Figure 7. Transfer Characteristics

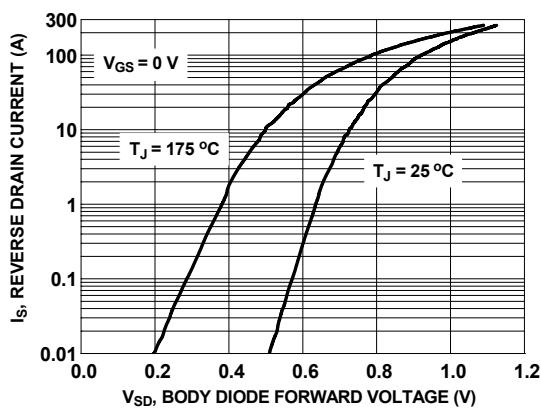


Figure 8. Forward Diode Characteristics

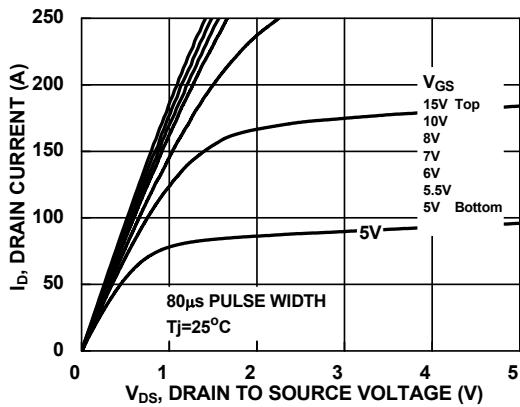


Figure 9. Saturation Characteristics

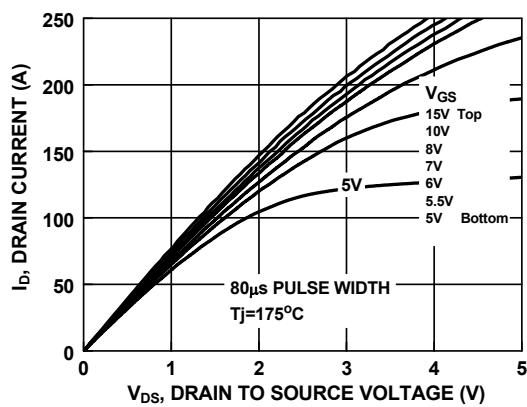
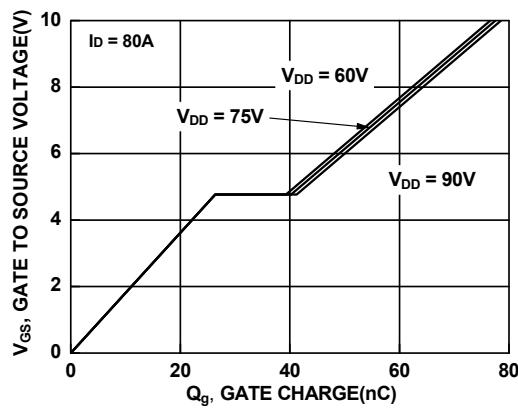
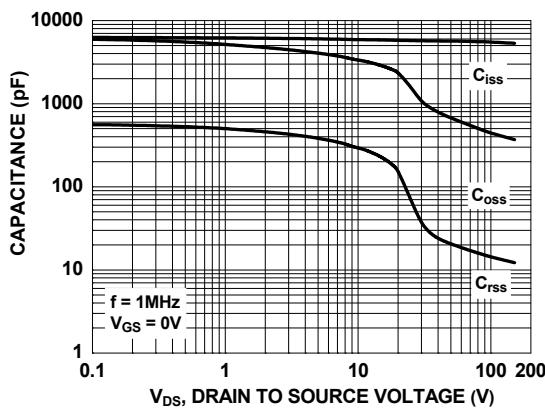
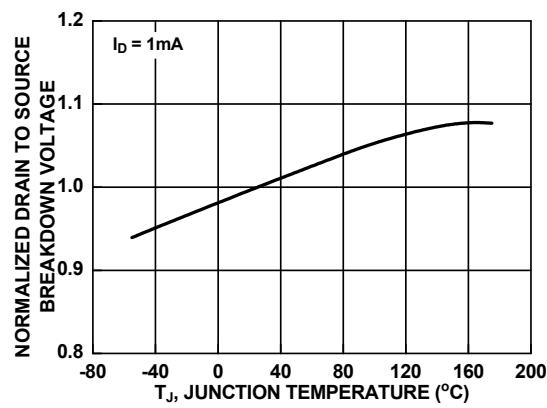
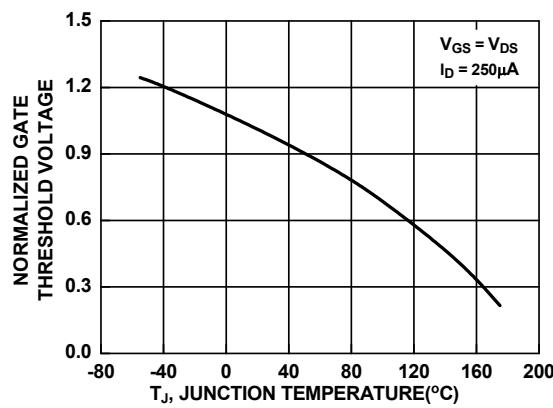
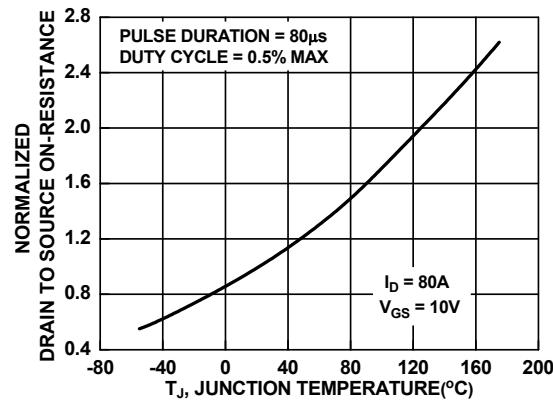
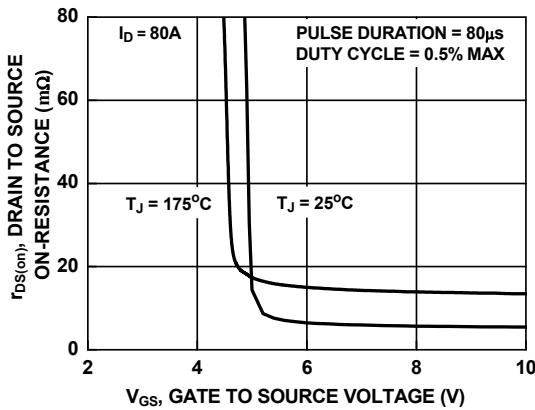


Figure 10. Saturation Characteristics

Typical Characteristics





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