SEMTECH

POWER MANAGEMENT

Features

- Input voltage — 0.7V to 4.5V
- Minimum input startup voltage — 0.865V
- Output voltage — fixed at 3.3V; adjustable from 1.8V to 5.0V
- Peak input current limit — 1.2A
- Output current at 3.3 V_{OUT} — 80mA with V_{IN} = 1.0V, 190mA with V_{IN} = 1.5V
- Efficiency up to 94%
- Internal synchronous rectifier
- Switching frequency — 1.2MHz
- Automatic power save
- Anti-ringing circuit
- Operating supply current (measured at OUT) — 50µA
- Shutdown current — 0.1µA (typ)
- No forward conduction path during shutdown
- Available in ultra-thin 1.5 × 2.0 × 0.6 (mm) MLPD-UT-6 and SOT23-6 packages
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- MP3 players
- Smart Phones and cellular phones
- Palmtop computers and handheld Instruments
- PCMCIA cards
- Memory cards
- Digital cordless phones
- Personal medical products
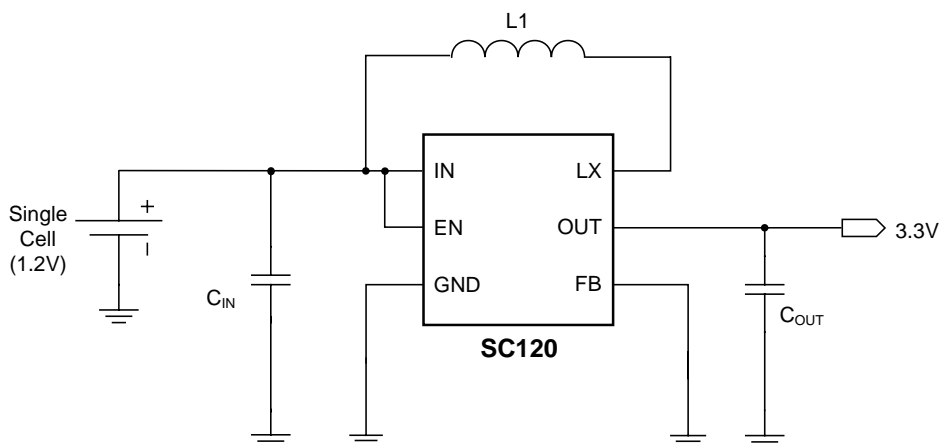- Wireless VoIP phones
- Small motors

Description

The SC120 is a high efficiency, low noise, synchronous step-up DC-DC converter that provides boosted voltage levels in low-voltage handheld applications. The wide input voltage range allows use in systems with single NiMH or alkaline battery cells as well as in systems with higher voltage battery supplies. It features an internal 1.2A switch and synchronous rectifier to achieve up to 94% efficiency and to eliminate the need for an external Schottky diode. The output voltage can be set to 3.3V with internal feedback, or to any voltage within the specified range using a standard resistor divider.
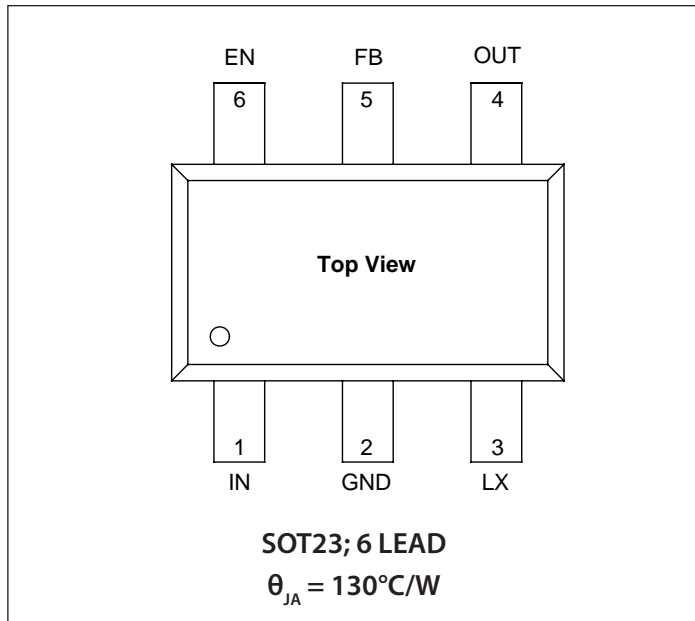
The SC120 operates in Pulse Width Modulation (PWM) mode for moderate to high loads and Power Save Mode (PSAVE) for improved efficiency under light load conditions. It features anti-ringing circuitry for reduced EMI in noise sensitive applications. Output disconnect capability is included to reduce leakage current, improve efficiency, and eliminate external components sometimes needed to disconnect the load from the supply during shutdown.

Low quiescent current is obtained despite a high 1.2MHz operating frequency. Small external components and the space saving MLPD-UT-6, 1.5×2.0×0.6 (mm) package, or low cost SOT23-6 package, make this device an excellent choice for small handheld applications that require the longest possible battery life.
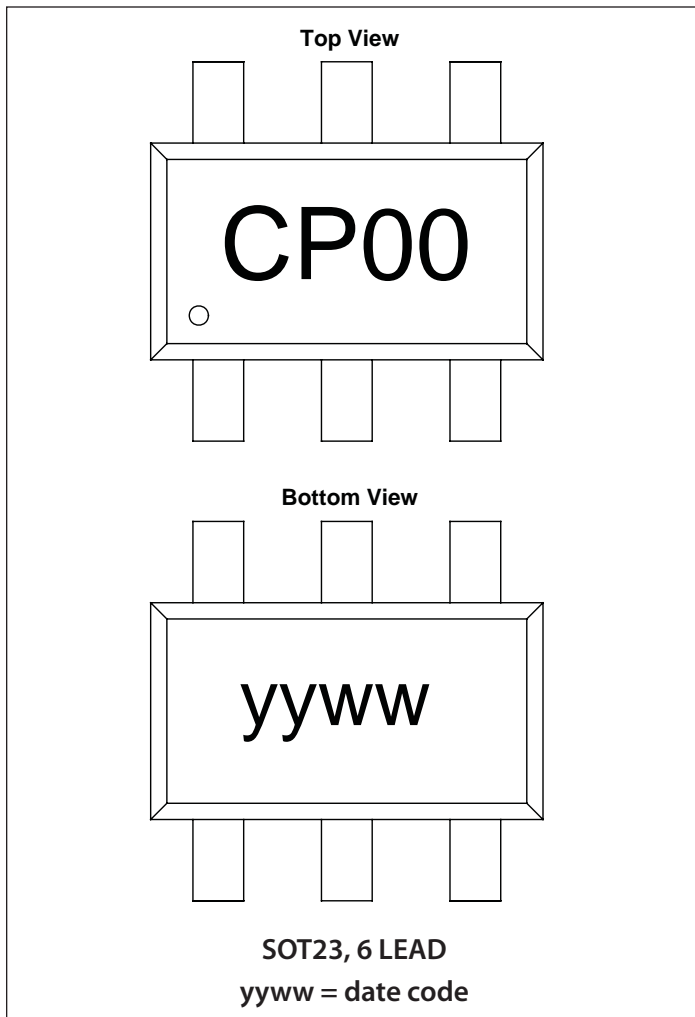
Typical Application Circuit

SEMTECH

Pin Configuration — SOT23

```
        EN        FB        OUT
        6         5         4


              Top View

          ○

        1         2         3
        IN       GND        LX
```

SOT23; 6 LEAD

$\theta_{JA} = 130°C/W$

Marking Information — SOT23

Top View

CP00
○

Bottom View

yyww

SOT23, 6 LEAD

yyww = date code

Ordering Information

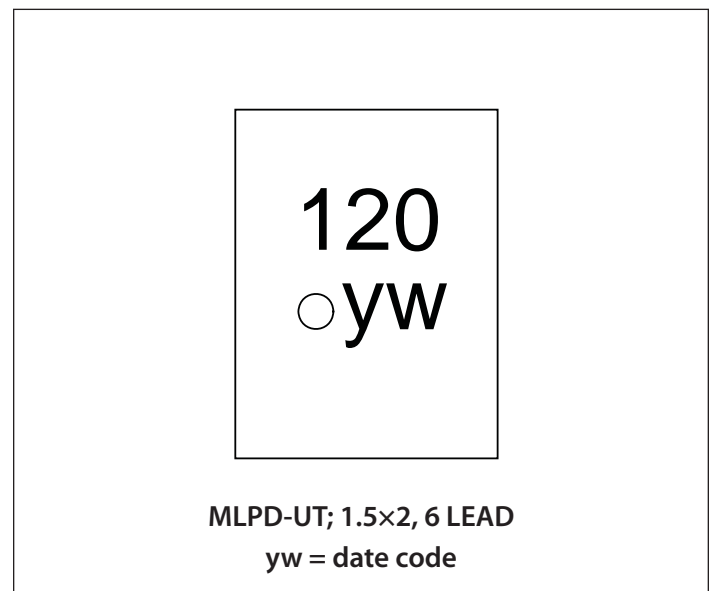| Device	Package
SC120ULTRT[1][2]	MLPD-UT-6 1.5×2
SC120SKTRT [1][2]	SOT23-6
SC120EVB	Evaluation Board, MLPD-UT-6 version
SC120SKEVB	Evaluation Board, SOT23-6 version

Notes:

(1)   Available in tape and reel only. A reel contains 3,000 devices.

(2)   Lead-free packaging, only. Device is WEEE and RoHS compliant, and halogen-free.

Pin Configuration — MLPD-UT

```
   ○
LX   [1]    TOP VIEW     [6]   OUT

GND  [2]         +       [5]   FB

IN   [3]         T       [4]   EN
```

MLPD-UT; 1.5×2, 6 LEAD

$\theta_{JA} = 84°C/W$
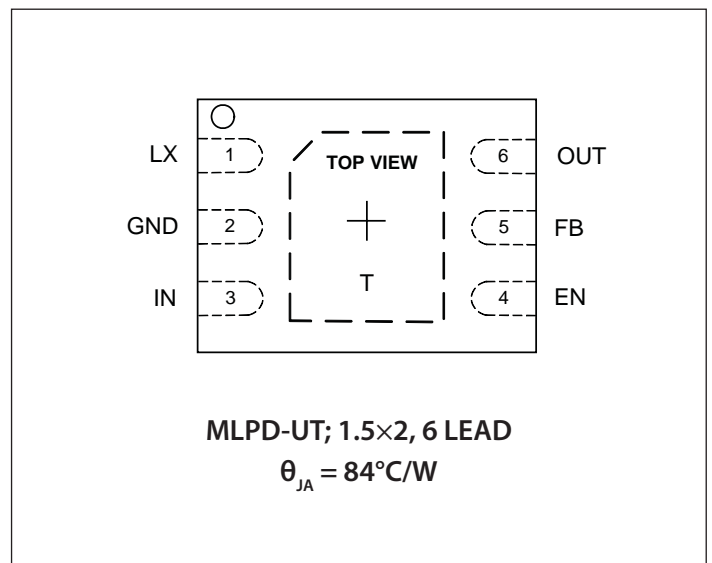
Marking Information — MLPD-UT

120
○ yw

MLPD-UT; 1.5×2, 6 LEAD

yw = date code

Absolute Maximum Ratings

IN, OUT, LX, FB (V) . . . . -0.3 to +6.0

EN (V) . . . . -0.3 to (V_{IN} + 0.3)

ESD Protection Level[1] (kV) 3

Recommended Operating Conditions

Ambient Temperature Range (℃). . . . . -40 to +85

V_{IN} (V) . . . . 0.7 to 4.5

V_{OUT} (V) . . . . 1.8 to 5.0

Thermal Information

Thermal Res. MLPD, Junction-Ambient[2] (℃/W) 84

Thermal Res., SOT23, Junction -Ambient[2] (℃/W) . . . 130

Maximum Junction Temperature (℃) 150

Storage Temperature Range (℃) . . . . -65 to +150

Peak IR Reflow Temperature (10s to 30s) (℃) . . . . . . +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted V_{IN} = 2.5V, C_{IN} = C_{OUT} = 22µF, L_1 = 4.7µH, T_A = -40 to +85℃. Typical values are at T_A = 25℃.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		0.7		4.5	V
Minimum Startup Voltage	V_{IN-SU}	I_{OUT} < 1mA, T_A = 0℃ to 85℃		0.865		V
Shutdown Current	I_{SHDN}	T_A = 25℃, V_{EN} = 0V		0.1	1	µA
Operating Supply Current[1]	I_Q	In PSAVE mode, non-switching, measured at OUT		50		µA
Internal Oscillator Frequency	f_{OSC}			1.2		MHz
Maximum Duty Cycle	D_{MAX}			90		%
Minimum Duty Cycle	D_{MIN}				15	%
Output Voltage	V_{OUT}	V_{FB} = 0V		3.3		V
Adjustable Output Voltage Range	V_{OUT_RNG}	For V_{IN} such that D_{MIN} < D < D_{MAX}	1.8		5.0	V
Regulation Feedback Reference Voltage Accuracy (Internal or External Programming)	$V_{Reg-Ref}$		-1.5		1.5	%
FB Pin Input Current	I_{FB}	V_{FB} = 1.2V			0.1	µA
Startup Time	t_{SU}			1		ms

SEMTECH

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
P-Channel ON Resistance	R_{DSP}	$V_{OUT} = 3.3V$		0.6		Ω
N-Channel ON Resistance	R_{DSN}	$V_{OUT} = 3.3V$		0.5		Ω
N-Channel Current Limit	$I_{LIM(N)}$	$V_{IN} = 3.0V$	0.9	1.2		A
P-Channel Startup Current Limit	$I_{LIM(P)-SU}$	$V_{IN} > V_{OUT}, V_{EN} > V_{IH}$		150		mA
LX Leakage Current PMOS	I_{LXP}	$T_A = 25°C, V_{LX} = 0V$			1	µA
LX Leakage Current NMOS	I_{LXN}	$T_A = 25°C, V_{LX} = 3.3V$			1	µA
Logic Input High	V_{IH}	$V_{IN} = 3.0V$	0.85			V
Logic Input Low	V_{IL}	$V_{IN} = 3.0V$			0.2	V
Logic Input Current High	I_{IH}	$V_{EN} = V_{IN} = 3.0V$			1	µA
Logic Input Current Low	I_{IL}	$V_{EN} = 0V$	-0.2			µA

NOTES:

(1)   Quiescent operating current is drawn from OUT while in regulation. The quiescent operating current projected to IN is approximately $I_Q \times (V_{OUT}/V_{IN})$.

SEMTECH

Typical Characteristics — V_{OUT} = 1.8V

Efficiency vs. I_{OUT} (V_{OUT} = 1.8V)

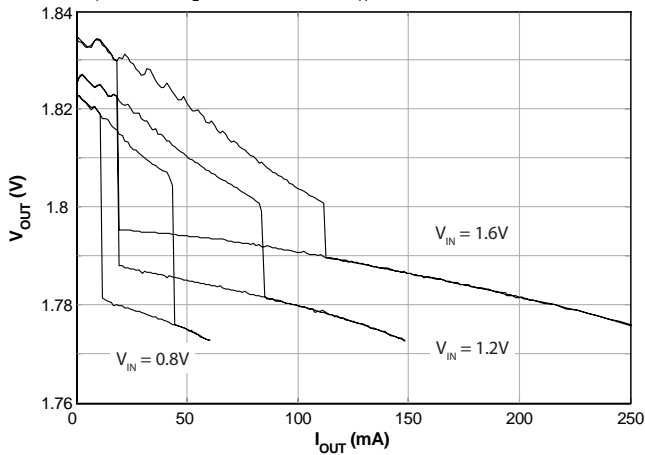R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, T_A = 25°C
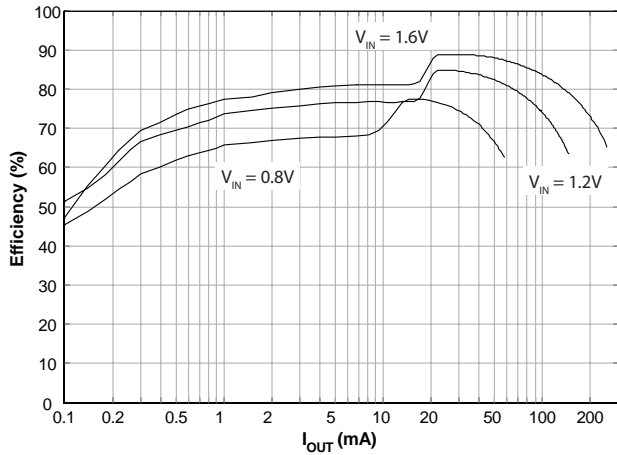
Efficiency vs. I_{OUT} (V_{OUT} = 1.8V)
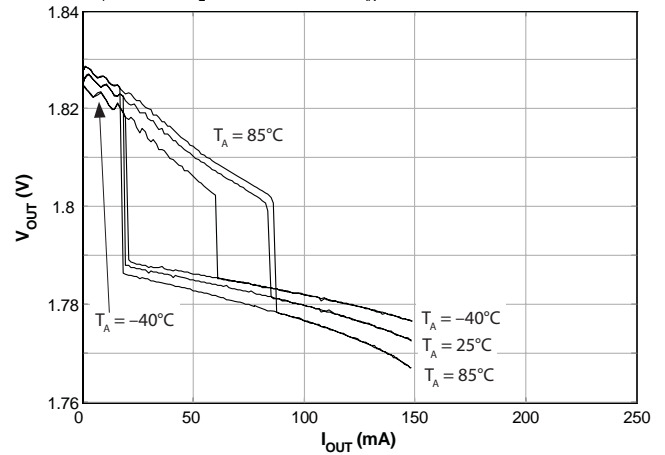
R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, V_{IN} = 1.2V
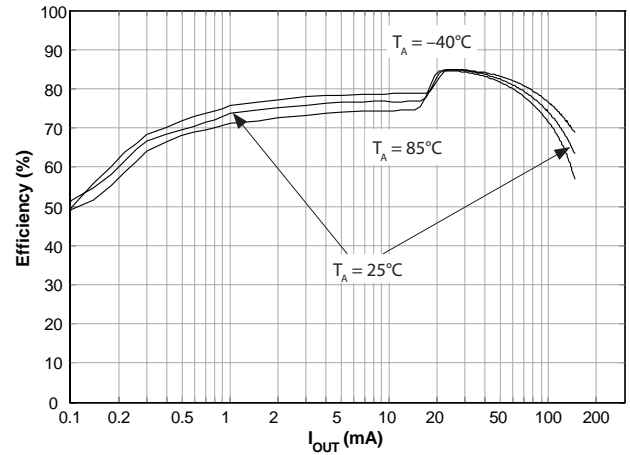
Load Regulation (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, T_A = 25°C

Load Regulation (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, V_{IN} = 1.2V

Line Regulation — PSAVE Mode (V_{OUT} = 1.8V)
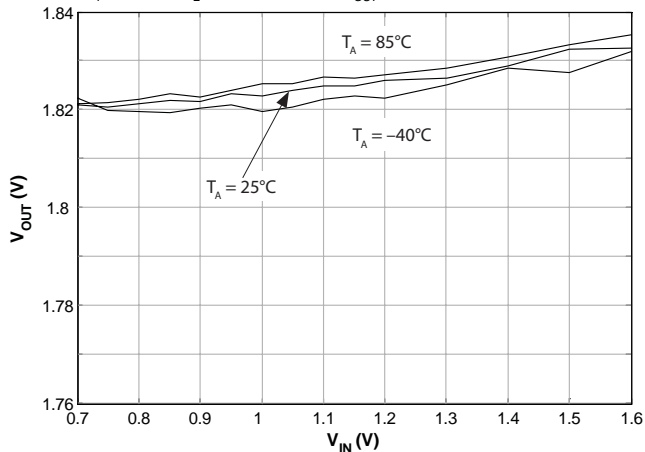
R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, I_{OUT} = 5mA

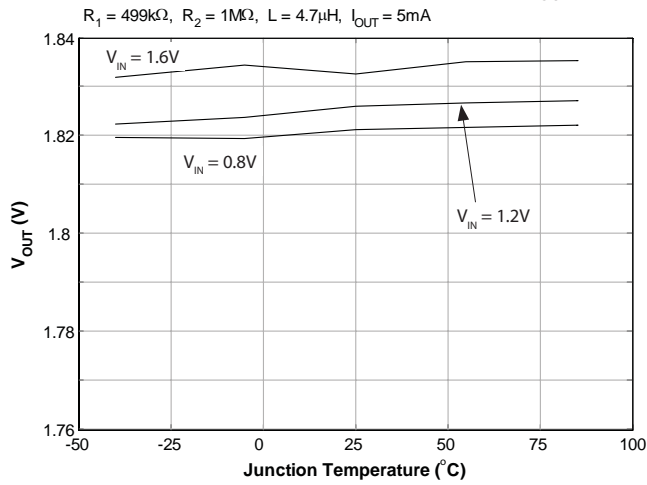### Line Regulation — PWM Mode (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, I_{OUT} = 35mA

SEMTECH
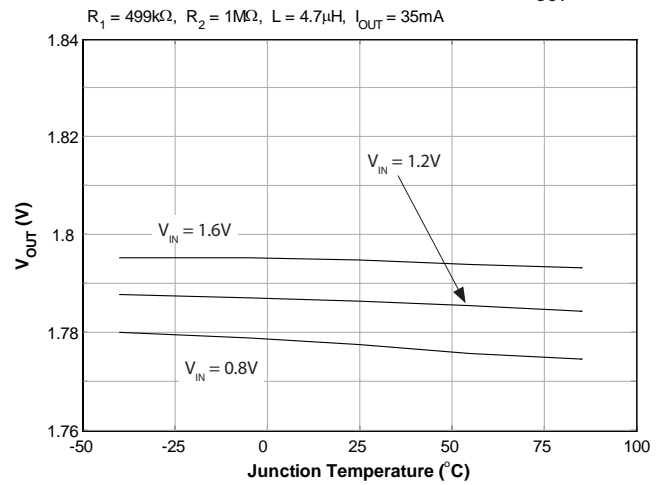
Typical Characteristics — V$_{OUT}$ = 1.8V (continued)

Temperature Regulation — PSAVE Mode (V$_{OUT}$ = 1.8V)

R$_1$ = 499kΩ, R$_2$ = 1MΩ, L = 4.7µH, I$_{OUT}$ = 5mA

Temperature Regulation — PWM Mode (V$_{OUT}$ = 1.8V)

R$_1$ = 499kΩ, R$_2$ = 1MΩ, L = 4.7µH, I$_{OUT}$ = 35mA

Startup Maximum Load Current vs. V$_{IN}$ (V$_{OUT}$ = 1.8V)

R$_1$ = 499kΩ, R$_2$ = 1MΩ, L = 4.7µH
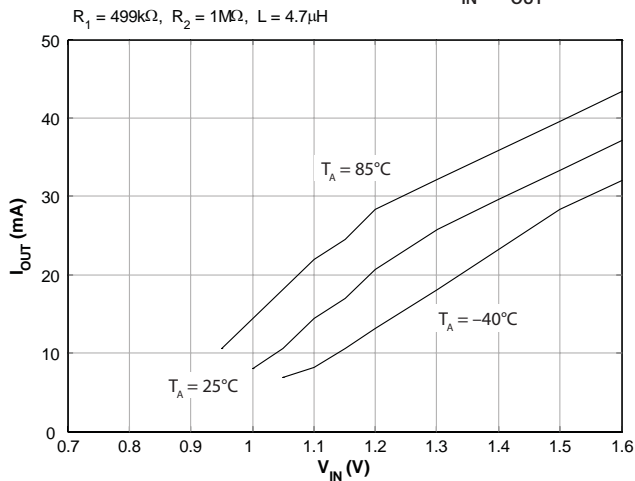
Startup Minimum Load Resistance vs. V$_{IN}$ (V$_{OUT}$ = 1.8V)

R$_1$ = 499kΩ, R$_2$ = 1MΩ, L = 4.7µH
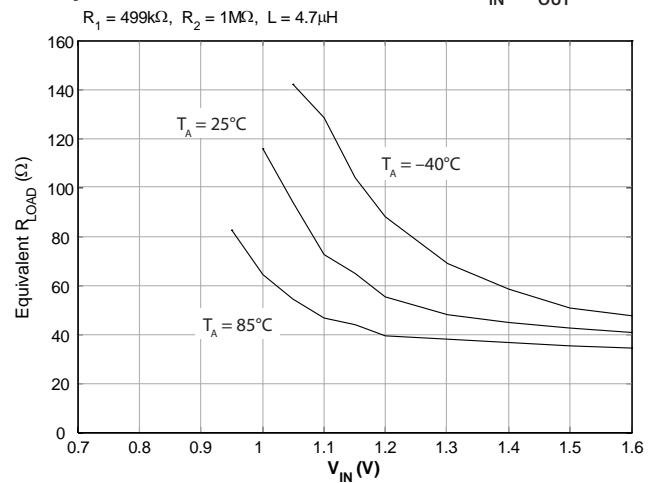
Maximum I$_{OUT}$ vs. V$_{IN}$ (V$_{OUT}$ = 1.8V)

R$_1$ = 499kΩ, R$_2$ = 1MΩ, L = 4.7µH

SEMTECH
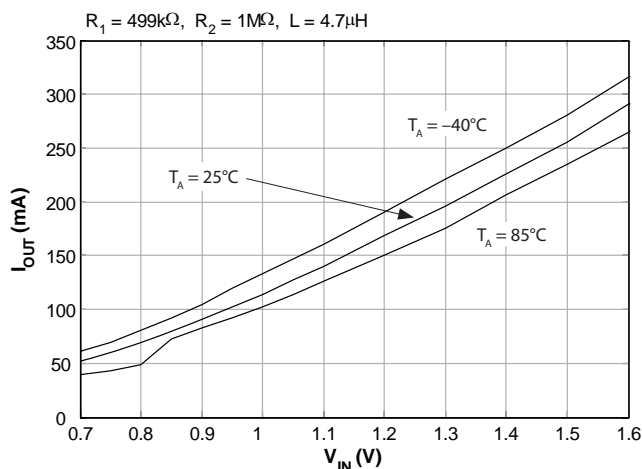
Typical Characteristics — V$_{OUT}$ = 3.3V

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 3.3V)
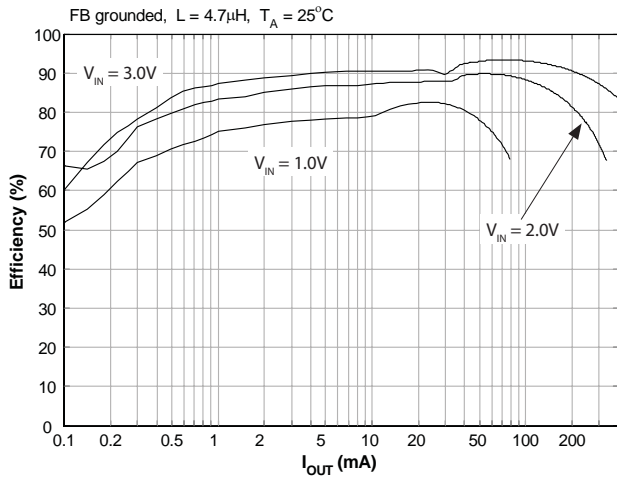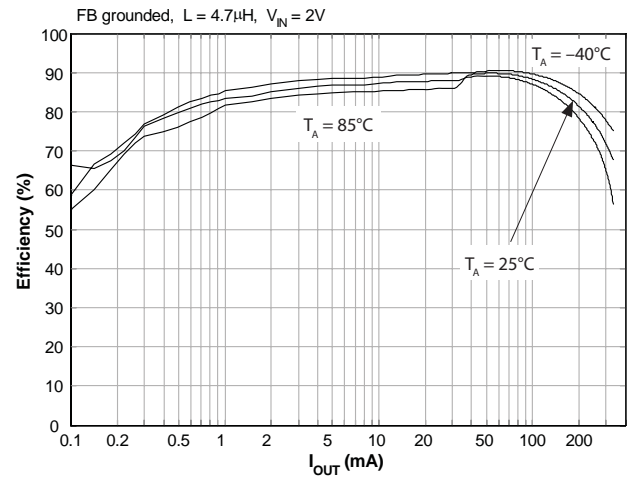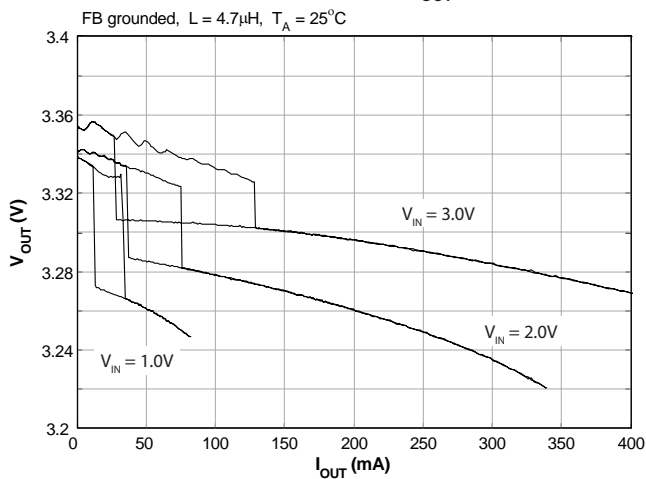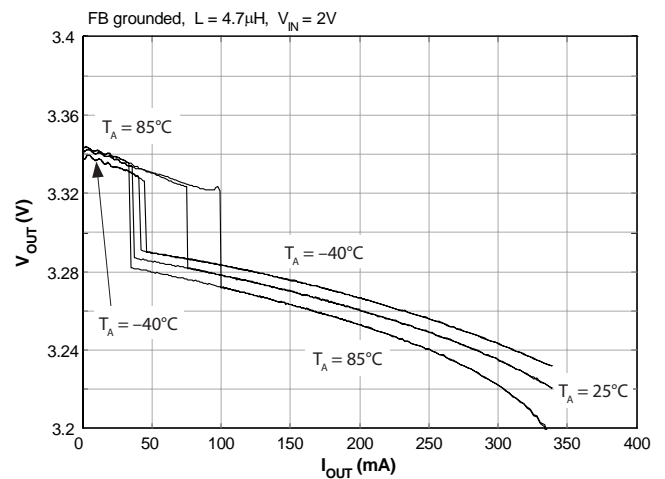
FB grounded, L = 4.7µH, T$_A$ = 25°C

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH, V$_{IN}$ = 2V

Load Regulation (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH, T$_A$ = 25°C

Load Regulation (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH, V$_{IN}$ = 2V

Line Regulation — PSAVE Mode (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH, I$_{OUT}$ = 5mA

Line Regulation — PWM Mode (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH, I$_{OUT}$ = 75mA

SEMTECH
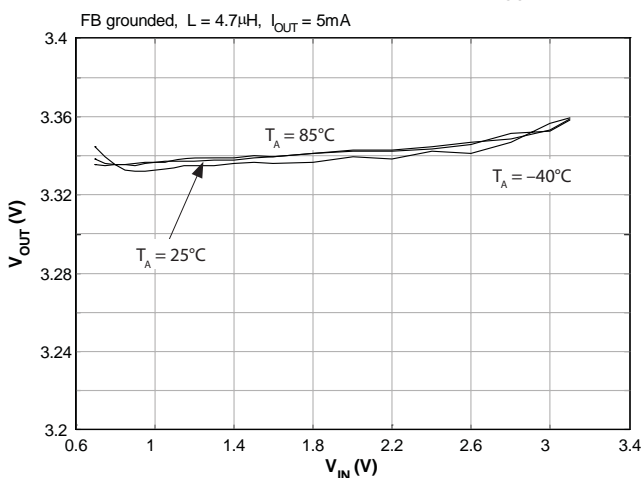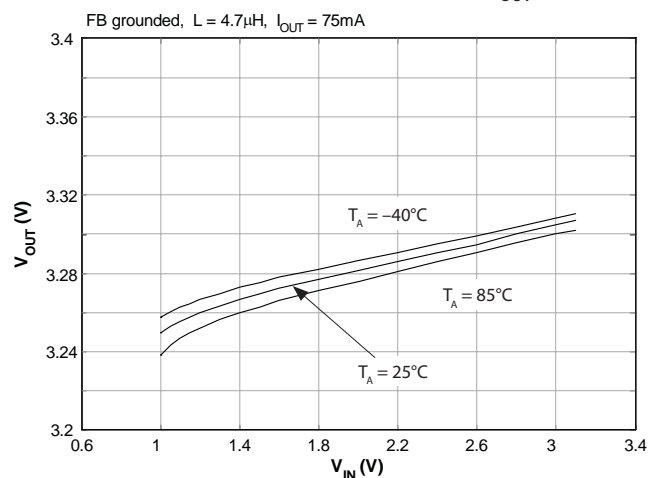
Typical Characteristics — V$_{OUT}$ = 3.3V (continued)

Temperature Regulation — PSAVE Mode (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH, I$_{OUT}$ = 5mA

Temperature Regulation — PWM Mode (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH, I$_{OUT}$ = 75mA
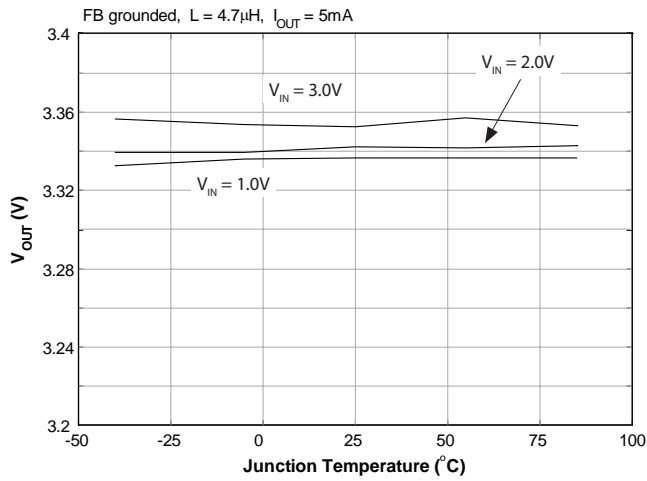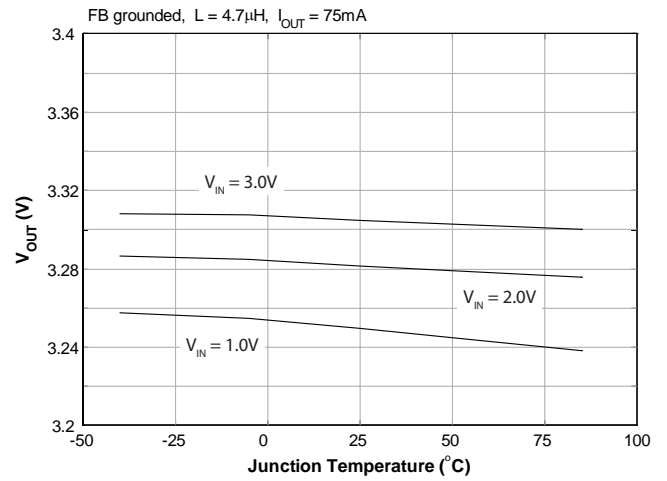
Startup Maximum Load Current vs. V$_{IN}$ (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH
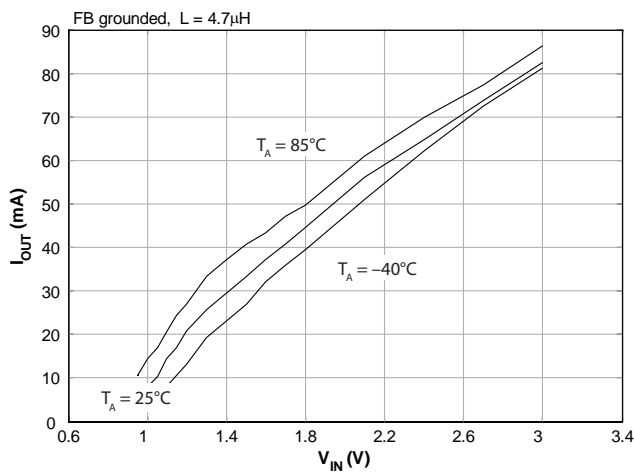
Startup Minimum Load Resistance vs. V$_{IN}$ (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH
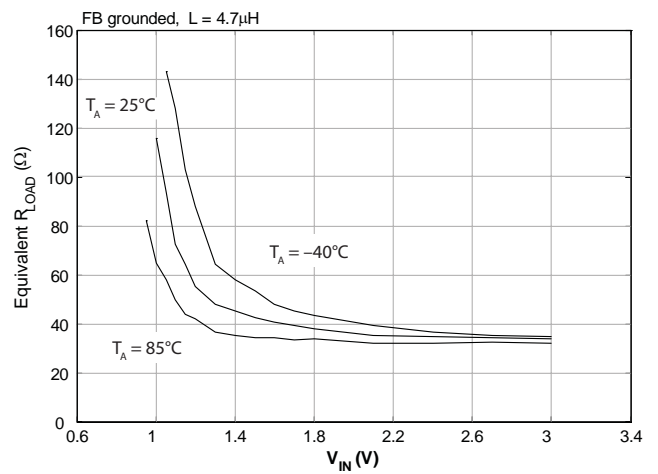
Maximum I$_{OUT}$ vs. V$_{IN}$ (V$_{OUT}$ = 3.3V)

FB grounded, L = 4.7µH
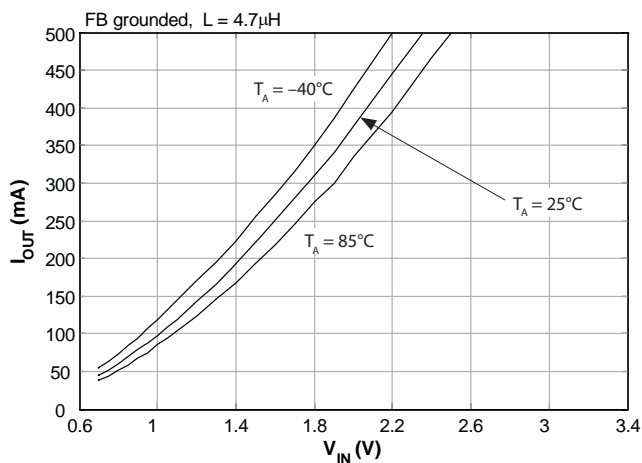
Typical Characteristics — V$_{OUT}$ = 4.0V

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 4.0V)

R$_1$ = 931kΩ, R$_2$ = 402kΩ, L = 4.7μH, C$_{FB}$ = 2.2pF, T$_A$ = 25°C

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 4.0V)

R$_1$ = 931kΩ, R$_2$ = 402kΩ, L = 4.7μH, C$_{FB}$ = 2.2pF, V$_{IN}$ = 2.4V

Load Regulation (V$_{OUT}$ = 4.0V)

R$_1$ = 931kΩ, R$_2$ = 402kΩ, L = 4.7μH, C$_{FB}$ = 2.2pF, T$_A$ = 25°C

Load Regulation (V$_{OUT}$ = 4.0V)

R$_1$ = 931kΩ, R$_2$ = 402kΩ, L = 4.7μH, C$_{FB}$ = 2.2pF, V$_{IN}$ = 2.4V

Line Regulation — PSAVE Mode (V$_{OUT}$ = 4.0V)

R$_1$ = 931kΩ, R$_2$ = 402kΩ, L = 4.7μH, C$_{FB}$ = 2.2pF, I$_{OUT}$ = 5mA

Line Regulation — PWM Mode (V$_{OUT}$ = 4.0V)

R$_1$ = 931kΩ, R$_2$ = 402kΩ, L = 4.7μH, C$_{FB}$ = 2.2pF, I$_{OUT}$ = 75mA

SEMTECH
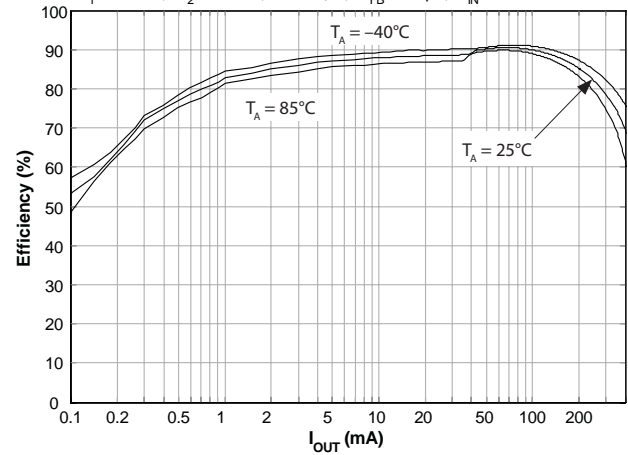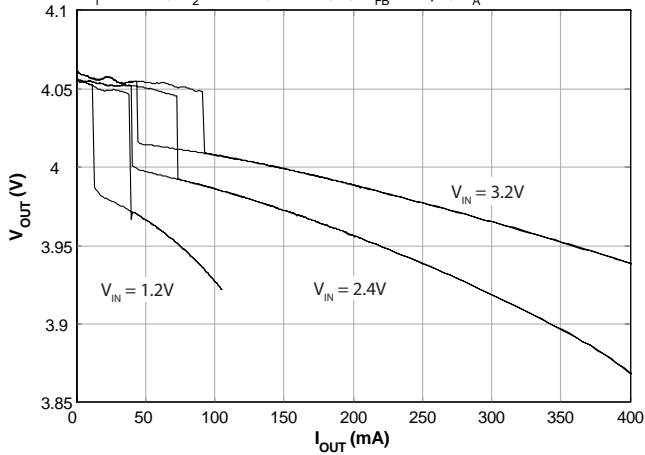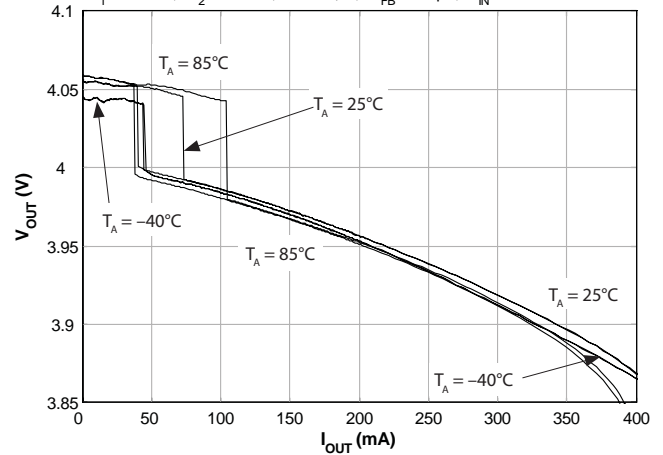
Typical Characteristics — V_{OUT} = 4.0V (continued)

Temperature Regulation — PSAVE Mode (V_{OUT} = 4.0V)

R_1 = 931kΩ, R_2 = 402kΩ, L = 4.7μH, C_{FB} = 2.2pF, I_{OUT} = 5mA

Y-axis: V_{OUT} (V), range 3.85 to 4.1
X-axis: Junction Temperature ($^{\circ}$C), range -50 to 100

Curves labeled: V_{IN} = 3.2V, V_{IN} = 1.2V, V_{IN} = 2.4V

Temperature Regulation — PWM Mode (V_{OUT} = 4.0V)

R_1 = 931kΩ, R_2 = 402kΩ, L = 4.7μH, C_{FB} = 2.2pF, I_{OUT} = 75mA

Y-axis: V_{OUT} (V), range 3.85 to 4.1
X-axis: Junction Temperature ($^{\circ}$C), range -50 to 100

Curves labeled: V_{IN} = 3.2V, V_{IN} = 2.4V, V_{IN} = 1.2V

Startup Maximum Load Current vs. V_{IN} (V_{OUT} = 4.0V)

R_1 = 931kΩ, R_2 = 402kΩ, L = 4.7μH, C_{FB} = 2.2pF

Y-axis: I_{OUT} (mA), range 0 to 100
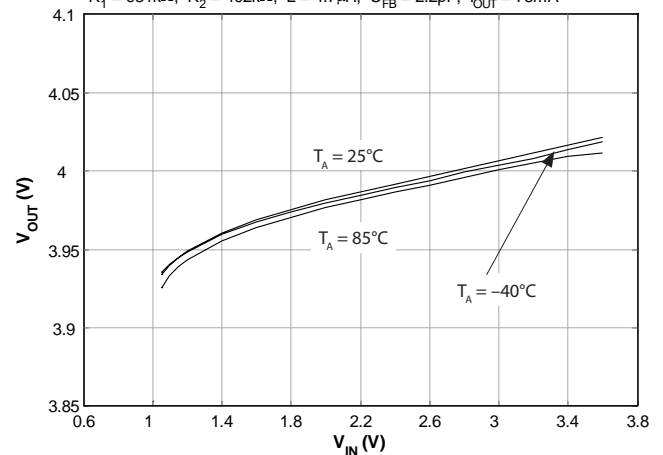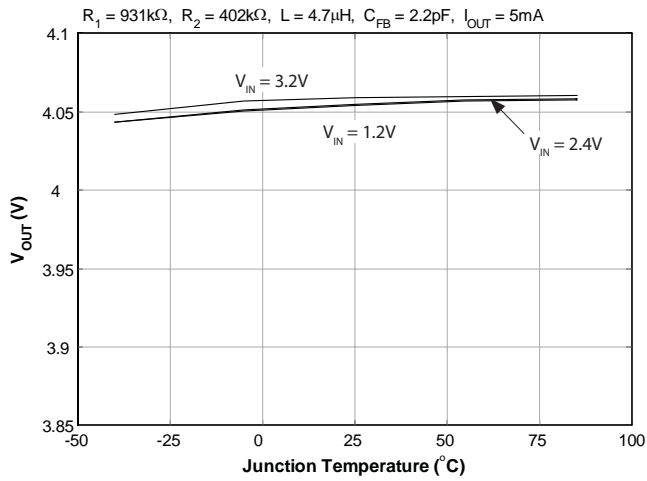X-axis: V_{IN} (V), range 0.6 to 3.8

Curves labeled: T_A = 85°C, T_A = −40°C, T_A = 25°C

Startup Minimum Load Resistance vs. V_{IN} (V_{OUT} = 4.0V)

R_1 = 931kΩ, R_2 = 402kΩ, L = 4.7μH, C_{FB} = 2.2pF

Y-axis: Equivalent R_{LOAD} (Ω), range 0 to 160
X-axis: V_{IN} (V), range 0.6 to 3.8

Curves labeled: T_A = 25°C, T_A = −40°C, T_A = 85°C

Maximum I_{OUT} vs. V_{IN} (V_{OUT} = 4.0V)

R_1 = 931kΩ, R_2 = 402kΩ, L = 4.7μH, C_{FB} = 2.2pF

Y-axis: I_{OUT} (mA), range 0 to 500
X-axis: V_{IN} (V), range 0.6 to 3.8

Curves labeled: T_A = 25°C, T_A = −40°C, T_A = 85°C

SEMTECH

Typical Characteristics — V$_{OUT}$ = 5.0V, Low V$_{IN}$ Range

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 5.0V)
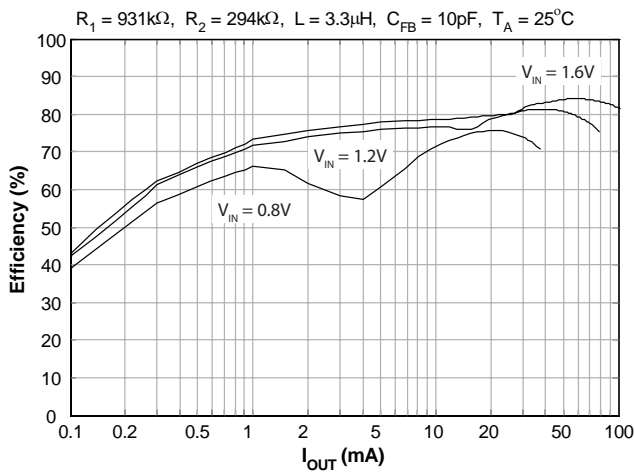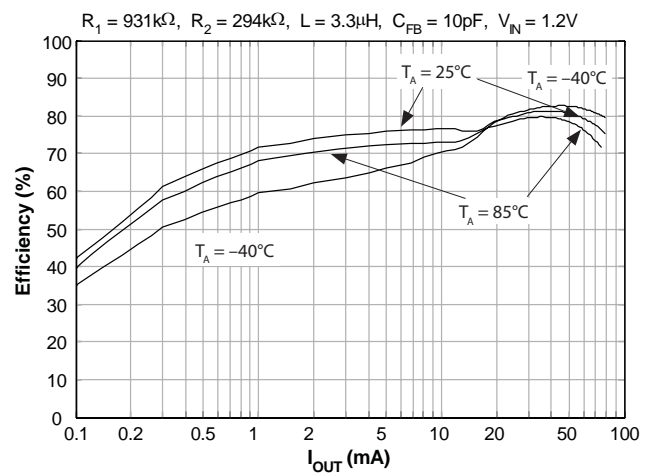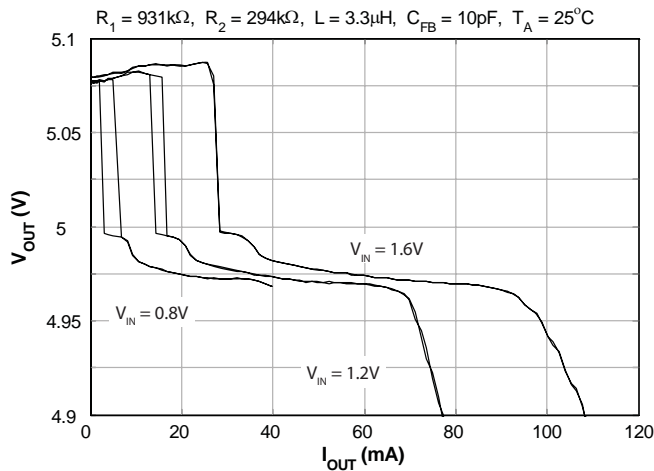
R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 3.3μH, C$_{FB}$ = 10pF, T$_A$ = 25°C

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 3.3μH, C$_{FB}$ = 10pF, V$_{IN}$ = 1.2V

Load Regulation (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 3.3μH, C$_{FB}$ = 10pF, T$_A$ = 25°C

Load Regulation (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 3.3μH, C$_{FB}$ = 10pF, V$_{IN}$ = 1.2V

Line Regulation — PSAVE Mode (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 3.3μH, C$_{FB}$ = 10pF, I$_{OUT}$ = 1mA

Line Regulation — PWM Mode (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 3.3μH, C$_{FB}$ = 10pF, I$_{OUT}$ = 35mA

SEMTECH
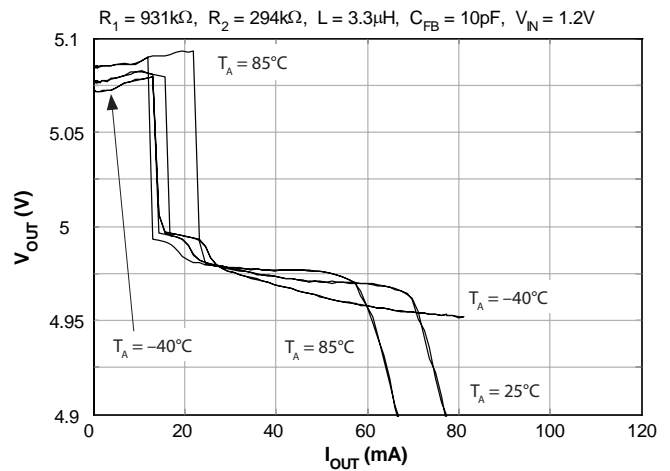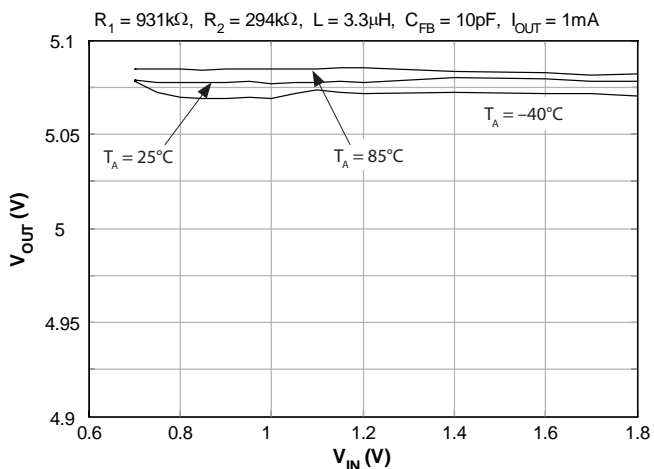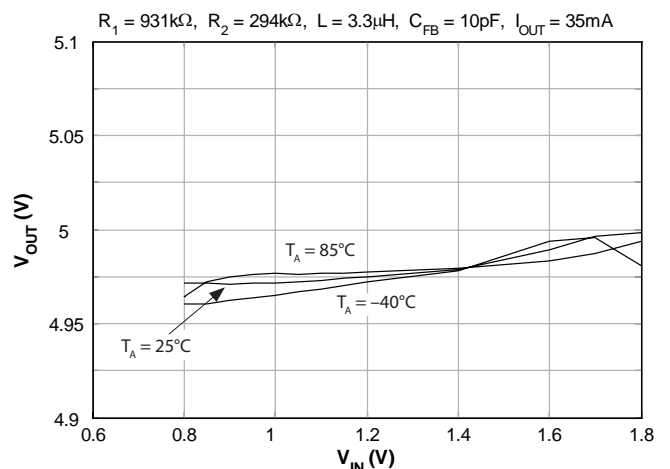
Typical Characteristics — V_{OUT} = 5.0V, Low V_{IN} Range (continued)
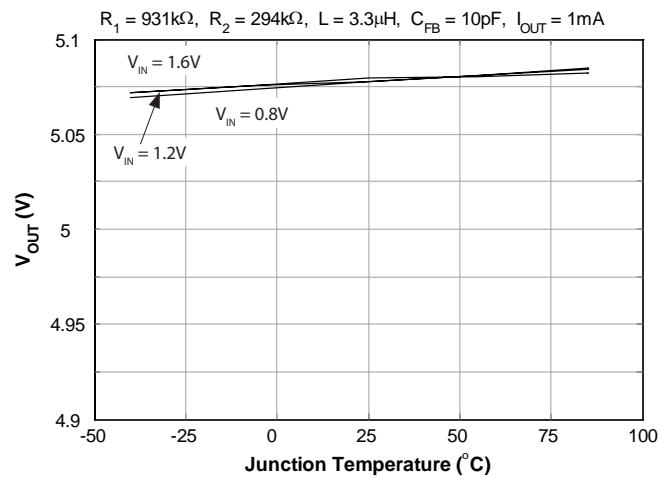
Temperature Regulation — PSAVE Mode (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 3.3µH, C_{FB} = 10pF, I_{OUT} = 1mA

Temperature Regulation — PWM Mode (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 3.3µH, C_{FB} = 10pF, I_{OUT} = 35mA

See page 16 for all V_{OUT} = 5.0V operation and startup load data.

SEMTECH
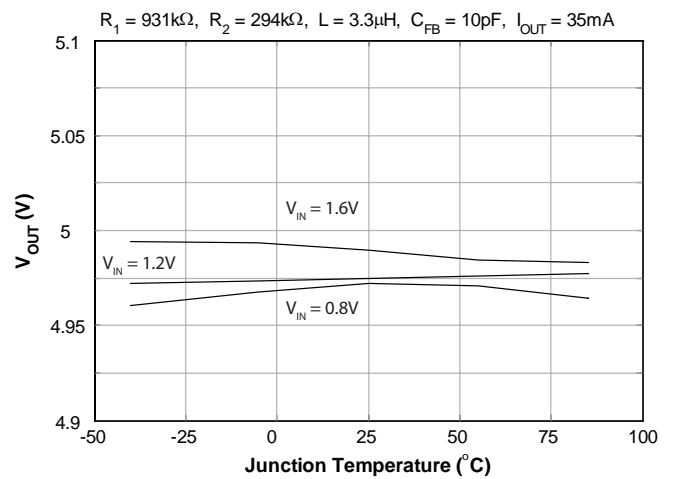
Typical Characteristics — V$_{OUT}$ = 5.0V, Mid V$_{IN}$ Range

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 5.0V)
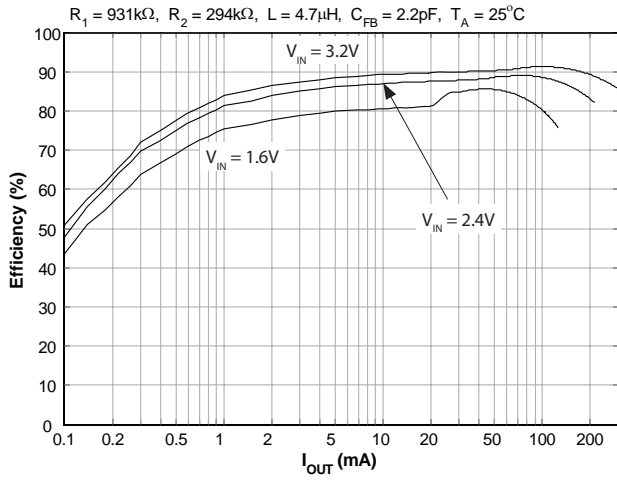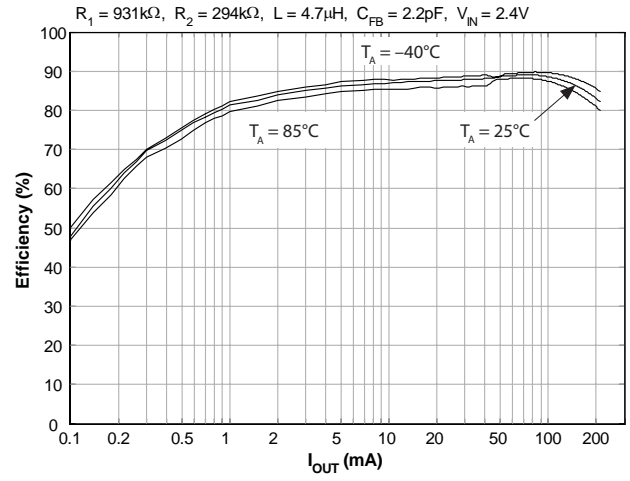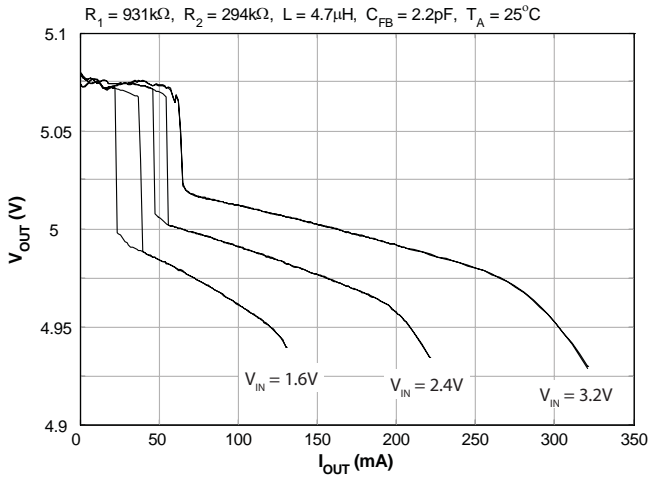
R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 4.7µH, C$_{FB}$ = 2.2pF, T$_A$ = 25°C

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 4.7µH, C$_{FB}$ = 2.2pF, V$_{IN}$ = 2.4V

Load Regulation (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 4.7µH, C$_{FB}$ = 2.2pF, T$_A$ = 25°C

Load Regulation (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 4.7µH, C$_{FB}$ = 2.2pF, V$_{IN}$ = 2.4V

Line Regulation — PSAVE Mode (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 4.7µH, C$_{FB}$ = 2.2pF, I$_{OUT}$ = 5mA

Line Regulation — PWM Mode (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 4.7µH, C$_{FB}$ = 2.2pF, I$_{OUT}$ = 75mA

SEMTECH
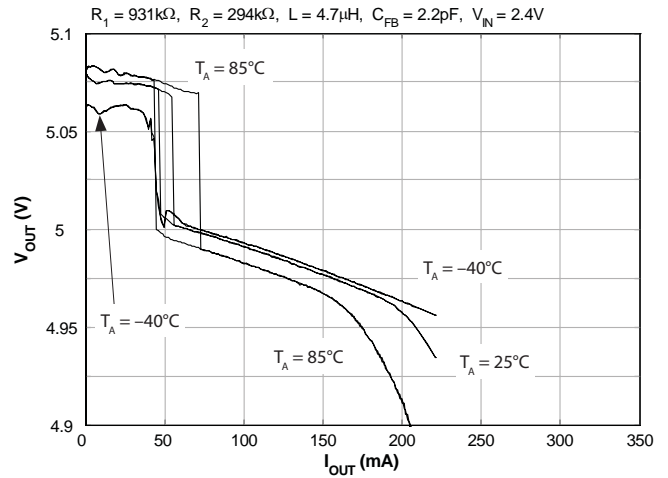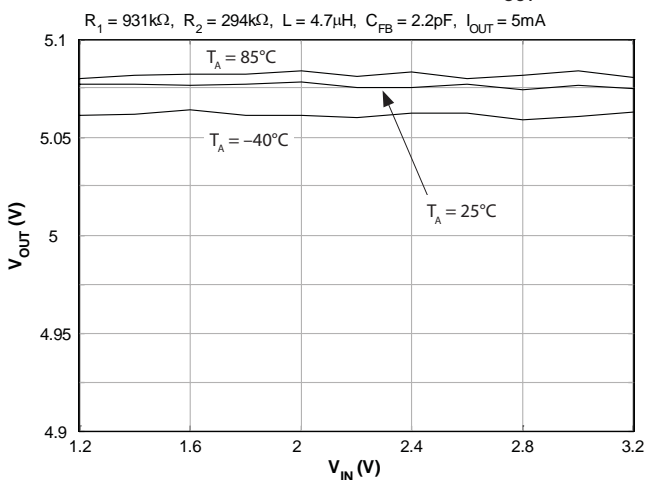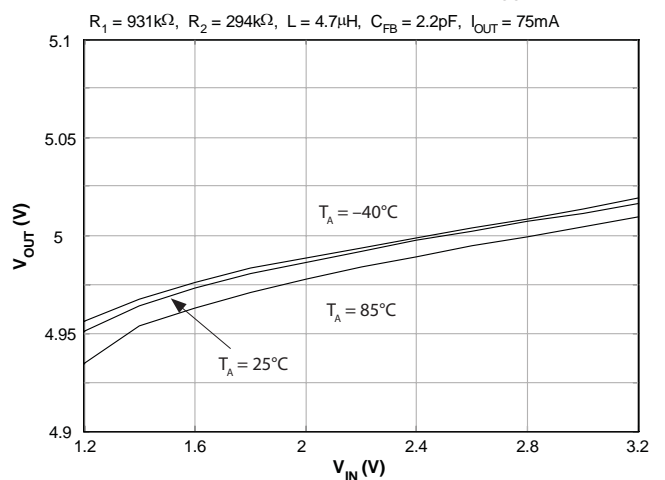
Typical Characteristics — V_OUT = 5.0V, Mid V_IN Range (continued)
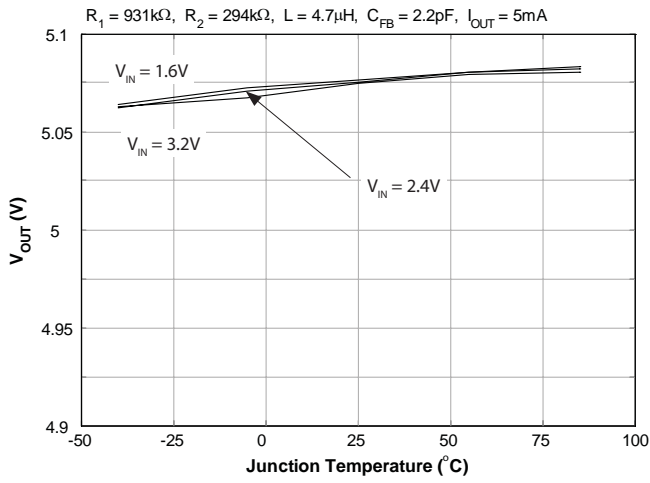
Temperature Regulation — PSAVE Mode (V_OUT = 5.0V)

R₁ = 931kΩ, R₂ = 294kΩ, L = 4.7µH, C_FB = 2.2pF, I_OUT = 5mA

Temperature Regulation — PWM Mode (V_OUT = 5.0V)

R₁ = 931kΩ, R₂ = 294kΩ, L = 4.7µH, C_FB = 2.2pF, I_OUT = 75mA

See page 16 for all V_OUT = 5.0V operation and startup load data.

SEMTECH
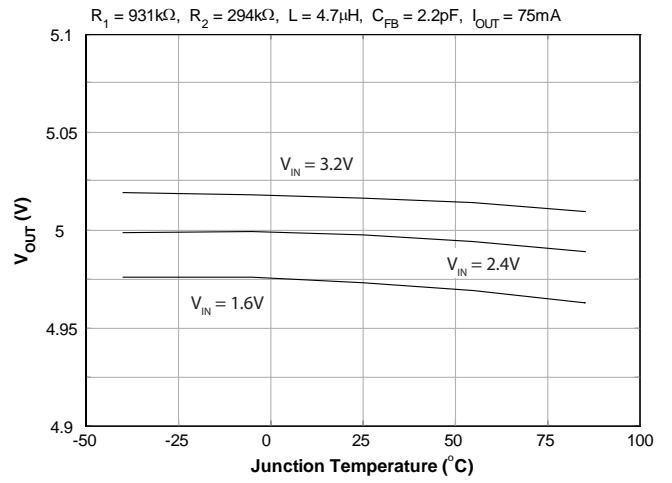
Typical Characteristics — V$_{OUT}$ = 5.0V, High V$_{IN}$ Range

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 5.0V)
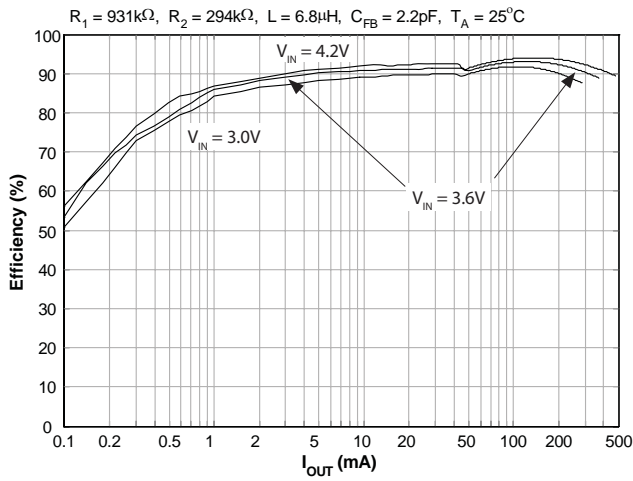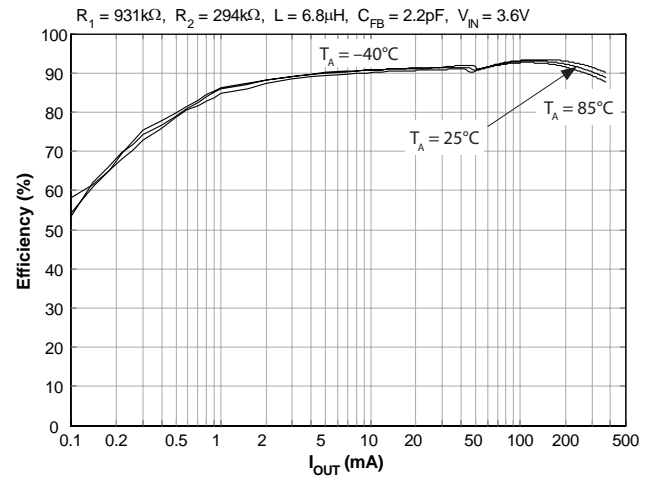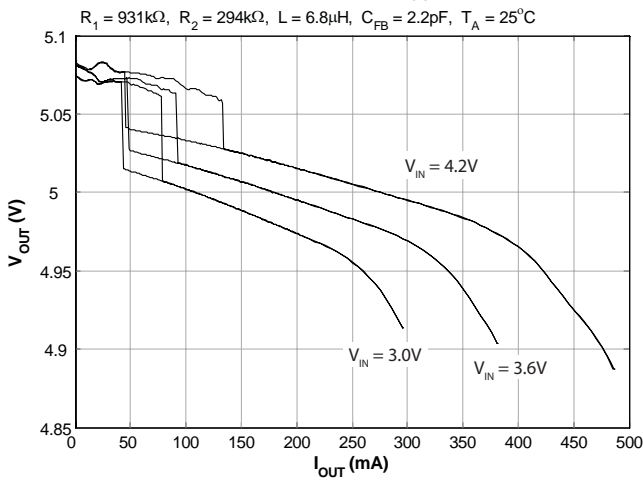
R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF, T$_A$ = 25°C

Efficiency vs. I$_{OUT}$ (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF, V$_{IN}$ = 3.6V

Load Regulation (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF, T$_A$ = 25°C

Load Regulation (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF, V$_{IN}$ = 3.6V

Line Regulation — PSAVE Mode (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF, I$_{OUT}$ = 5mA

Line Regulation — PWM Mode (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF, I$_{OUT}$ = 75mA

SEMTECH
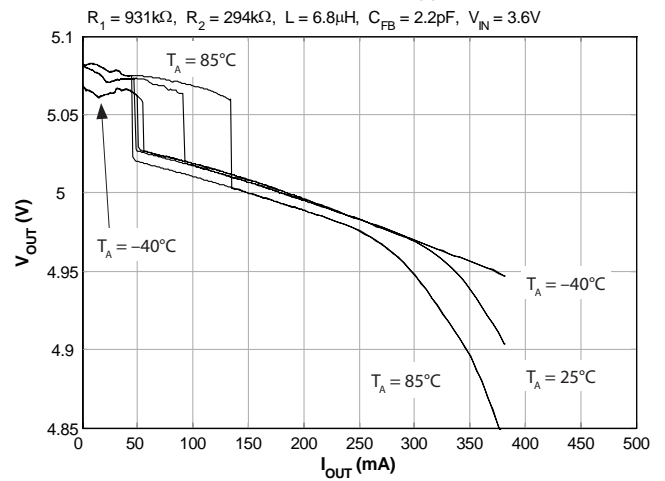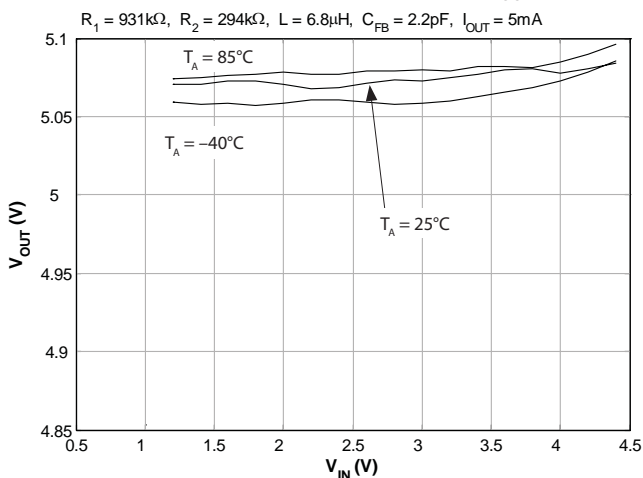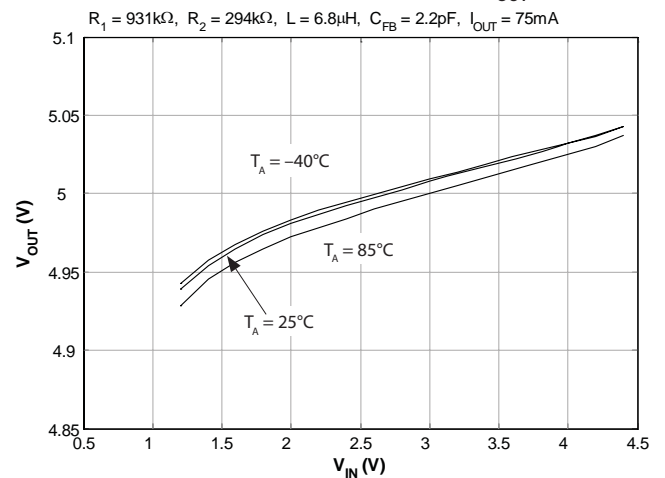
Typical Characteristics — V$_{OUT}$ = 5.0V, High V$_{IN}$ Range (continued)

Temperature Regulation — PSAVE Mode (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF, I$_{OUT}$ = 5mA

Temperature Regulation — PWM Mode (V$_{OUT}$ = 5.0V)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF, I$_{OUT}$ = 75mA
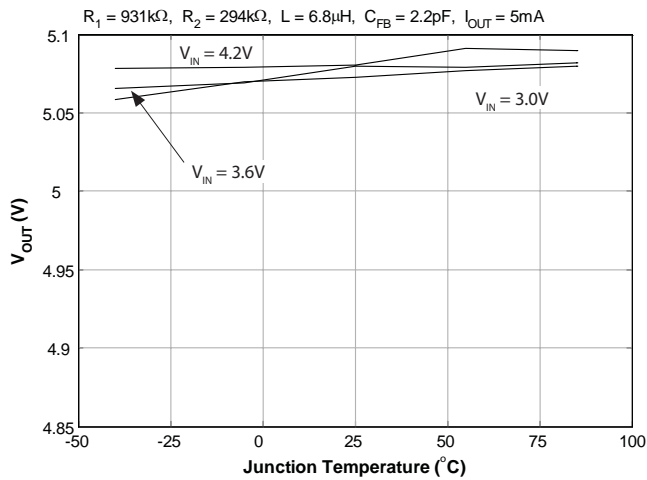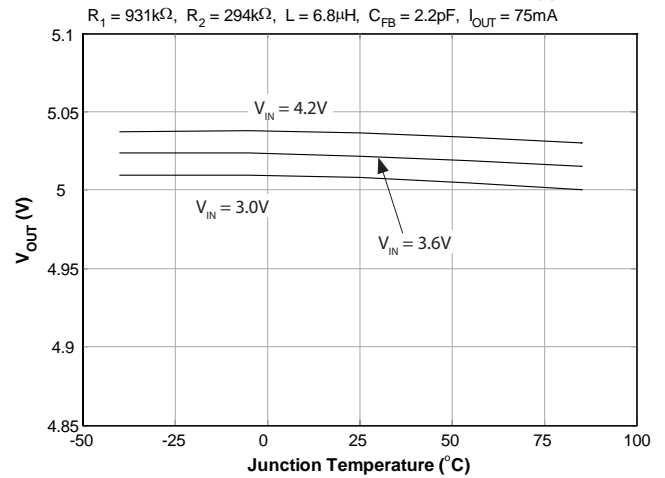

Startup Max. Load Current vs. V$_{IN}$ (V$_{OUT}$=5.0V, all V$_{IN}$'s)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF
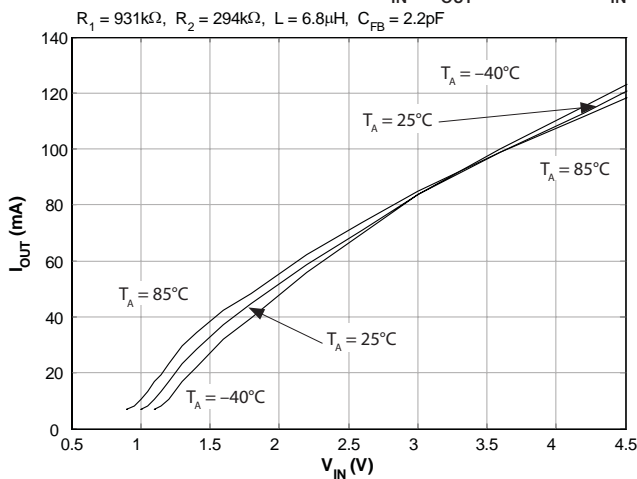
Startup Min. Load Res. vs. V$_{IN}$ (V$_{OUT}$=5.0V, all V$_{IN}$ Ranges)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 6.8µH, C$_{FB}$ = 2.2pF

Maximum I$_{OUT}$ vs. V$_{IN}$ (V$_{OUT}$ = 5.0V, all V$_{IN}$ Ranges)

R$_1$ = 931kΩ, R$_2$ = 294kΩ, L = 4.7µH, C$_{FB}$ = 2.2pF

SEMTECH
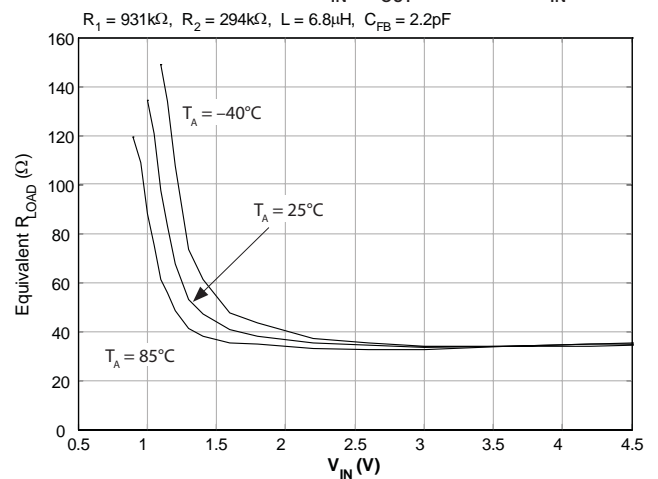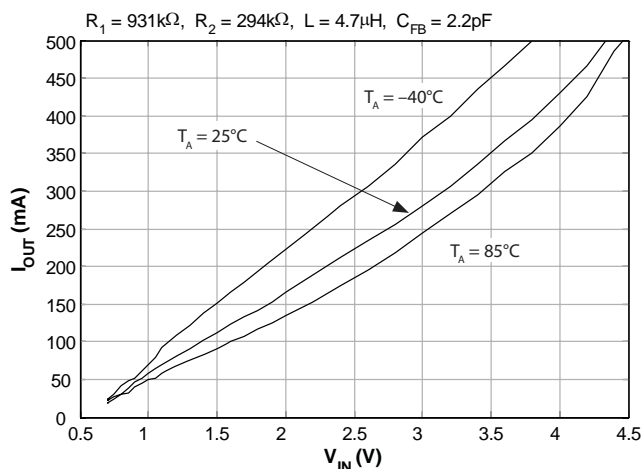
Typical Characteristics (continued)

Load Transient (PSAVE to PWM)

$V_{OUT} = 3.3V, V_{IN} = 1.2V, T_A = 25°C$

$I_{OUT} = 5mA$ to
100mA
(50mA/div)

V_{OUT}
(100mV/div)
AC Coupled

Time = (100µs/div)
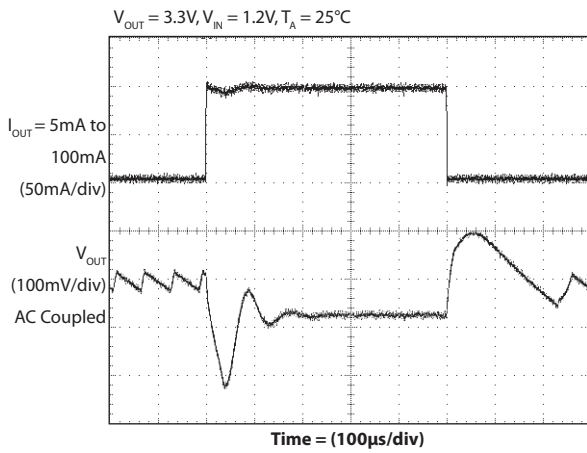
Load Transient (PWM to PWM)

$V_{OUT} = 3.3V, V_{IN} = 1.5V, T_A = 25°C$

$I_{OUT} = 40mA$ to
140mA
(50mA/div)

V_{OUT}
(100mV/div)
AC Coupled

Time = (100µs/div)

PSAVE Operation

$V_{OUT} = 3.3V, V_{IN} = 1.5V, I_{OUT} = 20mA$

V_{OUT} ripple
(50mV/div)

I_L
(100mA/div)

V_{LX}
(5V/div)

Time = (10µs/div)

PWM Operation

$V_{OUT} = 3.3V, V_{IN} = 1.5V, I_{OUT} = 50mA$

V_{OUT} ripple
(10mV/div)

I_L
(100mA/div)

V_{LX}
(5V/div)

Time = (400ns/div)
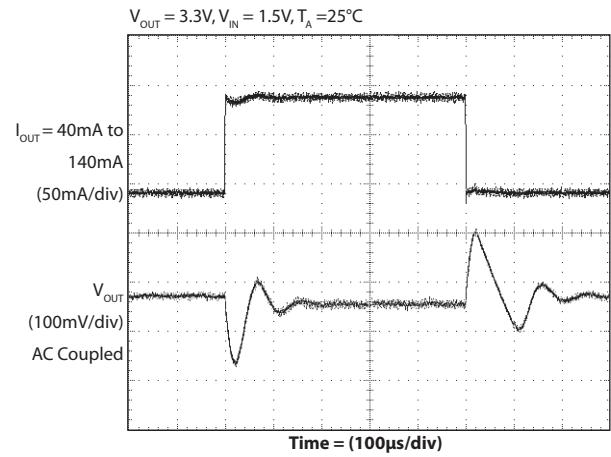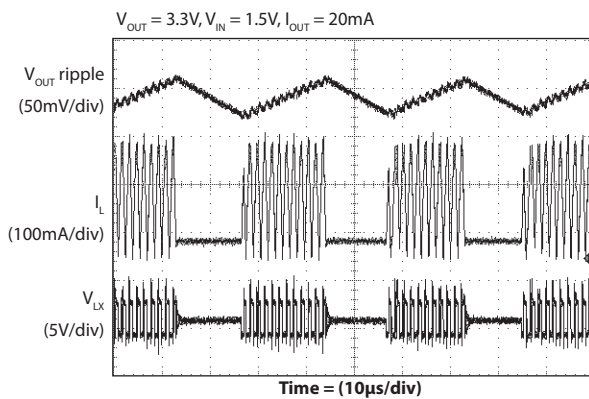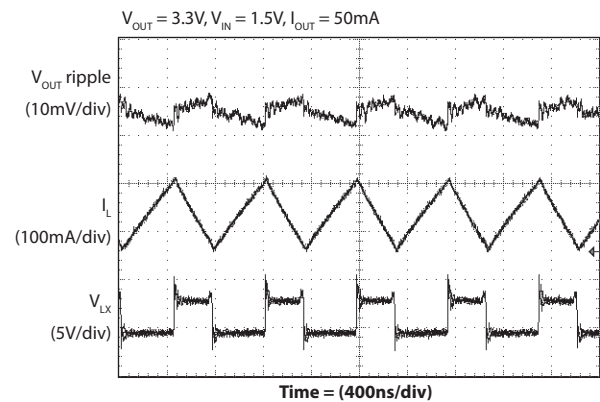
Minimum Startup V_{IN} vs. Temperature (Any V_{OUT})

Minimum Startup V_{IN} (V) vs. Junction Temperature (°C)

SEMTECH
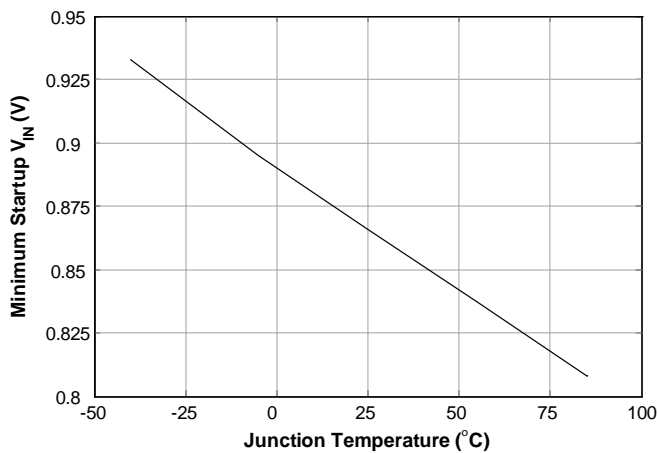
Pin Descriptions

MLPD Pin #	SOT23 Pin #	Pin Name	Pin Function
1	3	LX	Switching node — connect an inductor from the input supply to this pin.
2	2	GND	Signal and power ground.
3	1	IN	Battery or supply input — requires an external 10µF bypass capacitor (capacitance evaluated while under V_{IN} bias) for normal operation.
4	6	EN	Enable digital control input — active high.
5	5	FB	Feedback input — connect to GND for preset 3.3V output. A voltage divider is connected from OUT to GND to adjust output from 1.8V to 5.0V.
6	4	OUT	Output voltage pin — requires an external 10µF bypass capacitor (capacitance evaluated while under V_{OUT} bias) for normal operation.
T	NA	Thermal Pad	Thermal Pad (MLPD package only) is for heat sinking purposes — connect to ground plane using multiple vias — not connected internally.

SEMTECH

Block Diagram

SEMTECH
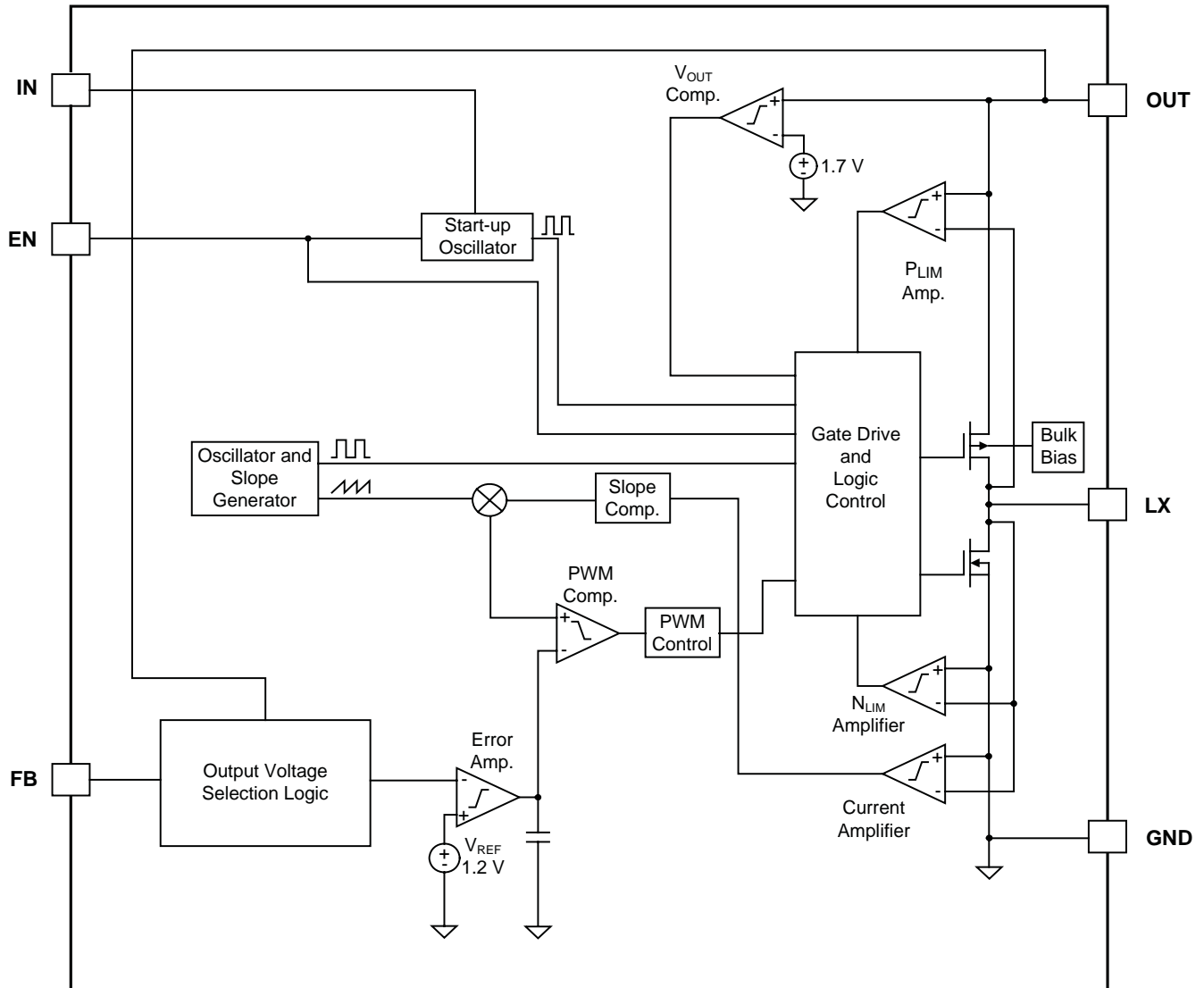
Applications Information

Detailed Description

The SC120 is a synchronous step-up Pulse Width Modulated (PWM) DC-DC converter utilizing a 1.2MHz fixed frequency current mode architecture. It is designed to provide output voltages in the range 1.8V to 5.0V from an input voltage as low as 0.7V, with a (output unloaded) start up input voltage of 0.85V.

The device operates in two modes: PWM and automatic PSAVE mode. In PWM operation, the devices uses pulse width modulation control to regulate the output under moderate to heavy load conditions. It switches to PSAVE mode when lightly loaded. Quiescent current consumption is as little as 50µA, into the OUT pin, when in PSAVE mode.

The regulator control circuitry is shown in the Block Diagram. It is comprised of a programmable feedback controller, an internal 1.2MHz oscillator, an n-channel Field Effect Transistor (FET) between the LX and GND pins, and a p-channel FET between the LX and OUT pins. The current flowing through both FETs is monitored and limited as required for startup, PWM operation, and PSAVE operation. An external inductor must be connected between the IN pin and the LX pin. When the n-channel FET is turned on, the LX pin is internally grounded, connecting the inductor between IN and GND. This is called the on-state. During the on-state, inductor current flows to ground and is increasing. When the n-channel FET is turned off and the p-channel FET is turned on (known as the off-state), the inductor is then connected between IN and OUT. The (now decreasing) inductor current flows from the input to the output, boosting the output voltage above the input voltage.

Output Voltage Selection

The SC120 output voltage can be programmed to an internally preset value or it can be programmed with external resistors. The output is internally programmed to 3.3V when the FB pin is connected to GND. Any output voltage in the range 1.8V to 5.0V can be programmed with a resistor voltage divider between OUT and the FB pin as shown in Figure 1.

The values of the resistors in the voltage divider network are chosen to satisfy the equation

$$V_{OUT} = 1.2 \times \left(1 + \frac{R_1}{R_2}\right) \quad (V)$$.

A large value of R_2, ideally 590kΩ or larger, is preferred for stability for V_{IN} within approximately 400mV of V_{OUT}. For lower V_{IN}, lower resistor values can be used. The values of R_1 and R_2 can be as large as desired to achieve low quiescent current.
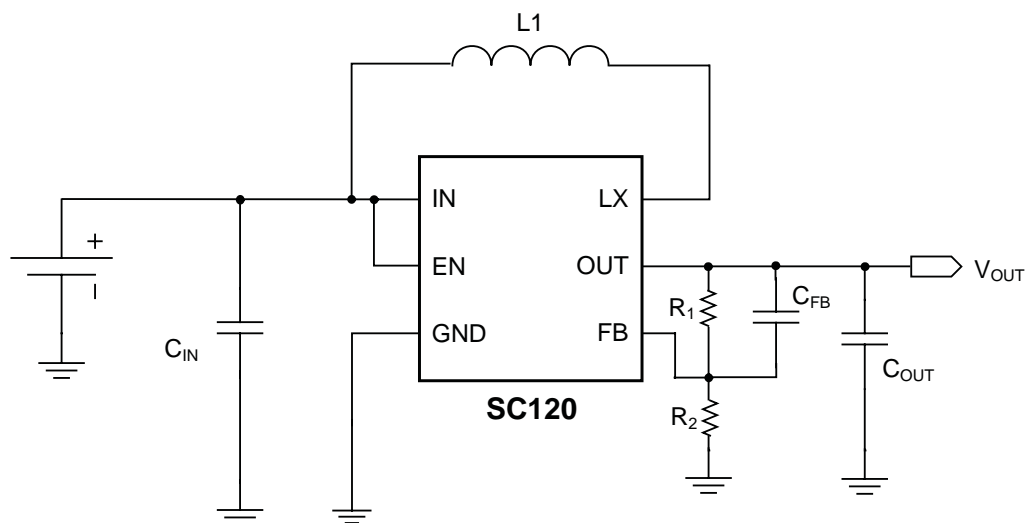

Figure 1 — Output Voltage Feedback Circuit

Applications Information (continued)

PWM Operation

The PWM cycle runs at a fixed frequency (f_{osc} = 1.2MHz), with a variable duty cycle (D). PWM operation continually draws current from the input supply (except for discontinuous mode, described subsequently). During the on-state of the PWM cycle, the n-channel FET is turned on, grounding the inductor at the LX pin. This causes the current flowing from the input supply through the inductor to ground to ramp up. During the off-state, the n-channel FET is turned off and the p-channel FET (synchronous rectifier) is turned on. This causes the inductor current to flow from the input supply through the inductor into the output capacitor and load, boosting the output voltage above the input voltage. The cycle then repeats to re-energize the inductor.

Ideally, the steady state (constant load) duty cycle is determined by $D = 1 - (V_{IN}/V_{OUT})$, but must be greater in practice to overcome dissipative losses. The SC120 PWM controller constrains the value of D such that $0.15 < D < 0.90$ (approximately).

The average inductor current during the off-state multiplied by (1-D) is equal to the average load current. The inductor current is alternately ramping up (on-state) and down (off-state) at a rate and amplitude determined by the inductance value, the input voltage, and the on-time ($T_{ON} = D \times T$, $T = 1/f_{osc}$). Therefore, the instantaneous inductor current will be alternately larger and smaller than the average. If the average output current is sufficiently small, the minimum inductor current can reach zero during the off-state. If the energy stored in the inductor is depleted (the inductor current decreases to zero) during the off-state, both FETs turn off for the remainder of the off-state. If this discontinuous mode (DM) operation persists, the SC120 transitions to PSAVE operation.

PSAVE Operation

At light loads, the SC120 will operate in PSAVE mode. At low output load, PSAVE mode will operate more efficiently than PWM mode. PSAVE mode also ensures regulation while the output load is too small to keep the PWM mode duty cycle above its minimum value, especially when V_{IN} is close to V_{OUT}. PSAVE operation is triggered by 256 consecutive cycles of DM operation in PWM mode, when the output of the P_{LIM} amplifier falls to 0V during the off-state due to low load current.

PSAVE mode requires fewer circuit resources than PWM mode. All unused circuitry is disabled to reduce quiescent power dissipation. In PSAVE mode, the OUT pin voltage monitoring circuit remains active and the output voltage error amplifier operates as a comparator. PSAVE regulation is shown in Figure 2. When $V_{OUT} < 1.008 \times V_{REG}$, where V_{REG} is the programmed output voltage, a burst of fixed-period switching occurs to boost the output voltage. The n-channel FET turns on (on-state) until the inductor current rises to approximately 240mA. The n-channel FET then turns off and the p-channel FET turns on to transfer the inductor energy to the output capacitor and load for the duration of the off-state. This cycle repeats until $V_{OUT} > 1.018 \times V_{REG}$, at which point both FETs are turned off. The output capacitor then discharges into the load until $V_{OUT} < 1.008 \times V_{REG}$, and the burst cycle repeats.

When the output current increases above a predetermined level, either of two PSAVE exit conditions will force the resumption of PWM operation. The first PSAVE exit criterion is shown in Figure 2. If the PSAVE burst cycle cannot provide sufficient current to the output, the output voltage will decrease during the burst. If $V_{OUT} < 0.98 \times V_{REG}$, PWM operation will resume. The second PSAVE exit criterion, illustrated in Figure 3, depends on the rate of discharge of the output capacitor between PSAVE bursts. If the time between bursts is less than 5μs, then PWM operation resumes. The output capacitance value will affect the second criterion, but not the first. Reducing the output capacitor will reduce the output load at which PSAVE mode exits to PWM mode.

Within each on/off cycle of a PSAVE burst, the rate of decrease of the inductor current during the off-state is proportional to ($V_{OUT} - V_{IN}$). If V_{IN} is sufficiently close to V_{OUT}, the decrease in current during the off-state may not overcome the increase in current during the minimum on-time of the on-state, approximately 100ns. This can result in the peak inductor current rising above the PSAVE mode n-channel FET current limit. (Normally, when the n-channel FET current limit is reached, the on-state ends immediately and the off-state begins. This sets the duty cycle on a cycle-by-cycle basis.) This inductor current rise
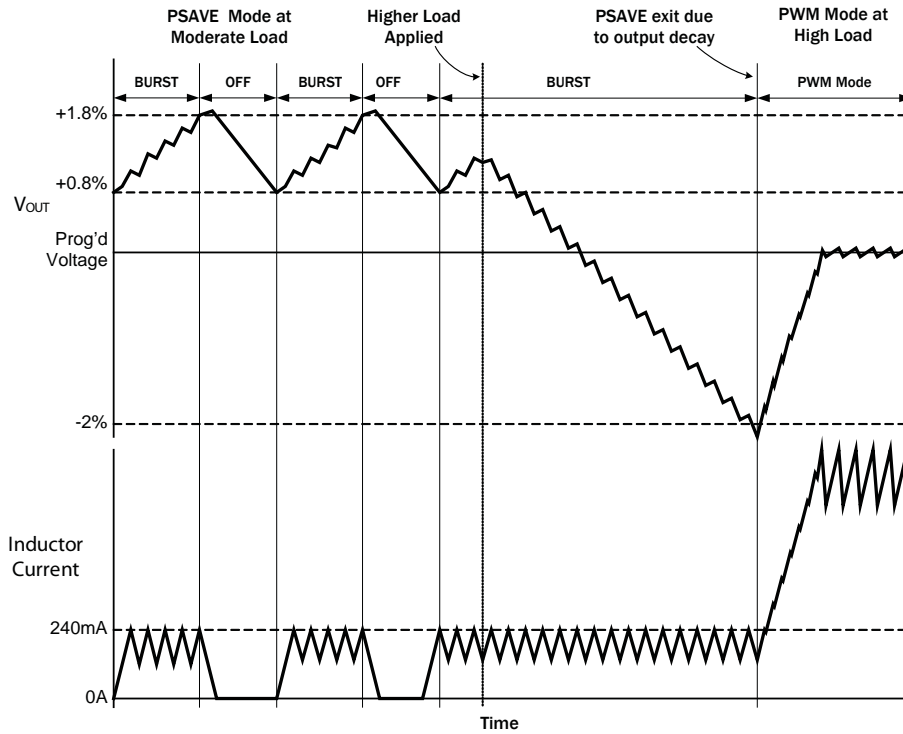
Applications Information (continued)

Figure 2 — PSAVE Operation With Exit to PWM Due To Output Voltage Decay
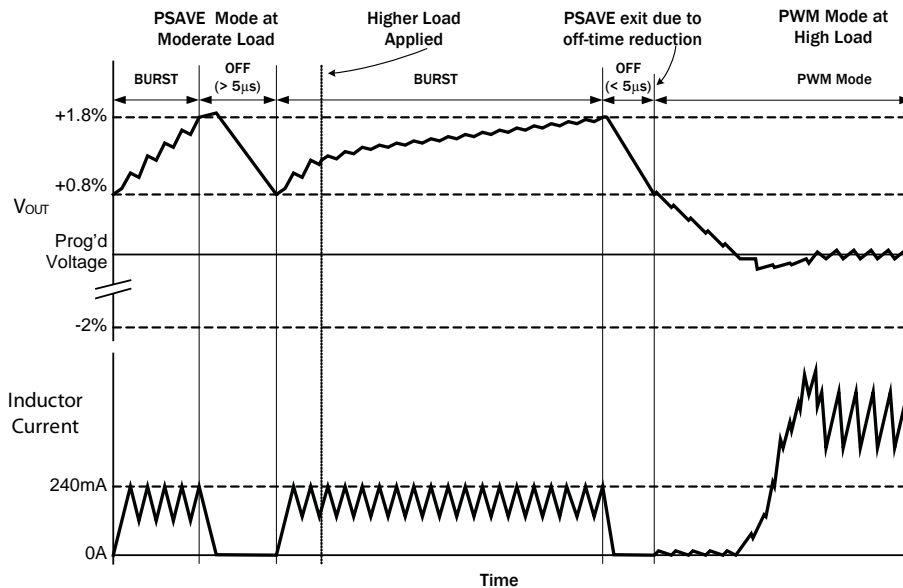

Figure 3 — PSAVE Operation With Exit to PWM Due To Off-time < 5µs

Applications Information (continued)

accumulates with each successive cycle in the burst. The result is that the output load current that can be supported in PSAVE under this high V_{IN} condition will be greater than occurs if the 240mA current limit can be enforced. Therefore the PSAVE exit load due to the first exit criterion (Figure 2) can increase significantly. This phenomenon is advantageous. Reverting to PWM operation with high V_{IN} can result in V_{OUT} rising above V_{REG}, due to the PWM minimum duty cycle. PSAVE operation avoids this voltage rise because of its hysteretic voltage-threshold on/off control. If the load remains low enough to remain in PSAVE, V_{IN} can approach and even slightly exceed V_{OUT}. To initally enter PSAVE mode, the initial startup load must be small enough to cause discontinuous mode PWM operation. This PSAVE mode startup load upper limit can be increased if needed by reducing the inductance. (Refer to the Inductor Selection section.) Sufficiently large output capacitance will prevent PSAVE exit due to the second exit criterion (Figure 3).

PSAVE V_{OUT} ripple may increase due to parasitic capacitance on the external FB pin network. If using external feedback programming, it is prudent to add a small capacitor between OUT and FB to the circuit board layout. When operating the SC120 in the final configuration in PSAVE, observe the amplitude of PSAVE ripple. If the ripple exceeds 50mV for the expected range of input voltage, a small-value capacitor should be tried. Capacitance on the order of a few picofarads is often sufficient to bring the ripple amplitude to approximately 50mV.

In the case of low V_{IN} and high V_{OUT}, larger values of CFB may be needed, perhaps 4.7pF or higher. If using the SOT23-6 package (SC120SKTRT) with low V_{IN} and high V_{OUT}, at least 10pF to 12pF is recommended.

The Enable Pin
The EN pin is a high impedance logical input that can be used to enable or disable the SC120 under processor control. $V_{EN} < 0.2V$ will disable regulation, set the LX pin in a high-impedance state (turn off both FET switches), and turn on an active discharge device to discharge the output capacitor via the OUT pin. $V_{EN} > 0.85V$ will enable the output. The startup sequence from the EN pin is identical to the startup sequence from the application of input power.

Regulator Startup, Short Circuit Protection, and Current Limits
The SC120 permits power up at input voltages from 0.85V to 4.5V. Startup current limiting of the internal switching n-channel and p-channel FET power devices protects them from damage in the event of a short between OUT and GND. As the output voltage rises, progressively less-restrictive current limits are applied. This protection unavoidably prevents startup into an excessive load.

To begin, the p-channel FET between the LX and OUT pins turns on with its current limited to approximately 150mA, the short-circuit output current. When V_{OUT} approaches V_{IN} (but is still below 1.7V), the n-channel current limit is set to 350mA (the p-channel limit is disabled), the internal oscillator turns on (approximately 200kHz), and a fixed 75% duty cycle PWM operation begins. (See the section PWM Operation.) When the output voltage exceeds 1.7V, fixed frequency PWM operation begins, with the duty cycle determined by an n-channel FET peak current limit of 350mA. When this n-channel FET startup current limit is exceeded, the on-state ends immediately and the off-state begins. This determines the duty cycle on a cycle-by-cycle basis. When V_{OUT} is within 2% of the programmed regulation voltage, the n-channel FET current limit is raised to 1.2A, and normal voltage regulation PWM control begins.

Once normal voltage regulation PWM control is initiated, the output becomes independent of V_{IN} and output regulation can be maintained for V_{IN} as low as 0.7V, subject to the maximum duty cycle and peak current limits. The duty cycle must remain between 15% and 90% for the device to operate within specification.

Note that startup with a regulated active load is not the same as startup with a resistive load. The resistive load output current increases proportionately as the output voltage rises until it reaches programmed V_{OUT}/R_{LOAD}, while a regulated active load presents a constant load as the output voltage rises from 0V to programmed V_{OUT}. Note also that if the load applied to the output exceeds an applicable V_{OUT} dependent startup current limit or duty cycle limit, the criterion to advance to the next startup stage may not be achieved. In this situation startup may

SEMTECH

Applications Information (continued)

pause at a reduced output voltage until the load is reduced further.

Output Overload and Recovery

When in PSAVE operation, an increasing load will eventually satisfy one of the PSAVE exit criteria and regulation will revert to PWM operation. As previously noted, the PWM steady state duty cycle is determined by $D = 1 - (V_{IN}/V_{OUT})$, but must be somewhat greater in practice to overcome dissipative losses. As the output load increases, the dissipative losses also increase. The PWM controller must increase the duty cycle to compensate. Eventually, one of two overload conditions will occur, determined by V_{IN}, V_{OUT}, and the overall dissipative losses due to the output load current. Either the maximum duty cycle of 90% will be reached or the n-channel FET 1.2A (nominal) peak current limit will be reached, which effectively limits the duty cycle to a lower value. Above that load, the output voltage will decrease rapidly and in reverse order the startup current limits will be invoked as the output voltage falls through its various voltage thresholds. How far the output voltage drops depends on the load voltage vs. current characteristic.

A reduction in input voltage, such as a discharging battery, will lower the load current at which overload occurs. Lower input voltage increases the duty cycle required to produce a given output voltage. And lower input voltage also increases the input current to maintain the input power, which increases dissipative losses and further increases the required duty cycle. Therefore an increase in load current or a decrease in input voltage can result in output overload. Once an overload has occurred, the load must be decreased to permit recovery. The conditions required for overload recovery are identical to those required for successful initial startup.

Anti-ringing Circuitry

In PWM operation, the n-channel and p-channel FETs are simultaneously turned off when the inductor current reaches zero. They remain off for the zero-inductor-current portion of the off-state. Note that discontinuous mode is a marginal-load condition, which if persistent will trigger a transition to PSAVE operation.

When both FET switches are simultaneously turned off, an internal switch between the IN and LX pins is closed, pro-

viding a moderate resistance path across the inductor to dampen the oscillations at the LX pin. This effectively reduces EMI that can develop from the resonant circuit formed by the inductor and the drain capacitance at LX.

The anti-ringing circuitry is disabled between PSAVE bursts.

Component Selection

The SC120 provides optimum performance when a 4.7µH inductor is used with a 10µF output capacitor. Different component values can be used to modify PSAVE exit or entry loads, modify output voltage ripple in PWM mode, improve transient response, or to reduce component size or cost.

Inductor Selection

The inductance value primarily affects the amplitude of inductor current ripple (ΔI_L). Reducing inductance increases ΔI_L. This raises the inductor peak current, $I_{L-max} = I_{L-avg} + \Delta I_L/2$, where I_{L-avg} is the inductor current averaged over a full on/off cycle. I_{L-max} is subject to the n-channel FET current limit $I_{LIM(N)}$, therefore reducing the inductance may lower the output overload current threshold. Increasing ΔI_L also lowers the inductor minimum current, $I_{L-min} = I_{L-avg} - \Delta I_L/2$, thus raising the PSAVE entry load current threshold. This is the output load below which $I_{L-min} = 0$, the boundary between continuous mode and discontinuous mode PWM regulation, which signals the SC120 controller to switch to PSAVE operation. In the extreme case of V_{IN} approaching V_{OUT}, smaller inductance can also *reduce* the PSAVE inductor burst-envelope current ripple and voltage ripple.

Equate input power to output power, note that input current equals inductor current, and average over a full PWM switching cycle to obtain

$$I_{L-avg} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}}$$

where η is efficiency.

ΔI_L is the inductor (and thus the input) peak-to-peak current. Neglecting the n-channel FET R_{DS-ON} and the inductor DCR, for duty cycle D, and with $T = 1/f_{osc}$,

Applications Information (continued)

$$\Delta I_{L-on} = \frac{1}{L}\int_0^{DT} V_{IN}\,dt = \frac{V_{IN}\times D\times T}{L}$$

This is the change in I_L during the on-state. During the off-state, again neglecting the p-channel FET R_{DS-ON} and the inductor DCR,

$$\Delta I_{L-off} = \frac{1}{L}\int_{DT}^{T}\left(V_{IN}-V_{OUT}\right)dt = \frac{\left(V_{IN}-V_{OUT}\right)\times T}{L}\left(1-D\right)$$

Note that this is a negative quantity, since $V_{OUT} > V_{IN}$ and $0 < D < 1$. For a constant load in steady-state, the inductor current must satisfy $\Delta I_{L-on} + \Delta I_{L-off} = 0$. Substituting the two expressions and solving for D, obtain D = 1 – V_{IN}/V_{OUT}. Using this expression, and the positive valued expression $\Delta I_L = \Delta I_{L-on}$ for current ripple amplitude, obtain expanded expression for I_{L-max} and I_{L-min}.

$$I_{L-max,min} = \frac{V_{OUT}\times I_{OUT}}{V_{IN}\times\eta} \pm \frac{T}{2\times L}\times\frac{V_{IN}}{V_{OUT}}\times\left(V_{OUT}-V_{IN}\right)$$

If the value of I_{OUT} decreases until $I_{L-min} = 0$, which is the boundary of continuous and discontinuous PWM operation, the SC120 will transition from PWM operation to PSAVE operation. Define this value of I_{OUT} as $I_{PSAVE-entry}$. Setting the expression for I_{L-min} to 0 and solving,

$$I_{PSAVE-entry} = \frac{\eta\times T}{2\times L}\left(\frac{V_{IN}}{V_{OUT}}\right)^2\left(V_{OUT}-V_{IN}\right)$$

The programmed value of V_{OUT} is constant. $I_{PSAVE-entry}$ is a polynomial function of V_{IN}. Equating $dI_{PSAVE-entry}/dV_{IN} = 0$ and solving for V_{IN} reveals that there is one non-zero extremum of this function, a maximum, at $V_{IN} = {}^2/_3\,V_{OUT}$.* Applying this value of V_{IN},

$$I_{PSAVE-entry-max} = \frac{\eta\times T}{L}\times\frac{2}{27}\times V_{OUT}$$

The value of the inductor determines the PSAVE entry output load current for a given V_{IN}. Evaluate $I_{PSAVE-entry}$ at the

* For simplicity, efficiency (η) is represented as a constant. But efficiency, itself a function of V_{IN}, decreases with decreasing V_{IN} (and decreases with increasing temperature). Therefore at a given temperature, the input voltage that produces the maximum PSAVE entry load current will be slightly greater than $^2/_3$ of V_{OUT}.

smallest and largest expected values of V_{IN}. If the input range includes $V_{IN} = {}^2/_3\,V_{OUT}$, also determine $I_{PSAVE-entry-max}$. Note that at high V_{IN} (V_{IN} close to V_{OUT}) PSAVE exit may require an unusually high output load current. In this case, PSAVE re-entry may be of little concern. So if the largest V_{IN} exceeds approximately 90% of V_{OUT}, instead evaluate PSAVE entry at $V_{IN} = 0.9V_{OUT}$.

To ensure that $I_{PSAVE-entry-max}$ will be less than the PSAVE exit current, evaluate the PSAVE-PWM mode transistions while applying increasing and decreasing loads with V_{IN} at and above $^2/_3\,V_{OUT}$. This should be done at the application's lowest specified ambient temperature as well as at room temperature. If the PSAVE exit current is not sufficiently greater than the PSAVE entry current, the separation can be enhanced by increasing the output capacitance to raise $I_{PSAVE-exit}$ due to the 5µs off-time criterion (see Figure 3), or by increasing the inductor value to reduce $I_{PSAVE-entry}$.

The inductor selection should also consider the n-channel FET current limit for the expected range of input voltage and output load current. The largest I_{L-avg} will occur at the expected smallest V_{IN} and largest I_{OUT}. Determine the largest allowable ΔI_L, based on the largest expected I_{L-avg}, the minimum n-channel FET current limit, and the inductor tolerance. Ensure that in the worst case, $I_{L-avg} + \Delta I_L/2 < I_{LIM(N)}$.

These calculations include the parameter η, efficiency. Efficiency varies with V_{IN}, I_{OUT}, and temperature. Estimate η using the plots provided in this datasheet, or from experimental data, at the operating condition of interest when computing the effect of a new inductor value on PSAVE entry and I-limit margin.

Any chosen inductor should have low DCR, compared to the R_{DS-ON} of the FET switches, to maintain efficiency, though for DCR << R_{DS-ON}, further reduction in DCR will provide diminishing benefit. The inductor I_{SAT} value should exceed the expected I_{L-max}. The inductor self-resonant frequency should exceed $5\times f_{osc}$. Any inductor with these properties should provide satisfactory performance.

L = 4.7µH should perform well for most applications. For high V_{OUT}, (4.0V to 5.0V), and relatively high V_{IN} (3.3V and above), L = 6.8µH, along with a larger output capacitance or larger-package output capacitor (for better V-bias per-

SEMTECH

Applications Information (continued)

formance), will ensure correct mode–switching behavior.

For very low V_{IN} (0.7V to 0.8V) such as is obtained with a nearly-depleted single-cell alkaline battery), a smaller value of inductance will help to ensure that PWM mode will switch to PSAVE mode as the load decreases. This consideration may be of little importance in most applications, as there is little energy remaining in such a deeply discharged battery.

The following table lists the manufacturers of recommended inductor options. The specification values shown are simplified approximations or averages of many device parameters under various test conditions. See manufacturers' documentation for full performance data.

Manufacturer/ Part #	Value (µH)	DCR (Ω)	Rated Current (mA)	Tolerance (%)	Dimensions LxWxH (mm)
Murata LQM31PN4R7M00	4.7	0.3	700	20	3.2 x 1.6 x 0.95
Coilcraft XFL2006-472	4.7	0.7	500	20	2 x 2 x 0.6

Capacitor Selection

Input and output capacitors must be chosen carefully to ensure that they are of the correct value and rating. The output capacitor requires a minimum capacitance value of 10µF at the programmed output voltage to ensure stability over the full operating range, and to ensure positive mode-switching hysteresis. The DC bias must be included in capacitor derating to ensure the required effective capacitance is provided, especially when considering small package-size capacitors. For example, a 10µF 0805 capacitor may provide sufficient capacitance at low output voltages but may be too low at higher output voltages. Therefore, a higher capacitance value may be required to provide the minimum of 10µF at these higher output voltages. Additional output capacitance may be required for V_{IN} close to V_{OUT} to reduce ripple in PSAVE mode, to increase the PSAVE exit threshold for high V_{IN}, and to ensure stability in PWM mode, especially at higher output load currents.

Low ESR capacitors such as X5R or X7R type ceramic capacitors are recommended for input bypassing and output filtering. Low-ESR tantalum capacitors are not recommended due to possible reduction in capacitance seen

at the switching frequency of the SC120. Ceramic capacitors of type Y5V are not recommended as their temperature coefficients and large capacitance tolerance make them unsuitable for this application. The following table lists recommended capacitors. For smaller values and smaller packages, it may be necessary to use multiple devices in parallel, especially for C_{OUT}.

| Manufacturer/ Part Number	Value (µF)	Rated Voltage (VDC)	Type	Case Size	Case Height (mm)
Murata GRM21BR60J226ME39B	22	6.3	X5R	0805	1.25
Murata GRM31CR71A226KE15L	22	10	X7R	1206	1.6
Murata GRM185R60G475ME15	4.7	4	X5R	0603	0.5
TDK C2012X5R1A226M	22	10	X5R	0805	0.85
Taiyo Yuden JMK212BJ226MG-T	22	20	X5R	0805	1.25

PCB Layout Considerations

Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following simple design rules can be implemented to ensure good layout:

- Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
- Route the output voltage feedback path away from the inductor and LX node to minimize noise and magnetic interference.
- Maximize ground metal on the component side to improve the return connection and thermal dissipation. Separation between the LX node and GND should be maintained to avoid coupling capacitance between the LX node and the ground plane.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

A layout drawing for the MLP package is shown in Figure 4 and a layout drawing for the SOT23 package is shown in Figure 5.

Applications Information (continued)
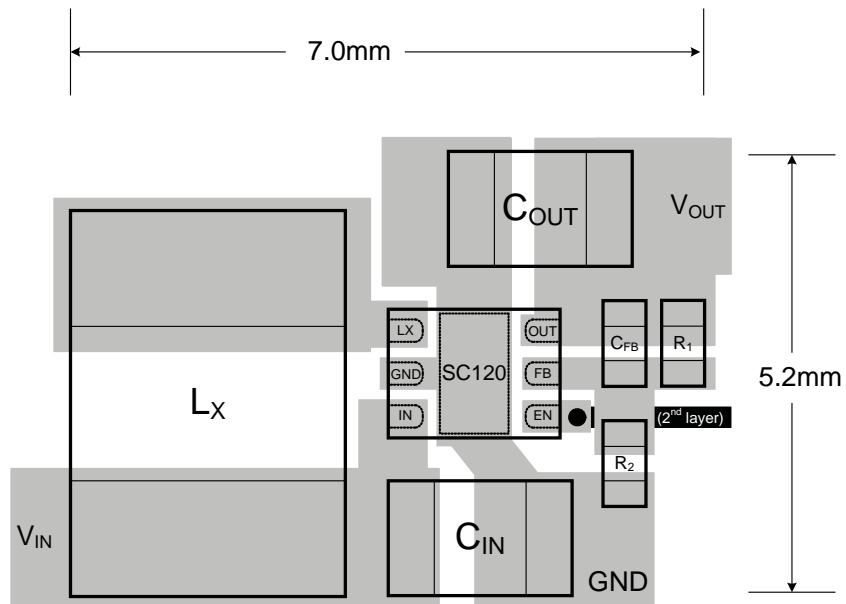
Figure 4 — Layout Drawing for MLP package
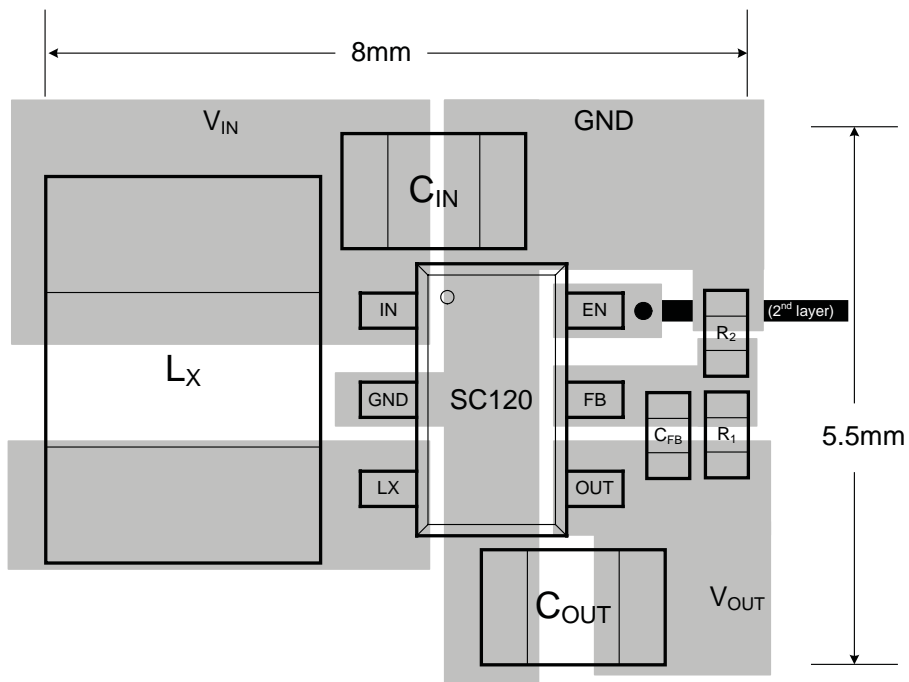
Figure 5 — Layout Drawing for SOT23-6 package

Outline Drawing — MLPD-UT-6 1.5x2
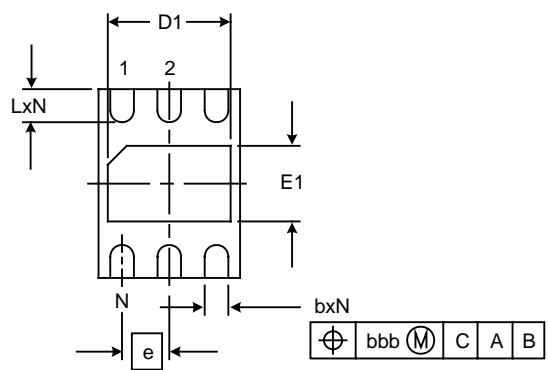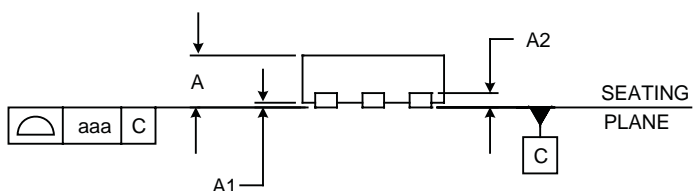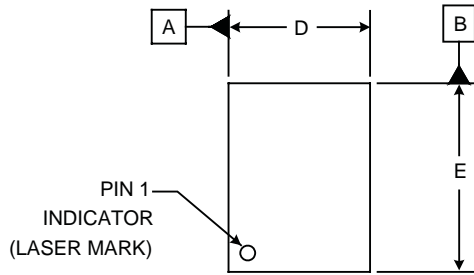
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2	(.006)			(.152)		
b	.007	.010	.012	0.18	0.25	0.30
D	.055	.059	.063	1.40	1.50	1.60
D1	.035	-	.055	0.90	-	1.40
E	.075	.079	.083	1.90	2.00	2.10
E1	.026	.031	.035	0.65	0.80	0.90
e	.020 BSC			0.50 BSC		
L	.012	.014	.016	0.30	0.35	0.40
N	6			6		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern — MLPD-UT-6 1.5x2
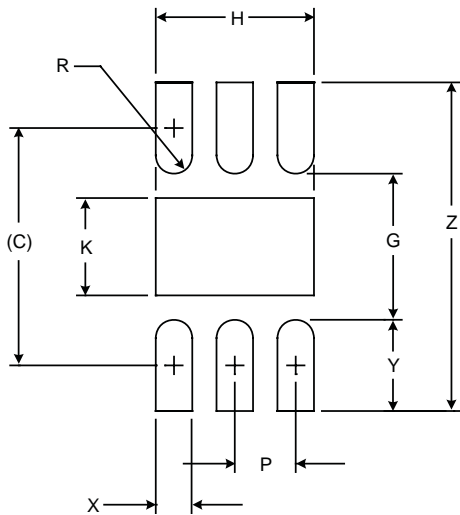
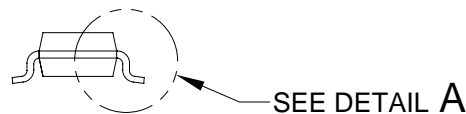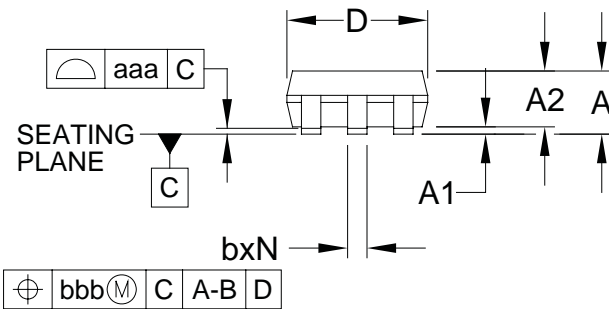| DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.077)	(1.95)
G	.047	1.20
H	.051	1.30
K	.031	0.80
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.030	0.75
Z	.106	2.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
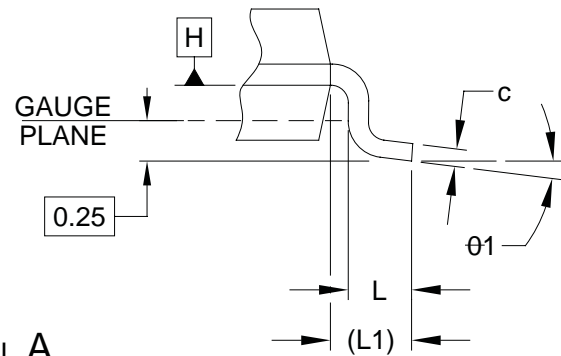   FUNCTIONAL PERFORMANCE OF THE DEVICE.

SEMTECH

Outline Drawing — SOT23-6
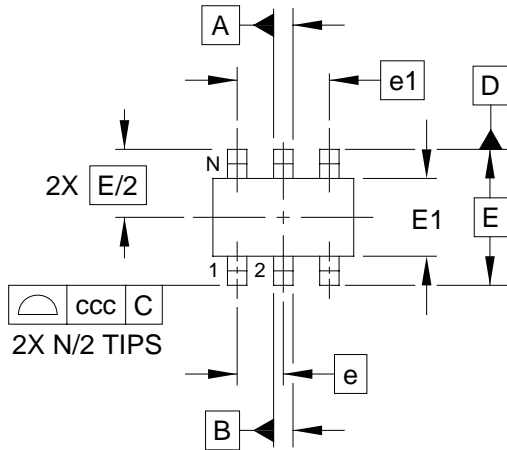
DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	-	1.45
A1	0.00	-	0.15
A2	0.90	1.15	1.30
b	0.25	-	0.50
c	0.08	-	0.22
D	2.80	2.90	3.10
E1	1.50	1.60	1.75
E	2.80 BSC		
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
L1	(0.60)		
N	6		
θ1	0°	-	10°
aaa	0.10		
bbb	0.20		
ccc	0.20		

SIDE VIEW

SEE DETAIL A

DETAIL A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

SEMTECH

Land Pattern — SOT23-6
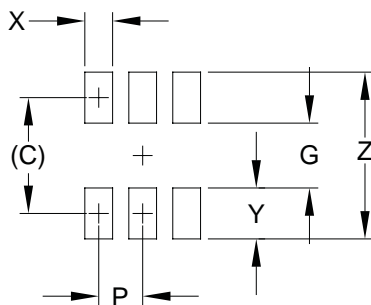
DIMENSIONS	
DIM	MILLIMETERS
C	(2.50)
G	1.40
P	0.95
X	0.60
Y	1.10
Z	3.60

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

SEMTECH

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111   Fax: (805) 498-3804

www.semtech.com

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А