EMC2106

Dual RPM-Based Linear Fan Controller with Hardware Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC2106 is an SMBus compliant fan controller with up to five (up to 4 external and 1 internal) temperature channels. The fan drivers can be operated using two methods each with two modes. The methods include an RPM based Fan Speed Control Algorithm and a direct drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors.

The EMC2106 also includes a hardware programmable temperature limits and dedicated system shutdown output for thermal protection of critical circuitry.

Applications

- Notebook Computers
- Embedded Applications
- Projectors
- Industrial and Networking Equipment

Features

- Two Programmable Fan Control circuits
  - 4-wire fan compatible
  - High speed PWM (26khz)
  - Low speed PWM (9.5Hz - 2240Hz)
  - 600mA, 5V, High Side Fan Driver
  - Optional detection of aging fans
  - 1mA Linear DAC Fan Driver
- RPM based fan control algorithm
  - 2% accuracy from 500RPM to 16k RPM
- Temperature Look-Up Table
  - Allows programmed fan response to temperature
  - 1 to 4 thermal zones to control each fan driver
  - Controls fan speed or drive setting
  - Allows externally generated temperature data to control fan drivers including two DTS channels
- Up to Four External Temperature Channels
  - Designed to support 45nm, 60nm, and 90nm CPUs
  - Automatically detects and supports CPUs requiring the BJT or Transistor models
  - Resistance error correction
  - 1°C accurate (60°C to 100°C)
  - 0.125°C resolution
  - Detects fan aging and variation
- Three dedicated comparator outputs for External Diode 1, External Diode 2, and External Diode 3 (OVERT1#, OVERT2#, OVERT3#)
- Up to three thermistor compatible voltage inputs
- Hardware Programmable Thermal Shutdown Temperature
  - Cannot be altered by software
  - 60°C to 122°C Range or 92°C to 154°C Range
- Programmable High and Low Limits for all channels
- 3.3V Supply Voltage
- SMBus 2.0 Compliant
  - 2 selectable SMBus addresses
  - SMBus Alert compatible
  - Option to load register set from external EEPROM
- Available in 28-pin QFN package - Lead Free RoHS compliant (5mm x 5mm)

ORDER NUMBER:

ORDERING NUMBER	PACKAGE	FEATURES
EMC2106-DZK	28 pin QFN Lead-Free RoHS compliant	Two independent fan drivers (one High Side, one Linear), up to 4 external diode measurement channels, one Critical / Thermal Shutdown input

REEL SIZE IS 4,000 PIECES

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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Chapter 1 Block Diagram

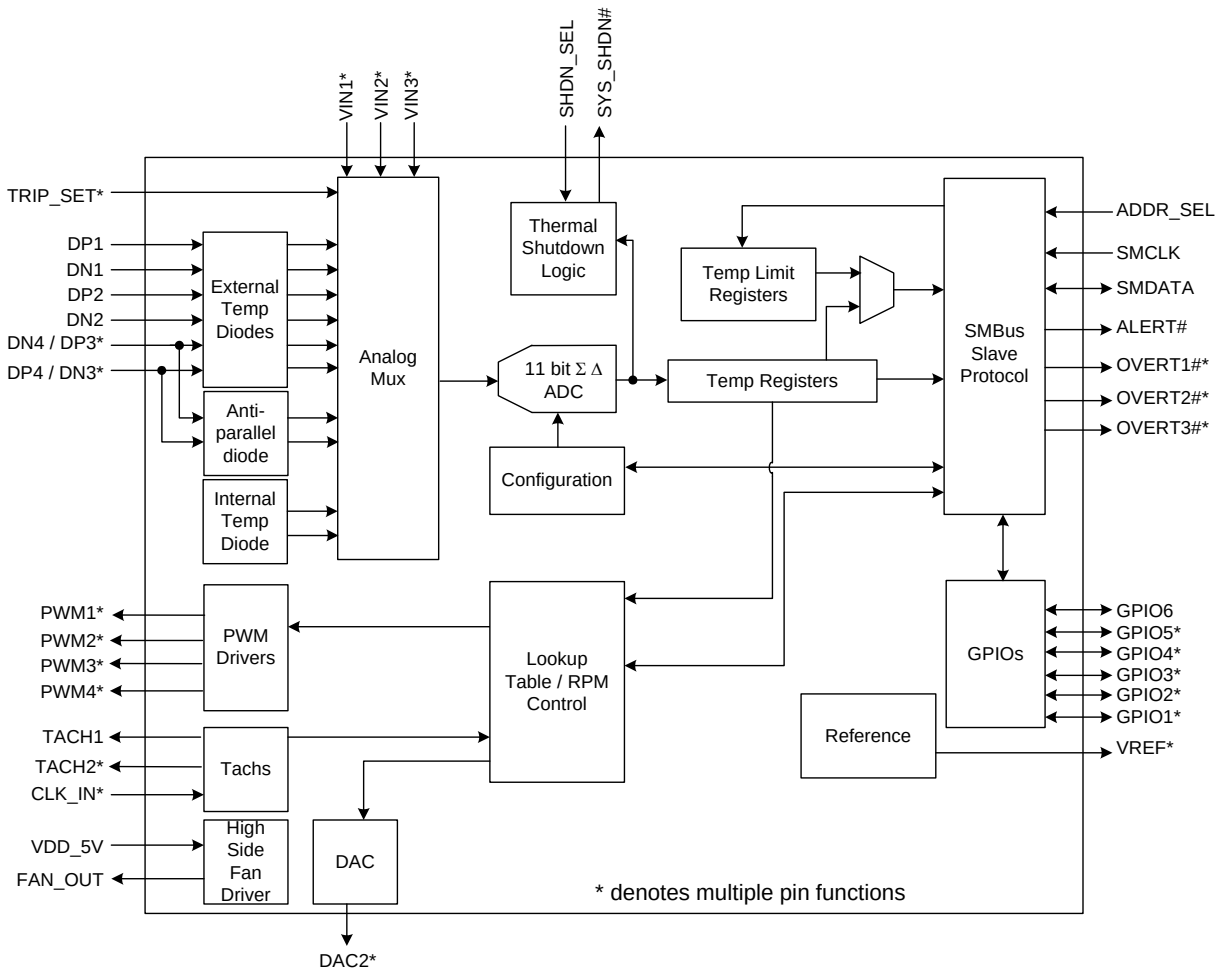


Figure 1.1 EMC2106 Block Diagram

Chapter 2 Pin Description

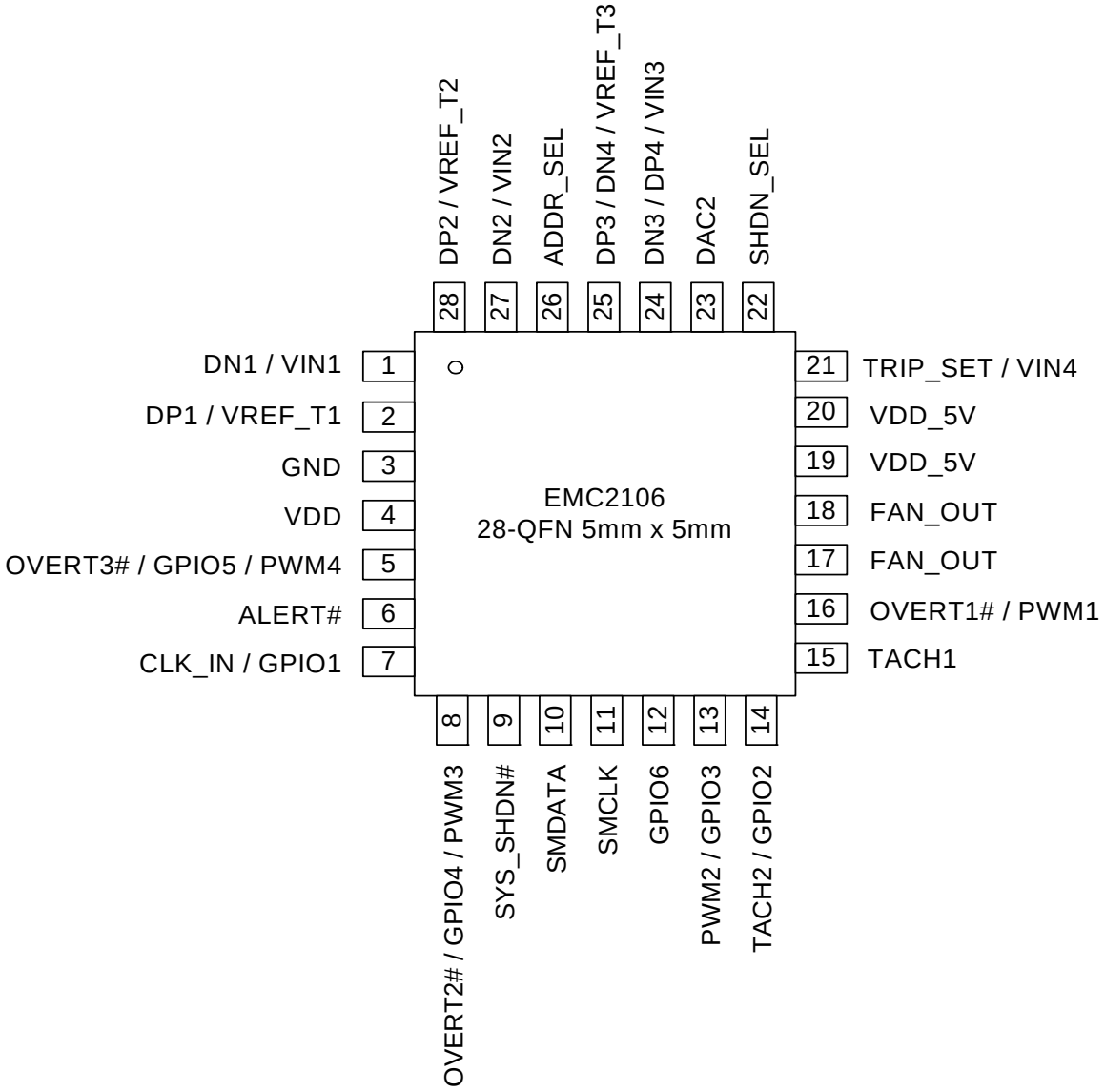


Figure 2.1 EMC2106 Pin Diagram (28 Pin QFN)

Table 2.1 Pin Description for EMC2106

PIN NUMBER EMC2106	PIN NAME	PIN FUNCTION	PIN TYPE
1	DN1 / VIN1	DN1 - Negative (cathode) analog input for External Diode 1 (default)	AIO (2V)
		VIN1 - General Voltage input to be used with a thermistor	AI (2V)
2	DP1 / VREF_T1	DP1 - Positive (anode) analog input for External Diode 1 (default)	AIO (2V)
		VREF_T1 - Reference output for use with a thermistor and to drive VIN1	AO (2V)
3	GND	Ground Connection	Power
4	VDD	Power Supply	Power
5	OVERT3#/ GPIO5/ PWM4	OVERT3# - Active low interrupt for the External Diode 3 channel (default)	OD (5V)
		GPI5 - General Purpose Input	DI (5V)
		GPO5 - General Purpose push/ pull Output	DO
		GPO5 - General Purpose open drain Output.	OD (5V)
		PWM4 - Open Drain PWM driver	OD (5V)
		PWM4 - Push-Pull PWM driver	DO
6	ALERT#	Active low interrupt - requires external pull-up resistor.	OD (5V)
7	CLK_IN / GPIO1	CLK_IN - 32.768KHz clock input.	DI (5V)
		GPI1 - General Purpose Input (default)	DI (5V)
		GPO1 - General Purpose push/ pull Output	DO
		GPO1 - General Purpose open drain Output.	OD (5V)
8	OVERT2# / GPIO4 / PWM3	OVERT2# - Active low Interrupt for the External Diode 2 channel (default)	OD (5V)
		GPI4 - General Purpose Input	DI (5V)
		GPO4 - General Purpose push/ pull Output	DO
		GPO4 - General Purpose open drain Output.	OD (5V)
		PWM3 - Open Drain PWM driver	OD (5V)
		PWM3 - Push-Pull PWM driver	DO

Table 2.1 Pin Description for EMC2106 (continued)

PIN NUMBER EMC2106	PIN NAME	PIN FUNCTION	PIN TYPE
9	SYS_SHDN#	Active low Critical System Shutdown output	OD (5V)
10	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
11	SMCLK	SMBus clock input - requires external pull-up resistor	DIOD (5V)
12	GPIO6	GPI6 - General Purpose Input (default)	DI (5V)
		GPO6 - General Purpose push/ pull Output	OD (5V)
		GPO6 - General Purpose open drain Output.)	DO
13	PWM2 / GPIO3	PWM2 - Open Drain PWM drive output for Fan 2 (default)	OD (5V)
		PWM2 - Push-Pull PWM drive output for Fan 2	DO
		GPI3 - General Purpose Input	DI (5V)
		GPO3 - General Purpose push-pull Output	DO
		GPO3 - General Purpose open drain Output	OD (5V)
14	TACH2 / GPIO2	TACH2 - Tachometer input for Fan 2 (default)	DI (5V)
		GPI2 - General Purpose Input	DI (5V)
		GPO2 - General Purpose push-pull Output	DO
		GPO2 - General Purpose open drain Output	OD (5V)
15	TACH1	Tachometer input for Fan 1	DI (5V)
16	OVERT1# / PWM1	OVERT1# - Active low interrupt for the External Diode 1 channel (default)	OD (5V)
		PWM1 - Open Drain PWM drive output for Fan 1	OD (5V)
		PWM1 - Push-Pull PWM drive output for Fan 1	DO
17	FAN_OUT	High Side Fan Driver Output	Power
18	FAN_OUT	High Side Fan Driver Output	Power
19	VDD_5V	Supply for High Side Fan Driver	Power
20	VDD_5V	Supply for High Side Fan Driver	Power

Table 2.1 Pin Description for EMC2106 (continued)

PIN NUMBER EMC2106	PIN NAME	PIN FUNCTION	PIN TYPE
21	TRIP_SET / VIN4	TRIP_SET - Determines HW Shutdown temperature features for the hardware shutdown channel	AI (2V)
		VIN4 - General voltage input when Thermal / Critical shutdown disabled	AI (2V)
22	SHDN_SEL	Determines HW Shutdown temperature features and measurement channel	AIO
23	DAC2	Linear Fan Driver Output	AO (2V)
24	DN3 / DP4 / VIN3	DN3 / DP4 - Negative (cathode) analog input for External Diode 3 and positive (anode) Analog Input for External Diode 4 (default)	AIO (2V)
		VIN3 - General voltage input for use with a thermistor	AI (2V)
25	DP3 / DN4 / VREF	DP3 / DN4 - Positive (anode) analog input for External Diode 3 and negative (cathode) analog input for External Diode 4 (default)	AIO (2V)
		VREF_T3 - Reference output for use with a thermistor and to drive VIN3	AO (2V)
26	ADDR_SEL	Selects SMBus slave address	DIT
27	DN2 / VIN2	DN2 - Negative (cathode) analog input for External Diode 2 (default)	AIO (2V)
		VIN2 - General voltage input for use with a thermistor	AI (2V)
28	DP2 / VREF_T2	DP2 - Positive (anode) analog input for External Diode 2 (default)	AIO (2V)
		VREF_T2 - Reference output for use with a thermistor and to drive VIN2	AO (2V)
Thermal Slug	GND	Ground	Power

The pin type are described in detail below. All pins labelled with (5V) are 5V tolerant.

All pin labelled with (2V) should not be exposed to any voltage level greater than 2V.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AI	Analog Input - this pin is used as an input for analog signals.

Table 2.2 Pin Types (continued)

PIN TYPE	DESCRIPTION
AO	Analog Output - this pin is used as an output for analog signals.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
DO	Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current.
DIOD	Digital Input / Open Drain Output this pin is used as an digital I/O. When it is used as an output, It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 3 Electrical Specifications

Table 3.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins including VDD_5V	-0.3 to 6.5	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on 2V tolerant pins	-0.3 to 2.5	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Package Power Dissipation See Note 3.1	1 up to T_A = 85°C	W
Junction to Ambient (θ_{JA}) See Note 3.2	40	°C/W
Operating Ambient Temperature Range	-40 to 85°C	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 3.1 All voltages are relative to ground.

Note 3.2 The Package Power Dissipation specification assumes a recommended thermal via design consisting of four 12mil vias connected to the ground plane with a 2x2mm thermal landing.

Note 3.3 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 52°C/W including localized PCB temperature increase.

3.1 Electrical Specifications

Table 3.2 Electrical Specifications

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Supply Current (active)	I_{DD}		2	3	mA	4 Conversions / second - Dynamic Averaging Enabled Fan Drivers enabled at max PWM frequency

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Supply Current	I_{DD}		500	750	uA	1 Conversions / second-Dynamic Averaging disabled, Fan Drivers disabled.
Supply Current from VDD_5V	I_{DD_5}		100		uA	Fan Driver enabled, No load current
SMBus Delay	t_{SMB}			15	ms	Delay from power to first SMBus communication
Time to First Round Robin				300	ms	
External Temperature Monitors						
Temperature Accuracy			±0.25	±1	°C	60°C < T_{DIODE} < 110°C 30°C < T_{DIE} < 85°C
			±0.5	±2	°C	0°C < T_{DIODE} < 125°C, 0°C < T_{DIE} < 115°C
Temperature Resolution			0.125		°C	
Diode decoupling capacitor	C_{FILTER}		2200	2700	pF	Connected across external diode, CPU, GPU, or AMD diode
Resistance Error Corrected	R_{SERIES}			100	Ohm	Sum of series resistance in both DP and DN lines
Internal Temperature Monitor						
Temperature Accuracy	T_{DIE}		±1	±2	°C	Note 3.4
Temperature Resolution			0.125		°C	
Voltage Measurement						
Total Unadjusted Error	TUE			1	%	Measured at 3/4 full scale
Reference Voltage	V_{REF}		800		mV	
Reference Accuracy	ΔV_{REF}		1		%	
PWM Fan Driver						
PWM Resolution	PWM		256		Steps	
PWM Duty Cycle	DUTY	0		100	%	
High Side Fan Driver						
Output High Voltage from 5V supply	V_{OH_5V}	VDD_5V - 0.35	VDD_5V - 0.3		V	I_{SOURCE} = 600mA, VDD_5V = 5V
Voltage Accuracy	ΔV_{FAN_OUT}		1	2	%	Measured at 3/4 full scale - Direct Setting Mode

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, VDD_5V = 4.5V to 5.5V, T_A = -40°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Fan Drive Current	I_{SOURCE}			600	mA	
Overcurrent Limit	I_{OVER}			2800	mA	Momentary Current drive at startup for < 2 seconds 1.5V < FAN_OUT < 3.5V
DC Short Circuit Current Limit	I_{SHORT}		700		mA	Sourcing current, Thermal shutdown not triggered, FAN_OUT = 0V
Short circuit delay	t_{DFS}		2		s	
Output Capacitive Load	C_{LOAD}			100	uF	Z_{ESR} < 100mΩ at 10kHz
Linear DAC Fan Driver						
DAC Output High Voltage	V_{DAC2_OH}	V_{DD} - 0.2			V	I_{DAC2} = 1mA current source
DAC Output Low Voltage	V_{DAC2_OL}			0.3	V	I_{DAC2} = -1mA current sink
Output Voltage Accuracy	ΔV_{DAC2}			2	%	Measured at 3/4 full scale - Direct Setting Mode
Fan Drive Current	I_{DAC2}	-1		1	mA	
RPM Based Fan Controller						
Tachometer Range	TACH	480		16000	RPM	
Tachometer Setting Accuracy	Δ_{TACH}		±1	±2	%	External oscillator 32.768kHz
	Δ_{TACH}		±2.5	±5	%	Internal Oscillator 40°C < T_{DIE} < 100°C
Thermal Shutdown						
Thermal Shutdown Threshold	TSD_{TH}		150		°C	
Thermal Shutdown Hysteresis	TSD_{HYST}		50		°C	
Digital I/O pins						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	4 mA current drive
Output Low Voltage	V_{OL}			0.4	V	4 mA current sink
Leakage current	I_{LEAK}			±5	uA	$\overline{ALERT}$ and $\overline{SYS_SHDN}$ pins Powered and unpowered

Note 3.4 T_{DIE} refers to the internal die temperature and may not match T_A due to self heating of the device. The internal temperature sensor will return T_{DIE}.

3.2 SMBus Electrical Specifications (client mode)

Table 3.3 SMBus Electrical Specifications

VDD= 3V to 3.6V, T_A = -40°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	
Output Low Voltage	V_{OL}			0.4	V	4 mA current sink
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered and unpowered
Input Capacitance	C_{IN}		5		pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

3.3 EEPROM Loader Electrical Specifications

Table 3.4 EEPROM Loader Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Interface						
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Hysteresis			420		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current		4			mA	V_{OL} = 0.4V
Timing						
Loading Delay	t_{DLY}		10		ms	Delay after power-up until EEPROM loading begins. (See Section 4.9.)
Loading Time	t_{LOAD}		50		ms	
Clock Frequency	f_{SMB}		50		kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 Communications

4.1 System Management Bus Interface Protocol

The EMC2106 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2106 will not stretch the clock signal.

The EMC2106 powers up as an SMBus client (after loading from EEPROM as applicable).

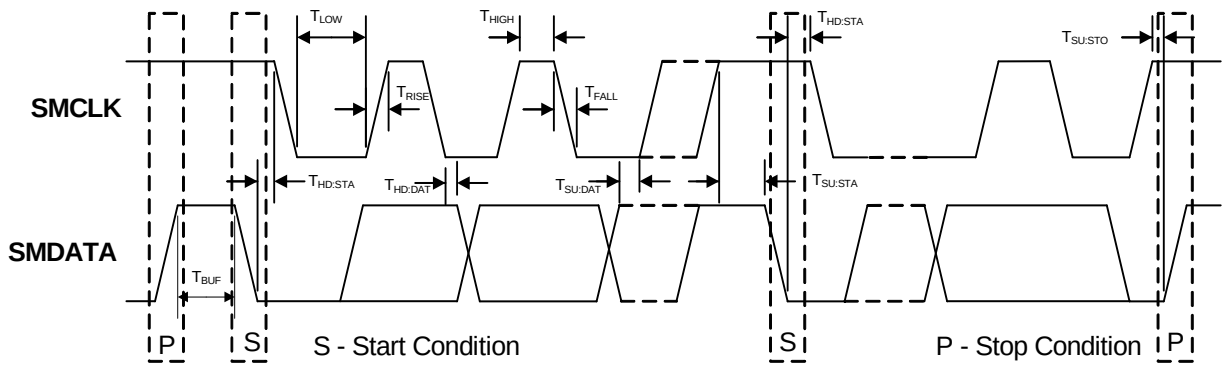


Figure 4.1 SMBus Timing Diagram

The EMC2106 contains a single SMBus interface. The SMBus address is determined by the ADDR_SEL pin (see Section 4.7)The EMC2106 client interfaces are SMBus 2.0 compatible and support Send Byte, Read Byte, Receive Byte and the Alert Response Address as valid protocols. These protocols are used as shown below.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
0 -> 1	0101_111	0	0	XXh	0	XXh	0	1 -> 0

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
0 -> 1	0101_111	0	0	XXh	0	0 -> 1	0101_111	1	0	XXh	1	1 -> 0

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
0 -> 1	0101_111	0	0	XXh	0	1 -> 0

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
0 -> 1	0101_111	1	0	XXh	1	1 -> 0

4.6 Alert Response Address

The ALERT# output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the ALERT# pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 4.6.

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
0 -> 1	0001_100	1	0	0101_111	1	1 -> 0

The EMC2106 will respond to the ARA in the following way if the ALERT# pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the ALERT# pin.
3. The ARA will NOT affect the OVERT1#, OVERT2#, and OVERT3# pins. These pins will be asserted as long as the error condition is present. When the error condition is removed, the pins will be cleared.

4.7 SMBus Address

The EMC2106 SMBus Address is determined by the status of the ADDR_SEL pin as shown in Table 4.7.

Table 4.7 ADDR_SEL Pin Decode

ADDR_SEL	SMBUS ADDRESS	FUNCTION
‘0’ (GND)	0101_111xb	SMBus Client
‘Z’ (open)	0101_111xb	EEPROM Programming
‘1’ (VDD)	0101_110xb	SMBus Client

Attempting to communicate with the EMC2106 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.8 SMBus Time-out

The EMC2106 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface. The SMBus Timeout defaults to enabled and can be disabled by setting the DIS_TO bit in the Configuration 2 register.

4.9 Programming from EEPROM

When configured to load from EEPROM (see Section 4.7), the EMC2106 acts as a simple SMBus Master to read data from a connected EEPROM using the following procedure.

1. After power-up the EMC2106 waits for 10ms with the SMDATA and SMCLK pins tri-stated.
2. Once the wait period has elapsed, the EMC2106 sends a START signal followed by the 7 bit client address 1010 _000xb followed by a ‘0b’ and waits for an ACK signal from the EEPROM.
3. When the EEPROM sends the ACK signal, the EMC2106 will send a second start signal and continue sending the Block Read Command (see Table 4.8) to the same slave address. It reads 256 data bytes from the EEPROM sending an ACK between each data byte. When 256 data bytes have been received, it sends a NACK signal followed by a STOP bit.
4. Resets the device as an SMBus Client with slave address 0101_111xb.

If the EMC2106 does not receive an acknowledge bit from the EEPROM then the following will occur:

1. The ALERT# pin will be asserted and will remain asserted until a Host device initiates communication with the EMC2106 and reads the Status Register. The ALERT# pin will be de-asserted after a single Status Register read.
2. The EMC2106 will reset its SMBus protocol as a slave interface and start operating from the default conditions with slave address 0101_111xb.

Table 4.8 Block Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	SLAVE ADDRESS	RD	ACK	Register Data (00h)	. . .
0-> 1	0101_111	0	0	00h	0	0 -> 1	0101_111	1	0	XXh	
ACK	**Register Data (01h)**	**ACK**	**Register Data (02h)**	**ACK**	**Register Data (03h)**	**. . .**	**ACK**	**Register Data (FFh)**		**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	. . .	0	XXh		1	1 -> 0

Note: The shaded columns represent data sent from the EMC2106 to the EEPROM device.

APPLICATION NOTE: It is recommended that the EEPROM that is used be an AT24C02B or equivalent device. The EEPROM slave address must be 1010_000xb. The device must support a block-read command, 8-bit addressing, and 8-bit data formatting using a 2-wire bus. The device must support 3.3V digital switching logic and may not pull the SMCLK and SMDATA pins above 5V. Data must be transmitted MSB first.

APPLICATION NOTE: No other SMBus Master should exist on the SMDATA and SMCLK lines. The presence of another SMBus Master will cause errors in reading from the EEPROM.

The EEPROM should be loaded to mirror the register set of the EMC2106 with the desired configuration set. All undefined registers in the EMC2106 register set should be loaded with 00h in the EEPROM. Likewise, all registers that are read-only in the EMC2106 register set should be loaded with 00h in the EEPROM.

Because of the interaction between the Fan Control Look-up Tables and the Fan Configuration Register, the EEPROM Loader stores the contents of the Fan Configuration Registers and updates these registers at the end of the EEPROM loading cycle.

Chapter 5 Product Description

The EMC2106 is an SMBus compliant fan controller with up to four (up to 4 external) temperature channels. It contains two fan drivers, a High Side fan driver capable of sourcing 600mA from a 5V supply and a linear DAC fan driver. In addition, the EMC2106 contains up to four (4) PWM outputs (two of which can be used with the RPM based Fan Speed Control Algorithm). The fan drivers can be operated using two methods each with two modes. The methods include an RPM based Fan Speed Control Algorithm and a direct fan drive setting. The modes include manually programming the desired settings or using the internal programmable temperature look-up table to select the desired setting based on measured temperature.

The temperature monitors offer 1°C accuracy (for external diodes) with sophisticated features to reduce errors introduced by series resistance and beta variation of substrate thermal diode transistors commonly found in processors (including support for BJT or transistor model for CPU diodes).

The EMC2106 also includes a hardware programmable temperature limit and dedicated system shutdown output for thermal protection of critical circuitry. Any of the three temperature channels can be configured to measure a thermistor or voltage channel using a precision reference voltage for reduced system complexity.

Figure 5.1 shows a system diagram of the EMC2106.

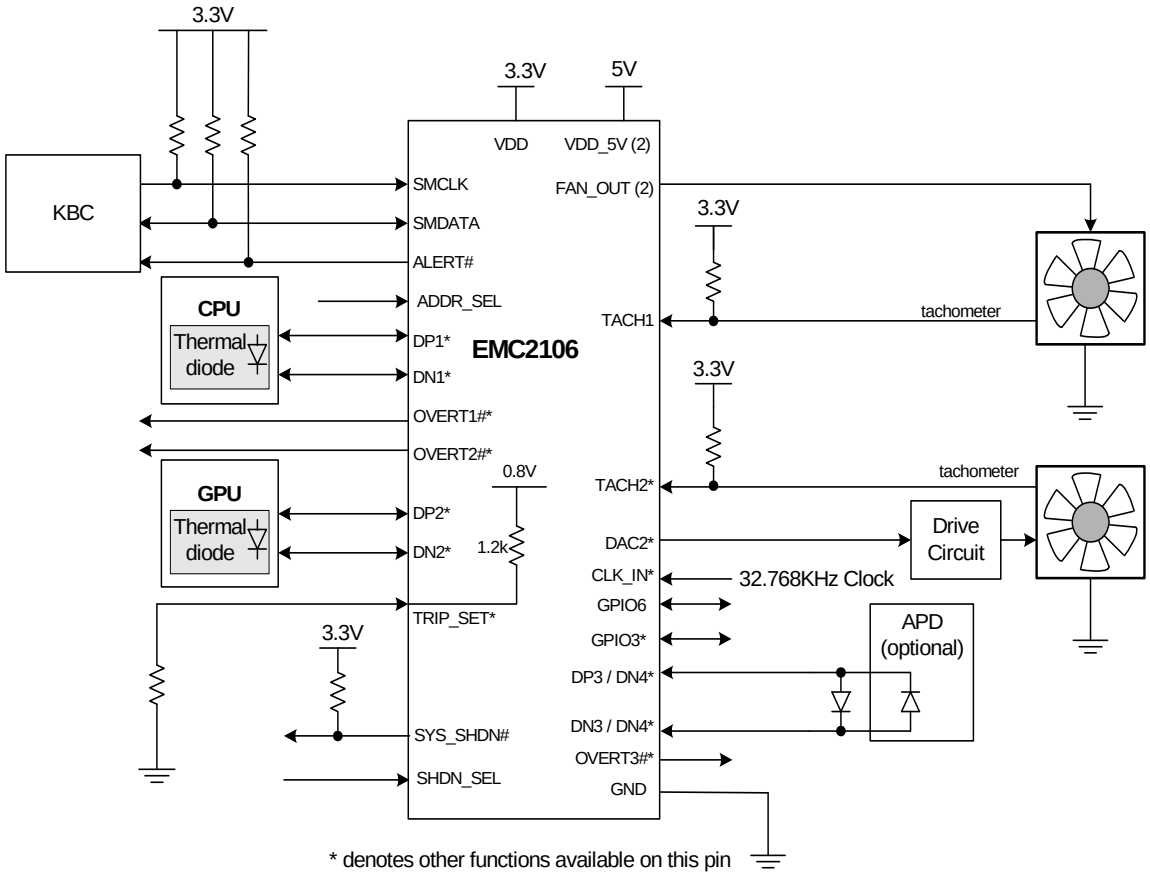


Figure 5.1 System Diagram of EMC2106

5.1 Critical/Thermal Shutdown

The EMC2106 provides a hardware Critical/Thermal Shutdown function for systems. Figure 5.2 is a block diagram of this Critical/Thermal Shutdown function. The Critical/Thermal Shutdown function in the EMC2106 accepts configuration information from the fixed states of the SHDN_SEL pin as described in Section 5.1.1.

Each of the software programmed temperature limits can be optionally configured to act as inputs to the Critical / Thermal Shutdown independent of the hardware shutdown operation. When configured to operate this way, the SYS_SHDN# pin will be asserted when the temperature meets or exceeds the limit. The pin will be released when the temperature drops below the limit however the individual status bits will not be cleared if set (see Section 6.13).

The analog portion of the Critical/Thermal Shutdown function monitors the hardware determined temperature channel (see Section 5.1.1). This measured temperature is then compared with TRIP_SET point. This TRIP_SET point is set by the system designer with a single external resistor divider as described in Section 5.1.2.

The SYS_SHDN# is asserted when the indicated temperature exceeds the temperature threshold established by the TRIP_SET input pin for a number of consecutive measurements defined by the fault queue. If the HW_SHDN output is asserted and the temperature drops below the Thermal / Critical Shutdown threshold then it will be set to a logic ‘0’ state.

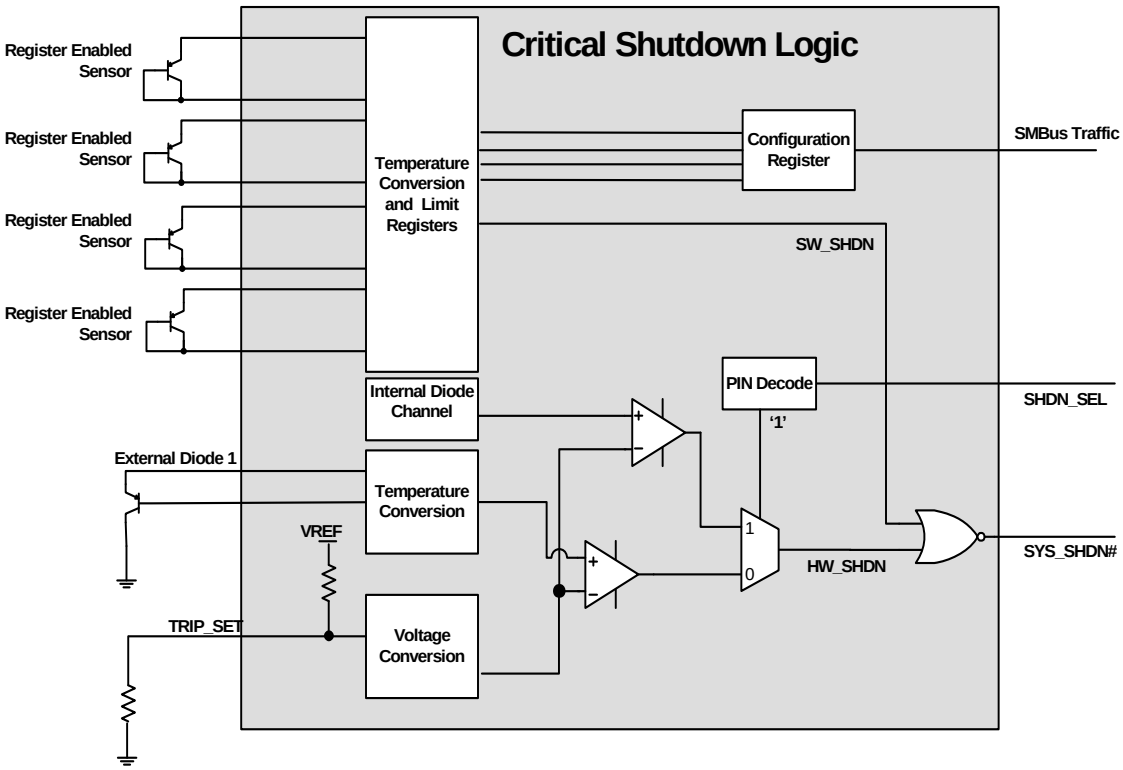


Figure 5.2 EMC2106 Critical/Thermal Shutdown Block Diagram

5.1.1 SHDN_SEL Pin

The EMC2106 has a 'strappable' input (SHDN_SEL) allowing for configuration of the hardware Critical/Thermal Shutdown input channels. This pin has 3 possible states and is monitored and decoded by the EMC2106 at power-up. The three possible states are 0 (tied to GND), 1 (tied to 3.3V) or High-Z (open). The state of this pin determines which external diode configuration is used for the Critical / Thermal shutdown function.

The different configurations of the SHDN_SEL pin are described in Table 5.1. SHDN_SEL applies only to the selected temperature channel.

Table 5.1 SHDN_SEL Pin Configuration

SHDN_SEL	FUNCTION NAME	TEMPERATURE MONITORING FEATURES	CRITICAL / THERMAL SHUTDOWN RANGE
0	Intel Transistor Mode (substrate PNP)	The external diode 1 channel is configured with Beta Compensation enabled and Resistance Error Correction enabled. This mode is ideal for monitoring a substrate transistor such as an Intel CPU thermal diode.	High - 92°C to 154°C
High-Z (open)	AMD CPU / Diode Mode	The external diode 1 channel is configured with Beta Compensation disabled and Resistance Error Correction disabled. This mode is ideal for monitoring an AMD processor diode or a 2N3904 diode.	Low - 60°C to 122°C
1	Internal	The internal diode is linked to the Hardware set Thermal / Critical shutdown circuitry and the SYS_SHDN# pin.	Low - 60°C to 122°C

5.1.2 TRIP_SET / VIN4 Pin

The EMC2106's TRIP_SET / VIN4 pin is an analog input to the Critical/Thermal Shutdown block which sets the Thermal Shutdown temperature. The system designer creates a voltage level at the input through a simple resistor connected to GND as shown in Figure 5.1. The value of this resistor is used to create an input voltage on the TRIP_SET / VIN4 pin which is translated into a temperature ranging from 60°C to 122°C or 90°C to 152°C as enumerated in Table 5.2.

When the SHDN_SEL pin is pulled to '1' at power up, then the TRIP_SET / VIN4 pin is configured to measure VIN4 as its primary function. The circuitry will still calculate the thermal / critical shutdown threshold based on the voltage and compare this temperature against the Internal Diode temperature. This will cause the SYS_SHDN# pin to assert if the measured temperature exceeds this threshold. The device will also compare the measured voltage against the VIN4 High and Low limits. This function is not available if SHDN_SEL is set to '0' or 'High-Z' at power up.

APPLICATION NOTE: If the SHDN_SEL pin is pulled to '1' at power up and the TRIP_SET / VIN4 pin is intended for use as a voltage input then the SYS_SHDN# pin should be ignored.

APPLICATION NOTE: If the SHDN_SEL pin is pulled to '1' at power up and the TRIP_SET / VIN4 pin is intended to be used to set a threshold level then the VIN4 channel should be masked. Furthermore, the voltage on the pin must be externally generated based on Equation [1]. Do not use Table 5.2.

APPLICATION NOTE: When used in its TRIP_SET mode (i.e. the SHDN_SEL pin is not set to a logic '1'), current only flows when the TRIP_SET / VIN4 pin is being monitored. At all other times, the internal reference voltage is removed and the TRIP_SET / VIN4 pin will be pulled down to ground.

APPLICATION NOTE: The TRIP_SET / VIN4 pin circuitry is designed to use a 1% resistor externally. Using a 1% resistor will result in the Thermal / Critical Shutdown temperature being decoded correctly. If a 5% resistor is used, then the Thermal / Critical Shutdown temperature may be decoded with as much as ±1°C error.

$$V_{TRIP} = \frac{T_{TRIP} - T_{MIN}}{80} \quad [1]$$

V_{TRIP} is the TRIP_SET voltage

T_{MIN} is the minimum temperature based on the range

Table 5.2 TRIP_SET Resistor Setting

T_{TRIP} (°C) LOW RANGE	T_{TRIP} (°C) HIGH RANGE	RSET (1%)	T_{TRIP} (°C) LOW RANGE	T_{TRIP} (°C) HIGH RANGE	RSET (1%)
60	92	0.0	92	124	1240
61	93	28.7	93	125	1330
62	94	48.7	94	126	1400
63	95	69.8	95	127	1500
64	96	90.9	96	128	1580
65	97	113	97	129	1690
66	98	137	98	130	1820
67	99	158	99	131	1960
68	100	182	100	132	2050
69	101	210	101	133	2210
70	102	237	102	134	2370
71	103	261	103	135	2550
72	104	294	104	136	2740
73	105	324	105	137	2940
74	106	348	106	138	3160
75	107	383	107	139	3480
76	108	412	108	140	3740
77	109	453	109	141	4120
78	110	487	110	142	4530
79	111	523	111	143	4990
80	112	562	112	144	5490
81	113	604	113	145	6040
82	114	649	114	146	6810

Table 5.2 TRIP_SET Resistor Setting (continued)

T_{TRIP} (°C) LOW RANGE	T_{TRIP} (°C) HIGH RANGE	RSET (1%)	T_{TRIP} (°C) LOW RANGE	T_{TRIP} (°C) HIGH RANGE	RSET (1%)
83	115	698	115	147	7870
84	116	750	116	148	9090
85	117	787	117	149	10700
86	118	845	118	150	12700
87	119	909	119	151	15800
88	120	953	120	152	20500
89	121	1020	121	153	29400
90	122	1100	122	154	49900
91	123	1150	60	92	Open

5.2 Fan Control Modes of Operation

The EMC2106 has four modes of operation for each fan driver. Each mode of operation uses the Ramp Rate control and Spin Up Routine.

1. Direct Setting Mode- in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 6.23) will instantly update the fan drive. Ramp Rate control is optional and enabled via the EN_RRC bits.
   - This is the default mode. The Direct Setting Mode is enabled by clearing the LUT_LOCK bit in the Look Up Table Configuration Register (see Section 6.35) while the TACH / DRIVE bit is set to ‘0’.
   - Whenever the Direct Setting Mode is enabled the current drive will be changed to what was last written into the Fan Driver Setting Register.
2. Fan Speed Control Mode (FSC) - in this mode of operation, the user determines a target tachometer count and the drive setting is automatically updated to achieve this target speed. The algorithm uses the Spin Up Routine and has user definable ramp rate controls.
   - This mode is enabled by clearing the LUT_LOCK bit in the Look Up Table (LUT) Configuration Register and setting the EN_ALGO bit in the Fan Configuration Register.
3. Using the Look Up Table with Fan Drive Settings (Direct Setting w/ LUT Mode) - In this mode of operation, the user programs the Look Up Table with fan drive settings and corresponding temperature thresholds. The fan drive is set based on the measured temperatures and the corresponding drive settings. Ramp Rate control is optional and enabled via the EN_RRC bits.
   - This mode is enabled by programming the Look Up Table then setting the LUT_LOCK bit while the TACH / DRIVE bit is set to ‘1’.
   - The TACH / DRIVE bit in the Look Up Table Configuration Register MUST be set to ‘1’ or the fan drive settings will be incorrectly set. Setting this bit to ‘1’ ensures the settings will be PWM settings.
4. Using the Look Up Table with RPM Target Settings (FSC w/ LUT Mode) - In this mode of operation, the user programs the Look Up Table with TACH Target values and corresponding temperature thresholds. The TACH Target will be set based on the measured temperatures and the corresponding target settings. The fan drive settings will be determined automatically based on the RPM based Fan Speed Control Algorithm.
   - This mode is enabled by programming the Look Up Table then setting the LUT_LOCK bit while the TACH / DRIVE bit is set to ‘0’.

- The TACH / DRIVE bit in the Look Up Table Configuration Register MUST be set to ‘0’ or the TACH Target values will be incorrectly set. Setting this bit to ‘0’ ensures that the settings will be RPM settings (Tachometer counts).

APPLICATION NOTE: It is important that the TACH Target settings are in the proper format when using the RPM based Fan Speed Control Algorithm.

Table 5.3 Fan Controls Active for Operating Mode

DIRECT SETTING MODE	FSC MODE	DIRECT SETTING W/ LUT MODE	FSC W/ LUT MODE
Fan Driver Setting (read / write)	Fan Driver Setting (read only)	Fan Driver Setting (read only)	Fan Driver Setting (read only)
EDGES[1:0]	EDGES[1:0] (Fan Configuration)	EDGES[1:0]	EDGES[1:0]
-	RANGE[1:0] (Fan Configuration)	-	RANGE[1:0] (Fan Configuration)
UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)
LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)
SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)
Fan Step	Fan Step	Fan Step	Fan Step
-	Fan Minimum Drive		Fan Minimum Drive
Valid TACH Count	Valid TACH Count	Valid TACH Count	Valid TACH Count
-	TACH Target (read / write)	-	TACH Target (read only)
TACH Reading	TACH Reading	TACH Reading	TACH Reading
-	-	Look Up Table Drive / Temperature Settings (read only)	Look up Table Drive / Temperature Settings (read only)
-	DRIVE_FAIL_CNT[1:0] and Drive Band Fail Registers	-	DRIVE_FAIL_CNT[1:0] and Drive Band Fail Registers

5.3 High Side Fan Driver

The EMC2106’s contains a 5V, 600mA, linear high side fan driver to directly drive a 5V fan. By fully integrating the linear fan driver, the typical requirement for the discrete pass device and other external linearization circuitry is completely eliminated. The linear fan driver is driven by an 8-bit DAC providing better than 20mV resolution between steps.

5.3.1 Over Current Limit

The High Side Fan Driver contains circuitry to allow for significant over current levels to accommodate transient conditions on the FAN pins. The over current limit is dependent upon the output voltage with the limit dropping as the voltage nears 0V.

If the fan driver current detects a short-circuit condition for longer than 2 seconds, then the I_SHORT status bit is set and an interrupt generated. Additionally, the High Side Fan Driver will be disabled for 8 seconds. After this 8 second time has elapsed, it will be allowed to restart invoking the Spin Up Routine before returning to its previous drive setting.

APPLICATION NOTE: If the FSC Algorithm is active, then it will generate errant SPIN_FAIL interrupts during the 8 second time that the fan driver is held off.

5.4 Linear DAC Fan Driver

The EMC2106 contains an internal linear DAC for use as a fan driver. This DAC output voltage has 8-bit resolution from 0V to 3.3V. The linear DAC fan driver is also capable of sourcing and sinking up to 1 mA of current.

The Linear DAC Fan Driver is biased from the VDD_5V supply and this voltage must be present for the DAC driver to operate properly.

5.5 PWM Fan Driver

The EMC2106 supports up to four (4) PWM output drivers. Each output driver can be configured to operate as an open-drain (default) or push-pull driver and each driver can be configured with normal or inverse polarity. Additionally, the PWM frequencies for PWM1, PWM2, and the two optional PWM drivers PWM3 and PWM4 are independently programmable with ranges from 9.5Hz to 26kHz in four programmable frequency bands.

5.6 Fan Control Look-Up Table

The EMC2106 uses a look-up table to apply a user-programmable fan control profile based on measured temperature to each fan driver. In this look-up table, each temperature channel is allowed to control the fan drive output independently (or jointly) by programming up to eight pairs of temperature and drive setting entries.

The user programs the look-up table based on the desired operation. If the RPM based Fan Speed Control Algorithm is to be used (see Section 5.7), then the user must program an RPM target for each temperature setting of interest. Alternately, if the RPM based Fan Speed Control Algorithm is not to be used, then the user must program a drive setting for each temperature setting of interest.

If the measured temperature on the External Diode channel meets or exceeds any of the temperature thresholds for any of the temperature columns (see Appendix B), the fan output will be automatically set to the desired setting corresponding to the exceeded temperature. In cases where multiple temperature channel thresholds are exceeded, the highest fan drive setting will take precedence.

When the measured temperature drops to a point below a lower threshold minus the hysteresis value, the fan output will be set to the corresponding lower set point.

Figure 5.3 shows an example of this operation using temperature - drive setting pairs for a single channel.

See Appendix B for examples of the Look Up Table operation.

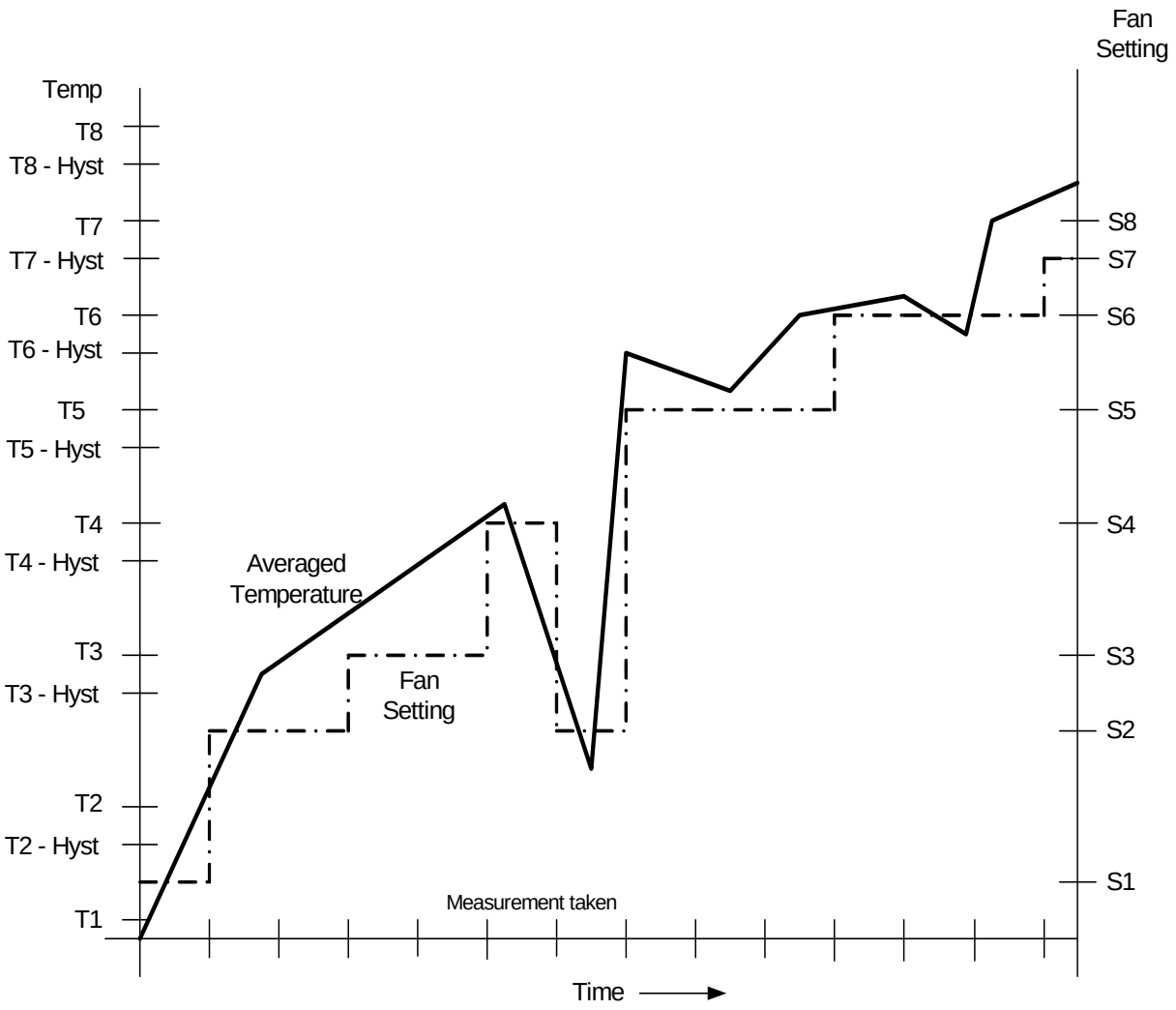


Figure 5.3 Fan Control Look-Up Table Example

5.6.1 Programming the Look Up Table

When the Look Up Table is used, it must be loaded and configured correctly based on the system requirements. The following steps outline the procedure.

1. Determine whether the Look Up Table will drive a fan setting or a tachometer target value and set the TACH / DRIVE bit in the Fan LUT Configuration Register.
2. Determine which measurement channels (up to four) are to be used with the Look Up Table and set the TEMP3_CFG and TEMP4_CFG bits accordingly in the Fan LUT Configuration Register.
3. For each step to be used in the LUT, set the Fan Setting (either fan setting or TACH Target as set by the TACH / DRIVE bit). If a setting is not used, then set it to FFh (if a fan setting) or 00h (if a TACH Target). Load the lowest settings first in ascending order (i.e. Fan Setting 1 is the lowest setting greater than “off”. Fan Setting 2 is the next highest setting, etc.).
4. For each step to be used in the LUT, set each of the measurement channel thresholds. These values must be set in the same data format that the data is presented. If DTS is to be used, then

the format should be in temperature with a maximum threshold of 100°C (64h). If a measurement channel is not used, then set the threshold at FFh.

5. Set the Hysteresis value to be smaller than the smallest threshold step.
6. Configure the RPM based Fan Speed Control Algorithm if it is to be used.
7. Set the LUT_LOCK bit to enable the Look Up Table and begin fan control.

5.6.2 DTS Support

The EMC2106 supports DTS (Intel's Digital Temperature Sensor) data in the Fan Control Look Up Table. Intel's DTS data is a positive number that represents the processor's relative temperature below a fixed value called $T_{CONTROL}$ which is generally equal to 100°C for Intel Mobile processors. For example, a DTS value of 10°C means that the actual processor temperature is 10°C below $T_{CONTROL}$ or equal to 90°C.

Either or both of the Pushed Temperature Registers can be written with DTS data and used to control the respective fan driver. When DTS data is entered, then the USE_DTS_Fx bit must be set in the Fan LUT Configuration register. Once this bit is set, the DTS data entered is automatically subtracted from a value of 100°C. This delta value is then used in the Look Up Table as standard temperature data. See Appendix B for examples on using DTS data in the Look Up Table.

APPLICATION NOTE: The device is designed with the assumption that $T_{CONTROL}$ is 100°C. As such, all DTS related conversions are done based on this value including Look Up Table comparisons. If $T_{CONTROL}$ is adjusted (i.e. $T_{CONTROL}$ is shifted to 105°C), then all of the Look Up Table thresholds should be adjusted by a value equal to $T_{CONTROL}$ - 100°C.

5.7 RPM based Fan Speed Control Algorithm (FSC)

The EMC2106 includes two RPM based Fan Speed Control Algorithms. Each algorithm operates independently and controls a separate fan driver. Each algorithm can be controlled manually (by setting the target fan speed) or via a look up table.

This fan control algorithm uses Proportional, Integral, and Derivative terms to automatically approach and maintain the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source. Figure 5.4 shows a simple flow diagram of the RPM based Fan Speed Control Algorithm operation.

The desired tachometer count is set by the user inputting the desired number of 32.768KHz cycles that occur per fan revolution. This is done by either manually setting the TACH Target Register or by programming the Temperature Look-Up Table. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000 RPMs, then the user would input the hexidecimal equivalent of 1296 (51h in the TACH Target Register). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs.

The EMC2106's RPM based Fan Speed Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the ALERT# pin. The EMC2106 works with fans that operate up to 16,000 RPMs and provide a valid tachometer signal. The fan controller will function either with an externally supplied 32.768KHz clock source or with it's own internal 32kHz oscillator depending on the required accuracy.

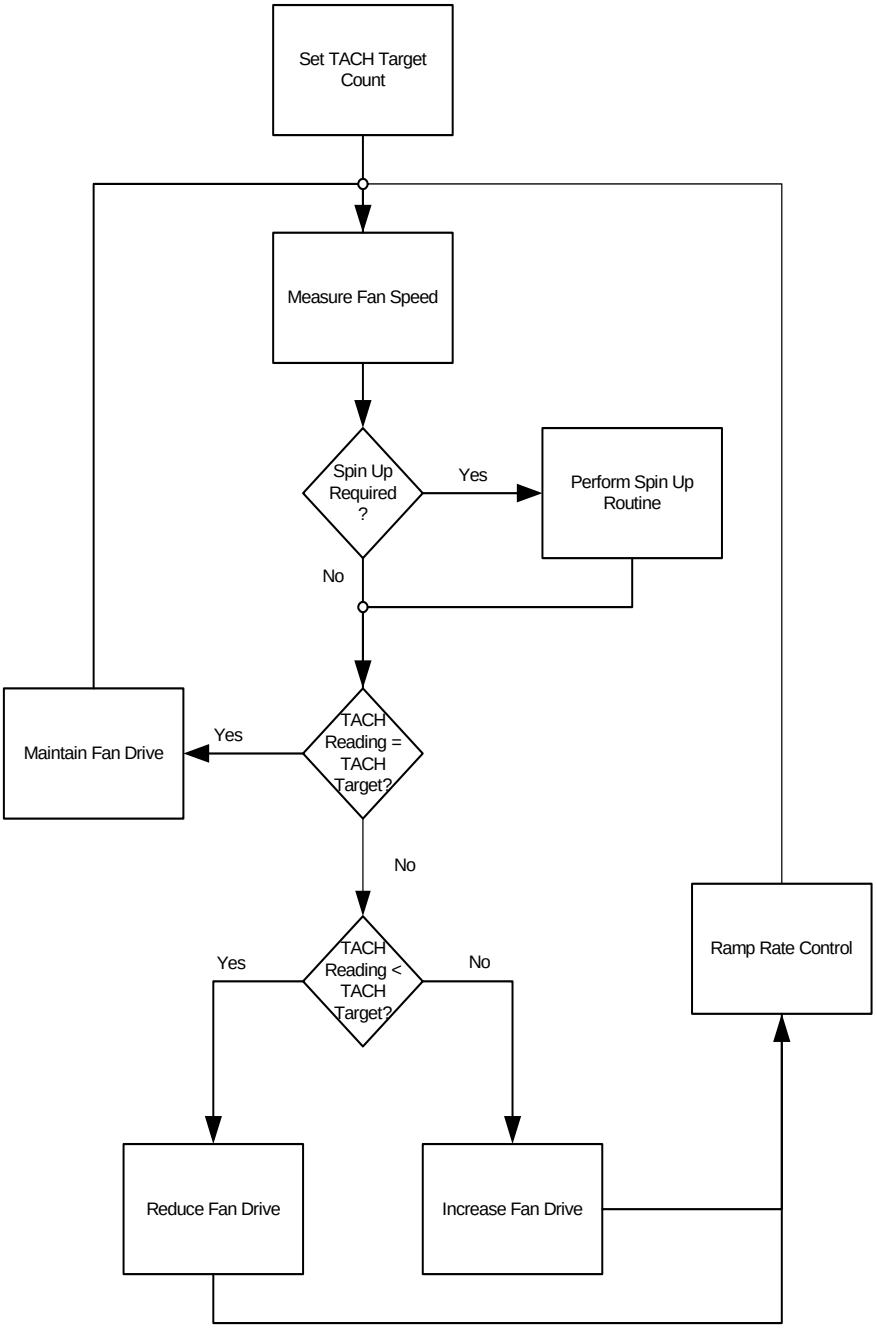


Figure 5.4 RPM based Fan Speed Control Algorithm

5.7.1 Programming the RPM Based Fan Speed Control Algorithm

The RPM based Fan Speed Control Algorithm is disabled upon device power up. The following registers control the algorithm. The EMC2106 fan control registers are pre-loaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

Note that steps 1 - 6 are optional and need only be performed if the default settings do not provide the desired fan response.

1. Set the Spin Up Configuration Register to the Spin Up Level and Spin Time desired.
2. Set the Fan Step Register to the desired step size.
3. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
4. Set the Update Time, and Edges options in the Fan Configuration Register.
5. Set the Valid TACH Count Register to the highest tach count that indicates the fan is spinning.
6. Set the TACH Target Register to the desired tachometer count.
7. Enable the RPM based Fan Speed Control Algorithm by setting the EN_ALGO bit.

5.8 Tachometer Measurement

The tachometer measurement circuitry is used in conjunction with the RPM based Fan Speed Control Algorithm to update the fan driver output. Additionally, it can be used in Direct Setting mode as a diagnostic for host based fan control.

This method monitors the TACHx signal in real time. It constantly updates the tachometer measurement by reporting the number of clocks between a user programmed number of edges on the TACHx signal (see Table 6.33).

The tachometer measurement provides fast response times for the RPM based Fan Speed Control Algorithm and the data is presented as a count value that represents the fan RPM period. When this method is used, all fan target values must be input as a count value for proper operation.

APPLICATION NOTE: The tachometer measurement method works independently of the drive settings. If the device is put into Direct Setting and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the tachometer measurement may signal a Stalled Fan condition and assert an interrupt.

5.8.1 Stalled Fan

A Stalled fan is detected if the tach counter exceeds the user-programmable Valid TACH Count setting then it will flag the fan as stalled and trigger an interrupt.

If the RPM based Fan Speed Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid tachometer level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- Whenever the Direct Setting Mode or Direct Setting with LUT Mode is enabled or whenever the Spin Up Routine is enabled, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time (see Table 6.43) to allow the fan an opportunity to reach a valid speed without generating unnecessary interrupts.
- In Direct Setting Mode or Direct Setting w/ LUT Mode, and the tachometer measurement is using the Tach Period Measurement method, then whenever the TACH Reading Register value exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.

- When using the RPM based Fan Speed Control Algorithm (either FSC Mode or LUT with FSC Mode), the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

5.8.2 32kHz Clock Source

The EMC2106 allows the user to choose between supplying an external 32.768kHz clock or use of the internal 32kHz oscillator to measure the tachometer signal. This clock source is used by the RPM based Fan Speed Control Algorithm to calculate the current fan speed. This fan controller accuracy is directly proportional to the accuracy of the clock source.

The external clock is provided on the CLK_IN. In order for the external clock to be used, the EXT_CLK bit must be set in the Configuration Register.

5.8.3 Aging Fan or Invalid Drive Detection

This is useful to detect aging fan conditions (where the fan's natural maximum speed degrades over time) or incorrect fan speed settings.The EMC2106 contains circuitry that detects that the programmed fan speed can be reached by the fan. If the target fan speed cannot be reached within a user defined band of tach counts at maximum drive then the DRIVE_FAIL status bits are set and the ALERT# pin is asserted.

5.9 Spin Up Routine

The EMC2106 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation.

The Spin Up Routine is initiated in Direct Setting mode (with or without the Look Up Table - when enabled) when the setting value changes from 00h to anything else.

When the Fan Speed Control Algorithm is enabled, the Spin Up Routine is initiated under the following conditions when the Tach Period Measurement method of tach measurement is used:

1. The TACH Target Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Section 6.31).
2. The RPM based Fan Speed Control Algorithm's measured TACH Reading Register value is greater than the Valid TACH Count setting.

When the Spin Up Routine is operating, the fan driver is set to full scale (optional) for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set a a user defined level (30% through 65% drive).

After the Spin Up Routine has finished, the EMC2106 measures the TACHx signal. If the measured TACH Reading Register value is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

Figure 5.5 shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

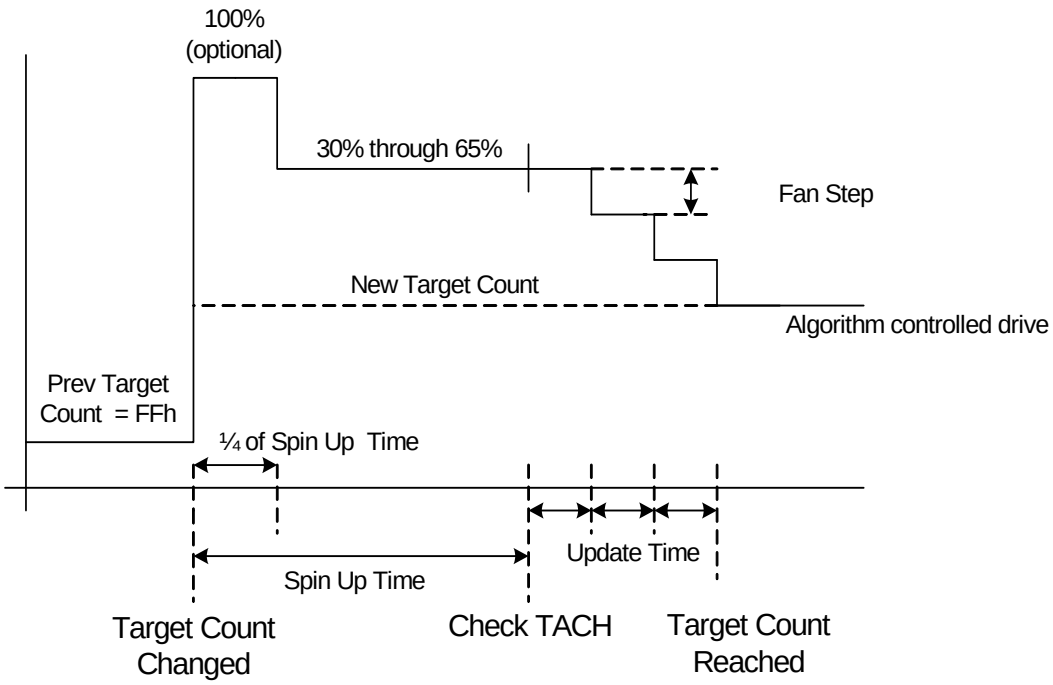


Figure 5.5 Spin Up Routine

5.10 Ramp Rate Control

The Fan Driver can be configured with automatic ramp rate control. Ramp rate control is accomplished by adjusting the drive output settings based on the Maximum Fan Step Register settings and the Update Time settings.

If the RPM based Fan Speed Control Algorithm is used, then this ramp rate control is automatically used. The user programs a maximum step size for the fan drive setting and an update time. The update time varies from 100ms to 1.6s while the fan drive maximum step can vary from 1 count to 31 counts.

When a new fan drive setting is entered, the delta from the next fan drive setting and the previous fan drive setting is determined. If this delta is greater than the Max Step settings, then the fan drive setting is incrementally adjusted every 100ms to 1.6s as determined by the Update Time until the target fan drive setting is reached. See Figure 5.6.

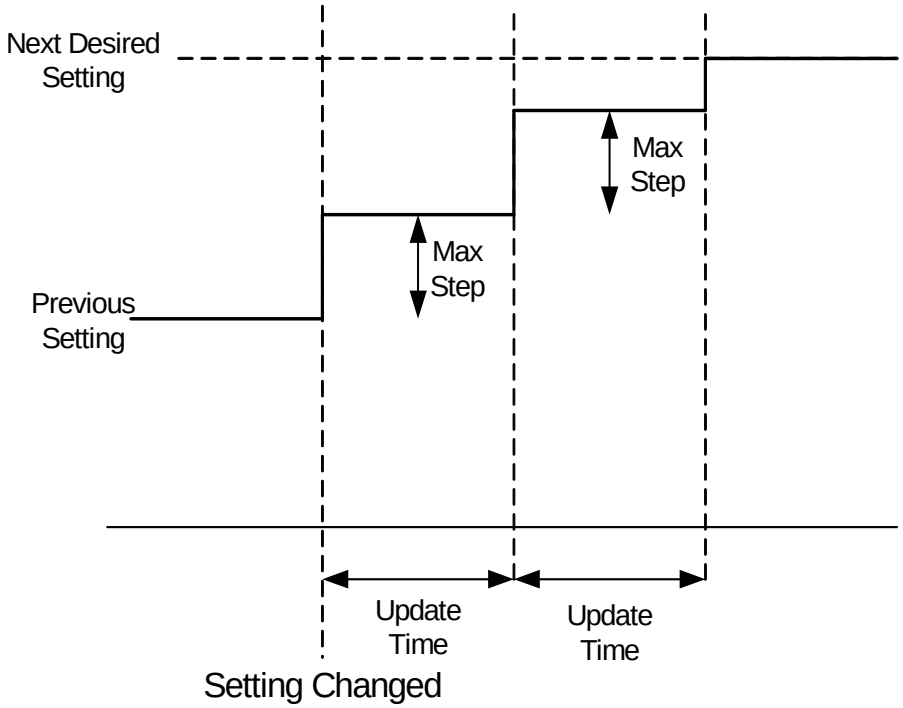


Figure 5.6 Ramp Rate Control

5.11 Watchdog Timer

The EMC2106 contains two internal Watchdog Timers. Once the device has powered up the watchdog timer monitors the SMBus traffic for signs of activity. The Watchdog Timer starts when the internal supply has reached its operating point. The Watchdog Timer only starts immediately after power-up and once it has been triggered or deactivated will not restart.

Each fan driver has an independent watchdog timer. Disabling the watchdog associated with Fan 1 will not disable the watchdog associated with Fan 2.

If four (4) seconds elapse without the system host programming the device, then the watchdog will be triggered and the following will occur:

1. The WATCH status bit will be set.
2. The fan driver will be set to full scale drive. It will remain at full scale drive until one of the three conditions listed below are met.

If the Watchdog Timer is triggered, the following three operations will disable the timer and return the device to normal operation. Alternately, if the Watchdog Timer has not yet been triggered performing any one of the following will disable it.

1. Writing the Fan Setting Register will disable the Watchdog Timer.
2. Enabling the RPM based Fan Speed Control Algorithm by setting the EN_ALGO bit will disable the Watchdog Timer. The fan driver will be set based on the RPM based Fan Speed Control Algorithm.
3. Setting the LUT_LOCK bit will disable the Watchdog Timer. The fan driver will be set based on the Look Up Table settings.

Writing any other configuration registers will not disable the Watchdog Timer.

APPLICATION NOTE: Disabling the Watchdog will not automatically set the fan drive. This must be done manually (or via the Look Up Table).

5.12 Internal Thermal Shutdown (TSD)

The EMC2106 contains an internal thermal shutdown circuit that monitors the internal die temperature. If the die temperature exceeds the Thermal Shutdown Threshold (see Table 3.2), then the following will occur:

1. The High Side Fan Driver is disabled. It will remain disabled until the internal temperature drops below the threshold temperature minus 50°C.
2. The TSD Status bit will be set and the SYS_SHDN# pin asserted.
3. The SYS_SHDN# pin is asserted.

APPLICATION NOTE: When the fan driver is disabled via a thermal shutdown event, the drive settings will not be altered. Thus, when the temperature drops below the threshold minus the hysteresis, the fan will return to its previous drive setting.

5.13 Fault Queue

The EMC2106 contains a programmable fault queue on all fault conditions except a FAN_SHORT or TSD condition (including all temperature high, low, and tcrit limits as well as the hardware set thermal limit). The fault queue defines how many consecutive out-of-limit conditions must be reported before the corresponding status bit is set (and the ALERT# pin asserted).

APPLICATION NOTE: With the exception of the Tcrit limit, the fault queue is not applied to the internal diode measurement.

5.14 Temperature Monitoring

The EMC2106 can monitor the temperature of up to four (4) externally connected diodes as well as the internal or ambient temperature. Each channel is configured with the following features enabled or disabled based on user settings and system requirements.

APPLICATION NOTE: When measuring an Intel 45nm CPU, the reported temperature will have an error of approximately 1.5°C at 100°C. This error is related to a non-perfect ideality factor of the CPU diode and is proportional to the diode temperature.

5.14.1 Dynamic Averaging

The EMC2106 supports dynamic averaging. When enabled, this feature changes the conversion time for all channels based on the selected conversion rate. This essentially increases the averaging factor as shown in Table 5.4. The benefits of Dynamic Averaging are improved noise rejection due to the longer integration time as well as less random variation on the temperature measurement.

Table 5.4 Dynamic Averaging Behavior

CONVERSION RATE	AVERAGING FACTOR (RELATIVE TO 11-BIT CONVERSI0N)	
	DYNAMIC AVERAGING ENABLED	DYNAMIC AVERAGING DISABLED
1 / sec	8x	1x
2 / sec	4x	1x

Table 5.4 Dynamic Averaging Behavior (continued)

CONVERSION RATE	AVERAGING FACTOR (RELATIVE TO 11-BIT CONVERSI0N)	
	DYNAMIC AVERAGING ENABLED	DYNAMIC AVERAGING DISABLED
4 / sec	2x	1x
8 / sec	1x	1x

5.14.2 Resistance Error Correction

The EMC2106 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of parasitic resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC2106 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

5.14.3 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. This correction is done by implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC2106 corrects for this beta variation to eliminate any error which would normally be induced. It automatically detects the appropriate beta setting to use.

5.14.4 Digital Averaging

The External Diode 1 channel support a 4x digital averaging filter. Every cycle, this filter updates the temperature data based an a running average of the last 4 measured temperature values. The digital averaging reduces temperature flickering and increases temperature measurement stability.

The digital averaging can be disabled by setting the DIS_AVG bit in the Configuration 2 Register (see Section 6.10).

5.15 Thermistor Support

The External Diode 1, External Diode 2, and External Diode 3 channels can be configured to monitor a thermistor. When this function is enabled, the data on the VIN1, VIN2, or VIN3 channels can be configured to measure a simple voltage input or a ground-connected thermistor circuit (see Appendix A for more information).

The External Diode 1 channel can only be configured as a voltage input if the SHDN_SEL pin is set to a logic ‘1’.

5.16 Diode Connections

The diode connection for the External Diode 1 channel is determined at power-up based on the SHDN_SEL pin (see Section 5.1.1). This channel can support a diode-connected transistor (such as a 2N3904) or a substrate transistor (such as those found in an CPU or GPU) as shown in Figure 5.7.

The External Diode 3 channel supports any diode connection shown or it can be configured to operate in anti-parallel diode (APD) mode. When configured in APD mode, a fourth temperature channel is available that shares the DP3 and DN3 pins. When in this mode, both the external diode 3 channel and external diode 4 channel thermal diodes must be connected as a diode.

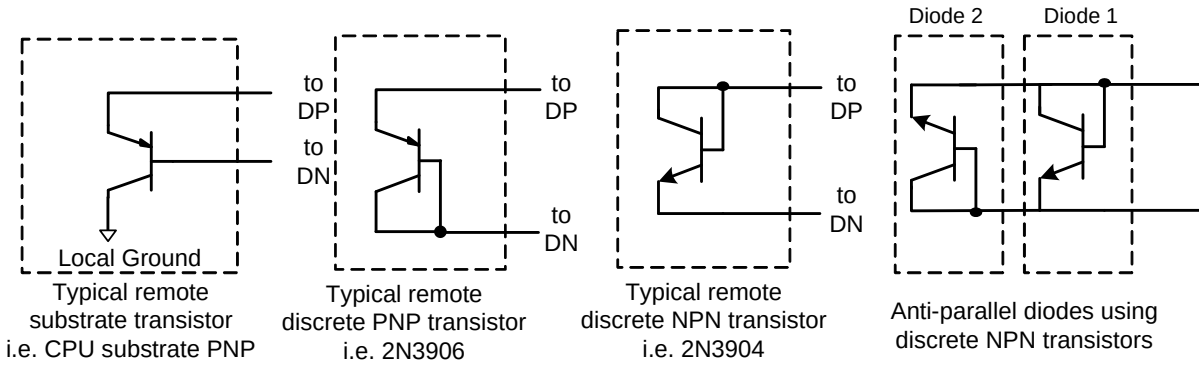


Figure 5.7 Diode Connections

5.16.1 Diode Faults

The EMC2106 actively detects an open and short condition on each measurement channel. When a diode fault is detected, the temperature data MSByte is forced to a value of 80h and the FAULT bit is set in the Status Register. When the External Diode 3 channel is configured to operate in APD mode, the circuitry will detect independent open fault conditions, however a short condition will be shared between the External Diode 3 and External Diode 4 channels.

5.17 GPIOs

The EMC2106 contains up to six (6) GPIO pins (all except GPIO6 are multiplexed with other functions). The GPIO pins can be individually configured as an input or an output and as a push-pull or open-drain output. Additionally, each GPIO pin, when configured as an input, can be individually enabled to trigger an interrupt when they change states.

5.18 Interrupts

If a change of state occurs (such as a temperature out-of-limit condition or a GPIO changing states) then the following will occur:

1. The appropriate status bits will be set in the Status Register and in the High, Low, and Fault Status Registers.
2. The ALERT# will be asserted if the specific channel interrupt is enabled (see Section 6.15).

The ALERT# pin is cleared by setting the MASK bit, disabling the specific interrupt channel enable, or reading the status registers. If the error conditions persist, then the status bits will remain set. Unless the Interrupt Status Enable bits are cleared or the MASK bit is set, the ALERT# pin will likewise be set.

5.19 Over Limit Outputs

The EMC2106 contains three dedicated output pins, OVERT1#, OVERT2#, and OVERT3#. Each of these pins is dedicated to reporting interrupts associated with the External Diode 1 channel, the External Diode 2 channel, and the External Diode 3 channel respectively. These interrupts work in addition to the general interrupt ALERT#.

The OVERT1#, OVERT2#, or OVERT3# pin will be asserted depending on which channel reported an error condition. These interrupt pins are not masked though they can be individually disabled by the user.

The OVERT1#, OVERT2# and/or OVERT3# pins are cleared automatically when the measured temperature drops below the high limit minus 4°C or exceeds the low limit plus 4°C.

Chapter 6 Register Set

6.1 Register Map

The following registers are accessible through the SMBus Interface. All register bits marked as '-' will always read '0'. A write to these bits will have no effect.

Table 6.1 EMC2106 Register Set

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
Temperature Registers						
00h	R	Internal Temp Reading High Byte	Stores the integer data of the Internal Diode	00h	No	Page 54
01h	R	Internal Temp Reading Low Byte	Stores the fractional data of the Internal Diode	00h	No	Page 54
02h	R	External Diode 1 Temp Reading High Byte	Stores the integer data of External Diode 1 and VIN1 channel	00h	No	Page 54
03h	R	External Diode 1 Temp Reading Low Byte	Stores the fractional data of External Diode 1	00h	No	Page 54
04h	R	External Diode 2 Temp Reading High Byte	Stores the integer data of External Diode 2 and VIN2 channel	00h	No	Page 54
05h	R	External Diode 2 Temp Reading Low Byte	Stores the fractional data of External Diode 2	00h	No	Page 54
06h	R	External Diode 3 Temp Reading High Byte	Stores the integer data of External Diode 3 and VIN3 channel	00h	No	Page 54
07h	R	External Diode 3 Temp Reading Low Byte	Stores the fractional data of External Diode 3	00h	No	Page 54
08h	R	External Diode 4 Temp Reading High Byte	Stores the integer data of External Diode 4	00h	No	Page 54
09h	R	External Diode 4 Temp Reading Low Byte	Stores the fractional data of External Diode 4	00h	No	Page 54
0Ah	R	Critical/Thermal Shutdown Temperature	Stores the calculated Critical/Thermal Shutdown temperature high limit derived from the voltage on TRIP_SET / VIN4	7Fh (+127°C)	No	Page 55
0Ch	R/W	Pushed Temperature 1	Stores the integer data for Pushed Temperature 1 to drive LUT 1	00h	No	Page 56

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
0Dh	R/W	Pushed Temperature 2	Stores the integer data for Pushed Temperature 2 to drive LUT 1	00h	No	Page 56
0Eh	R/W	Pushed Temperature 3	Stores the integer data for Pushed Temperature 3 to drive LUT2	00h	No	Page 56
0Fh	R/W	Pushed Temperature 4	Stores the integer data for Pushed Temperature 4 to drive LUT2	00h	No	Page 56
10h	R	Trip Set Voltage	Stores the raw measured TRIP_SET voltage or the VIN4 analog voltage input	FFh	No	Page 56
Diode Configuration						
14h	R/W	External Diode 1 Beta Configuration	Configures the beta compensation settings for External Diode 1	10h	SWL	Page 57
15h	R/W	External Diode 2 Beta Configuration	Configures the beta compensation settings for External Diode 2	10h	SWL	Page 57
16h	R/W	External Diode 3 Beta Configuration	Configures the beta compensation settings for External Diode 3	10h	SWL	Page 57
17h	R/W	External Diode REC Configuration	Configures the Resistance Error Correction functionality for all external diodes	07h	SWL	Page 58
19h	R/W	External Diode 1 Tcrit Limit	Stores the Critical temperature limit for the External Diode 1	64h (100°C)	Write Lock	Page 59
1Ah	R/W	External Diode 2 Tcrit Limit	Stores the Critical temperature limit for the External Diode 2	64h (100°C)	Write Lock	Page 59
1Bh	R/W	External Diode 3 Tcrit Limit	Stores the Critical temperature limit for the External Diode 3	64h (100°C)	Write Lock	Page 59
1Ch	R/W	External Diode 4 Tcrit Limit	Stores the Critical temperature limit for the External Diode 4	64h (100°C)	Write Lock	Page 59
1Dh	R/W	Internal Diode Tcrit Limit	Stores the Critical temperature limit for the Internal Diode	64h (100°C)	Write Lock	Page 59
Configuration and control						
1Fh	R-C	Tcrit Limit Status	Stores the status bits for all temperature channel Tcrit limits	00h	No	Page 62
20h	R/W	Configuration	Configures the Thermal / Critical Shutdown masking options and software lock	00h	SWL	Page 59
21h	R/W	Configuration 2	Controls the conversion rate for monitoring of all channels	0Eh	SWL	Page 60
22h	R/W	Configuration 3	Controls the VIN1 - 3 channels	00h	SWL	Page 61
23h	R	Interrupt Status	Stores the status bits for temperature channels	00h	No	Page 62

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
24h	R-C	High Limit Status	Stores the status bits for all temperature channel high limits	00h	No	Page 63
25h	R-C	Low Limit Status	Stores the status bits for all temperature channel low limits	00h	No	Page 63
26h	R-C	Diode Fault	Stores the status bits for all temperature channel diode faults	00h	No	Page 63
27h	R-C	Fan Status	Stores the status bits for the RPM based Fan Speed Control Algorithm	00h	No	Page 64
28h	R/W	Interrupt Enable Register	Controls the masking of interrupts on all temperature channels	00h	No	Page 64
29h	R/W	Fan Interrupt Enable Register	Controls the masking of interrupts on all fan related channels	00h	No	Page 65
2Ah	R/W	PWM Config	Configures all PWM drivers	00h	No	Page 66
2Bh	R/W	PWM Base Frequency	Selects the base frequency for all PWM drivers.	FFh	No	Page 66
2Ch	R/W	PWM 3 Frequency divide	Determines the frequency divide value for PWM driver 3 if enabled	50h (80)	No	Page 67
2Dh	R/W	PWM3 Setting	Stores the setting of the PWM3 output if enabled	00h	No	Page 67
2Eh	R/W	PWM4 Setting	Stores the setting of the PWM4 output if enabled	00h	No	Page 68
2Fh	R/W	PWM4 Frequency Divide	Determines the frequency divide value for PWM driver 3 if enabled	50h (80)	No	Page 67
Temperature Limit Registers						
30h	R/W	External Diode 1 Temp High Limit	High limit for External Diode 1 or VIN1	55h (+85°C)	SWL	Page 68
31h	R/W	External Diode 2 Temp High Limit	High limit for External Diode 2 or VIN2	55h (+85°C)	SWL	Page 68
32h	R/W	External Diode 3 Temp High Limit	High limit for External Diode 3 or VIN3	55h (+85°C)	SWL	Page 68
33h	R/W	External Diode 4 Temp High Limit	High Limit for External Diode 4	55h (85°C)	SWL	Page 68
34h	R/W	Internal Diode High Limit	High Limit for Internal Diode	55h (85°C)	SWL	Page 68
35h	R/W	Voltage 4 High Limit	High Limit for the Voltage 4 channel	FFh (0.8V)	SWL	Page 68
38h	R/W	External Diode 1 Temp Low Limit	Low Limit for External Diode 1 or VIN1	00h (0°C)	SWL	Page 68
39h	R/W	External Diode 2 Temp Low Limit	Low Limit for External Diode 2 or VIN2	00h (0°C)	SWL	Page 68

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
3Ah	R/W	External Diode 3 Temp Low Limit	Low Limit for External Diode 3 or VIN3	00h (0°C)	SWL	Page 68
3Bh	R/W	External Diode 4 Temp Low Limit	Low Limit for External Diode 4	00h (0°C)	SWL	Page 68
3Ch	R/W	Internal Diode Low Limit	Low Limit for Internal Diode	00h (0°C)	SWL	Page 68
3Dh	R/W	Voltage 4 Low Limit	Low limit for Voltage 4 Channel	00h (0V)	SWL	Page 68
Fan 1 Control Registers						
40h	R/W	Fan 1 Setting	Always displays the most recent fan driver input setting for Fan 1. If the RPM based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 69
41h	R/W	PWM 1 Divide	Stores the divide ratio to set the frequency for Fan 1	01h	No	Page 70
42h	R/W	Fan 1 Configuration 1	Sets configuration values for the RPM based Fan Speed Control Algorithm for the Fan 1 driver	2Bh	No	Page 70
43h	R/W	Fan 1 Configuration 2	Sets additional configuration values for the Fan 1 driver	38h	SWL	Page 72
45h	R/W	Gain 1	Holds the gain terms used by the RPM based Fan Speed Control Algorithm for the Fan 1 driver	2Ah	SWL	Page 74
46h	R/W	Fan 1 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 1 driver	19h	SWL	Page 75
47h	R/W	Fan 1 Step	Sets the maximum change per update for the Fan 1 driver	10h	SWL	Page 76
48h	R/W	Fan 1 Minimum Drive	Sets the minimum drive value for the Fan 1 driver	66h (40%)	SWL	Page 77
49h	R/W	Fan 1 Valid TACH Count	Holds the minimum tachometer reading that indicates the fan is spinning properly	F5h	SWL	Page 77
4Ah	R/W	Fan 1 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	Page 78
4Bh	R/W	Fan 1 Drive Fail Band High Byte		00h	SWL	
4Ch	R/W	TACH 1 Target Low Byte	Holds the target tachometer reading low byte Fan 1	F8h	No	Page 78
4Dh	R/W	TACH 1 Target High Byte	Holds the target tachometer reading high byte for Fan 1	FFh	No	Page 78
4Eh	R	TACH 1 Reading High Byte	Holds the tachometer reading high byte for Fan 1	FFh	No	Page 79

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
4Fh	R	TACH 1 Reading Low Byte	Holds the tachometer reading low byte for Fan 1	F8h	No	Page 79
Look Up Table 1 (LUT1)						
50h	R/W	LUT 1 Configuration	Stores and controls the configuration for LUT 1	00h	No	Page 80
51h	R/W	LUT 1 Drive 1	Stores the lowest programmed drive setting for LUT 1	FBh	LUT Lock 1	Page 82
52h	R/W	LUT 1 Temp 1 Setting 1	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock 1	Page 82
53h	R/W	LUT 1 Temp 2 Setting 1	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock 1	Page 82
54h	R/W	LUT 1 Temp 3 Setting 1	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 1 temp) that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock 1	Page 82
55h	R/W	LUT 1 Temp 4 Setting 1	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock 1	Page 82
56h	R/W	LUT 1 Drive 2	Stores the second programmed drive setting for LUT 1	E6h	LUT Lock 1	Page 82
57h	R/W	LUT 1 Temp 1 Setting 2	Stores the threshold level for the External Diode 1 (or VIN1)channel that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock 1	Page 82
58h	R/W	LUT 1 Temp 2 Setting 2	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock 1	Page 82
59h	R/W	LUT 1 Temp 3 Setting 2	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 1 temp) that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock 1	Page 82
5Ah	R/W	LUT 1 Temp 4 Setting 2	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock 1	Page 82
5Bh	R/W	LUT 1 Drive 3	Stores the third programmed drive setting for LUT 1	D1h	LUT Lock 1	Page 82
5Ch	R/W	LUT 1 Temp 1 Setting 3	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock 1	Page 82

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
5Dh	R/W	LUT 1 Temp 2 Setting 3	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock 1	Page 82
5Eh	R/W	LUT 1 Temp 3 Setting 3	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 1 temp) that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock 1	Page 82
5Fh	R/W	LUT 1 Temp 4 Setting 3	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock 1	Page 82
60h	R/W	LUT 1 Drive 4	Stores the fourth programmed drive setting for LUT 1	BCh	LUT Lock 1	Page 82
61h	R/W	LUT 1 Temp 1 Setting 4	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock 1	Page 82
62h	R/W	LUT 1 Temp 2 Setting 4	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock 1	Page 82
63h	R/W	LUT 1 Temp 3 Setting 4	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 1 temp) that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock 1	Page 82
64h	R/W	LUT 1 Temp 4 Setting 4	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock 1	Page 82
65h	R/W	LUT 1 Drive 5	Stores the fifth programmed drive setting for LUT 1	A7h	LUT Lock 1	Page 82
66h	R/W	LUT 1 Temp 1 Setting 5	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock 1	Page 82
67h	R/W	LUT 1 Temp 2 Setting 5	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock 1	Page 82
68h	R/W	LUT 1 Temp 3 Setting 5	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 1 temp) that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock 1	Page 82
69h	R/W	LUT 1 Temp 4 Setting 5	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock 1	Page 82
6Ah	R/W	LUT 1 Drive 6	Stores the sixth programmed drive setting for LUT 1	92h	LUT Lock 1	Page 82

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
6Bh	R/W	LUT 1 Temp 1 Setting 6	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock 1	Page 82
6Ch	R/W	LUT 1 Temp 2 Setting 6	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock 1	Page 82
6Dh	R/W	LUT 1 Temp 3 Setting 6	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 1 temp) that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock 1	Page 82
6Eh	R/W	LUT 1 Temp 4 Setting 6	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock 1	Page 82
6Fh	R/W	LUT 1 Drive 7	Stores the seventh programmed drive setting for LUT 1	92h	LUT Lock 1	Page 82
70h	R/W	LUT 1 Temp 1 Setting 7	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock 1	Page 82
71h	R/W	LUT 1 Temp 2 Setting 7	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock 1	Page 82
72h	R/W	LUT 1 Temp 3 Setting 7	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 1 temp) that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock 1	Page 82
73h	R/W	LUT 1 Temp 4 Setting 7	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock 1	Page 82
74h	R/W	LUT 1 Drive 8	Stores the highest programmed drive setting for LUT 1	92h	LUT Lock 1	Page 82
75h	R/W	LUT 1 Temp 1 Setting 8	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock 1	Page 82
76h	R/W	LUT 1 Temp 2 Setting 8	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock 1	Page 82
77h	R/W	LUT 1 Temp 3 Setting 8	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 1 temp) that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock 1	Page 82

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
78h	R/W	LUT 1 Temp 4 Setting 8	Stores the threshold level for the Internal Diode channel (or Pushed Temp 2 temp) that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock 1	Page 82
79h	R/W	LUT 1 Temp Hysteresis	Stores the hysteresis that is shared for all temperature inputs	0Ah (10°C)	LUT Lock 1	Page 82
Fan 2 Control Registers						
80h	R/W	Fan 2 Setting	Always displays the most recent fan driver input setting for Fan 2. If the RPM based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 69
81h	R/W	PWM2 Divide	Stores the divide ratio to set the frequency for Fan 2	01h	No	Page 70
82h	R/W	Fan 2 Configuration1	Sets configuration values for the RPM based Fan Speed Control Algorithm for Fan 2	2Bh	No	Page 70
83h	R/W	Fan 2 Configuration 2	Sets additional configuration values for the Fan 2 driver	38h	SWL	Page 72
85h	R/W	Gain 2	Holds the gain terms used by the RPM based Fan Speed Control Algorithm for Fan 2	2Ah	SWL	Page 74
86h	R/W	Fan 2 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 2 driver	19h	SWL	Page 75
87h	R/W	Fan 2 Step	Sets the maximum change per update for Fan 2	10h	SWL	Page 76
88h	R/W	Fan 2 Minimum Drive	Sets the minimum drive value for the Fan 2 driver	66h (40%)	SWL	Page 77
89h	R/W	Fan 2 Valid TACH Count	Holds the minimum tachometer reading that indicates the fan is spinning properly	F5h	SWL	Page 77
8Ah	R/W	Fan 2 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	Page 78
8Bh	R/W	Fan 2 Drive Fail Band High Byte		00h	SWL	
8Ch	R/W	TACH 2 Target Low Byte	Holds the target tachometer setting low byte for Fan 2	F8h	No	Page 78
8Dh	R/W	TACH 2 Target High Byte	Holds the target tachometer setting high byte for Fan 2	FFh	No	Page 78
8Eh	R	TACH 2 Reading High Byte	Holds the tachometer reading high byte for Fan 2	FFh	No	Page 79
8Fh	R	TACH 2 Reading Low Byte	Holds the tachometer reading low byte for Fan 2	F8h	No	Page 79
Look Up Table 2 (LUT2)						

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
90h	R/W	LUT 2 Configuration	Stores and controls the configuration for LUT 2	00h	No	Page 80
91h	R/W	LUT 2 Drive 1	Stores the lowest programmed drive setting for LUT 2	FBh	LUT Lock 2	Page 83
92h	R/W	LUT 2 Temp 1 Setting 1	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock 2	Page 83
93h	R/W	LUT 2 Temp 2 Setting 1	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock 2	Page 83
94h	R/W	LUT 2 Temp 3 Setting 1	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 3 temp) that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock 2	Page 83
95h	R/W	LUT 2 Temp 4 Setting 1	Stores the threshold level for the Internal Diode channel (or Pushed Temp 4 temp) that is associated with the Drive 1 value	7Fh (127°C)	LUT Lock 2	Page 83
96h	R/W	LUT 2 Drive 2	Stores the second programmed drive setting for LUT 2	E6h	LUT Lock 2	Page 83
97h	R/W	LUT 2 Temp 1 Setting 2	Stores the threshold level for the External Diode 1 (or VIN1)channel that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock 2	Page 83
98h	R/W	LUT 2 Temp 2 Setting 2	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock 2	Page 83
99h	R/W	LUT 2 Temp 3 Setting 2	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 3 temp) that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock 2	Page 83
9Ah	R/W	LUT 2 Temp 4 Setting 2	Stores the threshold level for the Internal Diode channel (or Pushed Temp 4 temp) that is associated with the Drive 2 value	7Fh (127°C)	LUT Lock 2	Page 83
9Bh	R/W	LUT 2 Drive 3	Stores the third programmed drive setting for LUT 2	D1h	LUT Lock 2	Page 83
9Ch	R/W	LUT 2 Temp 1 Setting 3	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock 2	Page 83
9Dh	R/W	LUT 2 Temp 2 Setting 3	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock 2	Page 83

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
9Eh	R/W	LUT 2 Temp 3 Setting 3	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 3 temp) that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock 2	Page 83
9Fh	R/W	LUT 2 Temp 4 Setting 3	Stores the threshold level for the Internal Diode channel (or Pushed Temp 4 temp) that is associated with the Drive 3 value	7Fh (127°C)	LUT Lock 2	Page 83
A0h	R/W	LUT 2 Drive 4	Stores the fourth programmed drive setting for LUT 2	BCh	LUT Lock 2	Page 83
A1h	R/W	LUT 2 Temp 1 Setting 4	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock 2	Page 83
A2h	R/W	LUT 2 Temp 2 Setting 4	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock 2	Page 83
A3h	R/W	LUT 2 Temp 3 Setting 4	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 3 temp) that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock 2	Page 83
A4h	R/W	LUT 2 Temp 4 Setting 4	Stores the threshold level for the Internal Diode channel (or Pushed Temp 4 temp) that is associated with the Drive 4 value	7Fh (127°C)	LUT Lock 2	Page 83
A5h	R/W	LUT 2 Drive 5	Stores the fifth programmed drive setting for LUT 2	A7h	LUT Lock 2	Page 83
A6h	R/W	LUT 2 Temp 1 Setting 5	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock 2	Page 83
A7h	R/W	LUT 2 Temp 2 Setting 5	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock 2	Page 83
A8h	R/W	LUT 2 Temp 3 Setting 5	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 3 temp) that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock 2	Page 83
A9h	R/W	LUT 2 Temp 4 Setting 5	Stores the threshold level for the Internal Diode channel (or Pushed Temp 4 temp) that is associated with the Drive 5 value	7Fh (127°C)	LUT Lock 2	Page 83
AAh	R/W	LUT 2 Drive 6	Stores the sixth programmed drive setting for LUT 2	92h	LUT Lock 2	Page 83
ABh	R/W	LUT 2 Temp 1 Setting 6	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock 2	Page 83

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
ACh	R/W	LUT 2 Temp 2 Setting 6	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock 2	Page 83
ADh	R/W	LUT 2 Temp 3 Setting 6	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 3 temp) that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock 2	Page 83
AEh	R/W	LUT 2 Temp 4 Setting 6	Stores the threshold level for the Internal Diode channel (or Pushed Temp 4 temp) that is associated with the Drive 6 value	7Fh (127°C)	LUT Lock 2	Page 83
AFh	R/W	LUT 2 Drive 7	Stores the seventh programmed drive setting for LUT 2	92h	LUT Lock 2	Page 83
B0h	R/W	LUT 2 Temp 1 Setting 6	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock 2	Page 83
B1h	R/W	LUT 2 Temp 2 Setting 6	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock 2	Page 83
B2h	R/W	LUT 2 Temp 3 Setting 6	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 3 temp) that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock 2	Page 83
B3h	R/W	LUT 2 Temp 4 Setting 6	Stores the threshold level for the Internal Diode channel (or Pushed Temp 4 temp) that is associated with the Drive 7 value	7Fh (127°C)	LUT Lock 2	Page 83
B4h	R/W	LUT 2 Drive 8	Stores the highest programmed drive setting for LUT 2	92h	LUT Lock 2	Page 83
B5h	R/W	LUT 2 Temp 1 Setting 8	Stores the threshold level for the External Diode 1 (or VIN1) channel that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock 2	Page 83
B6h	R/W	LUT 2 Temp 2 Setting 8	Stores the threshold level for the External Diode 2 (or VIN2) channel that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock 2	Page 83
B7h	R/W	LUT 2 Temp 3 Setting 8	Stores the threshold level for the External Diode 3 channel (or VIN3 or TRIP_SET voltage or Pushed Temp 3 temp) that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock 2	Page 83
B8h	R/W	LUT 2 Temp 4 Setting 8	Stores the threshold level for the Internal Diode channel (or Pushed Temp 4 temp) that is associated with the Drive 8 value	7Fh (127°C)	LUT Lock 2	Page 83
B9h	R/W	LUT 2 Temp Hysteresis	Stores the hysteresis that is shared for all temperature inputs	0Ah (10°C)	LUT Lock 2	Page 83

Table 6.1 EMC2106 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
GPIO Registers						
E0h	R/W	Muxed Pin Configuration Register	Controls the pin function for the pins muxed with PWMs or GPIOs	01h	No	Page 85
E1h	R/W	GPIO Direction Register	Controls the GPIO direction for GPIOs 1 - 6	00h	No	Page 86
E2h	R/W	GPIO Output Configuration Register	Controls the output type GPIOs 1 - 6	00h	No	Page 86
E3h	R	GPIO Input Register	Stores the inputs for GPIOs 1 - 6	00h	No	Page 87
E4h	R/W	GPIO Output Register	Controls the output state of GPIOs 1 - 6	00h	No	Page 87
E5h	R/W	GPIO Interrupt Enable Register	Enabled Interrupts for GPIOs 1 - 6	00h	No	Page 87
E6h	R	GPIO Status	Indicates change of state for inputs on GPIOs 1 - 6	00h	No	Page 88
Lock Register						
EF	R/W	Software Lock	Locks all SWL registers	00h	SWL	Page 88
Revision Registers						
FCh	R	Product Features	Stores information about which pin controlled product features are set	00h	No	Page 89
FDh	R	Product ID	Stores the unique Product ID	1Eh	No	Page 89
FEh	R	Manufacturer ID	Stores the Manufacturer ID	5Dh	No	Page 89
FFh	R	Revision	Revision	02h	No	Page 90

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

6.1.1 Lock Entries

The Lock Column describes the locking mechanism, if any, used for individual registers. All SWL registers are Software Locked and therefore made read-only when the LOCK bit is set.

6.2 Temperature Data Registers

Table 6.2 Temperature Data Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R	Internal Diode High Byte	Sign	64	32	16	8	4	2	1	00h
01h	R	Internal Diode Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
02h	R	External Diode 1 High Byte	Sign	64	32	16	8	4	2	1	00h
		VIN1	400	200	100	50	25	13.5	6.25	3.125	00h
03h	R	External Diode 1 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
04h	R	External Diode 2 High Byte	Sign	64	32	16	8	4	2	1	00h
		VIN2	400	200	100	50	25	13.5	6.25	3.125	00h
05h	R	External Diode 2 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
06h	R	External Diode 3 High Byte	Sign	64	32	16	8	4	2	1	00h
		VIN3	400	200	100	50	25	13.5	6.25	3.125	00h
07h	R	External Diode 3 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
08h	R	External Diode 4 High Byte	Sign	64	32	16	8	4	2	1	00h
09h	R	External Diode 4 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

The temperature measurement range is from -64°C to +128°C. The data format is a signed two's complement number as shown in Table 6.3.

APPLICATION NOTE: When each of the External Diode 1, External Diode 2, or External Diode 3 channels are configured as a voltage input, the voltage data will be stored in the corresponding data register. Each bit weight represents XmV of resolution so that the final voltage can be determined by adding the appropriately set bits together. This data will be compared against the limits normally (see Section 6.22).

Table 6.3 Temperature Data Format

TEMPERATURE (°C)	BINARY	HEX (AS READ BY REGISTERS)
Diode Fault	1000_0000_000b	80_00h
-63.875	1100_0000_001b	C0_20h
-63	1100_0001_000b	C1_00h
-1	1111_1111_000b	FF_00h
-0.125	1111_1111_111b	FF_E0h
0	0000_0000_000b	00_00h
0.125	0000_0000_001b	00_20h
1	0000_0001_000b	01_00h
63	0011_1111_000b	3F_00h
64	0100_0000_000b	40_00h
65	0100_0001_000b	41_00h
127	0111_1111_000b	7F_00h
127.875	0111_1111_111b	7F_E0h

6.3 Critical/Thermal Shutdown Temperature Registers

Table 6.4 Critical/Thermal Shutdown Temperature Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Ah	R	Critical/Thermal Shutdown Temperature	128	64	32	16	8	4	2	1	7Fh (+127°C)

The Critical/Thermal Shutdown Temperature Register is a read-only register that stores the Voltage Programmable Threshold temperature used in the Thermal / Critical Shutdown circuitry. The contents of the register reflect the calculated temperature based on the TRIP_SET voltage. This register is updated at the end of every monitoring cycle based on the current value of the TRIP_SET voltage.

The data format is shown in Table 6.5.

Table 6.5 Critical / Thermal Shutdown Data Format

TEMPERATURE (°C)	BINARY	HEX
0	0000_0000b	00h
1	0000_0001b	01h
63	0011_1111b	3Fh
64	0100_0000b	40h

Table 6.5 Critical / Thermal Shutdown Data Format (continued)

TEMPERATURE (°C)	BINARY	HEX
65	0100_0001b	41h
127	0111_1111b	7Fh
130	1000_0010b	82h
150	1001_0110b	96h

6.4 Pushed Temperature Registers

Table 6.6 Pushed Temperature Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Ch	R/W	Pushed Temperature 1	Sign	64	32	16	8	4	2	1	00h
0Dh	R/W	Pushed Temperature 2	Sign	64	32	16	8	4	2	1	00h
0Eh	R/W	Pushed Temperature 3	Sign	64	32	16	8	4	2	1	00h
0Fh	R/W	Pushed Temperature 4	Sign	64	32	16	8	4	2	1	00h

The Pushed Temperature Registers store user programmed temperature values that can be used by the look-up table to update the fan control algorithm. Data written in these registers is not compared against any limits and must match the data format shown in Table 6.3.

6.5 Voltage Registers

Table 6.7 TripSet Voltage Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
10h	R	TRIP_SET Voltage / VIN4 Voltage	400	200	100	50	25	13.5	6.25	3.125	FFh

The Voltage Registers hold the data read from the TRIP_SET voltage input. The TRIP_SET voltage is stored whether the TRIP_SET is used to set the Thermal / Critical Shutdown temperature or configured to act as the VIN4 input.

Each bit weight represents mV of resolution so that the final voltage can be determined by adding the appropriately set bits together.

6.6 Beta Configuration Registers

Table 6.8 Beta Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
14h	R/W	External Diode 1 Beta Configuration	-	-	-	AUTO	BETA1[3:0]				10h
15h	R/W	External Diode 2 Beta Configuration	-	-	-	AUTO	BETA2[3:0]				10h
16h	R/W	External Diode 3 Beta Configuration	-	-	-	AUTO	BETA3[3:0]				10h

The Beta Configuration Registers control advanced temperature measurement features for each External Diode channel. The Beta Configuration Registers are software locked. The External Diode 1 Beta Configuration Register Is hardware locked if the SHDN_SEL pin is not set to disable the Critical / Thermal Shutdown functionality (see Table 6.1).

Bit 4 - AUTO - Enables the Automatic Beta detection algorithm.

- ‘0’ - The Automatic Beta detection algorithm is disabled. The BETAx[3:0] bit settings will be used to control the beta compensation circuitry.
- ‘1’ (default) - The Automatic Beta detection algorithm is enabled. The circuitry will automatically detect the transistor type and beta values and configure the BETAx[3:0] bits for optimal performance.

Bits 3 - 0 - BETAx[3:0] - hold a value that corresponds to a range of betas that the Beta Compensation circuitry can compensate for. These four bits will always show the current beta setting used by the circuitry. If the AUTO bit is set (default), then these bits may updated by the device with every temperature conversion. If the AUTO bit is not set, then the value of these bits is used to drive the beta compensation circuitry. In this case, these bits should be set with a value corresponding to the lowest expected value of beta for the PNP transistor being used as a temperature sensing device.

See Table 6.9 for supported beta ranges. A value of 1111b indicates that the beta compensation circuitry is disabled. In this condition, the diode channels will function with default current levels and will not automatically adjust for beta variation. This mode is used when measuring a discrete 2N3904 transistor or AMD thermal diode.

All of the Beta Configuration Registers are Software Locked.

Table 6.9 Beta Compensation Look Up Table

AUTO	BETAX[3:0]				MINIMUM BETA
	3	2	1	0	
0	0	0	0	0	0.050
0	0	0	0	1	0.066
0	0	0	1	0	0.087
0	0	0	1	1	0.114
0	0	1	0	0	0.150

Table 6.9 Beta Compensation Look Up Table (continued)

AUTO	BETAX[3:0]				MINIMUM BETA
	3	2	1	0	
0	0	1	0	1	0.197
0	0	1	1	0	0.260
0	0	1	1	1	0.342
0	1	0	0	0	0.449
0	1	0	0	1	0.591
0	1	0	1	0	0.778
0	1	0	1	1	1.024
0	1	1	0	0	1.348
0	1	1	0	1	1.773
0	1	1	1	0	2.333
0	1	1	1	1	Disabled
1	X	X	X	X	Automatically detected

6.7 REC Configuration Register

Table 6.10 REC Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
17h	R/W	REC Configuration	-	-	-	-	-	REC3	REC2	REC1	07h

The REC Configuration Register determines whether Resistance Error Correction is used for each external diode channel. The REC Configuration Register is software locked.

Bit 2 - REC3 - Controls the Resistive Error Correction functionality of External Diode 3 and External Diode 4 (if APD is enabled, see Section 6.9)

- ‘0’ - the REC functionality for External Diode 3 is disabled
- ‘1’ (default) - the REC functionality for External Diode 3 is enabled.

Bit 1 - REC2 - Controls the Resistive Error Correction functionality of External Diode 2.

- ‘0’ - the REC functionality for External Diode 2 is disabled
- ‘1’ (default) - the REC functionality for External Diode 2 is enabled.

Bit 0 - REC1 - Controls the Resistive Error Correction functionality of External Diode 1. This bit is locked if the SHDN_SEL pin is not pulled to VDD (see Table 6.1).

- ‘0’ - the REC functionality for External Diode 1 is disabled
- ‘1’ (default) - the REC functionality for External Diode 1 is enabled.

6.8 Critical Temperature Limit Registers

Table 6.11 Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
19h	R/W once	External Diode 1 Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)
1Ah	R/W once	External Diode 2 Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)
1Bh	R/W once	External Diode 3 Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)
1Ch	R/W once	External Diode 4 Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)
1Dh	R/W once	Internal Diode Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (+100°C)

The Critical Temperature Limit Registers store the Critical Temperature Limit. At power up, none of the respective channels are linked to the SYS_SHDN pin or the Hardware set Thermal/Critical Shutdown circuitry.

Whenever one of the registers is updated, two things occur. First, the register is locked so that it cannot be updated again without a power on reset. Second, the respective temperature channel is linked to the SYS_SHDN pin and the Hardware set Thermal/Critical Shutdown Circuitry. At this point, if the measured temperature channel exceeds the Critical limit, the SYS_SHDN pin will be asserted, the appropriate bit set in the Tcrit Status Register, and the TCRIT bit in the Interrupt Status Register will be set.

6.9 Configuration Register

Table 6.12 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
20h	R/W	Configuration	MASK	-	-	SYS4	SYS3	SYS2	SYS1	APD	00h

The Configuration Register controls the basic functionality of the EMC2106. The bits are described below. The Configuration Register is software locked.

Bit 7 - MASK - Blocks the ALERT# pin from being asserted.

- ‘0’ (default) - The ALERT# pin is unmasked. If any bit in either status register is set, the ALERT# pins will be asserted (unless individually masked via the Mask Register)
- ‘1’ - The ALERT# pin is masked and will not be asserted.

Bit 4 - SYS4 - Enables the high temperature limit for the External Diode 4 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 6.1). This bit is ignored if the DP3 / DN3 pins are configured to measure a voltage input. In this case, the External Diode 4 channel is disabled and not compared against any limits.

- ‘0’ (default) - the External Diode 4 channel high limit will not be linked to the SYS_SHDN# pin. If the temperature exceeds the limit, the ALERT# pin will be asserted normally.
- ‘1’ - the External Diode 4 channel high limit will be linked to the SYS_SHDN# pin. If the temperature exceeds the limit then the SYS_SHDN# pin will be asserted. The SYS_SHDN# pin will be released

when the temperature drops below the high limit. The ALERT# pin will be asserted and released normally.

Bit 3 - SYS3 - Enables the high temperature limit for the External Diode 3 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 6.1).

Bit 2 - SYS2 - Enables the high temperature limit for the External Diode 2 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 6.1).

Bit 1 - SYS1 - Enables the high temperature limit for the External Diode 1 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 6.1).

Bit 0 - APD - This bit enables the Anti-parallel diode functionality on the External Diode 3 pins (DP3 and DN3).

- '0' (default) - The Anti-parallel diode functionality is disabled. The External Diode 3 channel can be configured for any type of diode
- '1' - The Anti-parallel diode functionality is enabled. Both the External Diode 3 and 4 channels are configured to support a diode or diode connected transistor (such as a 2N3904).

APPLICATION NOTE: When the APD diode is enabled, there will be a delay of a full temperature update before any comparisons and functionality associated with the External Diode 4 channel will be implemented. This includes the SYS4 bit operation, limit comparisons, and look up table comparisons.

6.10 Configuration 2 Register

Table 6.13 Configuration 2 Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
21h	R/W	Config 2	-	DIS_ DYN	DIS_ TO	DIS_ AVG	QUEUE[1:0]		CONV[1:0]		0Eh

The Configuration 2 Register controls conversion rate of the temperature monitoring as well as the fault queue. This register is software locked.

Bit 6 - DIS_DYN - Disables the Dynamic Averaging Feature.

- '0' (default) - The Dynamic Averaging function is enabled. The conversion time for all temperature channels is scaled based on the chosen conversion rate to maximize accuracy and immunity to random temperature measurement variation.
- '1' - The Dynamic Averaging function is disabled. The conversion time for all temperature channels is fixed regardless of the chosen conversion rate.

Bit 5 - DIS_TO - Disables the SMBus time out function for the SMBus client (if enabled).

- '0' (default) - The SMBus time out function is enabled.
- '1' - The SMBus time out function is disabled allowing the device to be fully I^2C compliant.

Bit 4 - DIS_AVG - Disables digital averaging of the External Diode 1 channel.

- '0' (default) - The External Diode 1 channel has digital averaging enabled. The temperature data is the average of the previous four measurements.
- '1' - The External Diode 1 channel has digital averaging disabled. The temperature data is the last measured data.

Bits 3-2 - QUEUE[1:0] - Determines the number of consecutive out of limit conditions that are necessary to trigger an interrupt. Each measurement channel has a separate fault queue associated with the high limit, low limit, and diode fault condition except the internal diode.

The Critical / Thermal Shutdown temperature has a separate fault queue that applies to the selected hardware shutdown channel (see Section 6.1.1) when compared against the threshold set by the TRIP_SET pin.

APPLICATION NOTE: If the fault queue for any channel is currently active (i.e. an out of limit condition has been detected and caused the fault queue to increment) then changing the settings will not take effect until the fault queue is zeroed. This occurs by the ALERT# pin asserting or the out of limit condition being removed.

Table 6.14 Fault Queue

QUEUE[1:0]		NUMBER OF CONSECUTIVE OUT OF LIMIT CONDITIONS
1	**0**	
0	0	1 (disabled)
0	1	2
1	0	3
1	1	4 (default)

Bit 1 - 0 - CONV[1:0] - determines the conversion rate of the temperature monitoring. This conversion rate does not affect the fan driver. The supply current from VDD_3V is nominally dependent upon the conversion rate and the average current will increase as the conversion rate increases.

Table 6.15 Conversion Rate

CONV[1:0]		CONVERSION RATE	TEMPERATURE OVER SAMPLING FROM 11 BITS	
1	**0**		**DYN_DIS = ‘0’**	**DYN_DIS = ‘1’**
0	0	1 / sec	x8	x1
0	1	2 / sec	x4	x1
1	0	4 / sec (default)	x2	x1
1	1	Continuous	x1	x1

6.11 Configuration 3 Register

Table 6.16 Configuration 3 Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	R/W	Config 3	-	VIN4_INV	VIN3_EN	VIN3_INV	VIN2_EN	VIN2_INV	VIN1_EN	VIN1_INV	00h

The Configuration 3 Register controls the four voltage input channels. This register is software locked.

Bit 6 - VIN4_INV - Determines whether the VIN4 channel data is inverted.

- ‘0’ (default) - The VIN4 channel data is not inverted.

- '1' - The VIN4 channel data is inverted. The data presented to the reading registers and compared against the limits is determined as FFh - the measured input voltage.

APPLICATION NOTE: If the TRIP_SET / VIN4 pin is configured to be used to set the Critical / Thermal Shutdown temperature associated with the External Diode 1 channel, then this bit cannot be set.

Bit 5 - VIN3_EN - Enables the voltage mode on the External Diode 3 channel.

- '0' (default) - The External Diode 3 channel operates as a diode channel.
- '1' - The External Diode 3 channel operates as a voltage input. The DP3 / DN4 / VREF_T3 pin acts as a reference output voltage and the DN3 / DP4 /. VIN3 pin acts as a voltage input. This overrides the APD bit in the Configuration 1 Register (20h).

Bit 4 - VIN3_INV - Determines whether the VIN3 channel data is inverted.

Bit 3 - VIN2_EN - Enables the voltage mode on the External Diode 2 channel.

Bit 2 - VIN2_INV - Determines whether the VIN2 channel data is inverted.

Bit 1 - VIN1_EN - Enables the voltage mode on the External Diode 1 channel.

Bit 0 - VIN1_INV - Determines whether the VIN1 channel data is inverted.

APPLICATION NOTE: If the TRIP_SET / VIN4 pin is configured to be used to set the Critical / Thermal Shutdown temperature associated with the External Diode 1 channel, then neither Bit 1 nor Bit 0 can be set.

6.12 Interrupt Status Register

Table 6.17 Interrupt Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
23h	R-C	Interrupt Status Register	EEPROM	TSD	TCRIT	GPIO	FAN	HIGH	LOW	FAULT	00h

The Interrupt Status Register reports the operating condition of the EMC2106. If any of the bits are set to a logic '1' (other than TSD and HWS) then the ALERT# pin will be asserted low if the corresponding channel is enabled. Reading from the status register clears all status bits if the error conditions is removed. If there are no set status bits, then the ALERT# pin will be released.

The bits that cause the ALERT# pin to be asserted can be masked based on the channel they are associated with unless stated otherwise.

Bit 7 - EEPROM - This bit is set to '1' if the EEPROM loader circuitry detects an error when writing data from the EEPROM. This bit is cleared when the register is read. This bit is not masked except via the MASK bit.

Bit 6 - TSD - This bit is set to '1' if the internal Thermal Shutdown (TSD) circuit trips indicating that the die temperature has exceeded its threshold. When this bit is set, it will not cause the ALERT# pin to be asserted however will coincide with the SYS_SHDN# pin being asserted. This bit is cleared when the register is read and the error condition has been removed.

Bit 5 - TCRIT - This bit is set to '1' whenever the any bit in the Tcrit Status Register is set. This bit is automatically cleared when the Tcrit Status Register is cleared.

Bit 4 - GPIO - This bit is set to '1' if any of the bits in the GPIO Status Registers are set.

Bit 3 - FAN - This bit is set to '1' if any bit in the Fan Status Register is set. This bit is automatically cleared when the Fan Status Register is read and the bits are cleared.

Bit 2 - HIGH - This bit is set to ‘1’ if any bit in the High Status Register is set. This bit is automatically cleared when the High Status Register is read and the bits are cleared.

Bit 1- LOW - This bit is set to ‘1’ if any bit in the Low Status Register is set. This bit is automatically cleared when the Low Status Register is read and the bits are cleared.

Bit 0 - FAULT - This bit is set to ‘1’ if any bit in the Diode Fault Register is set. This bit is automatically cleared when the Diode Fault Register is read and the bits are cleared.

6.13 Error Status Registers

Table 6.18 Error Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R-C	Tcrit Status	HWS	-	-	EXT4_ CRIT	EXT3_ CRIT	EXT2_ CRIT	EXT1 _CRIT	INT_ CRIT	00h
24h	R-C	High Status	-	-	VOLT 4_HI	EXT4_ HI	EXT3_ HI	EXT2_ HI	EXT1 _HI	INT_ HI	00h
25h	R-C	Low Status	-	-	VOLT 4_LO	EXT4_ LO	EXT3_ LO	EXT2_ LO	EXT1 _LO	INT_L O	00h
26h	R-C	Diode Fault	-	-	-	EXT4_ FLT	EXT3_ FLT	EXT2_ FLT	EXT1 _FLT	-	00h

The Error Status Registers report the specific error condition for all measurement channels with limits. If any bit is set in the High, Low, or Diode Fault Status register, the corresponding High, Low, or Fault bit is set in the Interrupt Status Register.

Reading the Interrupt Status Register does not clear the Error Status bit. Reading from any Error Status Register that has bits set will clear the register and the corresponding bit in the Interrupt Status Register if the error condition has been removed. If the error condition is persistent, reading the Error Status Registers will have no affect.

If any of the External Diode 1, External Diode 2, or External Diode 3 channels are configured as a voltage input, then the corresponding temperature channel status bit will be set if the measured voltage exceeds the high limit or falls below the low limit. In this condition, a diode fault will be ignored.

APPLICATION NOTE: If any of the External Diode 1, 2, or 3 channels are configured as a voltage input and thermistor or other voltage source is used on the corresponding pins at device power up, then the corresponding diode fault status bits will be set. The status bits should be cleared prior to enabling the interrupts to avoid erroneous alert conditions.

6.13.1 Tcrit Status Register

The Tcrit Status Register stores the event that caused the SYS_SHDN# pin to be asserted. Each of the temperature channels must be associated with the SYS_SHDN# pin before they can be set (see Section 6.8). Once the SYS_SHDN# pin is asserted, it will be released when the temperature drops below the threshold level however the individual status bit will not be cleared until read.

Bit 7 - HWS - This bit is set if the hardware set temperature channel meets or exceeds the temperature threshold determined by the TRIP_SET voltage.

6.14 Fan Status Register

Table 6.19 Fan Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
27h	R-C	Fan Status Register	WATCH	DRIVE _FAIL2	DRIVE _FAIL1	FAN_ SHORT	FAN_ SPIN2	FAN_ STALL2	FAN_ SPIN1	FAN_ STALL1	00h

The Fan Status Register contains the status bits associated with each fan driver. This register is cleared when read if the error condition has been removed.

Bit 7 - WATCH - This bit is asserted ‘1’ if the host has not programmed the fan driver(s) within four (4) seconds after power up.

Bit 6 - DRIVE_FAIL2 - Indicates that the RPM based Fan Speed Control Algorithm cannot drive Fan 2 to the desired target setting at maximum drive. This bit can be masked from asserting the ALERT# pin.

- ‘0’ - The RPM based Fan Speed Control Algorithm can drive Fan 2 to the desired target setting.
- ‘1’ - The RPM based Fan Speed Control Algorithm cannot drive Fan 2 to the desired target setting at maximum drive.

Bit 6 - DRIVE_FAIL1 - Indicates that the RPM based Fan Speed Control Algorithm cannot drive Fan 1 to the desired target setting at maximum drive. This bit can be masked from asserting the ALERT# pin.

- ‘0’ - The RPM based Fan Speed Control Algorithm can drive Fan 1 to the desired target setting.
- ‘1’ - The RPM based Fan Speed Control Algorithm cannot drive Fan 1 to the desired target setting at maximum drive.

Bit 5 - FAN_SHORT - This bit is asserted ‘1’ if the High Side Fan Driver detects an over current condition that lasts for longer than 2 seconds.

Bit 3 - FAN_SPIN 2- This bit is asserted ‘1’ if the Spin up Routine for Fan 2 cannot detect a valid tachometer reading within its maximum time window. This bit can be masked from asserting the ALERT# pin.

Bit 2 - FAN_STALL 2 - This bit is asserted ‘1’ if the tachometer measurement on Fan 2 detects a stalled fan. This bit can be masked from asserting the ALERT# pin.

Bit 1- FAN_SPIN1- This bit is asserted ‘1’ if the Spin up Routine for Fan 1 cannot detect a valid tachometer reading within its maximum time window. This bit can be masked from asserting the ALERT# pin.

Bit 0 - FAN_STALL1 - This bit is asserted ‘1’ if the tachometer measurement on Fan 1 detects a stalled fan. This bit can be masked from asserting the ALERT# pin.

6.15 Interrupt Enable Register

Table 6.20 Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
28	R/W	Interrupt Enable	-	-	VOLT4_I NT_EN	EXT4_I NT_EN	EXT3_I NT_EN	EXT2_I NT_EN	EXT1_I NT_EN	INT_IN T_EN	00h

The Interrupt Enable Register controls the masking for each temperature channel. When a channel is masked, it will not cause the ALERT# pin to be asserted when an error condition is detected.

Bit 5 - VOLT4_INT_EN - Allows the Voltage Input 4 channel to assert the ALERT# pin.

- ‘0’ (default) - The ALERT# pin will be not be asserted for any error condition associated with Voltage Channel 4 (TRIP_SET / VIN4).
- ‘1’ - The ALERT# pin will be asserted for an error condition associated with Voltage Channel 4.

Bit 4 - EXT4_INT_EN - Allows the External Diode 4 channel to assert the ALERT# pin.

- ‘0’ (default) - The ALERT# pin will be not be asserted for any error condition associated with External Diode 4.
- ‘1’ - The ALERT# pin will be asserted for an error condition associated with External Diode 4.

Bit 3 - EXT3_INT_EN - Allows the External Diode 3 or VIN3 channel to assert the ALERT# pin.

- ‘0’ (default) - The ALERT# pin will not be asserted for any error condition associated with External Diode 3 or VIN3 channels.
- ‘1’ - The ALERT# pin will be asserted for an error condition associated with External Diode 3 or VIN3 channels.

Bit 2 - EXT2_INT_EN - Allows the External Diode 2 or VIN2 channel to assert the ALERT# pin.

- ‘0’ (default) - The ALERT# pin will not be asserted for any error condition associated with External Diode 2 or VIN2 channels.
- ‘1’ - The ALERT# pin will be asserted for an error condition associated with External Diode 2 or VIN2 channels.

Bit 1 - EXT1_INT_EN - Allows the External Diode 1 or VIN1 channel to assert the ALERT# pin.

- ‘0’ (default) - The ALERT# pin will not be asserted for any error condition associated with External Diode 1 or VIN1 channels.
- ‘1’ - The ALERT# pin will be asserted for an error condition associated with External Diode 1 or VIN1 channels.

Bit 0 - INT_INT_EN - Allows the Internal Diode channel to assert the ALERT# pin.

- ‘0’ (default) - The ALERT# pin will not be asserted for any error condition associated with the Internal Diode.
- ‘1’ - The ALERT# pin will be asserted for an error condition associated with the Internal Diode.

6.16 Fan Interrupt Enable Register

Table 6.21 Fan Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
29h	R/W	Fan Interrupt Enable	-	-	-	-	SPIN_ INT_EN2	STALL_ INT_EN2	SPIN_ INT_EN 1	STALL_ INT_EN 1	00h

The Fan Interrupt Enable controls the masking for each Fan channel. When a channel is enabled, it will cause the ALERT# pin to be asserted when an error condition is detected.

Bit 3 - SPIN_INT_EN2 - Allows the FAN_SPIN 2 bit to assert the ALERT# pin.

- ‘0’ (default) - the FAN_SPIN 2 bit will not assert the ALERT# pin though will still update the Status Register normally
- ‘1’ - the FAN_SPIN2 bit will assert the ALERT# pin.

Bit 2 - STALL_INT_EN2 - Allows the FAN_STALL2 bit or DRIVE_FAIL2 bit to assert the ALERT# pin.

- '0' (default) - the FAN_STALL2 bit or DRIVE_FAIL2 bit will not assert the ALERT# pin though it will still update the Status Register normally.
- '1' - the FAN_STALL 2 or DRIVE_FAIL2 bits will assert the ALERT# pin if set.

Bit 1 - SPIN_INT_EN1 - Allows the FAN_SPIN1 bit to assert the ALERT# pin.

- '0' (default) - the FAN_SPIN1 bit will not assert the ALERT# pin though it will still update the Status Register normally.
- '1' - the FAN_SPIN1 bit will assert the ALERT# pin.

Bit 0 - STALL_INT_EN1 - Allows the FAN_STALL1 bit or DRIVE_FAIL1 bit to assert the ALERT# pin.

- '0' (default) - the FAN_STALL1 bit or DRIVE_FAIL1 bit will not assert the ALERT# pin though will still update the Status Register normally.
- '1' - the FAN_STALL1 or DRIVE_FAIL1 bit will assert the ALERT# pin if set.

6.17 PWM Configuration Register

Table 6.22 PWM Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Ah	R/W	PWM Config	-	-	-	-	POLARITY4	POLARITY3	POLARITY2	POLARITY1	00h

The PWM Config Register controls the output type and polarity of all PWM outputs.

Bit 3 - POLARITY4 - Determines the polarity of PWM4 (if enabled).

- '0' (default) - the Polarity of the PWM driver is normal. A drive setting of 00h will cause the output to be set at 0% duty cycle and a drive setting of FFh will cause the output to be set at 100% duty cycle.
- '1' - The Polarity of the PWM driver is inverted. A drive setting of 00h will cause the output to be set at 100% duty cycle and a drive setting of FFh will cause the output to be set at 0% duty cycle.

Bit 2 - POLARITY3 - Determines the polarity of PWM3 (if enabled).

Bit 1 - POLARITY2 - Determines the polarity of PWM2 (if enabled).

Bit 0 - POLARITY1 - Determines the polarity of PWM1 (if enabled).

6.18 PWM Base Frequency Register

Table 6.23 PWM Base Frequency Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Bh	R/W	PWM Base Frequency	PWM_BASE4_1	PWM_BASE4_0	PWM_BASE3_1	PWM_BASE3_0	PWM_BASE2_1	PWM_BASE2_0	PWM_BASE1_1	PWM_BASE1_0	FFh

The PWM Base Frequency Register determines the base frequency that is used with the PWM Divide register to determine the final PWM frequency. Each PWM driver uses the same divide ratio as set by the PWM Divide Register.

Bits 7-6 - PWM_BASE4[1:0] - Determines the base frequency of the PWM4 driver (GPIO3 / PWM4 pin).

Bits 5-4 - PWM_BASE3[1:0] - Determines the base frequency of the PWM3 driver (GPIO2 / PWM3 pin).

Bits 3-2 - PWM_BASE2[1:0] - Determines the base frequency of the PWM2 driver (PWM2 / GPIO4 pin).

Bits 1-0 - PWM_BASE1[1:0] - Determines the base frequency of the PWM1 driver (PWM1).

Table 6.24 PWM_BASEx[1:0] Bit Decode

PWM_BASEX[1:0]		BASE FREQUENCY
1	**0**	
0	0	26.00kHz
0	1	19.531kHz
1	0	4,882Hz
1	1	2,441Hz (default)

6.19 PWM 3 and 4 Divide Registers

Table 6.25 PWM Divide Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Ch	R/W	PWM 3 Divide	128	64	32	16	8	4	2	1	50h (80)
2Fh	R/W	PWM 4 Divide	128	64	32	16	8	4	2	1	50h (80)

The PWM 3 and PWM 4 Divide Registers determine the final frequency of the PWM 3 and PWM 4 drivers respectively. Each driver base frequency is divided by the value of the PWM Divide Register to determine the final frequency. The duty cycle settings are not affected by these settings, only the final frequency of the PWM driver. A value of 00h will be decoded as 01h.

6.20 PWM 3 Setting Register

Table 6.26 PWM 3 Setting Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Dh	R/W	PWM 3 Setting	128	64	32	16	8	4	2	1	00h

The PWM 3 Input Register controls the output of the GPIO2 / PWM3 pin when it is configured as a PWM output. The input code represents the number of counts out of a total of 255 that the output will be high for.

The setting operates independently of the PWM polarity A value of FFh corresponds to fully on (default 100% duty cycle) while a value of 00h corresponds to a fully off (default 0% duty cycle).

6.21 PWM 4 Setting Register

Table 6.27 PWM 4 Setting Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Eh	R/W	PWM 4 Setting	128	64	32	16	8	4	2	1	00h

The PWM 4 Input Register controls the output of the GPIO3 / PWM4 pin when it is configured as a PWM output. The input code represents the number of counts out of a total of 255 that the output will be high for.

The setting operates independently of the PWM polarity A value of FFh corresponds to fully on (default 100% duty cycle) while a value of 00h corresponds to a fully off (default 0% duty cycle).

6.22 Limit Registers

Table 6.28 Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
30h	R/W	External Diode 1 High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
31h	R/W	External Diode 2 High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
32h	R/W	External Diode 3 High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
33h	R/W	External Diode 4 High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
34h	R/W	Internal Diode High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
35h	R/W	VIN4 High Limit	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	FFh (0.8V)
38h	R/W	External Diode 1 Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)
39h	R/W	External Diode 2 Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)
3Ah	R/W	External Diode 3 Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)
3Bh	R/W	External Diode 4 Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)

Table 6.28 Limit Registers (continued)

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
3Ch	R/W	Internal Diode Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)
3Dh	R/W	VIN 4 Low Limit	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	00h (0V)

The EMC2106 contains high limits for all temperature channels and voltage channels. If any measurement meets or exceeds the high limit then the appropriate status bit is set and the ALERT# pin are asserted (if enabled).

APPLICATION NOTE: If any of the External Diode 1, External Diode 2, External Diode 3 is configured to operate as a voltage input, then the corresponding temperature high and low limit registers are compared against the measured voltage. The data format is the same as the measured voltage and these registers should be updated accordingly.

Additionally, the EMC2106 contains low limits for all temperature channels. If the temperature channel drops below the low limit, then the appropriate status bit is set and the ALERT# pin are asserted (if enabled).

All Limit Registers are Software Locked.

6.23 Fan Setting Registers

Table 6.29 Fan Driver Setting Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Fan 1 Setting	128	64	32	16	8	4	2	1	00h
80h	R/W	Fan 2 Setting	128	64	32	16	8	4	2	1	00h

The Fan 1 Setting Register always displays the current setting of the Fan 1 Driver. Likewise, the Fan 2 Setting Register always displays the current setting of the Fan 2 driver. Reading from either register will report the current fan speed setting of the appropriate fan driver regardless of the operating mode. Therefore it is possible that reading from this register will not report data that was previously written into this register.

While the RPM based Fan Speed Control Algorithm or the Look Up Table are active (or both), then the register is read only. Writing to the register will have no affect and the data will not be stored.

If both the RPM based Fan Control Algorithm and the Look Up Table are disabled, then the register will be set with the previous value that was used. The register is read / write and writing to this register will affect the fan speed.

If the Fan 2 fan driver is disabled and the DAC2 / PWM2 / GPIO2 and TACH2 / GPIO1 pins are used as GPIOs, then the Fan 2 Setting Register will read 00h.

The contents of the register represent the weighting of each bit in determining the final output voltage. The output drive for a PWM output is given by Equation [2]. The output drive for the Linear DAC driver is given by Equation [3].The output drive for the High Side Fan Driver output is given by Equation [4].

$$Drive = \left(\frac{VALUE}{255}\right) \times 100\% \quad [2]$$

$$Drive = \left(\frac{VALUE}{255}\right) \times VDD \quad [3]$$

$$Drive = \left(\frac{VALUE}{255}\right) \times VDD_5V \quad [4]$$

6.24 PWM 1 and 2 Divide Registers

Table 6.30 PWM 1 and 2 Divide Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
41h	R/W	PWM 1 Divide	128	64	32	16	8	4	2	1	01h
81h	R/W	PWM 2 Divide	128	64	32	16	8	4	2	1	01h

The PWM 1 and 2 Divide Registers determine the final frequency of the PWM 1and PWM 2 drivers. Each driver base frequency is divided by the value of the respective PWM Divide Register to determine the final frequency. The duty cycle settings are not affected by these settings, only the final frequency of the PWM driver. A value of 00h will be decoded as 01h.

6.25 Fan Configuration 1 Registers

Table 6.31 Fan Configuration 1 Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
42h	R/W	Fan 1 Configuration 1	EN_ ALGO	RANGE[1:0]		EDGES[1:0]		UPDATE[2:0]			2Bh
82h	R/W	Fan 2 Configuration 1	EN_ ALGO	RANGE[1:0]		EDGES[1:0]		UPDATE[2:0]			2Bh

The Fan Configuration 1 Register controls the general operation of the RPM based Fan Speed Control Algorithm used for the Fan 1 driver.

Bit 7 - EN_ALGO - enables the RPM based Fan Speed Control Algorithm. This bit is set and cleared automatically when the LUT_LOCK bit is set based on the setting of the TACH / DRIVE bit (see Section 6.35). When the LUT_LOCK bit is cleared, then setting this bit will enable the FSC without using the Look Up Table.

- ‘0’ - (default) the control circuitry is disabled and the fan driver output is determined by the Fan Driver Setting Register.
- ‘1’ - the control circuitry is enabled and the Fan Driver output will be automatically updated to maintain the programmed fan speed as indicated by the TACH Target Register.

Bits 6- 5 - RANGE[1:0] - Adjusts the range of reported and programmed tachometer reading values. The RANGE bits determine the weighting of all TACH values (including the Valid TACH Count, TACH Target, and TACH reading) as shown in Table 6.32.

Table 6.32 Range Decode

RANGE[1:0]		REPORTED MINIMUM RPM	TACH COUNT MULTIPLIER
1	**0**		
0	0	500	1
0	1	1000 (default)	2
1	0	2000	4
1	1	4000	8

Bits 4-3 - EDGES[1:0] - determines the minimum number of edges that must be detected on the TACHx signal to determine a single rotation. A typical fan measured 5 edges (for a 2-pole fan). For more accurate tachometer measurement, the minimum number of edges measured may be increased.

Increasing the number of edges measured with respect to the number of poles of the fan will cause the TACH Reading registers to indicate a fan speed that is higher or lower than the actual speed. In order for the FSC Algorithm to operate correctly, the TACH Target must be updated by the user to accommodate this shift. The Effective Tach Multiplier shown in Table 6.33 is used as a direct multiplier term that is applied to the Actual RPM to achieve the Reported RPM. It should only be applied if the number of edges measured does not match the number of edges expected based on the number of poles of the fan (which is fixed for any given fan).

Contact SMSC for recommended settings when using fans with more or less than 2 poles.

Table 6.33 Minimum Edges for Fan Rotation

EDGES[1:0]		MINIMUM TACH EDGES	NUMBER OF FAN POLES	EFFECTIVE TACH MULTIPLIER (BASED ON 2 POLE FANS)
1	**0**			
0	0	3	1 pole	0.5
0	1	5	2 poles (default)	1
1	0	7	3 poles	1.5
1	1	9	4 poles	2

Bit 2-0 - UPDATE - determines the base time between fan driver updates. The Update Time, along with the Fan Step Register, is used to control the ramp rate of the drive response to provide a cleaner transition of the actual fan operation as the desired fan speed changes. The Update Time is set as shown in Table 6.34.

Table 6.34 Update Time

UPDATE[2:0]			UPDATE TIME
2	**1**	**0**	
0	0	0	100ms
0	0	1	200ms
0	1	0	300ms
0	1	1	400ms (default)
1	0	0	500ms
1	0	1	800ms
1	1	0	1200ms
1	1	1	1600ms

6.26 Fan Configuration 2 Registers

Table 6.35 Fan Configuration 1 Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
43h	R/W	Fan 1 Configuration 2	-	EN_ RRC1	GLITCH _EN1	DER_OPT1 [1:0]		ERR_RNG[1:0]		LOWD RIVE1	38h
83h	R/W	Fan 2 Configuration 2	-	EN_ RRC2	GLITCH _EN2	DER_OPT2 [1:0]		ERR_RNG[1:0]		LOWD RIVE2	38h

The Fan Configuration 2 Register controls the tachometer measurement and advanced features of the RPM based Fan Speed Control Algorithm.

Bit 6 - EN_RRCx - Enables ramp rate control when the corresponding fan driver is operated in the Direct Setting Mode or the Direct Setting with LUT mode.

- ‘0’ (default) - Ramp rate control is disabled. When the fan driver is operating in Direct Setting mode or Direct Setting with LUT mode, the fan setting will instantly transition to the next programmed setting.
- ‘1’ - Ramp rate control is enabled. When the fan driver is operating in Direct Setting mode or Direct Setting with LUT mode, the fan drive setting will follow the ramp rate controls as determined by the Fan Step and Update Time settings. The maximum fan drive setting step is capped at the Fan Step setting and is updated based on the Update Time as given by Table 6.34.

Bit 5 - GLITCH_ENx - Disables the low pass glitch filter that removes high frequency noise injected on the TACHx pin. If the LOWDRIVE bit is set, this bit is ignored and the filter is automatically disabled.

- ‘0’ - The glitch filter is disabled.
- ‘1’ (default) - The glitch filter is enabled.

Bits 4 - 3 - DER_OPTx[1:0] - Control some of the advanced options that affect the derivative portion of the RPM based Fan Speed Control Algorithm as shown in Table 6.36.

Table 6.36 Derivative Options

DER_OPTX[1:0]		OPERATION
1	**0**	
0	0	No derivative options used
0	1	Basic derivative. The derivative of the error from the current drive setting and the target is added to the iterative Fan Drive Register setting (in addition to proportional and integral terms)
1	0	Step derivative. The derivative of the error from the current drive setting and the target is added to the iterative Fan Drive Register setting and is not capped by the Fan Step Register.
1	1	Both the basic derivative and the step derivative are used effectively causing the derivative term to have double the effect of the derivative term (default).

Bit 2 - 1 - ERR_RNGx[1:0] - Control some of the advanced options that affect the error window. When the measured fan speed is within the programmed error window around the target speed, then the fan drive setting is not updated. The algorithm will continue to monitor the fan speed and calculate necessary drive setting changes based on the error, however these changes are ignored.

Table 6.37 Error Range Options

ERR_RNGX[1:0]		OPERATION
1	**0**	
0	0	0 RPM (default)
0	1	50 RPM
1	0	100 RPM
1	1	200 RPM

Bit 0 - LOWDRIVEx - Determines whether the tachometer measurement circuit will use the Tach Period Measurement method of fan speed measurement or the Tach Pulse Count Method of fan speed measurement. Setting this bit allows the use of low side fan drive circuits as shown in Figure 6.1 without requiring additional tachometer recovery circuitry.

- ‘0’ (default) - The tachometer signal must always be present when measuring the fan speed regardless of the measurement method.
- ‘1’ - Low side PWM drive circuits are supported and the tachometer signal does not need to be present at all times (which is common with such drive techniques). The tachometer measurement circuitry will use the Tach Pulse Count Method to determine the fan speed (contact SMSC for details on this operation). All tachometer related data is in the form of edge counts over a fixed time period. This method is significantly slower and the tachometer updates are non-continuous.

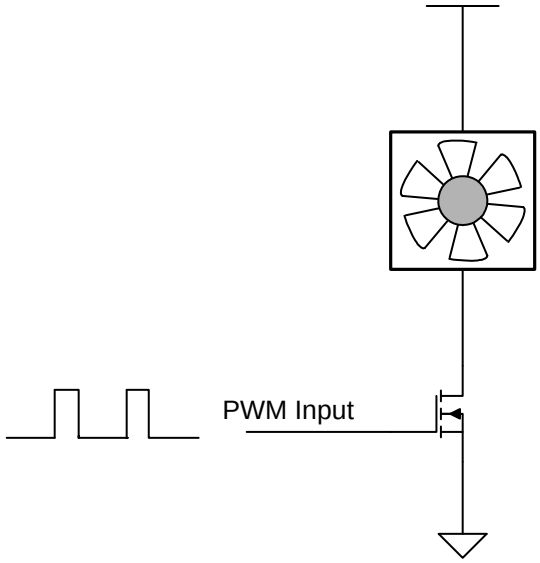


Figure 6.1 LOWDRIVE Supported Drive Circuit

6.27 Gain Registers

Table 6.38 Gain Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
45h	R/W	Gain 1 Register	-	-	GAIND[1:0]		GAINI[1:0]		GAINP[1:0]		2Ah
85h	R/W	Gain 2 Register	-	-	GAIND[1:0]		GAINI[1:0]		GAINP[1:0]		2Ah

The Gain Register stores the gain terms used by the proportional and integral portions of each of the RPM based Fan Speed Control Algorithms. These gain terms are used as the KD, KI, and KP gain terms in a classic PID control solution.

Table 6.39 Gain Decode

GAIND OR GAINP OR GAINI [1:0]		RESPECTIVE GAIN FACTOR
1	**0**	
0	0	1x
0	1	2x
1	0	4x (default)
1	1	8x

6.28 Fan Spin Up Configuration Registers

Table 6.40 Fan Spin Up Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
46h	R/W	Fan 1 Spin Up Configuration	DRIVE_FAIL _CNT1 [1:0]		NOK ICK1	SPIN_LVL[2:0]			SPINUP_TIM E [1:0]		0Dh
86h	R/W	Fan 2 Spin up Configuration	DRIVE_FAIL _CNT2 [1:0]		NOK ICK2	SPIN_LVL[2:0]			SPINUP_TIM E [1:0]		0Dh

The Fan Spin Up Configuration Register controls the settings of Spin Up Routine. The Fan Spin Up Configuration Register is software locked.

Bit 7 - 6 - DRIVE_FAIL_CNTx[1:0] - Determines how many update cycles are used for the Drive Fail detection function as shown in Table 6.41. This circuitry determines whether the fan can be driven to the desired tach target.

Table 6.41 DRIVE_FAIL_CNT[1:0] Bit Decode

DRIVE_FAIL_CNT[1:0]		NUMBER OF UPDATE PERIODS
1	0	
0	0	Disabled - the Drive Fail detection circuitry is disabled (default)
0	1	16 - the Drive Fail detection circuitry will count for 16 update periods
1	0	32 - the Drive Fail detection circuitry will count for 32 update periods
1	1	64 - the Drive Fail detection circuitry will count for 64 update periods

Bit 5 - NOKICKx - Determines if the Spin Up Routine will drive the fan to 100% duty cycle for 1/4 of the programmed spin up time before driving it at the programmed level.

- ‘0’ (default) - The Spin Up Routine will drive the fan driver to 100% for 1/4 of the programmed spin up time before reverting to the programmed spin level.
- ‘1’ - The Spin Up Routine will not drive the fan driver to 100%. It will set the drive at the programmed spin level for the entire duration of the programmed spin up time.

Bits 4 - 2 - SPIN_LVL[2:0] - Determines the final drive level that is used by the Spin Up Routine as shown in Table 6.42.

Table 6.42 Spin Level

SPIN_LVL[2:0]			SPIN UP DRIVE LEVEL
2	1	0	
0	0	0	30%
0	0	1	35%

Table 6.42 Spin Level (continued)

SPIN_LVL[2:0]			SPIN UP DRIVE LEVEL
2	**1**	**0**	
0	1	0	40%
0	1	1	45%
1	0	0	50%
1	0	1	55%
1	1	0	60% (default)
1	1	1	65%

Bit 1 -0 - SPINUP_TIME[1:0] - determines the maximum Spin Time that the Spin Up Routine will run for (see Section 6.9). If a valid tachometer measurement is not detected before the Spin Time has elapsed, then an interrupt will be generated. When the RPM based Fan Speed Control Algorithm is active, the fan driver will attempt to re-start the fan immediately after the end of the last spin up attempt.

The Spin Time is set as shown in Table 6.43.

Table 6.43 Spin Time

SPINUP_TIME[1:0]		TOTAL SPIN UP TIME
1	**0**	
0	0	250 ms
0	1	500 ms (default)
1	0	1 sec
1	1	2 sec

6.29 Fan Step Registers

Table 6.44 Fan Step Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
47h	R/W	Fan 1 Max Step	-	-	32	16	8	4	2	1	10h
87h	R/W	Fan 2 Max Step	-	-	32	16	8	4	2	1	10h

The Fan Step Registers, along with the Update Time, controls the ramp rate of the fan driver response calculated by the RPM based Fan Speed Control Algorithm. The value of the registers represents the maximum step size each fan driver will take between update times (see Section 6.25).

When the FSC algorithm is enabled, Ramp Rate control is automatically used. When the FSC is not active, then Ramp Rate control can be enabled by asserting the EN_RRC bit (see Section 6.26)

APPLICATION NOTE: The UPDATE bits and Fan Step Register settings operate independently of the RPM based Fan Speed Control Algorithm and will always limit the fan drive setting. That is, if the programmed fan drive setting (either in determined by the RPM based Fan Speed Control Algorithm, the Look Up Table, or by manual settings) exceeds the current fan drive setting by greater than the Fan Step Register setting, the EMC2106 will limit the fan drive change to the value of the Fan Step Register. It will use the Update Time to determine how often to update the drive settings.

APPLICATION NOTE: If the Fan Speed Control Algorithm is used, the default settings in the Fan Configuration 2 Register will cause the maximum fan step settings to be ignored.

The Fan Step Registers are software locked.

6.30 Fan Minimum Drive Registers

Table 6.45 Minimum Fan Drive Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
48h	R/W	Fan 1 Minimum Drive	128	64	32	16	8	4	2	1	66h (40%)
88h	R/W	Fan 2 Minimum Drive	128	64	32	16	8	4	2	1	66h (40%)

The Fan Minimum Drive Register stores the minimum drive setting for each RPM based Fan Speed Control Algorithm. The RPM based Fan Speed Control Algorithm will not drive the fan at a level lower than the minimum drive unless the target Fan Speed is set at FFh (see Section 6.33)

During normal operation, if the fan stops for any reason (including low drive), the RPM based Fan Speed Control Algorithm will attempt to restart the fan. Setting the Fan Minimum Drive Registers to a setting that will maintain fan operation is a useful way to avoid potential fan oscillations as the control circuitry attempts to drive it at a level that cannot support fan operation.

The Fan Minimum Drive Register is software locked.

6.31 Valid TACH Count Registers

Table 6.46 Valid TACH Count Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
49h	R/W	Valid TACH Count 1	4096	2048	1024	512	256	128	64	32	F5h
89h	R/W	Valid TACH Count 2	4096	2048	1024	512	256	128	64	32	F5h

The Valid TACH Count Register stores the maximum TACH Reading Register value to indicate that the each fan is spinning properly. The value is referenced at the end of the Spin Up Routine to determine if the fan has started operating and decide if the device needs to retry. See Equation [5] for translating the count to an RPM. This register is only used when the FSC is active.

If the TACH Reading Register value exceeds the Valid TACH Count Register (indicating that the Fan RPM is below the threshold set by this count), then a stalled fan is detected. In this condition, the algorithm will automatically begin its Spin Up Routine.

If a TACH Target setting is set above the Valid TACH Count setting, then that setting will be ignored and the algorithm will use the current fan drive setting.

The Valid TACH Count Register is software locked.

6.32 Fan Drive Fail Band Registers

Table 6.47 Fan Drive Fail Band Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Ah	R/W	Fan 1 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	00h
4Bh	R/W	Fan 1 Drive Fail Band High Byte	4096	2048	1024	512	256	128	64	32	00h
8Ah	R/W	Fan 2 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	00h
8Bh	R/W	Fan 2 Drive Fall Band High Byte	4096	2048	1024	512	256	128	64	32	00h

The Fan Drive Fail Band Registers store the number of tach counts used by the Fan Drive Fail detection circuitry. This circuitry is activated when the fan drive setting high byte is at FFh. When it is enabled, the actual measured fan speed is compared against the target fan speed. These registers are only used when the FSC is active.

This circuitry is used to indicate that the target fan speed at full drive is higher than the fan is actually capable of reaching. If the measured fan speed does not exceed the target fan speed minus the Fan Drive Fail Band Register settings for a period of time longer than set by the DRIVE_FAIL_CNTx[1:0] bits then the DRIVE_FAIL status bit will be set and an interrupt generated.

6.33 TACH Target Registers

Table 6.48 TACH Target Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Ch	R/W	TACH Target 1 Low Byte	16	8	4	2	1	-	-	-	F8h
4Dh	R/W	TACH Target 1 High Byte	4096	2048	1024	512	256	128	64	32	FFh
8Ch	R	TACH Target 2 Low Byte	16	8	4	2	1	-	-	-	F8h
8Dh	R/W	TACH Target 2 High Byte	4096	2048	1024	512	256	128	64	32	FFh

The TACH Target Registers hold the target tachometer value that is maintained each of the RPM based Fan Speed Control Algorithms.

The value in the TACH Target Registers will always reflect the current TACH Target value. If the Look Up Table is active and configured to operate in RPM Mode, then this register will be read only. Writing to this register will have no affect and the data will not be stored.

If one of the algorithms is enabled then setting the TACH Target Register to FFh will disable the fan driver (set the fan drive setting to 0%). Setting the TACH Target to any other value (from a setting of FFh) will cause the algorithm to invoke the Spin Up Routine after which it will function normally.

The Tach Target is not applied until the high byte is written. Once the high byte is written, the current value of both high and low bytes will be used as the next Tach target. 3

6.34 TACH Reading Registers

Table 6.49 TACH Reading Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Eh	R	Fan 1 TACH	4096	2048	1024	512	256	128	64	32	FFh
4Fh	R	Fan 1 TACH Low Byte	16	8	4	2	1	-	-	-	F8h
8Eh	R	Fan 2 TACH	4096	2048	1024	512	256	128	64	32	FFh
8Fh	R	Fan 2 TACH Low Byte	16	8	4	2	1	-	-	-	F8h

The TACH Reading Registers' contents describe the current tachometer reading for each of the fan. By default, the data represents the fan speed as the number of 32kHz clock periods that occur for a single revolution of the fan.

Equation [5] shows the detailed conversion from TACH measurement (COUNT) to RPM while Equation [6] shows the simplified translation of TACH Reading Register count to RPM assuming a 2-pole fan, measuring 5 edges, with a frequency of 32.768kHz. These equations are solved and tabulated for ease of use in AN17.4 RPM to TACH Counts Conversion.

Whenever the high byte register is read, the corresponding low byte data will be loaded to internal shadow registers so that when the low byte is read, the data will always coincide with the previously read high byte.

$$RPM = \frac{1}{(poles)} \times \frac{(n-1)}{COUNT \times \frac{1}{m}} \times f_{TACH} \times 60 \quad \textbf{[5]}$$

where:

poles = number of poles of the fan (typically 2)

f_{TACH} = the tachometer measurement frequency (typically 32.768kHz)

n = number of edges measured (typically 5 for a 2 pole fan)

m = the multiplier defined by the RANGe bits

$$RPM = \frac{3{,}932{,}160 \times m}{COUNT} \quad \textbf{[6]}$$

COUNT = TACH Reading Register value (in decimal)

6.35 Look Up Table Configuration Registers

Table 6.50 Look Up Table Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
50h	R/W	LUT 1 Configuration	USE_DTS_F1	USE_DTS_F2	LUT_LOCK	TACH / DRIVE	TEMP3_CFG [1:0]		TEMP4_CFG [1:0]		00h
90h	R/W	LUT2 Configuration	USE_DTS_F3	USE_DTS_F4	LUT_LOCK	TACH / DRIVE	TEMP3_CFG [1:0]		TEMP4_CFG [1:0]		00h

The Look Up Table Configuration Register holds the setup information for the two temperature to fan drive look up tables.

Bit 7 - USE_DTS_F1 or USE_DTS_F3 - This bit determines whether the Pushed Temperature 1 or Pushed Temperature 3 registers are using DTS data.

- ‘0’ (default) - The Pushed Temperature 1 or Pushed Temperature 3 registers are not using DTS data. The contents of these registers are standard 2’s complement temperature data.
- ‘1’ - The Pushed Temperature 1 or Pushed Temperature 3 registers are loaded with DTS data. The contents of these registers are automatically subtracted from a fixed value of 100°C before they are compared to the Look Up Table threshold levels.

Bit 6 - USE_DTS_F2 or USE_DTS_F4 - This bit determines whether the Pushed Temperature 2 or Pushed Temperature 4 Registers are using DTS data.

- ‘0’ (default) - The Pushed Temperature 2 or Pushed Temperature 4 registers are not using DTS data. The contents of these registers are standard 2’s complement temperature data.
- ‘1’ - The Pushed Temperature 2 or Pushed Temperature 4 registers are loaded with DTS data. The contents of these registers are automatically subtracted from a fixed value of 100°C before they are compared to the Look Up Table threshold levels.

Bit 5 - LUT_LOCK - This bit locks updating the Look Up Table entries and determines whether the look up table is being used.

- ‘0’ (default) - The Look Up Table entries can be updated normally. The Look Up Table will not be used while the Look Up Table entries are unlocked. During this condition, the fan drive output will not change states regardless of temperature or tachometer variation.

- '1' - The Look Up Table entries are locked and cannot be updated. The Look Up Table is fully active and will be used based on the loaded values. The fan drive output will be updated depending on the temperature and / or TACH variations.

APPLICATION NOTE: When the LUT_LOCK bit is set at a logic '0', the fan drive setting will be set at whatever value was last used by the RPM based Fan Speed Control Algorithm or the Look Up Table.

Bit 4 - TACH / DRIVEx - This bit selects the data format for the LUT drive settings.

- '0' (default) - The Look Up Table drive settings are RPM TACH count values for use by the RPM based Fan Speed Control Algorithm. The Look Up Table drive settings should be loaded highest value to lowest value (to coincide with the inversion between TACH counts and actual RPM).
- '1' - The Look Up Table drive settings are fan drive setting values and are used directly. The drive settings should be loaded lowest value to highest value.

APPLICATION NOTE: The TACH / DRIVE bit should be set prior to the LUT_LOCK bit being set so that, if the fan driver is disabled, the output drive is in the proper state.

Bits 3-2 - TEMP3_CFG[1:0] - These bits determine the temperature channel that is used for the Temperature 3 inputs to the Look Up Table as shown in Table 6.51.

Table 6.51 TEMP3_CFG Decode

TEMP3_CFG [1:0]		TEMPERATURE CHANNEL USED
1	**0**	
0	0	External Diode 3 (default)
0	1	TRIP_SET / VIN4 Voltage
1	0	Pushed Temperature 1 (LUT1) Pushed Temperature 3 (LUT2)
1	1	Reserved

Bits 1-0 - TEMP4_CFG[1:0] - These bits determine the temperature channel that is used for the Temperature 4 inputs to the Look Up Table as shown in Table 6.52.

Table 6.52 TEMP4_CFG Decode

TEMP4_CFG [1:0]		TEMPERATURE CHANNEL USED
1	**0**	
0	0	Internal Diode (default)
0	1	External Diode 4
1	0	Pushed Temperature 2 (LUT1) Pushed Temperature 4 (LUT2)
1	1	Reserved

APPLICATION NOTE: When any of the External Diode 1, External Diode 2, and External Diode 3 channels are configured to operate as voltage inputs, the voltage data is used in the Look Up Table instead of the corresponding temperature data. Therefore, the threshold settings must be updated accordingly. All voltage channels (including VIN1, VIN2, and VIN3) are assumed to be increasing (i.e. a larger voltage reading indicates a higher fan speed).

6.36 Look Up Table 1 Registers

Table 6.53 Look Up Table 1 Registers

ADDR	R/W	REGISTER	TACH / DRIVE	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
51h	R/W	LUT 1 Drive Setting 1	‘0’	4096	2048	1024	512	256	128	64	32	FBh
			‘1’	128	64	32	16	8	4	2	1	
52h	R/W	LUT 1 Ext Diode 1 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT 1 VIN1 Setting 1	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
53h	R/W	LUT 1 Ext Diode 2 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT 1 VIN2 Setting 1	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
54h	R/W	LUT 1 Temp 3 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT 1 Voltage 3 Setting 1	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
55h	R/W	LUT 1 Temp 4 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
...	...	...	...	...	...	...	...	...	...	...	...	.. .
74h	R/W	LUT 1 Drive Setting 8	‘0’	4096	2048	1024	512	256	128	64	32	92h
			‘1’	128	64	32	16	8	4	2	1	
75h	R/W	LUT 1 Ext Diode 1 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT 1 VIN1 Setting 8	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
76h	R/W	LUT 1 Ext Diode 2 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT 1 VIN2 Setting 8	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
77h	R/W	LUT 1 Temp 3 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT 1 Voltage 3 Setting 8	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)

Table 6.53 Look Up Table 1 Registers (continued)

ADDR	R/W	REGISTER	TACH / DRIVE	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
78h	R/W	LUT 1 Temp 4 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
79h	R/W	LUT 1 Temp Hysteresis	X	-	-	-	16	8	4	2	1	0Ah

The Look Up Table 1 Registers hold the 40 entries of the Look Up Table that controls the drive of Fan 1. As the temperature (or voltage) channels are updated, the measured value for each channel is compared against the respective entries in the Look Up Table and the associated drive setting is loaded into an internal shadow register and stored.

The bit weighting for temperature inputs represents °C and is compared against the measured data. Note that the LUT entry does not include a sign bit. The Look Up Table does not support negative temperature values and the MSBit should not be set for a temperature input.

The bit weighting for voltage inputs represents mV above 0V and is compared against the measured data.

Each temperature (or voltage) channel threshold shares the same hysteresis value. When the measured temperature for any of the channels meets or exceeds the programmed threshold, the drive setting associated with that threshold is used. The temperature must drop below the threshold minus the hysteresis value before the drive setting will be set to the previous value.

APPLICATION NOTE: For proper operation, the hysteresis must be smaller than the difference between two consecutive thresholds.

If the RPM based Fan Speed Control Algorithm is used, the TACH Target is updated after every conversion. It is always set to the minimum TACH Target that is stored by the Look Up Table. The fan drive setting cycle is updated based on the RPM based Fan Speed Control Algorithm configuration settings.

If the RPM based Fan Speed Control Algorithm is not used, then the fan drive setting is updated after every conversion. It is set to the maximum duty cycle that is stored by the Look Up Table.

6.37 Look Up Table 2 Registers

Table 6.54 Look Up Table2 Registers

ADDR	R/W	REGISTER	TACH / DRIVE	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
91h	R/W	LUT 2 Drive Setting 1	‘0’	4096	2048	1024	512	256	128	64	32	FBh
			‘1’	128	64	32	16	8	4	2	1	FBh
92h	R/W	LUT 2 Ext Diode 1 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT2 VIN1 Setting 1	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)

Table 6.54 Look Up Table2 Registers (continued)

ADDR	R/W	REGISTER	TACH / DRIVE	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
93h	R/W	LUT 2 Ext Diode 2 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT2 VIN2 Setting 1	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
94h	R/W	LUT 2 Temp 3 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT2 Voltage 3 Setting 1	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
95h	R/W	LUT2 Temp 4 Setting 1	X	-	64	32	16	8	4	2	1	7Fh (127°C)
...	...	...	...	...	...	...	...	...	...	...	...	...
B4h	R/W	LUT 2 Drive Setting 8	'0'	4096	2048	1024	512	256	128	64	32	92h
			'1'	128	64	32	16	8	4	2	1	
B5h	R/W	LUT 2 Ext Diode 1 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT2 VIN1 Setting 8	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
B6h	R/W	LUT 2 Ext Diode 2 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT2 VIN2 Setting 8	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
B7h	R/W	LUT 2 Temp 3 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
		LUT2 Voltage 3 Setting 8	X	752.9	376.5	188.2	94.12	47.06	23.53	11.76	5.88	7Fh (0.4V)
B8h	R/W	LUT2 Temp 4 Setting 8	X	-	64	32	16	8	4	2	1	7Fh (127°C)
B9h	R/W	LUT 2 Temp Hysteresis	X	-	-	-	16	8	4	2	1	0Ah

The Look Up Table 2 Registers hold the 40 entries of the Look Up Table that controls the drive of Fan 2. As the temperature (or voltage) channels are updated, the measured temperature for each channel is compared against the respective entries in the Look Up Table and the associated drive setting is loaded into an internal shadow register and stored.

6.38 Muxed Pin Configuration Register

Table 6.55 Muxed Pin Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E0h	R/W	Muxed Pin Config	PWM1 _EN	GPIO5 _CFG1	GPIO5_ CFG0	GPIO4_ CFG1	GPIO4 _CFG0	GPIO3 _CFG	GPIO2 _CFG	GPIO1 _CFG	01h

The Muxed Pin Configuration Register controls the pin function for all of the multiple function GPIO pins.

Bit 7 - PWM1_EN - Enables the OVERT1# / PWM1 pin as a PWM output.

- ‘0’ (default) - The OVERT1# / PWM1 pin acts as a dedicated interrupt pin for the External Diode 1 channel. All PWM1 controls will be ignored though can be updated normally.
- ‘1’ - The OVERT1# / PWM1 pin acts as a PWM output. The High Side Fan Driver will be disabled.

Bit 6 - 5 - GPIO5_CFG[1:0] - Determines the pin function for the OVERT3# / GPIO5 / PWM4 pin as shown in Table 6.56. When not configured as a PWM output, all PWM4 controls will be ignored though can be updated normally.

Table 6.56 GPIO5_CFG[1:0] Decode

GPIO5_CFG[1:0]		OVERT3# / GPIO5 / PWM4 PIN FUNCTION
1	**0**	
0	0	OVERT3# - the pin will act as a dedicated alert for the External Diode 2 channel (default)
0	1	GPIO - the pin will act as a GPIO
1	0	GPIO - the pin will act as a GPIO
1	1	PWM - the pin will act as a PWM output controlled by the PWM4 Setting Register

Bits 4 - 3 - GPIO4_CFG[1:0] - Determines the pin functions for the OVERT2# / GPIO4 / PWM3 pin as shown in Table 6.57. When not configured as an output, all PWM3 controls will be ignored though can be updated normally.

Table 6.57 GPIO4_CFG[1:0] Decode

GPIO4_CFG[1:0]		OVERT2# / GPIO4 / PWM3 PIN FUNCTION
1	**0**	
0	0	OVERT2# - the pin will act as a dedicated alert for the External Diode 2 channel (default)
0	1	GPIO - the pin will act as a GPIO
1	0	GPIO - the pin will act as a GPIO
1	1	PWM - the pin will act as a PWM output controlled by the PWM3 Setting Register

Bit 2 - GPIO3_CFG - Determines the pin function for the PWM2 / GPIO3 pin as well as the DAC2 pin.

- ‘0’ (default) - The PWM2/ GPIO3 pin functions as a PWM output for the 2nd the RPM based Fan Speed Control Algorithm (FSC). The Linear DAC Fan Driver is disabled and the DAC2 pin will be in a high impedance state.
- ‘1’ - The PWM2 / GPIO3 pin functions as a GPIO. The Linear DAC Fan Driver is enabled and driven by the 2nd RPM based Fan Speed Control Algorithm (FSC). All PWM2 controls will be ignored though are still writable via the SMBus.

Bit 1 - GPIO2_CFG - Determines the pin functions for the TACH2 / GPIO2 pin.

- ‘0’ (default) - The TACH2 / GPIO2 pin functions as a tachometer input for the 2nd the RPM based Fan Speed Control Algorithm (FSC).
- ‘1’ - The TACH2 / GPIO2 pin functions as a GPIO. When set, the EN_ALGO2 bit will automatically be set to ‘0’ and cannot be set.

Bit 0 - GPIO1_CFG - Determines the pin function for the CLK_IN / GPIO1 pin.

- ‘0’ - The CLK_IN / GPIO1 pin functions as a clock input for the RPM based Fan Speed Control Algorithm (FSC).
- ‘1’ (default) - The CLK_IN / GPIO1 pin functions as a GPIO.

6.39 GPIO Direction Register

Table 6.58 GPIO Direction Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E1h	R/W	GPIO Direction 1	-	-	GPIO 6_DIR	GPIO 5_DIR	GPIO 4_DIR	GPIO 3_DIR	GPIO 2_DIR	GPIO 1_DIR	00h

The GPIO Direction Register 1 controls the direction of GPIOs 1 through 6. When muxable pins are not configured as a GPIO ports the respective bits are ignored.

Bit 5 - 0 - GPIOx_DIR - Controls the input / output state of GPIOs. The bit is not used if the pin is not configured as a GPIO.

- ‘0’ (default) - The GPIO is configured as an input.
- ‘1’ - The GPIO is configured as an output.

6.40 GPIO / PWM Pin Output Configuration Register

Table 6.59 GPIO / PWM Pin Output Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E2	R/W	GPIO Output Config	-	PWM 1_OT	GPIO 6_OT	GPIO 5_OT	GPIO 4_OT	GPIO 3_OT	GPIO 2_OT	GPIO 1_OT	00h

The GPIO Output Configuration Register controls the output pin type of each GPIO pin. These settings apply to the pin if it is configured as a GPIO output or a PWM. These bits do not apply if the pin is configured as a DAC output or one of the three dedicated OVERTx pins (which are always open drain).

Bit 6 - PWM1_OT - Determines the output type for the PWM1 pin.

- ‘0’ (default) - The PWM1 output is configured as an open drain output (if enabled as a PWM output).
- ‘1’ - The PWM1 output is configured as a push-pull output (if enabled as an a PWM output).

Bit 5 - 0 - GPIOx_OT - Determines the output type for GPIOx.

- ‘0’ (default) - GPIOx is configured as an open drain output (if enabled as an output).
- ‘1’ - GPIOxis configured as a push-pull output (if enabled as an output).

6.41 GPIO Input Register

Table 6.60 GPIO Input Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E3h	R	GPIO Input	-	-	GPIO 6_IN	GPIO 5_IN	GPIO 4_IN	GPIO 3_IN	GPIO 2_IN	GPIO 1_IN	00h

The GPIO Input Register indicates the state of the corresponding GPIO pin regardless of the functionality of the pin (GPIO, PWM, or TACH) or the direction of the GPIO (input, push-pull output, open-drain output). When a GPIO is configured as an input, any change of state will assert the ALERT# pin (unless GPIO interrupts are masked, see Section 6.15).

6.42 GPIO Output Register

Table 6.61 GPIO Output Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E4h	R/W	GPIO Output 1	-	-	GPIO6_ OUT	GPIO5_ OUT	GPIO4_ OUT	GPIO3 _OUT	GPIO2 _OUT	GPIO1 _OUT	00h

The GPIO Output Register controls the state of the corresponding GPIO pins when they areconfigured as GPIOs and as outputs.

If the output is configured as an open-drain output, then it requires a pull-up resistor to VDD. Setting the corresponding bit to a ‘1’ will act to disable the output allowing the pull-up resistor to pull the output high. Setting the corresponding bit to a ‘0’ will enable the output and drive the pin to a logical ‘0’ state.

If the output is configured as a push-pull output, then output pin will immediately be driven to match the corresponding bit setting.

6.43 GPIO Interrupt Enable Register

Table 6.62 GPIO Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E5h	R/W	GPIO Interrupt Enable	-	-	GPIO6_ INT_EN	GPIO5_ INT_EN	GPIO4_ INT_EN	GPIO3_ INT_EN	GPIO2_ INT_EN	GPIO1_ INT_EN	00h

The GPIO Interrupt Enable Register enables the GPIOs to assert the ALERT pin when they change state. When the GPIO pins are disabled or configured as outputs, then these bits are ignored.

Bit 5 - 0 - GPIOx_INT_EN - Allows the ALERT# pin to be asserted when the GPIOx pin changes state (when configured as an input).

- ‘0’ (default) - The ALERT# pin will not be asserted when the GPIOx pin changes state (when configured as an input).
- ‘1’ - The ALERT# pin will be asserted when the GPIOxpin changes state (when configured as an input).

6.44 GPIO Status Register

Table 6.63 GPIO Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
E6h	R-C	GPIO Status	-	-	GPIO6_ STS	GPIO5_ STS	GPIO4_ STS	GPIO3_ STS	GPIO2_ STS	GPIO1_ STS	00h

The GPIO Status Register indicates which GPIO has changed states to cause the ALERT pins to be asserted. This register is cleared when it is read. The bits in this register are set whenever the corresponding GPIO changes states regardless if the ALERT pins are asserted. Once a bit is set, it will remain set until read.

If any bit in this register is set, then the GPIO status bit will be set.

Bit 5 - 0 - GPIOx_STS - Indicates that the GPIOx pin has changed states from a ‘0’ to a ‘1’ or a ‘1’ to a ‘0’ (when configured as a GPIO input).

6.45 Software Lock Register

Table 6.64 Software Lock Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
EFh	R/W	Software Lock	-	-	-	-	-	-	-	LOCK	00h

The Software Lock Register controls the software locking of critical registers. This register is software locked.

Bit 0 - LOCK - this bit acts on all registers that are designated SWL. When this bit is set, the locked registers become read only and cannot be updated.

- ‘0’ (default) - all SWL registers can be updated normally.
- ‘1’ - all SWL registers cannot be updated and a hard-reset is required to unlock them.

6.46 Product Features Register

Table 6.65 Product Features Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FCh	R	Product Features	-	-	-	-	-	-	SHDN_SEL[1:0]		00h

The Product Features Register indicates which pin selected functionality is enabled.

Bit 1 - 0 - SHDN_SEL[1:0] - Indicates what the detected pin state of the SHDN_SEL pin was and which functions are enabled.

Table 6.66 SHDN_SEL Bit Decode

FUN_SEL[1:0]		EXTERNAL DIODE 1 MODE	CRITICAL / THERMAL SHUTDOWN TEMPERATURE RANGE	VIN4 OR TRIP_SET
1	0			
0	0	Transistor mode - Beta = automatic REC = enabled	High range - 92°C to 154°C	TRIP_SET
0	1	Diode mode - Beta = 1111b REC = disabled	Low Range 60°C to 122°C	TRIP_SET
1	0	Not used - Internal diode linked to Hardware Thermal / Critical Shutdown circuitry	Low Range 60°C to 122°C	TRIP_SET or VIN4 (see Section 6.1.2)

6.47 Product ID Register

Table 6.67 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID Register	0	0	0	1	1	1	1	0	1Eh

The Product ID Register contains a unique 8 bit word that identifies the product.

6.48 Manufacturer ID Register

Table 6.68 Manufacturer ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	Manufacturer ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID Register contains a 8 bit word that identifies SMSC.

6.49 Revision Register

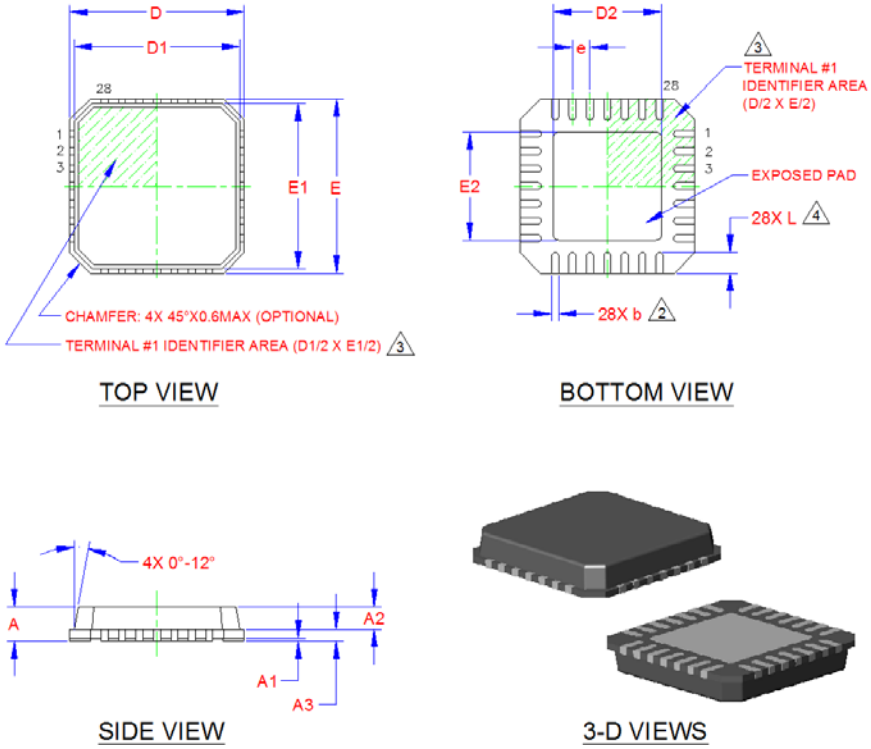
Table 6.69 Revision Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	0	0	0	0	0	0	1	0	02h

The Revision Register contains a 8 bit word that identifies the die revision.

Chapter 7 Package Drawing

7.1 QFN 28-Pin 5mm x 5mm



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	-	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	0.60	-	0.80	-	MOLD CAP THICKNESS
A3	0.20			-	LEADFRAME THICKNESS
D/E	4.85	5.00	5.15	-	X/Y BODY SIZE
D1/E1	4.55	-	4.95	-	X/Y MOLD CAP SIZE
D2/E2	SEE VARIATIONS			2	X/Y EXPOSED PAD SIZE
L	0.50	-	0.75	4	TERMINAL LENGTH
b	0.18	-	0.30	2	TERMINAL WIDTH
e	0.50 BSC			-	TERMINAL PITCH

D2/E2 VARIATIONS				
MIN	NOM	MAX	NOTE	CATALOG PART #
2.95	3.10	3.25	2	EMC2102

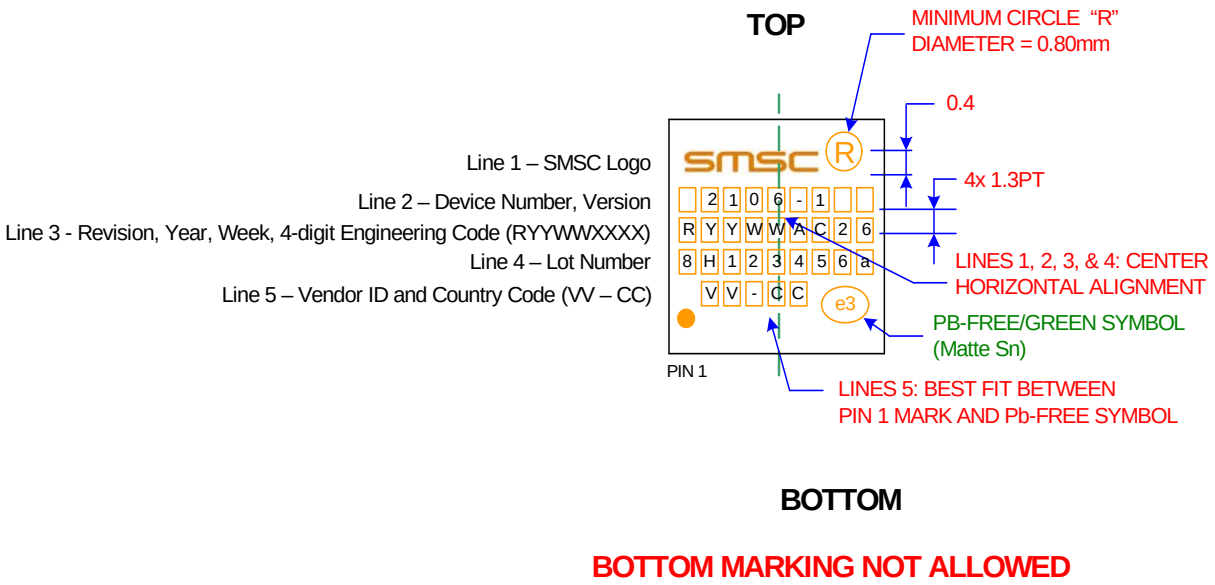
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.
4. ROUNDED INNER TIPS ON TERMINALS ARE OPTIONAL.

Figure 7.1 EMC2106 28-Pin 5x5mm QFN Package Outline and Parameters

7.2 Package Markings

All devices will be marked on the first line of the top side with “2106”. On the second line, they will be marked with the Functional Revision “C”, followed by “YWW-AC26”. On the third line, they will be marked with the Lot Number, and on the fourth line, they will be marked with the Vendor and Country Codes.



BOTTOM

BOTTOM MARKING NOT ALLOWED

Figure 7.2 EMC2106 Package Marking

Appendix A Thermistors

The EMC2106 can monitor thermistor inputs on the TRIP_SET / VIN4 as well as supporting a thermistor option on the all of the external diode pins pairs (DP1 / VREF_T1 and DN1 / VIN1,etc.). The Thermistors can be connected as shown in Figure A.1.

Figure A.1 is representative of one of the thermistor channels and will apply to DP1 / VREF_T1 and DN1 / VIN1, DP2 / VREF_T2 and DN2 / VIN2.

The top side resistor is internally integrated in the case of the TRIP_SET / VIN4 channel and the VREF voltage will not be brought out externally. The Thermistor should be connected in the same way as RSET.

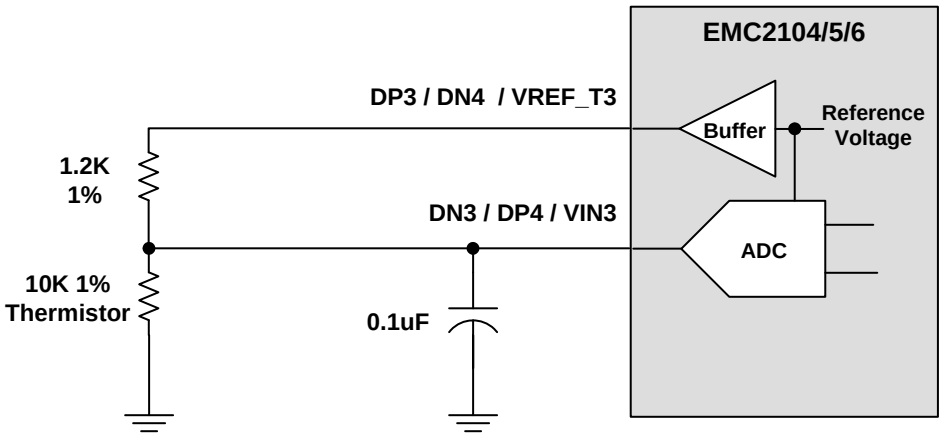


Figure A.1 "Low Side" Thermistor Connection

The relationship between voltage and temperature is roughly linear. the measured voltage by the EMC2106 will be inversely proportional to temperature .

Linearization methods can only accurately capture the temperature over a limited window of temperatures.

For a 10k Ohm type 3370 Thermistor and a 1.2k ohm ±1% setting resistor, the output response corresponding to a thermistor is tabulated in Table A.1.

If the INV_VINx bit is set then the results of the circuit (configured as shown in Figure A.1) is shown in Table A.2.

The EMC2106 does not perform any numerical calculations on the thermistor value if a thermistor is monitored on TRIP_SET / VIN4 pin. If the External Diode 1, External Diode 2, or External Diode 3 channels are configured to measure a thermistor, it must be configured as shown in Figure A.1.

When measuring a thermistor input with Fan Control Look Up Table, care must be taken that the temperature thresholds are entered as a unsigned voltage number that corresponds to the desired thermal threshold. Also note that the LUT assumes that the VIN1 and TRIP_SET / VIN4 voltage inputs are directly proportional to temperature.

A.1 Thermistor Look Up Tables

Table A.1 "Low Side" Thermistor Look Up Table

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-45	254	15	235	75	157	135	72
-44	253	16	235	76	155	136	71
-43	253	17	234	77	154	137	70
-42	253	18	233	78	152	138	69
-41	253	19	232	79	150	139	68
-40	253	20	231	80	148	140	67
-39	253	21	231	81	146	141	66
-38	253	22	230	82	145	142	65
-37	252	23	229	83	143	143	64
-36	252	24	228	84	141	144	63
-35	252	25	227	85	139	145	62
-34	252	26	226	86	138	146	61
-33	252	27	225	87	136	147	60
-32	252	28	224	88	135	148	59
-31	252	29	223	89	133	149	59
-30	252	30	222	90	131	150	58
-29	251	31	221	91	129	151	57
-28	251	32	220	92	128	152	56
-27	251	33	219	93	126	153	55
-26	251	34	218	94	124	154	54
-25	251	35	217	95	123	155	54
-24	251	36	216	96	121	156	53
-23	250	37	215	97	119	157	52
-22	250	38	213	98	118	158	51
-21	250	39	212	99	116	159	51
-20	250	40	211	100	114	160	50
-19	250	41	210	101	113	161	49
-18	249	42	208	102	111	162	48
-17	249	43	207	103	110	163	48
-16	249	44	206	104	108	164	47

Table A.1 "Low Side" Thermistor Look Up Table (continued)

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-15	249	45	205	105	106	165	46
-14	248	46	203	106	105	166	46
-13	248	47	202	107	103	167	45
-12	248	48	200	108	102	168	44
-11	247	49	199	109	100	169	44
-10	247	50	198	110	99	170	43
-9	247	51	196	111	97	171	43
-8	246	52	195	112	96	172	42
-7	246	53	193	113	95	173	41
-6	246	54	192	114	93	174	41
-5	245	55	190	115	92	175	40
-4	245	56	189	116	90	176	40
-3	245	57	187	117	89	177	39
-2	244	58	185	118	88	178	38
-1	244	59	184	119	86	179	38
0	243	60	182	120	85	180	37
1	243	61	181	121	84	181	37
2	243	62	179	122	82	182	36
3	242	63	177	123	81	183	36
4	242	64	176	124	80	184	35
5	241	65	174	125	79	185	35
6	241	66	172	126	82	186	34
7	240	67	171	127	81	187	34
8	240	68	169	128	80	188	33
9	239	69	167	129	78	189	33
10	238	70	166	130	77	190	32
11	238	71	164	131	76	191	32
12	237	72	162	132	75		
13	237	73	160	133	74		
14	236	74	159	134	73		

Table A.2 Inverted Thermistor Look Up Table

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-45	0	15	19	75	97	135	182
-44	1	16	20	76	99	136	183
-43	1	17	20	77	100	137	184
-42	1	18	21	78	102	138	185
-41	1	19	22	79	104	139	186
-40	1	20	23	80	106	140	187
-39	1	21	23	81	108	141	188
-38	1	22	24	82	109	142	189
-37	2	23	25	83	111	143	190
-36	2	24	26	84	113	144	191
-35	2	25	27	85	115	145	192
-34	2	26	28	86	116	146	193
-33	2	27	29	87	118	147	194
-32	2	28	30	88	120	148	195
-31	2	29	31	89	121	149	195
-30	2	30	32	90	123	150	196
-29	3	31	33	91	125	151	197
-28	3	32	34	92	126	152	198
-27	3	33	35	93	128	153	199
-26	3	34	36	94	130	154	200
-25	3	35	37	95	131	155	200
-24	3	36	38	96	133	156	201
-23	4	37	39	97	135	157	202
-22	4	38	41	98	136	158	203
-21	4	39	42	99	138	159	203
-20	4	40	43	100	140	160	204
-19	4	41	44	101	141	161	205
-18	5	42	46	102	143	162	206
-17	5	43	47	103	144	163	206
-16	5	44	48	104	146	164	207
-15	5	45	50	105	148	165	208

Table A.2 Inverted Thermistor Look Up Table (continued)

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-14	6	46	51	106	149	166	208
-13	6	47	52	107	151	167	209
-12	6	48	54	108	152	168	210
-11	7	49	55	109	154	169	210
-10	7	50	56	110	155	170	211
-9	7	51	58	111	157	171	211
-8	8	52	59	112	158	172	212
-7	8	53	61	113	159	173	213
-6	8	54	62	114	161	174	213
-5	9	55	64	115	162	175	214
-4	9	56	65	116	164	176	214
-3	9	57	67	117	165	177	215
-2	10	58	69	118	166	178	216
-1	10	59	70	119	168	179	216
0	11	60	72	120	169	180	217
1	11	61	73	121	170	181	217
2	11	62	75	122	172	182	218
3	12	63	77	123	173	183	218
4	12	64	78	124	174	184	219
5	13	65	80	125	175	185	219
6	13	66	82	126	172	186	220
7	14	67	83	127	173	187	220
8	15	68	85	128	174	188	221
9	15	69	87	129	176	189	221
10	16	70	88	130	177	190	222
11	16	71	90	131	178	191	222
12	17	72	92	132	179		
13	18	73	94	133	180		
14	18	74	95	134	181		

Appendix B Look Up Table Operation

The EMC2106 uses a look-up table to apply a user-programmable fan control profile based on measured temperature to each fan driver. In this look-up table, each temperature channel is allowed to control the fan drive output independently (or jointly) by programming up to eight pairs of temperature and drive setting entries.

The user programs the look-up table based on the desired operation. If the RPM based Fan Speed Control Algorithm is to be used (see Section 6.6), then the user must program an RPM target for each temperature setting of interest. Alternately, if the RPM based Fan Speed Control Algorithm is not to be used, then the user must program a drive setting for each temperature setting of interest.

If the measured temperature on the External Diode channel meets or exceeds any of the temperature thresholds for any of the channels, the fan output will be automatically set to the desired setting corresponding to the exceeded temperature. In cases where multiple temperature channel thresholds are exceeded, the highest fan drive setting will take precedence.

When the measured temperature drops to a point below a lower threshold minus the hysteresis value, the fan output will be set to the corresponding lower set point.

The following sections show examples of how the Look Up Table is used and configured. Each Look Up Table Example uses the Fan 1 Look Up Table Registers configured as shown in Table B.1.

Table B.1 Look Up Table Format

STEP	TEMP 1	TEMP 2	TEMP 3	TEMP 4	LUT DRIVE
1	LUT Temp 1 Setting 1 (52h)	LUT Temp 2 Setting 1 (53h)	LUT Temp 3 Setting 1 (54h)	LUT Temp 4 Setting 1 (55h)	LUT Drive Setting 1 (51h)
2	LUT Temp 1 Setting 2 (57h)	LUT Temp 2 Setting 2 (58h)	LUT Temp 3 Setting 2 (59h)	LUT Temp 4 Setting 2 (5Ah)	LUT Drive Setting 2 (56h)
3	LUT Temp 1 Setting 3 (5Ch)	LUT Temp 2 Setting 3 (5Dh)	LUT Temp 3 Setting 3 (5Eh)	LUT Temp 4 Setting 3 (5Fh)	LUT Drive Setting 3 (5Bh)
4	LUT Temp 1 Setting 4 (61h)	LUT Temp 2 Setting 4 (62h)	LUT Temp 3 Setting 4 (63h)	LUT Temp 4 Setting 4 (64h)	LUT Drive Setting 4 (60h)
5	LUT Temp 1 Setting 5 (66h)	LUT Temp 2 Setting 5 (67h)	LUT Temp 3 Setting 5 (68h)	LUT Temp 4 Setting 5 (69h)	LUT Drive Setting 5 (65h)
6	LUT Temp 1 Setting 6 (6Bh)	LUT Temp 2 Setting 6 (6Ch)	LUT Temp 3 Setting 6 (6Dh)	LUT Temp 4 Setting 6 (6Eh)	LUT Drive Setting 6 (6Ah)
7	LUT Temp 1 Setting 7 (70h)	LUT Temp 2 Setting 7 (71h)	LUT Temp 3 Setting 7 (72h)	LUT Temp 4 Setting 7 (73h)	LUT Drive Setting 7 (6Fh)
8	LUT Temp 1 Setting 8 (75h)	LUT Temp 2 Setting 8 (76h)	LUT Temp 3 Setting 8 (77h)	LUT Temp 4 Setting 8 (78h)	LUT Drive Setting 8 (74h)

B.1 Example #1

This example does not use the RPM based Fan Speed Control Algorithm. Instead, the Look Up Table is configured to directly set a fan drive setting based on the temperature of four of its measured inputs. The configuration is set as shown in Table B.2.

Once configured, the Look Up Table is loaded as shown in Table B.3. Table B.3 shows three temperature configurations using the settings in Table B.3 and the final fan drive setting that the Look Up Table will select.

Table B.2 Look Up Table Example #1 Configuration

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	SETTING
50h	LUT 1 Configuration	USE_DTS_F1	USE_DTS_F2	LUT_LOCK	TACH / DRIVE	TEMP3_CFG [1:0]		TEMP4_CFG [1:0]		C0h
		0	0	1	1	0	0	0	0	

B.1.1 LUT Configuration Bit Description

Bit 7 - USE_DTS_F1 = ‘0b’ tells the circuitry that the Forced Temperature 1 register data is not in DTS format.

Bit 6 - USE_DTS_F2 = ‘0b’ tells the circuitry that the Forced Temperature 2 register data is not in DTS format.

Bit 5 - LUT_LOCK = ‘1b’ tells the circuitry that the LUT is programmed and is active. This bit must be set for the LUT to function.

Bit 4 - TACH / DRIVE = ‘1b’ tells the Look Up Table that the FSC algorithm is not used and that the LUT target values will be PWM drive settings instead of TACH Target settings.

Bits 3- 2 - TEMP3_CFG = ‘00b’ tells the LUT to reference the External Diode 3 data instead of Forced Temperature 1 data or the TRIP_SET / VIN4 voltage data. This is the default setting.

Bit 0 - TEMP4_CFG = ‘0b’ tells the LUT to reference the Internal Diode data instead of Forced Temperature 2 data or the External Diode 4 temperature data. This is the default setting.

Table B.3 Fan Speed Control Table Example #1

FAN SPEED STEP #	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	EXTERNAL DIODE 3 TEMPERATURE (SKIN)	INTERNAL DIODE TEMPERATURE (AMBIENT)	FAN DRIVE SETTINGS
1	35°C	60°C	30°C	40°C	0%
2	40°C	70°C	35°C	45°C	30%
3	50°C	75°C	40°C	50°C	40%
4	60°C	80°C	45°C	55°C	50%
5	70°C	85°C	50°C	60°C	60%
6	80°C	90°C	55°C	65°C	70%
7	90°C	95°C	60°C	70°C	80%
8	100°C	100°C	65°C	75°C	100%

Note: The values shown in Table B.3 are example settings. All the cells in the look-up table are programmable via SMBus.

Table B.4 Fan Speed Determination for Example #1 (using settings in Table B.3)

	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	EXTERNAL DIODE 3 TEMPERATURE (SKIN)	INTERNAL DIODE TEMPERATURE (AMBIENT)	FAN DRIVE SETTING RESULT
Example 1:	**82°C**	82°C	48°C	58°C	70% (CPU temp requires highest drive)
Example 2:	82C°	**97°C**	**62°C**	58°C	80% (GPU and Skin require highest drive)
Example 3:	82°C	97°C	62°C	**75°C**	100% (Internal temp requires highest drive)

B.2 Example #2

This example uses the RPM based Fan Speed Control Algorithm. The Spin Level (used by the Spin Up Routine) should be changed to 50% drive for a total Spin Time of 1 second. For all other RPM configuration settings, the default conditions are used.

For control inputs, it uses the External Diode 1 channel normally, a thermistor input on the External Diode 2 channel, the internal diode channel, and a Pushed Temperature that represents the MCU temperature in standard format. The configuration is set as shown in Table B.5 while Table B.6 shows how the table is loaded.

Note that when using Thermistor data, the VIN2_INV bit should be set. The circuitry will automatically subtract the measured thermistor voltage from a quantity of FFh (effectively inverting it). Therefore, the Look Up Table is loaded with ascending voltage thresholds with respect to the drive settings. Additionally, the reading register will show this same value (subtracted from FFh).

Table B.5 Look Up Table Example #2 Configuration

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	SETTING
22h	Configuration 3	-	VIN4_INV	VIN3_EN	VIN3_INV	VIN2_EN	VIN2_INV	VIN1_EN	VIN1_INV	0Ch
		-	0	0	0	1	1	0	0	
42h	Fan 1 Configuration 1	EN_ALGO	RANGE[1:0]		EDGES[1:0]		UPDATE[2:0]			ABh
		1	0	1	0	1	0	1	1	
46h	Fan 1 Spin Up Configuration	DRIVE_FAIL_CNT 1 [1:0]		NOKICK 1	SPIN_LVL[2:0]			SPINUP_TIME [1:0]		0Ah
		0	0	0	0	1	0	1	0	
50h	LUT 1 Configuration	USE_DTS_F1	USE_DTS_F2	LUT_LOCK	TACH / DRIVE	TEMP3_CFG [1:0]		TEMP4_CFG [1:0]		28h
		0	0	1	0	1	0	0	0	

B.2.1 Configuration 3 Bit Description

Bit 6 - VIN4_INV = ‘0b’ tells the circuitry that the VIN4 voltage is not inverted and will be asscending (i.e. a value of 7Fh will represent a larger value than a value of 30h) If used by the LUT, no special processing needs to be done. This is the default setting.

Bit 5 - VIN3_EN = ‘0b’ tells the circuitry that the VIN3 voltage is not measured. The External Diode 3 pins will measure the External Diode 3 temperature. This is the default setting.

Bit 4 - VIN3_INV = ‘0b’ tells the circuitry that the VIN3 voltage is not inverted. This bit is ignored because VIN3_EN = ‘0b’. This is the default setting

Bit 3 - VIN2_EN = ‘1b’ tells the circuitry that the External Diode 2 pins (DP2 and DN2) will measure the VIN2 voltage and will not measure the External Diode 2 temperature. This voltage will automatically be used by the LUT.

Bit 2 - VIN2_INV = ‘1b’ tells the circuitry that the VIN2 voltage should be inverted. This means that prior to any limit comparasions (via the high / low limits or the LUT), the measured value will be subtracted from a value of FFh.

Bit 1 - VIN1_EN = ‘0b’ tells the circuitry that the VIN1 voltage is not measrued. The External Diode 1 pins (DP1 and DN1) will measure the External Diode 1 temperature and will be used by the LUT. This is the default setting.

Bit 0 - VIN1_INV = ‘0b’ tells the circuitry that the VIN1 voltage is not inverted. This bit is ignored because VIN1_EN = ‘0b’. This is the defautl setting.

B.2.2 Fan Configuration 1 Bit Description

Bit 7 - EN-ALGO = ‘1b’ tells the circuitry that the FSC alogrithm is active.

Bits 6 - 5 - RANGE[1:0] = ‘01b’ tells the FSC that the expected minimum RPM is 1000. This is the defautl setting.

Bits 4-3 - EDGES[1:0] = ‘01b’ tells the FSC that the fan is a 2-pole fan generating tach edges per rotation. This is the defautl setting.

Bits 2 - 0 - UPDATE[2:0] = ‘011b’ tells the FSC to update the fan drive every 400ms. This is the default setting.

B.2.3 Fan Spin Up Configuration Bit Description

Bits 7-6 - DRIVE_FAIL_CNT[1:0] = ‘00b’ tells the circuitry that the drive fail detection circuitry is not enabled. This is the default setting.

Bit 5 - NOKICK = ‘0b’ tells the circuitry that if than Spin Up Routine is invoked, it will drive to 100% duty cycle for 25% of the spin up time. This is the default setting.

Bits 4-2 - SPIN_LVL[2:0] = ‘010b’ tells the circuitry that if the Spin Up Routine is invoked, it should run at 40% drive.

Bits 1-0 - SPINUP_TIME[1:0] = ‘10b’ tells the circuitry that if the Spin Up Routine is invoked, it will run at 100% duty cycle for 250ms and at 40% duty cycle for 750ms for a total spin up time of 1s.

B.2.4 LUT Configuration - Bit Description

7 - USE_DTS_F1 = ‘0b’ tells the circuitry that the data in the Pushed Temperature 1 register is in normal format.

Bit 6 - USE_DTS_F2 = ‘0b’ tells the circuitry that the data in the Pushed Temperature 2 register is in normal format.

Bit 5 - LUT_LOCK = ‘1b’ tells the circuitry that the LUT is programmed and is active. This bit must be set for the LUT to function.

Bit 4 -TACH / DRIVE = ‘0b’ tells the LUT circuitry that the FSC algorithm is active and that the LUT values are TACH Target settings. This is the default setting.

Bits 3-2 - TEMP3_CFG = ‘10’b tells the Look Up Table to reference the Forced Temperature 1 data instead of the External Diode 3 data or the TRIP_SET / VIN4 data.

Bits 1- 0- TEMP4_CFG = ‘00b’ tells the Look Up Table to reference the Internal Temperature data instead of the External Diode 4 data or the Forced Temperature 2 data.

Table B.6 Fan Speed Control Table Example #2

FAN SPEED STEP #	EXTERNAL DIODE 1 TEMPERATURE (CPU)	THERMISTOR 2 VOLTAGE READING	PUSHED TEMPERATURE SETTING	INTERNAL DIODE TEMPERATURE (AMBIENT)	TACH TARGET
1	35°C	156.25mV (45°C)	30°C	40°C	EFh (1028 RPM)
2	40°C	178.125mV (50°C)	35°C	45°C	A3h (1508 RPM)
3	50°C	203.125mV (55°C)	40°C	50°C	7Ah (2014 RPM)
4	60°C	228.125mV (60°C)	45°C	55°C	62h (2508 RPM)
5	70°C	253.125mV (65°C)	50°C	60°C	52h (2997 RPM)
6	80°C	278.125mV (70°C)	55°C	65°C	3Dh (4029 RPM)
7	90°C	306.25mV (75°C)	60°C	70°C	31h (5016 RPM)
8	100°C	334.375mV (80°C)	65°C	75°C	29h (5994 RPM)

Note: The values shown in Table B.6 are example settings. All the cells in the look-up table are programmable via SMBus.

Table B.7 Fan Speed Determination for Example #2 (using settings in Table B.6)

	EXTERNAL DIODE 1 TEMPERATURE (CPU)	THERMISTOR 2 VOLTAGE READING	PUSHED TEMPERATURE	INTERNAL DIODE TEMPERATURE (AMBIENT)	FAN DRIVE SETTING RESULT
Example 1:	**75°C**	140.375mV	48°C	58°C	52h (2997 RPM) - CPU requires highest target
Example 2:	75°C	**310mV**	58°C	58°C	31h (5016 RPM) Thermistor requires highest target

Table B.7 Fan Speed Determination for Example #2 (using settings in Table B.6)

	EXTERNAL DIODE 1 TEMPERATURE (CPU)	THERMISTOR 2 VOLTAGE READING	PUSHED TEMPERATURE	INTERNAL DIODE TEMPERATURE (AMBIENT)	FAN DRIVE SETTING RESULT
Example 3:	75°C	235.125mV	**62°C**	58°C	31h (5016 RPM) Pushed Temperature requires highest target

B.3 Example #3

This example uses the RPM based Fan Speed Control Algorithm. The Spin Level (used by the Spin Up Routine) should be changed to 50% drive for a total Spin Time of 1 second. For all other RPM configuration settings, the default conditions are used.

For control inputs, it uses the External Diode 1 channel normally, the External Diode 2 channel normally, and both Pushed Temperature registers in DTS format. The configuration is set as shown in Table B.8 while Table B.9 shows how the table is loaded.

Note that when using DTS data, the USE_DTS_F1 and / or USE_DTS_F2 bits should be set. The Pushed Temperature Registers are loaded with the normal DTS values as received by the processor. When the DTS value is used by the Look Up Table, the value that is stored in the Pushed Temperature Register is subtracted from a fixed temperature of 100°C.

This resultant value is then compared against the Look Up Table thresholds normally. When programming the Look Up Table, it is necessary to take this translation into account else incorrect settings may be selected.

Table B.8 Look Up Table Example #3 Configuration

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	SETTING
42h	Fan 1 Configuration 1	EN_ ALGO	RANGE[1:0]		EDGES[1:0]		UPDATE[2:0]			ABh
		1	0	1	0	1	0	1	1	
46h	Fan 1 Spin Up Configuration	DRIVE_FAIL_CNT 1 [1:0]		NOKICK 1	SPIN_LVL[2:0]			SPINUP_TIME [1:0]		0Ah
		0	0	0	0	1	0	1	0	
50h	LUT 1 Configuration	USE_D TS_F1	USE_D TS_F2	LUT_LO CK	TACH / DRIVE	TEMP3_CFG [1:0]		TEMP4_CFG [1:0]		EAh
		1	1	1	0	1	0	1	0	

B.3.1 Fan Configuration 1 Bit Description

Bit 7 - EN-ALGO = ‘1b’ tells the circuitry that the FSC alogrithm is active.

Bits 6 - 5 - RANGE[1:0] = ‘01b’ tells the FSC that the expected minimum RPM is 1000. This is the defautl setting.

Bits 4-3 - EDGES[1:0] = ‘01b’ tells the FSC that the fan is a 2-pole fan generating tach edges per rotation. This is the defautl setting.

Bits 2 - 0 - UPDATE[2:0] = ‘011b’ tells the FSC to update the fan drive every 400ms. This is the default setting.

B.3.2 Fan Spin Up Configuration Bit Description

Bits 7-6 - DRIVE_FAIL_CNT[1:0] = ‘00b’ tells the circuitry that the drive fail detection circuitry is not enabled. This is the default setting.

Bit 5 - NOKICK = ‘0b’ tells the circuitry that if than Spin Up Routine is invoked, it will drive to 100% duty cycle for 25% of the spin up time. This is the default setting.

Bits 4-2 - SPIN_LVL[2:0] = ‘010b’ tells the circuitry that if the Spin Up Routine is invoked, it should run at 40% drive.

Bits 1-0 - SPINUP_TIME[1:0] = ‘10b’ tells the circuitry that if the Spin Up Routine is invoked, it will run at 100% duty cycle for 250ms and at 40% duty cycle for 750ms for a total spin up time of 1s.

B.3.3 LUT Configuration - Bit Description

Bit 7 - USE_DTS_F1 = ‘1b’ tells the circuitry that the data in the Pushed Temperature 1 register is in DTS format which means that the value in the register is equal to 100C - CPU Temp.

Bit 6 - USE_DTS_F2 = ‘1b’ tells the circuitry that the data in the Pushed Temperature 2 register is in DTS format which means that the value in the register is equal to 100°C - CPU temp.

Bit 5 - LUT_LOCK = ‘1b’ tells the circuitry that the LUT is programmed and is active. This bit must be set for the LUT to function.

Bit 4 -TACH / DRIVE = ‘0b’ tells the LUT circuitry that the FSC algorithm is active and that the LUT values are TACH Target settings. This is the default setting.

Bits 3-2 - TEMP3_CFG = ‘10’b tells the Look Up Table to reference the Forced Temperature 1 data instead of the External Diode 3 data or the TRIP_SET / VIN4 data.

Bits 1- 0- TEMP4_CFG = ‘10b’ tells the Look Up Table to reference the Forced Temeprature 2 data instead of the Internal Diode data or the External Diode 4 data.

Table B.9 Fan Speed Control Table Example #3

FAN SPEED STEP #	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	PUSHED TEMPERATURE SETTING (DTS1)	PUSHED TEMPERATURE SETTING (DTS2)	TACH TARGET
1	35°C	65°C	50°C	40°C	EFh (1028 RPM)
2	40°C	75°C	55°C	45°C	A3h (1508 RPM)
3	50°C	85°C	60°C	50°C	7Ah (2014 RPM)
4	60°C	90°C	65°C	55°C	62h (2508 RPM)
5	70°C	95°C	70°C	60°C	52h (2997 RPM)
6	80°C	100°C	75°C	65°C	3Dh (4029 RPM)

Table B.9 Fan Speed Control Table Example #3 (continued)

FAN SPEED STEP #	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	PUSHED TEMPERATURE SETTING (DTS1)	PUSHED TEMPERATURE SETTING (DTS2)	TACH TARGET
7	90°C	105°C	80°C	80°C	31h (5016 RPM)
8	100°C	110°C	85°C	100°C	29h (5994 RPM)

Note: The values shown in Table B.9 are example settings. All the cells in the look-up table are programmable via SMBus.

Table B.10 Fan Speed Determination for Example #3 (using settings in Table B.9)

	EXTERNAL DIODE 1 TEMPERATURE (CPU)	EXTERNAL DIODE 2 TEMPERATURE (GPU)	PUSHED TEMPERATURE (DTS1)	PUSHED TEMPERATURE (DTS2)	FAN DRIVE SETTING RESULT
Example 1:	**75°C**	75°C	35°C (translated as 65°C)	50°C (translated as 50°C)	52h (2997 RPM) - CPU requires highest target
Example 2:	75°C	90°C	**15°C (translated as 85°C)**	20°C (translated as 80°C)	29h (5994 RPM) - DTS1 requires highest target
Example 3:	75°C	97.25°C	30°C (translated as 70°C)	**23°C (translated as 77°C)**	3Dh (40296 RPM) - DTS2 requires highest target

Chapter 8 Revision History

Table 8.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.78 (04-21-09)	Table 3.2, "Electrical Specifications"	Added electrical specs for SMbus delay and time to first conversion
	Section 7.2, "Package Markings"	Added figures for package markings
Rev. 1.77 (03-16-09)	RPM Appendix	Removed this appendix to consolidate information in application note
Rev. 1.76 (03-11-09)	Section 6.34, "TACH Reading Registers"	Added reference to application note AN17.4
Rev. 1.75 (03-06-09)	Appendix B "Look Up Table Operation"	Updated entire section - examples were incorrect for RPM values and fleshed out bit descriptions

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Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А