# SY88236L/AL

## 2.5Gbps Burst Mode Laser Driver with Integrated Limiting Amplifier

## General Description

The SY88236L is a single supply 3.3V integrated burst mode laser driver and post amplifier for A-PON, B-PON, EPON, GE-PON, and G-PON applications with data rates from 155Mbps up to 2.5Gbps. The driver can deliver modulation current up to 85mA, and provides a high compliance voltage that makes it suitable for high-current operation with the laser DC-coupled to it. The post amplifier can detect signals with amplitude as low as $5mV_{PP}$.

The SY88236AL is a version of the SY88236L without 50Ω termination resistors at the inputs of the driver and the post amplifier. The SY88236AL is to be used specially in SFF modules mounted on ONU mother boards which have preinstalled terminations. Removing post amplifier input terminations will allow for receiver gain control.

All support documentation can be found on Micrel's web site at: www.micrel.com.

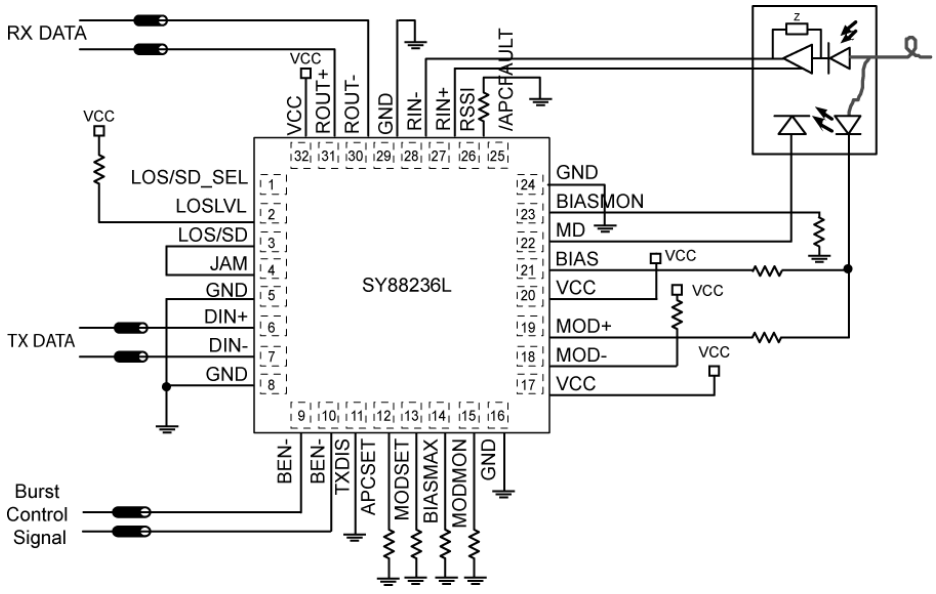
## Features

- 2.4V minimum laser compliance voltage
- Operation up to 2.5Gbps
- Fast burst mode enable/disable delay
- Modulation current up to 85mA
- Bias current up to 70mA
- Infinite bias current hold time between bursts
- Bias, Modulation, and power monitoring
- High input sensitivity post amplifier, $5mV_{PP}$
- Programmable LOS level
- Available in 32-pin (5mm x 5mm) QFN package

## Applications

- Multi-rate burst mode applications: A-PON, B-PON, G-PON, E-PON, GE-PON

## Typical Application



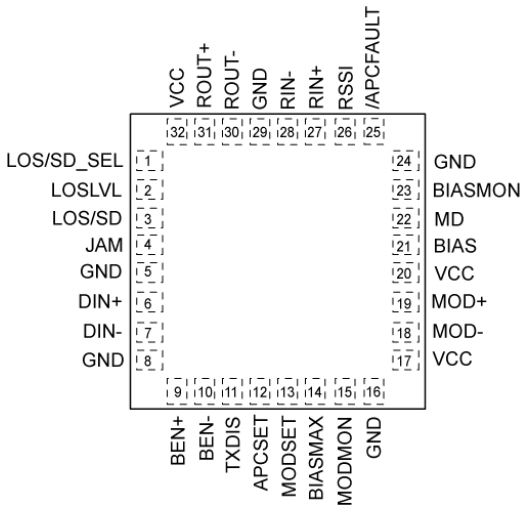
## Ordering Information[1]

| Part Number | Voltage | Temperature Range | Package Type | Package Marking | Lead Finish |
|---|---|---|---|---|---|
| SY88236LMG | 3.3V | –40° to +85°C | QFN-32 | SY88236L with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY88236LMGTR[2] | 3.3V | –40° to +85°C | QFN-32 | SY88236L with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY88236ALMG | 3.3V | –40° to +85°C | QFN-32 | SY88236A with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY88236ALMGTR[2] | 3.3V | –40° to +85°C | QFN-32 | SY88236A with Pb-Free bar-line indicator | NiPdAu Pb-Free |

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at $T_A$ = +25°C, DC Electricals only.
2. Tape and Reel.

## Pin Configuration




**32-Pin QFN**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1 | LOS/SD_SEL | LOS or SD selection, TTL input. Set high, connect to VCC, or leave open to select LOS. Set low or connect to GND to select SD. |
| 2 | LOSLVL | Loss-of-Signal Level Set. A resistor from this pin to $V_{CC}$ sets the threshold for the data input amplitude at which LOS will be asserted. |
| 3 | LOS/SD | Loss-of-Signal (LOS selected): asserts high when the data input amplitude falls below the threshold set by $LOS_{LVL}$.<br>Signal Detect (SD selected): asserts low when the data input amplitude falls below the threshold set by $LOS_{LVL}$. |
| 4 | JAM | Active low TTL/CMOS. Internally pulled-up with 75kΩ. Connect to GND or apply a low level signal (<0.8 V) to enable the post amp output. Can be shorted to LOS/SD (pin 3) to create a squelch function. The polarity of this input follows the polarity of LOS/SD. |
| 6 | DIN+ | SY88236L: Driver Non-inverting input data. Internally terminated with 50 Ω to a reference voltage. |
| | | SY88236AL: Driver Non-inverting input data. No internal termination. |
| 7 | DIN- | SY88236L: Driver inverting input data. Internally terminated with 50 Ω to a reference voltage. |
| | | SY88236AL: Driver inverting input data. No internal termination. |
| 9 | BEN+ | Non-Inverting burst enable. Accepts any input, single-ended or differential: TTL/CMOS, LVPECL, CML, LVDS, and HSTL. BEN requires an external termination. See Figure 2-a-d. |
| 10 | BEN- | Inverting burst enable. Accepts any input, single-ended or differential: TTL/CMOS, LVPECL, CML, LVDS, and HSTL. BEN requires an external termination. See Figure 2-a-d. |
| 11 | TXDIS | Internally pulled-up. Pull-down with a 22kΩ or lower resistance or apply a low level signal (<0.8 V) to enable bias and modulation. Keep floating or apply a high level (>2V) to disable bias and modulation. |

## Pin Description (continued)

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 12 | APCSET | Bias current setting and control. The bias current is set by installing an external resistor from this pin to ground or using a current source. Connect a 50kΩ resistor to GND for open loop operation. |
| 13 | MODSET | Modulation current setting and control. The modulation current is set by installing an external resistor from this pin to ground or using a current source. |
| 14 | BIASMAX | Install a resistor between this pin and GND to set the maximum bias current for the closed loop operation. The APC loop controls the bias current up to the level of BIASMAX. When the bias current reaches the maximum value set through this pin, the driver continues to sink a current equal to this maximum. For open loop operations, this pin sets the bias current. |
| 15 | MODMON | Modulation Current Monitor. Provides a current, which represents 1/100 of the modulation current. Install a resistor between this pin and GND to convert that current to a voltage proportional to the modulation current. |
| 18 | MOD- | Inverted modulation current output. Provides modulation current when input data is negative. |
| 19 | MOD+ | Non-inverted modulation current output. Provides modulation current when input data is positive. |
| 21 | BIAS | Bias current output, sources current when BEN+ is high. Connect to the cathode of the laser through a resistor. |
| 22 | MD | Input from the laser monitoring photodiode. Connect to the anode of the laser photodiode for APC operation. |
| 23 | BIASMON | Bias Monitor. Provides a current, which represents 1/50 of the bias current. Install a resistor between this pin and GND to convert that current to a voltage. |
| 24 | RSSI | Received Signal Strength Indicator. Install a resistor from this pin to GND to get a voltage proportional to the received signal. |
| 25 | /APCFAULT | Indicates APC failure when Low. Active Low TTL/CMOS. |
| 27 | RIN+ | **SY88236L:** Post amplifier Non-inverting input data. Internally terminated with 50Ω to a reference voltage. |
| | | **SY88236AL:** Post amplifier Non-inverting input data. No internal termination. |
| 28 | RIN- | **SY88236L:** Driver inverting input data. Internally terminated with 50Ω to a reference voltage. |
| | | **SY88236AL:** Driver inverting input data. No internal termination. |
| 30 | ROUT- | Post Amplifier Complementary CML data output. |
| 31 | ROUT+ | Post Amplifier true CML data output. |
| 5, 8, 16, 24, 29 | GND | Ground. Ground and exposed pad must be connected to the plane of the most negative potential. |
| 17, 20, 32 | | Supply Voltage. Bypass with a 0.1µF//0.01µF low ESR capacitor as close to VCC pin as possible. |

## Truth Tables

| DIN+ | DIN- | TXDIS | MOD+[2] | MOD- | Laser Output Power[3] |
|---|---|---|---|---|---|
| L | H | L | H | L | L |
| H | L | L | L | H | H |
| X | X | X | H | L | L |

**Table 1. Modulation Output Truth Table[1, 3]**

| TXDIS | BEN+ | BEN- | BIAS |
|---|---|---|---|
| L | H | L | ON |
| L | L | H | OFF |
| H | X | X | OFF |

**Table 2. BIAS Output Truth Table**

**Notes:**

1. Assuming BEN+ = H and BEN- = L.
2. $I_{MOD}$ = 0 when MOD+ = H.
3. Assuming that the cathode of the laser is connected to MOD+.

| LOS/SD_SEL | Function Selected | JAM | Output |
|---|---|---|---|
| H | LOS | L | Enabled |
| H | LOS | H | Disabled |
| L | SD | L | Disabled |
| L | SD | H | Enabled |

**Table 3. Post Amp Output Truth Table**


hbwhelp@micrel.com or (408) 955-1690

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{IN}$) ..... –0.5V to +4.0V
CML Input Voltage ($V_{IN}$) ..... $V_{CC}$–1.2V to $V_{CC}$+0.5V
TTL Control Input Voltage ($V_{IN}$) ..... 0V to $V_{CC}$
Lead Temperature (soldering, 20sec.) ..... +260°C
Storage Temperature ($T_s$) ..... –65°C to +150°C

## Operating Ratings[2]

Supply Voltage ($V_{CC}$) ..... +3.0V to +3.6V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance[3]
QFN
($\theta_{JA}$) Still-air ..... 60°C/W
($\psi_{JB}$) ..... 33°C/W

## DC Electrical Characteristics

$T_A$ = –40°C to +85°C and $V_{CC}$ = +3.0V to +3.6V, unless otherwise noted. Typical values are $V_{CC}$ = +3.3V, $T_A$ = 25°C, $I_{MOD}$ = 30mA, $I_{BIAS}$ = 30mA.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current | Modulation and Bias currents excluded | | 90 | 150[4] | mA |
| $V_{IL}$ | TXDIS, JAM, and LOS/SD_SEL Input Low | | -0.3 | | 0.8 | V |
| $V_{IH}$ | TXDIS, JAM, and LOS/SD_SEL Input High | | 2 | | $V_{CC}$ + 0.3 | V |
| **Laser Driver** | | | | | | |
| $V_{MOD_MIN}$ | Minimum Voltage Required at the Driver Output, MOD+ and MOD-, for Proper Operation | | 0.6 | | | V |
| $V_{BIAS_MIN}$ | Minimum Voltage Required at the Driver Output, BIAS pin, for Proper Operation | | 0.8 | | | V |
| $I_{BIAS}$ | Bias-ON Current | Voltage at Bias pin ≥ 0.8V | 1 | | 70 | mA |
| $I_{BIAS_OFF}$ | Bias-OFF Current | Current at BIAS pin when TXDIS is high or BEN is low | | | 150 | µA |
| $R_{IN}$ (SY88236L only) | Input Resistance at DIN+ and DIN- | Single ended | 42.5 | 50 | 57.5 | Ω |
| BEN+, BEN- | Burst Mode Enable Signal | Single ended | | 0.8 | | V |
| $V_{IH}$(BEN) | High Voltage | BEN+, BEN- | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$(BEN) | Low Voltage | BEN+, BEN- | -0.3 | | 0.8 | V |
| $V_{OL}$ | /APCFAULT Output Low | $I_{OL}$ = 2mA | | | 0.5 | V |
| $I_{OH}$ | /APCFAULT Output Leakage | $V_{OH}$ = $V_{CC}$ | | | 100 | µA |
| $I_{MD}$ | Current range at MD pin | | 50 | | 1500 | µA |

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. $\theta_{JB}$ uses a 4-layer and $\theta_{JA}$ in still air unless otherwise stated.
4. $I_{CC}$ = 150mA for worst-case conditions with $I_{MOD}$ = 85mA, $I_{Bias}$ = 70mA, $T_A$ = +85°C, $V_{CC}$ = 3.6V.

**Post Amplifier**

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $LOS_{LVL}$ | $LOS_{LVL}$ Voltage | | $V_{CC}$ -1.3 | | $V_{CC}$ | V |
| $V_{OH}$ | ROUT+, ROUT- HIGH Voltage | | $V_{CC}$-0.020 | $V_{CC}$-0.005 | $V_{CC}$ | V |
| $V_{OL}$ | ROUT+, ROUT- LOW Voltage | | $V_{CC}$-0.475 | $V_{CC}$-0.400 | $V_{CC}$-0.350 | V |
| $V_{OFFSET}$ | Differential Output Offset | | | | ±80 | mV |
| $Z_0$ (ROUT) | Single-Ended Output Impedance | | 42.5 | 50 | 57.5 | Ω |
| $Z_I$ (RIN) (SY88236L only) | Single-Ended Input Impedance | | 42.5 | 50 | 57.5 | Ω |
| $V_{OL}$(LOS/SD) | LOS/SD Output Low | $I_{OL}$ = 2mA | | | 0.5 | V |
| $I_{OH}$(LOS/SD) | LOS/SD Output Leakage | $V_{OH} = V_{CC}$ | | | 100 | µA |

## AC Electrical Characteristics

$T_A$ = –40°C to +85°C and $V_{CC}$ = +3.0V to +3.6V, unless otherwise noted. Typical values are $V_{CC}$ = +3.3V, $T_A$ = 25°C, $I_{MOD}$ = 30mA, $I_{BIAS}$ = 30mA.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Laser Driver** | | | | | | |
| | Data Rate | NRZ | 0.155 | | 2.5 | Gbps |
| $V_{DIFF-IN}$ (DIN) | Differential Input Voltage Swing | | 100 | | 2400 | $mV_{PP}$ |
| $V_{IN}$ (BEN+/BEN-) | Input Voltage Swing, Single Ended | BEN+, BEN- | 100 | | | mV |
| $V_{DIFF-IN}$ (BEN+/BEN-) | Differential Input Voltage Swing | BEN+, BEN- | 200 | | | $mV_{PP}$ |
| $I_{MOD}$ | Modulation Current[5] | AC-coupled | 10 | | 85 | mA |
| | | DC-coupled, Voltage at MOD pin ≥0.6V | 10 | | 70[6] | mA |
| $I_{MOD_OFF}$ | Modulation OFF Current | Current at MOD+ when TXDIS is high or BEN+ is low | | | 150 | µA |
| | | Current at MOD- when TXDIS is high or BEN+ is low | | | 150 | µA |
| $t_r$ | Output Current Rise Time | 20% to 80%, $I_{MOD}$ = 60mA | | 60 | 85 | ps |
| $t_f$ | Output Current Fall Time | 20% to 80%, $I_{MOD}$ = 60mA | | 60 | 85 | ps |
| Jitter | Total Jitter[7] | 155Mbps data rate | | | 30 | $ps_{PP}$ |
| | | 622Mbps data rate | | | 30 | $ps_{PP}$ |
| | | 1.25Gbps data rate | | | 30 | $ps_{PP}$ |
| | | 2.5Gbps data rate | | | 30 | $ps_{PP}$ |
| $t_{INIT}$ | APC Loop Initialization Time | Power up with TXDIS low and BEN+ high | | | 12 | µs |
| | | TXDIS changes from high to low with power ON and BEN+ high | | | 10 | µs |
| | | BEN changes from low to high with power ON and TXDIS low | | | 2.5 | ns |
| | Burst Enable Delay[8, 9] | | | | 2.5 | ns |
| | Burst Disable Delay[8,10] | | | | 2 | ns |
| | Burst ON-Time | 155Mbps | 1.9 | | | µs |
| | | 622Mbps | 720 | | | ns |
| | | 1.25Gbps | 576 | | | ns |
| | | 2.5Gbps | 576 | | | ns |
| | Burst OFF-Time | 155Mbps | 1.9 | | | µs |
| | | 622Mbps | 720 | | | ns |
| | | 1.25Gbps | 576 | | | ns |
| | | 2.5Gbps | 576 | | | ns |

**Notes:**

5. Load = 15Ω.
6. Assuming $V_{CC}$ = 3.0V, Laser bandgap voltage = 1V, laser package inductance = 1nH, laser equivalent series resistor = 5 Ω, and damping resistor = 10Ω.
7. Total jitter is measured using $2^7$ – 1 PRBS pattern.
8. Measured with a laser equivalent resistive load.
9. Burst Enable Delay is measured as the time between the instant when the BEN+ signal going from low to high reaches 50% of its amplitude and the instant at which the modulation current or the bias current (whichever takes longer) reaches 90% of its final value.
10. Burst Disable Delay is measured as the time between the instant when the BEN+ signal going from high to low reaches 50% of its amplitude and the instant at which the modulation current or the bias current (whichever takes longer) goes below 10% of its final value.

### Post Amplifier

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time (20% to 80%) | Note 11 | | 60 | 120 | ps |
| $t_{JITTER}$ | Deterministic<br>Random | Note 12<br>Note 13 | | 15<br>5 | | $ps_{PP}$<br>$ps_{RMS}$ |
| $V_{Diff_IN}$ (RIN) | Differential Input Voltage Swing | | 5 | | 1800 | $mV_{PP}$ |
| $V_{Diff_OUT}$ (ROUT) | Differential Output Voltage Swing | Note 11 | 700 | 800 | 950 | $mV_{PP}$ |
| $G_{RSSI}$ | RSSI Gain = $I_{RSSI}$ / $V_{Diff_IN}$ (RIN) | $5mV_{PP} \le V_{Diff_IN}$ (RIN) $\le 200mV_{PP}$ | | 5 | | µA/ $mV_{PP}$ |
| RSSI Linearity | | $5mV_{PP} \le V_{Diff_IN}$ (RIN) $\le 200mV_{PP}$ | | ± 2.5 | | % |
| $LOS_{AL}$ | Low LOS Assert Level | $R_{LOSLVL}$ = 15kΩ | 2 | 8 | | $mV_{PP}$ |
| $LOS_{DL}$ | Low LOS De-assert Level | $R_{LOSLVL}$ = 15kΩ | | 10 | 20 | $mV_{PP}$ |
| $HSY_L$ | Low LOS Hysteresis | $R_{LOSLVL}$ = 15kΩ, Note 14 | 1.5 | 2.6 | 6 | dB |
| $LOS_{AM}$ | Medium LOS Assert Level | $R_{LOSLVL}$ = 5kΩ | 4 | 12 | | $mV_{PP}$ |
| $LOS_{DM}$ | Medium LOS De-assert Level | $R_{LOSLVL}$ = 5kΩ | | 16 | 30 | $mV_{PP}$ |
| $HSY_M$ | Medium LOS Hysteresis | $R_{LOSLVL}$ = 5kΩ, Note 14 | 1.5 | 2.8 | 6 | dB |
| $LOS_{AH}$ | High LOS Assert Level | $R_{LOSLVL}$ = 100Ω | 15 | 25 | | $mV_{PP}$ |
| $LOS_{DH}$ | High LOS De-assert Level | $R_{LOSLVL}$ = 100Ω | | 36 | 50 | $mV_{PP}$ |
| $HSY_H$ | High LOS Hysteresis | $R_{LOSLVL}$ = 100Ω | 1.5 | 3.2 | 6 | dB |
| $T_{OFF}$ | LOS Release Time | Note 15 | | 2 | 10 | µs |
| $T_{ON}$ | LOS Assert Time | Note 15 | | 2 | 10 | µs |
| $B_{-3dB}$ | 3dB Bandwidth | | | 2.0 | | GHz |
| $A_{V(Diff)}$ | Differential Voltage Gain | | | 38 | | dB |
| $S_{21}$ | Single-Ended Small-Signal Gain | | 26 | 32 | | dB |

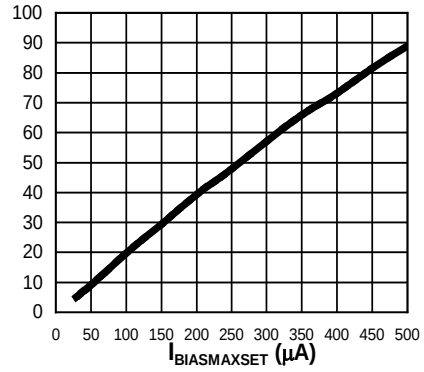
**Notes:**

11. Amplifier in limiting mode. Input is a 200MHz square wave.
12. Deterministic jitter measured using 2.5Gbps K28.5 pattern, $V_{ID}$ = $10mV_{PP}$.
13. Random jitter measured using 2.5Gbps K28.7 pattern, $V_{ID}$ = $10mV_{PP}$.
14. This specification defines electrical hysteresis as 20log (LOS De-Assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 1dB-4.5 dB, shown in the AC characteristics table, will be 0.5dB-3dB Optical Hysteresis.
15. In real world applications, the LOS Release/Assert time can be strongly influenced by the RC time constant of the AC-coupling cap and the 50Ω input termination. To keep this time low, use a decoupling cap with the lowest value that is allowed by the data rate and the number of consecutive identical bits in the application (typical values are in the range of 0.001µF to 1.0µF).

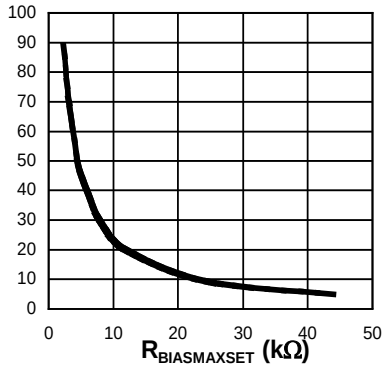
# Typical Characteristics

## Laser Driver

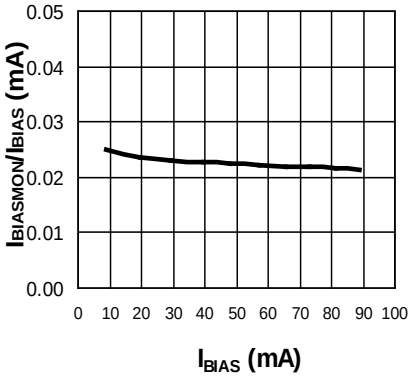
**$I_{BIAS}$ vs. $I_{BIASMAXSET}$**



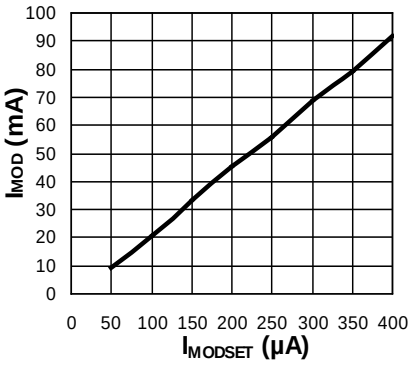

**$I_{BIAS}$ vs. $R_{BIASMAXSET}$**



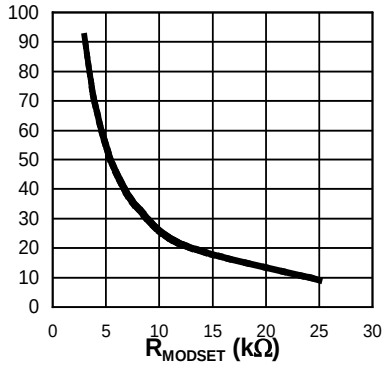

**$I_{BIASMON}$ Gain**




**Modulation Gain**

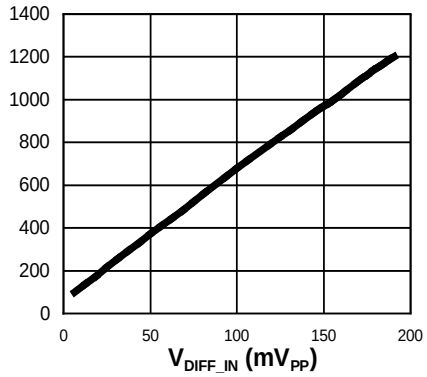



**$I_{MOD}$ vs. $R_{MODSET}$**

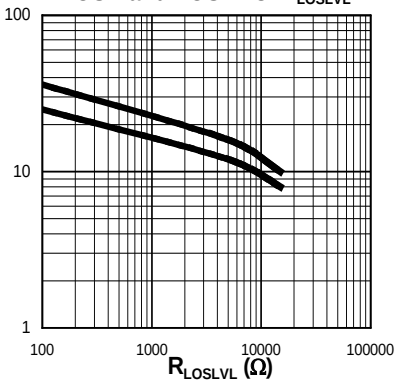



## Post Amplifier

**$I_{RSSI}$ vs. RIN**



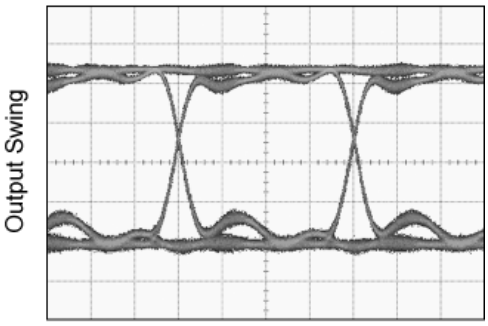

**LOSA and LOSD vs. $R_{LOSLVL}$**



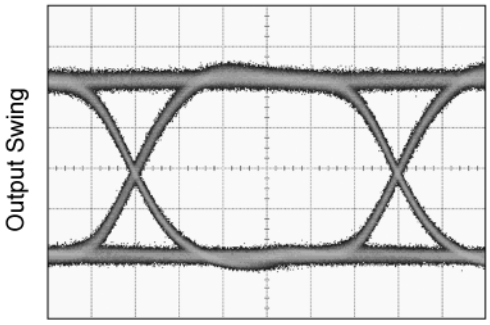
# Functional Characteristics

## Laser Driver

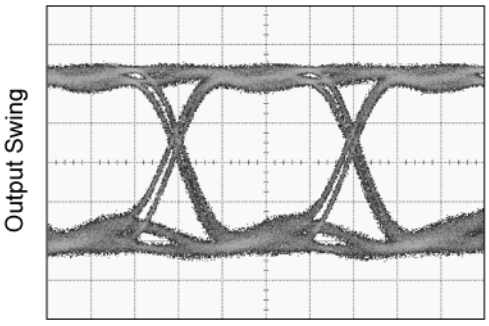
**Electrical Eye Diagram @1.25Gbps**



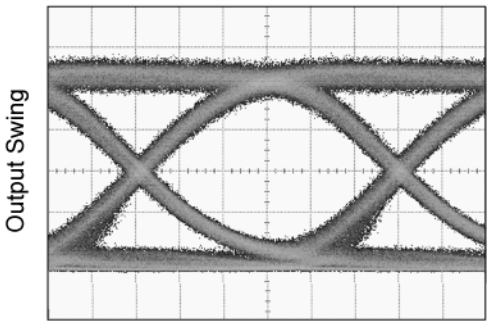

**Optical Eye Diagram @1.25Gbps with 2.3G Filter Laser DC-Coupled to the Driver**



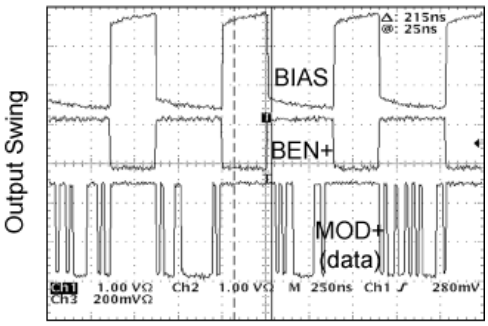

**Electrical Eye Diagram @2.5Gbps**



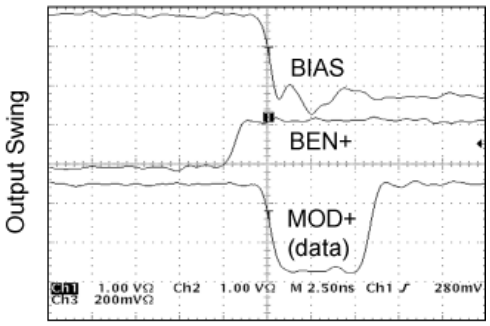

**Optical Eye Diagram @2.5Gbps with 2.3G Filter Laser DC-Coupled to the Driver**



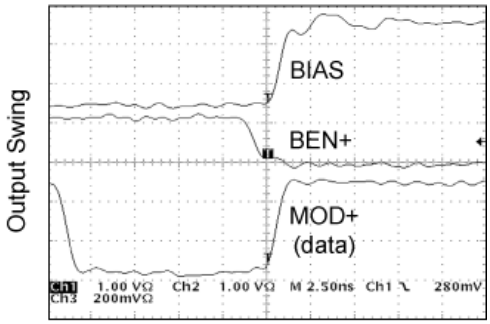

**Driver Burst Mode Operation**




**Bias and Modulation Turn On**

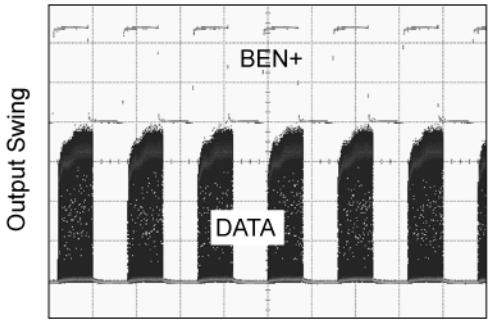


**Bias and Modulation Turn Off**



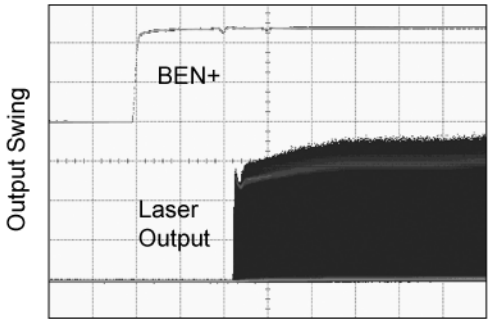

TIME (2.5ns/div.)

**Burst Mode Operation with Laser**



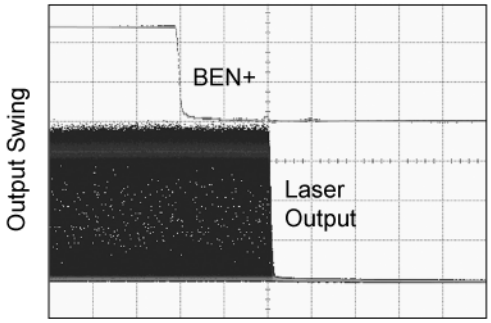

TIME (5ns/div.)

**Laser Turn On**




TIME (5ns/div.)

**Laser Turn Off**

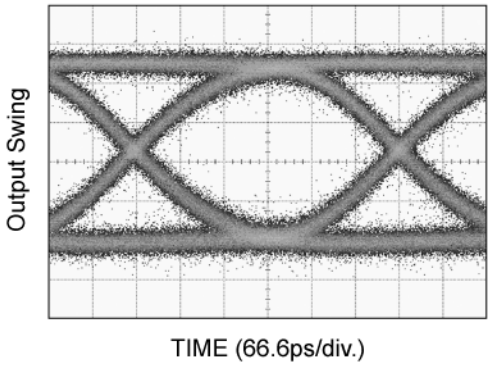



TIME (5ns/div.)

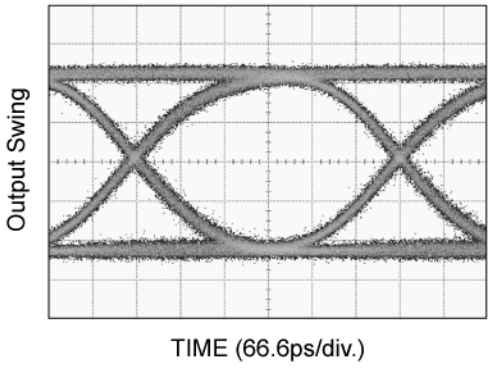
## Functional Characteristics (continued)

### Post Amplifier

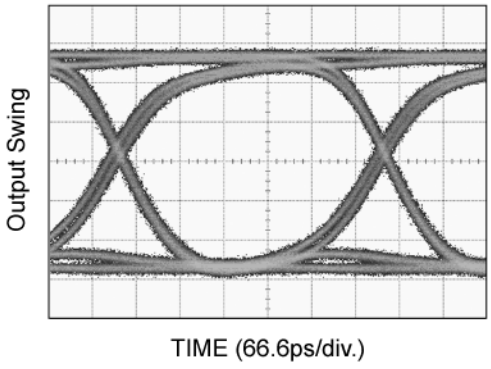
**Electrical Eye Diagram @2.5Gbps**
**$V_{DIFF_IN}$ = 2.5m$V_{PP}$**



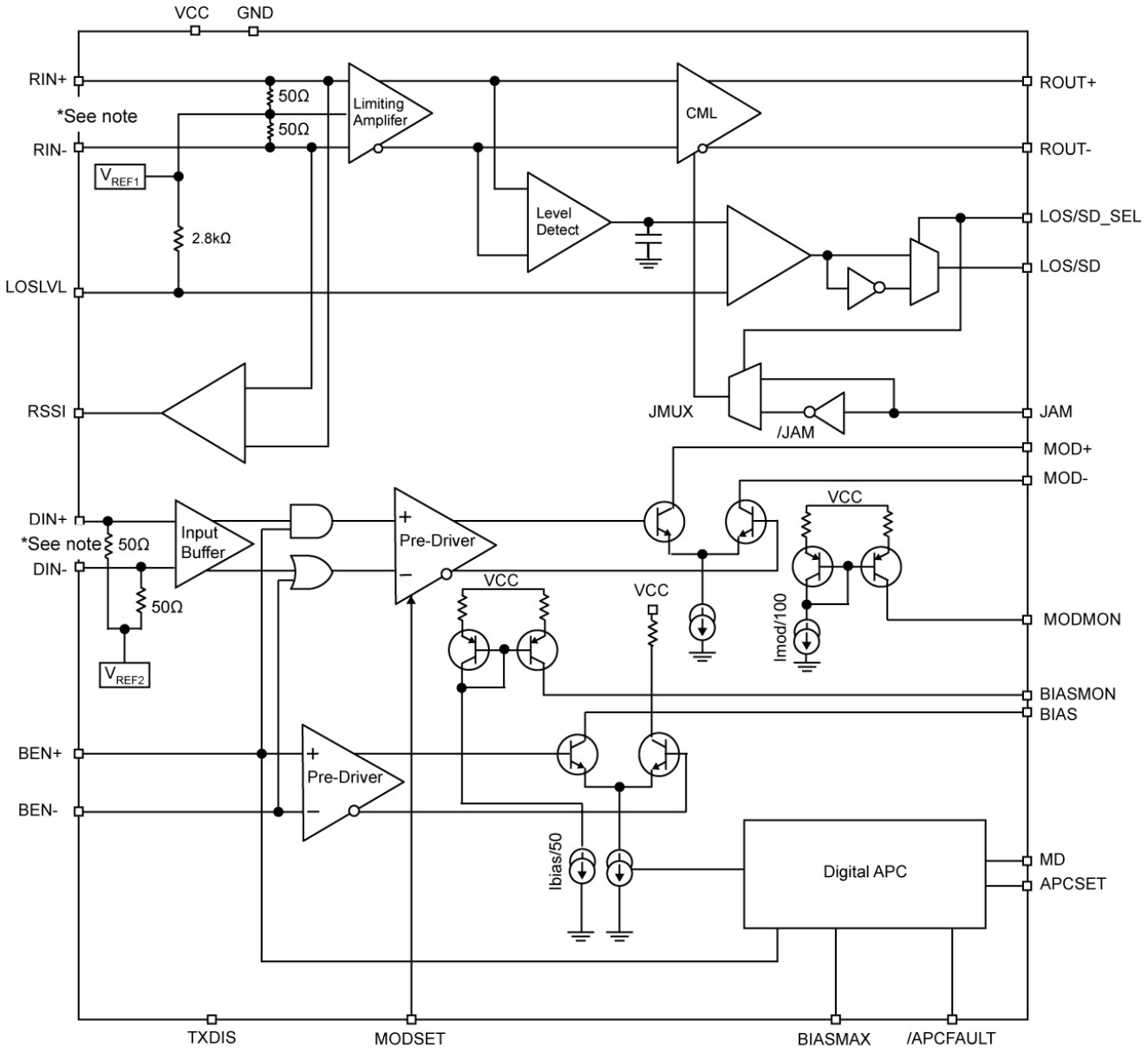

**Electrical Eye Diagram @2.5Gbps**
**$V_{DIFF_IN}$ = 5m$V_{PP}$**




**Electrical Eye Diagram @2.5Gbps**
**$V_{DIFF_IN}$ = 10m$V_{PP}$**



## Functional Diagram




*note: The internal terminations at DIN+, DIN-, RIN+, RIN- apply for SY88236L only.
SY88236AL doesn't have internal terminations at those inputs

**The SY88236L is shown. For the SY88236AL, 50Ω terminations should be removed from DIN± and RIN±.**

# Functional Description

## Laser Driver

The laser driver is comprised from a modulator, a bias circuit, and a digital APC loop.

The driver features bias and modulation current monitoring functions, which can be configured for optical power monitoring.

### *BIAS and Modulation Setting*

Bias and modulation currents are set by installing resistors from APCSET to ground and from MODSET to ground respectively or by applying a negative current at those pins. $I_{BIAS}$ variation versus $R_{BIASMAXSET}$ resistor and $I_{BIASMAXSET}$ , and $I_{MOD}$ variation versus $R_{MODSET}$ resistor and $I_{MODSET}$ are shown on page 10.

### *BIASMAX*

A resistor between BIASMAX pin and ground sets the maximum bias the driver can sink. At normal operation, the bias current tracks the laser optical power through the laser monitoring photodiode and the APC loop to compensate for any power deviation from the nominal value set at the start of operation using APCSET. If for any failure (laser or photodiode degradation, open feedback circuit, etc.) the APC loop keeps increasing the bias current to compensate for the low power indication, the bias current will stop increasing when it reaches BIASMAX value and continues to operate at that maximum value and APCFAULT is asserted.

BIASMAX also sets the bias current when the circuit is operating in the open loop mode.

### *APC Loop Function*

At start up, with the driver enabled, TXDIS low and BEN+ high, the laser turns ON within a few microseconds and its back facet monitoring photodiode starts to generate a photocurrent proportional to the optical power. The photocurrent is fed back to the MD pin on the driver where it's converted to a voltage. The conversion voltage is compared to APCSET on the driver. At equilibrium, the feedback voltage equals the APCSET voltage and the laser optical power reaches its nominal value. If the laser power deviates from its nominal value, the APC loop brings it back to its nominal setting.

### *APC Loop Failure*

The APCFAULT is asserted Low if the bias current reaches BIASMAX or if the APC loop counter reaches its minimum or its maximum counts.

### *Interfacing the Driver with the Laser Diode*

As shown on the "Typical Application" drawing, MOD+ pin is connected to the laser cathode through a 10Ω resistor and MOD- pin is connected to VCC with a 150Ω resistor equivalent to 100Ω (damping resistor) in series with the laser (equivalent resistor of 50Ω). The laser can be driven differentially by connecting MOD- to the anode of the laser through 0.1µF (150Ω pull -up removed) and isolating the anode of the laser from VCC with an inductor.

## Post Amplifier

The post amplifier detects and amplifies signals with data rates from DC up to 3.2Gbps, and amplitude as small as $5mV_{PP}$. To reduce the noise at the output of the post amplifier when the input signal is absent or lower than the minimum detectable level set by $LOS_{LVL}$, a JAM pin is provided, which can be connected to LOS/SD output to turn off the output buffer when LOSS/SD is asserted.

### *Input Amplifier/Buffer*

Figure 1-d shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as $5mV_{PP}$ to be detected and amplified. The input amplifier allows input signals as large as $1800mV_{PP}$. Small input signals below typically $12mV_{PP}$ are linearly amplified with a typically 38dB differential voltage gain. For input signals larger than $12mV_{PP}$, the output signal is limited to typically $800mV_{PP}$.

### *Output Buffer*

The post amplifier CML output buffer is designed to drive 50Ω lines and is internally terminated with 50Ω to $V_{CC}$. Figure 1e shows a simplified schematic of the output stage.

### *Loss-of-Signal*

The post amplifier generates a selectable chatter-free loss-of-signal (LOS) or signal detect (SD) open-collector TTL output as shown in Figure 2g. LOS/SD is used to determine that the input amplitude is too small to be considered as a valid input. When the LOSS function is selected (LOS/SD_SEL=1), LOS/SD asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. IF SD function is selected (LOS/SD_SEL=0), LOS/SD asserts low if the input amplitude falls below the threshold set by LOSLVL and de-asserts high otherwise. LOS/SD can be fed back to the JAM input to maintain output stability under a loss of signal condition. Jam de-asserts low the true output signal without removing the input signals. Typically, 3dB LOS hysteresis is provided to prevent chattering.

### *Loss/Signal Detect Selection*

A pin (LOS/SD_SEL) is provided to select between LOS (set to high) or SD (set to low) function. It also controls the internal circuitry of JAM input to follow LOS/SD selection.

### *Loss-of-Signal-Level Set*

A programmable LOS/SD level set pin ($LOS_{LVL}$) sets the threshold of the input amplitude detection. Connecting an external resistor between $V_{CC}$ and $LOS_{LVL}$ sets the voltage at $LOS_{LVL}$. This voltage ranges from $V_{CC}$ to $V_{CC}$ -1.3V. The external resistor creates a voltage divider between $V_{CC}$ and $V_{CC}$-1.3V, as shown in Figure 2f.

### *Hysteresis*

The post amplifier provides typically 3dB LOS electrical hysteresis, which is defined as 20log ($VIN_{LOS\text{-}Assert}$ / $VIN_{LOS\text{-}De\text{-}Assert}$). Since the relationship between the voltage out of the ROSA to optical power at its input is linear, the optical hysteresis will be typically half of the electrical hysteresis reported in the datasheet, but in practice, the ratio between electrical and optical hysteresis is found to be within the range 1.5 to 1.8. Thus, 3dB electrical hysteresis will correspond to an optical hysteresis within the range 1.6dB to 2dB.

### *RSSI Pin*

The post amplifier has an RSSI (Received Signal Strength) pin, which provides a current proportional to the amplitude of the signal at the input of the post amplifier from the ROSA. Install a resistor between this pin and GND to convert the current into a monitoring voltage proportional to the amplitude of the signal at the input of the post amplifier. The value of the resistor should be selected to keep the voltage at the RSSI pin under its limits of 1.2V to maintain RSSI linearity.

## Input and Output Stages (SY88236L) [1]

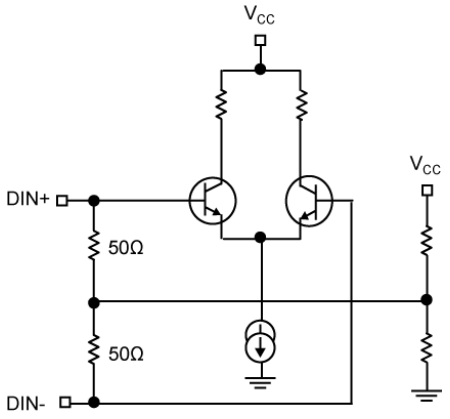



**Figure 1a. Simplified Driver Input Stage[1]**

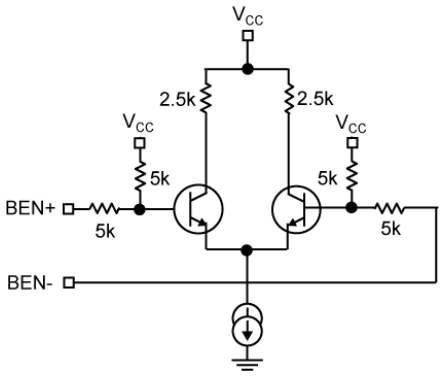



**Figure 1b. Simplified BEN Input Stage**

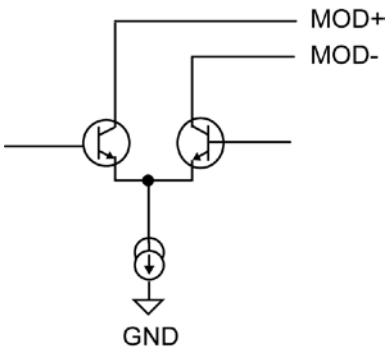



**Figure 1c. Simplified Driver Output Stage**

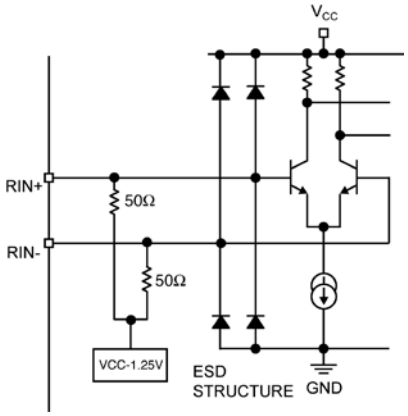



**Figure 1d. Post Amplifier Input Stage[1]**

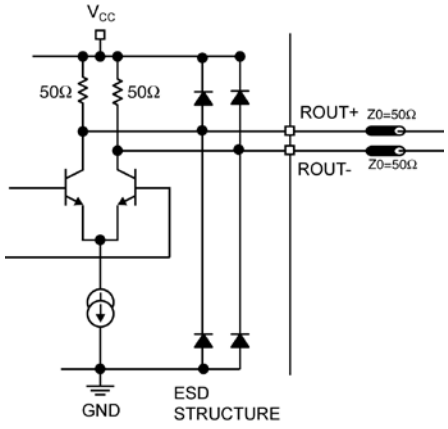



**Figure 1e. Post Amplifier Output Stage**

**Note:**

1. Applies for SY88236L only. For SY88236AL input terminations need to be removed.

## Interfacing DIN and BEN Inputs to Different Logic Drivers (SY88236L) [1]

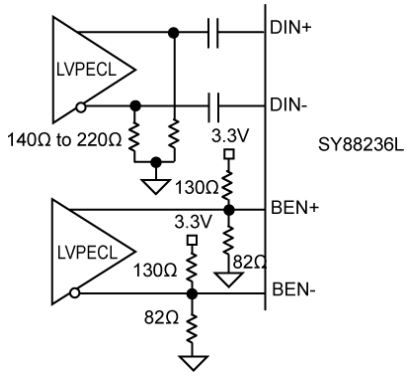



**Figure 2a. Driving DIN and BEN with PECL Outputs[1]**

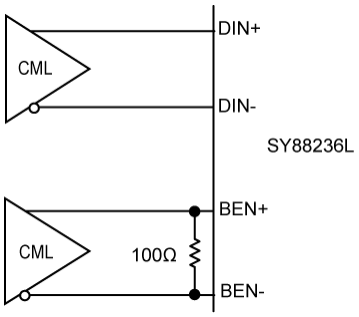



**Figure 2b. Driving DIN and BEN with CML Outputs[1]**

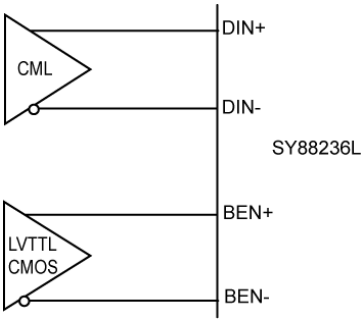



**Figure 2c. Driving BEN with LVTTL/CMOS Outputs[1]**

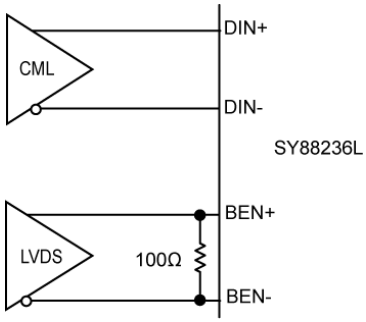



**Figure 2d. Driving BEN with LVDS Outputs[1]**

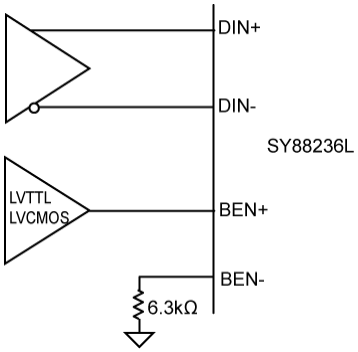



**Figure 2e. Driving BEN with Single-Ended LVTTL/CMOS**

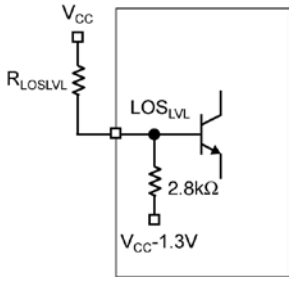



**Figure 2f. $LOS_{LVL}$ Setting Circuit**

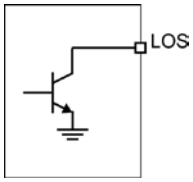
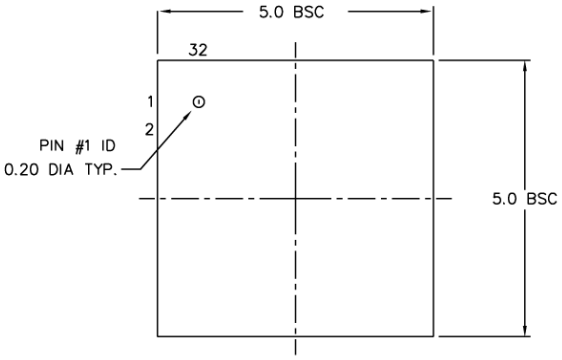



**Figure 2g. LOS Output Structure**

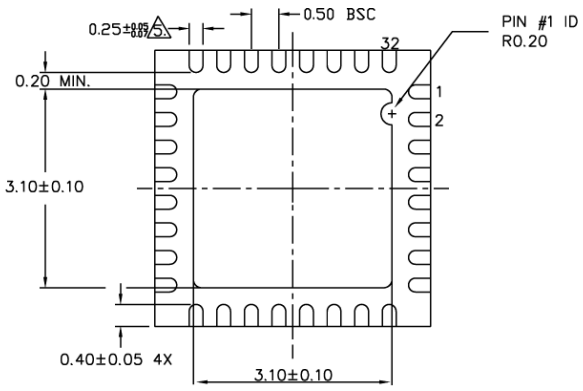
**Note:**

1. Applies for SY88236L only. For SY88236AL input terminations need to be added.

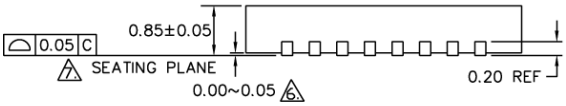
## Package Information




TOP VIEW




BOTTOM VIEW




SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

**32-Pin (5mm x 5mm) QFN**

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**
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