

#### **General Description**

The MAX5548 dual, 8-bit, digital-to-analog converter (DAC) features high-output-current capability. The MAX5548 sources up to 30mA per DAC, making it ideal for PIN diode biasing applications. Outputs can also be paralleled for high-current applications (up to 60mA typ). Operating from a single +2.7V to +5.25V supply, the MAX5548 typically consumes 1.5mA per DAC in normal operation and less than 1µA (max) in shutdown mode. The MAX5548 also features low output leakage current in shutdown mode (±1µA max) that is essential to ensure that the external PIN diodes are off.

Additional features include an integrated +1.25V bandgap reference, and a control amplifier to ensure high accuracy and low-noise performance. A separate reference input (REFIN) allows for the use of an external reference source, such as the MAX6126, for improved gain accuracy. A pin-selectable I<sup>2</sup>C-/SPI<sup>TM</sup>-compatible serial interface provides optimum flexibility for the MAX5548. The maximum programmable output current value is set using software and an adjustment resistor.

The MAX5548 is available in a 3mm x 3mm, 16-pin, thin QFN package, and is specified over the extended (-40°C to +85°C) temperature range.

#### **Applications**

PIN Diode Biasing RF Attenuator Control **VCO Tuning** 

#### **Features**

- ♦ Pin-Selectable I<sup>2</sup>C- or SPI-Compatible Interface
- **♦** Guaranteed Low Output Leakage Current in Shutdown (±1µA max)
- ♦ Guaranteed Monotonic over Extended **Temperature Range**
- ♦ Dual Outputs for Balanced Systems
- ♦ Current Outputs Source Up to 30mA per DAC
- ♦ Parallelable Outputs for 60mA Applications
- ♦ Output Stable with RF Filters
- **♦** Internal or External Reference Capability
- ♦ Digital Output (DOUT) Available for Daisy Chaining in SPI Mode
- ♦ +2.7V to +5.25V Single-Supply Operation
- ♦ 16-Pin (3mm x 3mm) Thin QFN Package
- ♦ Programmable Output Current Range Set by **Software and Adjustment Resistor**

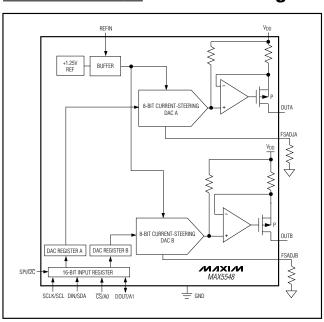
#### **Ordering Information**

PART	PIN-	PKG	TOP
	PACKAGE	CODE	MARK
MAX5548ETE	16 Thin QFN-EP*	T1633F-3	ACY

\*EP = Exposed paddle.

Note: Device is specified over the -40°C to +85°C operating range.

#### Functional Diagram



SPI is a trademark of Motorola, Inc.

Pin Configuration appears at end of data sheet.

MIXIM

Maxim Integrated Products 1

#### **ABSOLUTE MAXIMUM RATINGS**

V <sub>DD</sub> to GND0.3V to +6V OUTA, OUTB to GND0.3V to (V <sub>DD</sub> + 0.3V)	Operating Temperature Range40°C Junction Temperature	
REFIN CS/AO, DOUT/AI, SPI/IZC, FSADJA,	Storage Temperature Range65°C to	
FSADJB to GND0.3V to (V <sub>DD</sub> + 0.3V)	Lead Temperature (soldering, 10s)	+300°C
SCLK/SCL, DIN/SDA0.3V to +6V		
Continuous Power Dissipation (T <sub>A</sub> = +85°C)		
16-Pin Thin QFN (derate 17.5mW/°C above +70°C)1398.6mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{DD} = +2.7 V \text{ to } +5.25 V, \text{ GND} = 0, V_{REFIN} = +1.25 V, \text{ internal reference, } R_{FSADJ} = 20 k\Omega; \text{ compliance voltage} = (V_{DD} - 0.6 V), V_{SCLK/SCL} = 0, T_{A} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}, \text{ unless otherwise noted.}$ 

PARAMETER	SYMBOL	CON	IDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANAL	OG SECTIO	N					· I
Resolution				8			Bits
Integral Nonlinearity	INL	$I_{OUT} = 1$ mA to 30m	nA (Note 2)		±1		LSB
Differential Nonlinearity	DNL	Guaranteed monoto	nic			±1	LSB
Offset	los			-13	-4		LSB
Zero-Scale Error		$I_{OUT}$ = 1mA to 30m	nA, code = 0x00			1	μΑ
Full-Scale Error		I <sub>OUT</sub> = 1mA to 30m includes offset	nA, code = 0xFF,		-4		LSB
REFERENCE							
Internal Reference Range				1.21	1.25	1.29	V
Internal Reference Tempco					30		ppm/°C
External Reference Range				0.5		1.5	V
External Reference Input Current					108	225	μΑ
DAC OUTPUTS							
Full-Scale Current		(Note 3)		1		30	mA
Output Current Leakage in Shutdown						±1	μΑ
Output Capacitance					10		рF
		I <sub>OUT</sub> = 30mA		1			
Current Source Dropout Voltage (VDD - VOUT_)		Jan 00m A	$T_A = +25^{\circ}C$	0.55			V
(VDD - VOO1_)		$I_{OUT} = 20mA$	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	0.6			
Output Impedance at Full-Scale Current					100		kΩ
Capacitive Load to Ground	CLOAD				10		nF
Series Inductive Load	LLOAD				100		nH
Maximum FSADJ_ Capacitive Load	CFSADJ_				75		рF
DYNAMIC PERFORMANCE							
Settling Time	ts	C <sub>LOAD</sub> = 24pF, L <sub>LO</sub>	AD = 27nH (Note 4)		30		μs
Digital Feedthrough					2		nVs
Digital-to-Analog Glitch Impulse					40		nVs

#### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD} = +2.7V \text{ to } +5.25V, \text{ GND} = 0, V_{REFIN} = +1.25V, \text{ internal reference}, R_{FSADJ} = 20k\Omega; \text{ compliance voltage} = (V_{DD} - 0.6V), V_{SCLK/SCL} = 0, T_{A} = -40^{\circ}\text{C}$  to +85°C, unless otherwise noted. Typical values are at  $V_{DD} = +3.0V$  and  $T_{A} = +25^{\circ}\text{C}$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC-to-DAC Current Matching				2		%
Walta I la Tiasa		$V_{DD} = +3V, R_L = 65\Omega, C_L = 24pF$		400		
Wake-Up Time		V <sub>DD</sub> = +5V, no load		10		μs
POWER SUPPLIES						
Supply Voltage	$V_{DD}$		+2.70		+5.25	V
Supply Current	I <sub>DD</sub>	$V_{DD} = +5.25V$ , no load		3	6	mA
Shutdown Current					1.2	μΑ
LOGIC AND CONTROL INPUTS						
Input High Voltage (Note 5)	VIH	+2.7V ≤ V <sub>DD</sub> ≤ +3.4V	0.7 x V <sub>DD</sub>			V
		+34V < V <sub>DD</sub> ≤ +5.25V	2.4			
Input Low Voltage	V <sub>IL</sub>	(Note 5)			0.8	V
Input Hysteresis	V <sub>HYS</sub>			0.1 x V <sub>DD</sub>		V
Input Capacitance	CIN			10		рF
Input Leakage Current	I <sub>IN</sub>				±1	μΑ
Output Low Voltage	VoL	ISINK = 3mA			0.6	V
Output High Voltage	Voн	ISOURCE = 2mA	V <sub>DD</sub> - 0.5			V
I <sup>2</sup> C TIMING CHARACTERISTICS	(Figure 2)					
SCL Clock Frequency	fscl				400	kHz
Setup Time for START Condition	tsu:sta		600			ns
Hold Time for START Condition	thd:sta		600			ns
SCL Pulse-Width Low	tLOW		130			ns
SCL Pulse-Width High	thigh		600			ns
Data Setup Time	tsu:dat		100			ns
Data Hold Time	thd:dat		0		70	ns
SCL Rise Time	tRCL		20 + 0.1 x C <sub>B</sub>		300	ns
SCL Fall Time	tFCL		20 + 0.1 x C <sub>B</sub>		300	ns
SDA Rise Time	t <sub>RDA</sub>		20 + 0.1 x C <sub>B</sub>	_	300	ns
SDA Fall Time	tFDA		20 + 0.1 x C <sub>B</sub>		300	ns
Bus Free Time Between a STOP and START Condition	tBUF		1.3	_		μs

#### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD} = +2.7V \ to \ +5.25V, \ GND = 0, \ V_{REFIN} = +1.25V, \ internal \ reference, \ R_{FSADJ} = 20k\Omega; \ compliance \ voltage = (V_{DD} - 0.6V), \ V_{SCLK/SCL} = 0, \ T_{A} = -40^{\circ}C \ to \ +85^{\circ}C, \ unless \ otherwise \ noted. \ Typical \ values \ are \ at \ V_{DD} = +3.0V \ and \ T_{A} = +25^{\circ}C.) \ (Note \ 1)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for STOP Condition	tsu:sto		160			ns
Maximum Capacitive Load for Each Bus Line	Св			400		pF
SPI TIMING CHARACTERISTICS	(Figure 6)		·			
SCLK Clock Period	tcp		100			ns
SCLK Pulse-Width High	tch		40			ns
SCLK Pulse-Width Low	tcL		40			ns
CS Fall to SCLK Rise Setup Time	tcss		25			ns
SCLK Rise to CS Rise Hold Time	tcsh		50			ns
DIN Setup Time	t <sub>DS</sub>		40			ns
DIN Hold Time	tDH		0			ns
SCLK Fall to DOUT Transition	t <sub>DO1</sub>	C <sub>LOAD</sub> = 30pF			40	ns
CS Fall to DOUT Enable	tcse	C <sub>LOAD</sub> = 30pF			40	ns
CS Rise to DOUT Disable	tcsd	C <sub>LOAD</sub> = 30pF			40	ns
SCLK Rise to CS Fall Delay	tcso		50			ns
CS Rise to SCLK Rise Hold Time	tCS1		40			ns
CS Pulse-Width High	tcsw		100			ns
SPI TIMING CHARACTERISTICS	FOR DAISY	CHAINING (Figure 6)				
SCLK Clock Period	tcp		200			ns
SCLK Pulse-Width High	tch		80			ns
SCLK Pulse-Width Low	tcL		80			ns
CS Fall to SCLK Rise Setup Time	tcss		25			ns
SCLK Rise to $\overline{\text{CS}}$ Rise Hold Time	tcsh		50			ns
DIN Setup Time	t <sub>DS</sub>		40			ns
DIN Hold Time	tDH		0			ns
SCLK Fall to DOUT Transition	t <sub>DO1</sub>	CLOAD = 30pF			40	ns
CS Fall to DOUT Enable	t <sub>CSE</sub>	C <sub>LOAD</sub> = 30pF			40	ns
CS Rise to DOUT Disable	tcsd	C <sub>LOAD</sub> = 30pF			40	ns
SCLK Rise to CS Fall Delay	tcso		50			ns
CS Rise to SCLK Rise Hold Time	tcs1		40			ns
CS Pulse-Width High	tcsw		100			ns

Note 1: 100% production tested at T<sub>A</sub> = +25°C. Limits over temperature are guaranteed by design.

Note 2: INL linearity is guaranteed from code 15 to code 255.

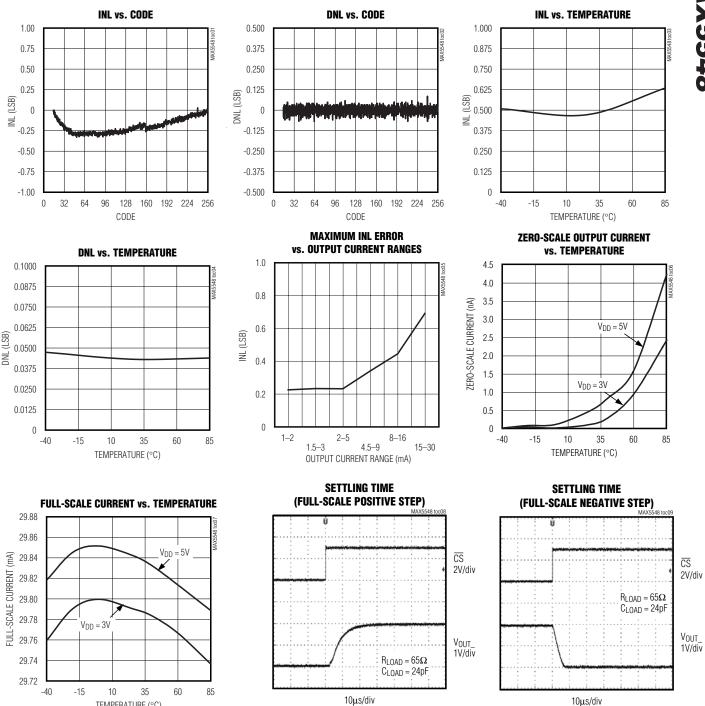
Note 3: Connect a resistor from FSADJ\_ to GND to adjust the full-scale current. See the Reference Architecture and Operation section.

Note 4: Settling time is measured from (0.25 x full scale) to (0.75 x full scale).

**Note 5:** The device draws higher supply current when the digital inputs are driven with voltages between (V<sub>DD</sub> - 0.5V) and (GND + 0.5V). See the Supply Current vs. Digital Input Voltage graph in the *Typical Operating Characteristics*.

### **Typical Operating Characteristics**

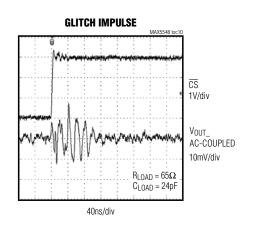
 $(V_{DD} = +3.0V, GND = 0, V_{REFIN} = +1.25V, internal reference, R_{FSADJ} = 20k\Omega, T_{A} = +25^{\circ}C.$  unless otherwise noted).

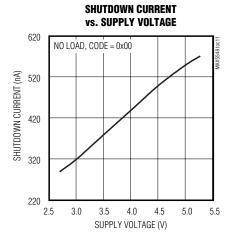


TEMPERATURE (°C)

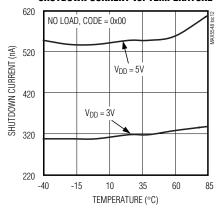
#### Typical Operating Characteristics (continued)

 $(V_{DD} = +3.0V, GND = 0, V_{REFIN} = +1.25V, internal reference, R_{FSADJ} = 20k\Omega, T_A = +25^{\circ}C.$  unless otherwise noted).

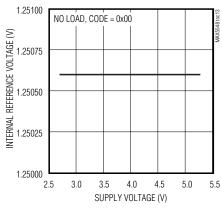




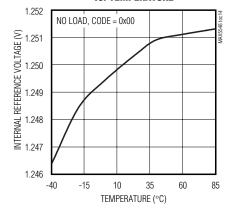
#### SHUTDOWN CURRENT vs. TEMPERATURE



### INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE

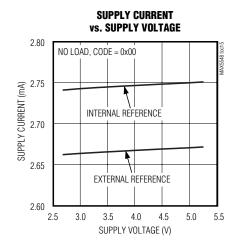


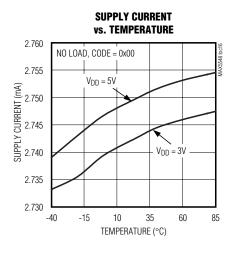
### INTERNAL REFERENCE VOLTAGE vs. Temperature

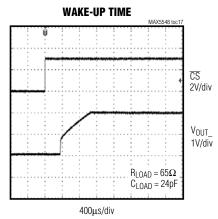


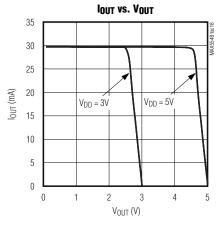
### Typical Operating Characteristics (continued)

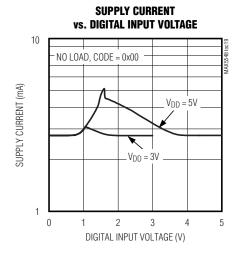
 $(V_{DD} = +3.0V, GND = 0, V_{REFIN} = +1.25V, internal reference, R_{FSADJ} = 20k\Omega, T_{A} = +25^{\circ}C.$  unless otherwise noted).

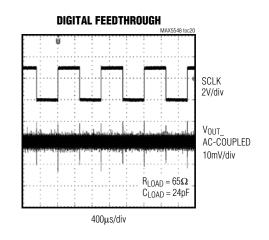












#### **Pin Description**

PIN	NAME	FUNCTION
1	SCLK/SCL	Serial Clock Input. Connect SCL to V <sub>DD</sub> through a 2.4kΩ resistor in I <sup>2</sup> C mode.
2	DIN/SDA	Serial Data Input. Connect SDA to $V_{DD}$ through a 2.4k $\Omega$ resistor in I <sup>2</sup> C mode.
3	CS/A0	Chip-Select Input in SPI Mode/Address Select 0 in I2C Mode. $\overline{\text{CS}}$ is an active-low input. Connect A0 to VDD or GND to set the device address in I2C mode.
4	SPI/Ī2C	SPI/I2C Select Input. Connect SPI/I2C to V <sub>DD</sub> to select SPI mode, or connect SPI/I2C to GND to select I2C mode.
5	DOUT/A1	Serial Data Output in SPI Mode/Address Select 1 in I2C Mode. Use DOUT to daisy chain the MAX5548 to other devices or to read back in SPI mode. The digital data is clocked out on SCLK's falling edge. Connect A1 to V <sub>DD</sub> or GND to set the device address in I2C mode.
6, 13, 15	N.C.	No Connection. Leave unconnected or connect to GND.
7	REFIN	Reference Input. Drive REFIN with an external reference source between +0.5V and +1.5V. Leave REFIN unconnected in internal reference mode. Bypass REFIN with a 0.1µF capacitor to GND as close to the device as possible.
8, 16	GND	Ground
9	OUTB	DACB Output. OUTB provides up to 30mA of output current.
10	FSADJB	DACB Full-Scale Adjust Input. For maximum full-scale output current, connect a $20k\Omega$ resistor between FSADJB and GND. For minimum full-scale current, connect a $40k\Omega$ resistor between FSADJB and GND.
11	FSADJA	DACA Full-Scale Adjust Input. For maximum full-scale output current, connect a $20k\Omega$ resistor between FSADJA and GND. For minimum full-scale current, connect a $40k\Omega$ resistor between FSADJA and GND.
12	OUTA	DACA Output. OUTA provides up to 30mA of output current.
14	V <sub>DD</sub>	Power-Supply Input. Connect V <sub>DD</sub> to a +2.7 to +5.25V power supply. Bypass V <sub>DD</sub> to GND with a 0.1µF capacitor as close to the device as possible.
_	EP	Exposed Pad. Connect to GND. Do not use as a substitute ground connection.

#### **Detailed Description**

#### **Architecture**

The MAX5548 8-bit, dual current-steering DAC (see the *Functional Diagram*) operates with DAC update rates up to 10Msps in SPI mode and 400ksps in I<sup>2</sup>C mode. The converter consists of a 16-bit shift register and input DAC registers, followed by a current-steering array. The current-steering array generates full-scale currents up to 30mA per DAC. An integrated +1.25V bandgap reference, control amplifier, and an external resistor determine each data converter's full-scale output range.

#### Reference Architecture and Operation

The MAX5548 provides an internal +1.25V bandgap reference or accepts an external reference voltage source between +0.5V and +1.5V. REFIN serves as the input for an external low-impedance reference source. Leave REFIN unconnected in internal reference mode. Internal or external reference mode is software selectable through the SPI/I<sup>2</sup>C serial interface.

The MAX5548's reference circuit (Figure 1) employs a control amplifier to regulate the full-scale current (IFS) for the current outputs of the DAC. This device has a software-selectable full-scale current range (see the command summary in Table 4). After selecting a current range, an external resistor (RFSADJ\_) sets the full-scale current. See Table 1 for a matrix of IFS and RFSADJ selections.

During startup, when the power is first applied, the MAX5548 defaults to the external reference mode, and to the 1mA-2mA full-scale current-range mode.

#### **DAC Data**

The 8-bit DAC data is decoded as offset binary, MSB first, with 1 LSB = IFS / 256, and converted into the corresponding current as shown in Table 2.

#### **Serial Interface**

The MAX5548 features a pin-selectable SPI/I<sup>2</sup>C serial interface. Connect SPI/I<sup>2</sup>C to GND to select I<sup>2</sup>C mode, or connect SPI/I<sup>2</sup>C to V<sub>DD</sub> to select SPI mode. SDA

and SCL ( $I^2C$  mode) and DIN, SCLK, and  $\overline{CS}$  (SPI mode) facilitate communication between the MAX5548 and the master. The serial interface remains active in shutdown.

#### $I^2C$ Compatibility (SPI/ $\overline{I2C}$ = GND)

The MAX5548 is compatible with existing I²C systems (Figure 2). SCL and SDA are high-impedance inputs; SDA has an open-drain output that pulls the data line low during the ninth clock pulse. SDA and SCL require pullup resistors (2.4k $\Omega$  or greater) to VDD. Optional resistors (24 $\Omega$ ) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot of the bus signals. The communication protocol supports standard I²C 8-bit communications. The device's address is compatible with 7-bit I²C addressing protocol only. Ten-bit address formats are not supported. Only write commands are accepted by the MAX5548.

Note: I<sup>2</sup>C readback is not supported.

#### Bit Transfer

One data bit transfers during each SCL rising edge. The MAX5548 requires nine clock cycles to transfer data into or out of the DAC register. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are read as control signals (see the *START and STOP Conditions* section). Both SDA and SCL idle high.

#### START and STOP Conditions

The master initiates a transmission with a START condition (S), (a high-to-low transition on SDA with SCL high). The master terminates a transmission with a STOP condition (P), (a low-to-high transition on SDA while SCL is high) (Figure 3). A START condition from the master signals the beginning of a transmission to the MAX5548. The master terminates transmission by issuing a STOP condition. The STOP condition frees the bus.

If a repeated START condition  $(S_r)$  is generated instead of a STOP condition, the bus remains active.

Table 1. Full-Scale Output Current and RFSADJ\_ Selection Based on a +1.25V (typ) Reference Voltage

	FUL	L-SCALE OUTP	UT CURRENT (r	nA)*		RFSAD	)J (kΩ)
1mA-2mA	1.5mA-3mA	2.5mA-5mA	4.5mA-9mA	8mA-16mA	15mA-30mA	Calculated	1% EIA Std.
1.00	1.500	2.500	4.500	8.00	15.00	40	40.2
1.25	1.875	3.125	5.625	10.00	18.75	35	34.8
1.50	2.250	3.750	6.750	12.00	22.50	30	30.1
1.75	2.625	4.375	7.875	14.00	26.25	25	24.9
2.00	3.000	5.000	9.000	16.00	30.00	20	20.0

<sup>\*</sup>See the command summary in Table 4.

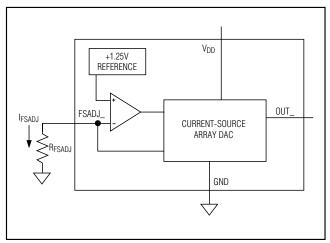


Figure 1. Reference Architecture and Output Current Adjustment

**Table 2. DAC Output Code Table** 

DAC CODE	I <sub>OUT</sub> _
1111 1111	255 × <sup>I</sup> FS
1000 0000	128×   IFS   -   IOS
0000 0001*	<u> FS</u> -   I <sub>OS</sub>
0000 0000	0

<sup>\*</sup>Negative output current values = 0.

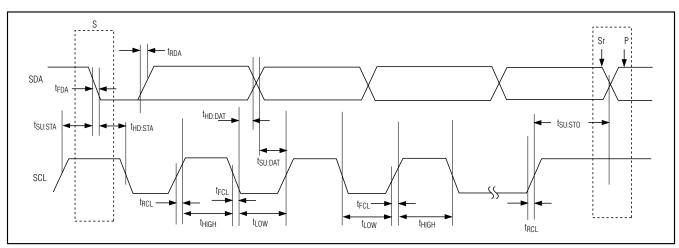


Figure 2. I<sup>2</sup>C Serial-Interface Timing Diagram

#### Early STOP Conditions

The MAX5548 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition (Figure 4). This condition is not allowed in the I<sup>2</sup>C format.

#### Repeated START Conditions

A repeated START ( $S_r$ ) condition is used when the bus master is writing to several I<sup>2</sup>C devices and does not want to relinquish control of the bus. The MAX5548's serial interface supports continuous write operations with an  $S_r$  condition separating them.

#### Acknowledge Bit (ACK)

Successful data transfers are acknowledged with an acknowledge bit (ACK). Both the master and the MAX5548 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 5).

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

#### Slave Address

A master initiates communication with a slave device by issuing a START condition followed by a slave address (see Table 3). The slave address consists of 7

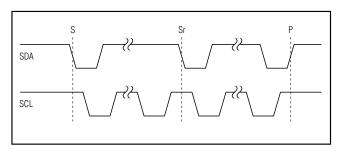


Figure 3. START and STOP Conditions

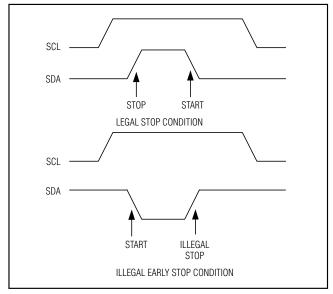


Figure 4. Early STOP Conditions

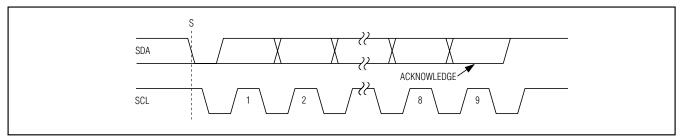


Figure 5. Acknowledge Condition

#### **Table 3. Write Operation**

	S T A R T				ORE	SS E		R/\	<del>//</del> **			cc	)MM	AND/	DAT	A BY	TE					D	ΑΤ	AΒ	/TE*				S T O P
Master SDA	S	0	1	1	0	0	A 1	A0	0		C5	C4	СЗ	C2	C1	CO	D7	D6		D5	D4	D3	D2	D1	D0	S1**	S0**		Р
Slave SDA										A C K									ACK									А С К	

<sup>\*</sup>S1 and S0 are subbits. Set S1 and S0 to zero for proper 8-bit operation.

address bits and a read/write bit ( $R\overline{W}$ ). When idle, the device continuously waits for a START condition followed by its slave address. When the device recognizes its slave address, it acquires the data and executes the command. The first 5 bits (MSBs) of the slave address have been factory programmed and are always 01100. Connect A1 and A0 to  $V_{DD}$  or GND to program the remaining 2 bits of the slave address. Set the least significant bit (LSB) of the address byte ( $R\overline{W}$ ) to zero to write to the MAX5548. After receiving the address, the MAX5548 (slave) issues an acknowledge by pulling SDA low for one clock cycle. I<sup>2</sup>C read commands ( $R/\overline{W}$  = 1) are not acknowledged by the MAX5548.

#### Write Cycle

The write command requires 27 clock cycles. In write mode (R/W=0), the command/data byte that follows the address byte controls the MAX5548 (Table 3). The registers update on the rising edge of the 26th SCL pulse. Prematurely aborting the write cycle does not update the DAC. See Table 4 for a command summary.

#### SPI Compatibility (SPI/ $\overline{I2C} = V_{DD}$ )

The MAX5548 is compatible with the 3-wire SPI serial interface (Figure 6). This interface mode requires three

inputs: chip-select  $(\overline{CS})$ , data clock (SCLK), and data in (DIN). Drive  $\overline{CS}$  low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge.

The MAX5548 requires 16 clock cycles to clock in 6 command bits (C5–C0) and 8 data bits (D7–D0) and S1 = S0 = 0 (Figure 7). After loading data into the shift register, drive  $\overline{CS}$  high to latch the data into the appropriate DAC register and disable the serial interface. Keep  $\overline{CS}$  low during the entire serial data stream to avoid corruption of the data. See Table 4 for a command summary.

#### **Shutdown Mode**

The MAX5548 has a software shutdown mode that reduces the supply current to less than  $1\mu A$ . Shutdown mode disables the DAC outputs. The serial interface remains active in shutdown. This provides the flexibility to update the registers while in shutdown. Recycling the power supply resets the device to the default settings.

<sup>\*\*</sup>Read operation not supported.

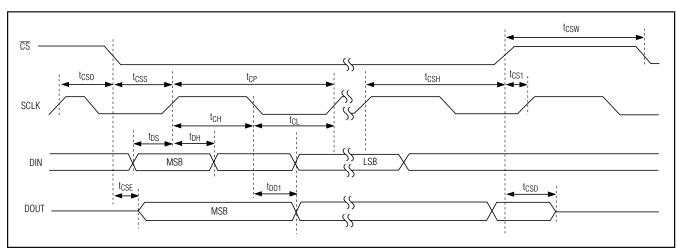


Figure 6. SPI-Interface Timing Diagram

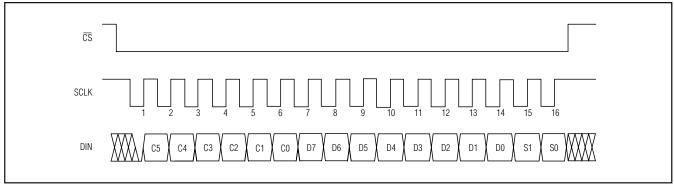


Figure 7. SPI-Interface Format

#### Applications Information

#### Daisy Chaining (SPI/ $\overline{I2C} = V_{DD}$ )

In standard SPI-/QSPITM-/MICROWIRETM-compatible systems, a microcontroller ( $\mu$ C) communicates with its slave devices through a 3- or 4-wire serial interface. The typical interface includes a chip-select signal ( $\overline{CS}$ ), a serial clock (SCLK), a data input signal (DIN), and sometimes a data signal output (DOUT). In this system, the  $\mu$ C allots an independent slave-select signal ( $\overline{SS}$ \_) to each slave device so that they can be addressed individually. Only the slaves with their  $\overline{CS}$  inputs asserted low acknowledge and respond to the activity on the serial clock and data lines. This is simple to implement when there are very few slave devices in the system.

An alternative method is daisy chaining. Daisy chaining, in serial-interface applications, is the method of propagating commands through devices connected in series (see Figure 8).

Daisy chain devices by connecting the DOUT of one device to the DIN of the next. Connect the SCLK of all devices to a common clock and connect the  $\overline{\text{CS}}$  of all devices to a common slave-select line. Data shifts out of DOUT 16.5 clock cycles after it is shifted into DIN on the falling edge of SCLK. In this configuration, the  $\mu\text{C}$  only needs three signals ( $\overline{\text{SS}}$ , SCK, and MOSI) to control all of the slaves in the network. The SPI-/QSPI-/MICROWIRE-compatible serial interface normally works at up to 10MHz, but must be slowed to 5MHz if daisy chaining. DOUT is high impedance when  $\overline{\text{CS}}$  is high.

QSPI is a trademark of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

**Table 4. Command Summary** 

			SEF	RIAL	DATA	INPUT	
C5	C4	СЗ	C2	C1	C0	D7-D0, S1 AND S0	FUNCTIONS
0	0	0	0	0	0	XXXXXXXXX	No operation.
0	0	0	0	0	1	8-bit DAC data	Load DAC data to both DAC registers and both input registers from the shift register.
0	0	0	0	1	0	8-bit DAC data	Load DAC register A and input register A from the shift register.
0	0	0	0	1	1	8-bit DAC data	Load DAC register B and input register B from the shift register.
0	0	0	1	0	0	8-bit DAC data	Load both channel input registers from the shift register; both DAC registers are unchanged.
0	0	0	1	0	1	8-bit DAC data	Load input register A from the shift register; DAC register A is unchanged.
0	0	0	1	1	0	8-bit DAC data	Load input register B from the shift register; DAC register B is unchanged.
0	0	0	1	1	1	XXXXXXXXX	Update both DAC registers from their corresponding input registers.
0	0	1	0	0	1	XXXXXXXXX	Update DAC register A from input register A.
0	0	1	0	1	0	XXXXXXXXX	Update DAC register B from input register B.
0	0	1	0	1	1	XXXXXXXXX	Internal reference mode.
0	0	1	1	0	0	XXXXXXXXX	External reference mode (default mode at power-up).
0	0	1	1	0	1	XXXXXXXXX	Shut down both DACs.
0	0	1	1	1	0	XXXXXXXXX	Shut down DACA.
0	0	1	1	1	1	XXXXXXXXX	Shut down DACB.
0	1	0	0	0	0	XXXXXXXXX	DACA 1mA-2mA full-scale current range mode (default mode at power-up)
0	1	0	0	0	1	XXXXXXXXX	DACA 1.5mA-3mA full-scale current range mode.
0	1	0	0	1	0	XXXXXXXXX	DACA 2.5mA-5mA full-scale current range mode.
0	1	0	0	1	1	XXXXXXXXX	DACA 4.5mA-9mA full-scale current range mode.
0	1	0	1	0	0	XXXXXXXXX	DACA 8mA–16mA full-scale current range mode.
0	1	0	1	0	1	XXXXXXXXX	DACA 15mA-30mA full-scale current range mode.
1	0	1	1	0	1	XXXXXXXXX	Power up both channels of the DACs.
1	0	1	1	1	0	XXXXXXXXX	Power up DACA.
1	0	1	1	1	1	XXXXXXXXX	Power up DACB.
1	1	0	0	0	0	XXXXXXXXX	DACB 1mA-2mA full-scale current range mode (default mode at power-up)
1	1	0	0	0	1	XXXXXXXXX	DACB 1.5mA–3mA full-scale current range mode.
1	1	0	0	1	0	XXXXXXXXX	DACB 2.5mA–5mA full-scale current range mode.
1	1	0	0	1	1	XXXXXXXXX	DACB 4.5mA–9mA full-scale current range mode.
1	1	0	1	0	0	XXXXXXXXX	DACB 8mA-16mA full-scale current range mode.
1	1	0	1	0	1	XXXXXXXXX	DACB 15mA-30mA full-scale current range mode.

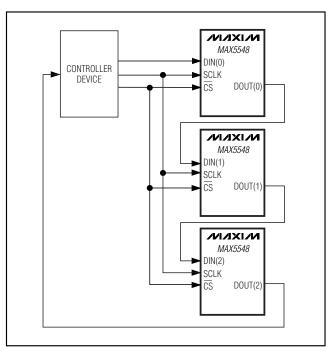


Figure 8. Daisy-Chain Configuration

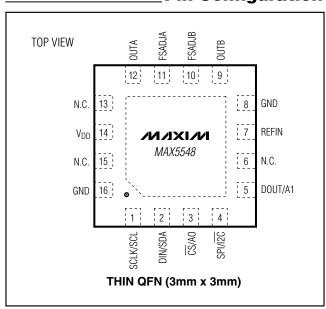
#### **Power Sequencing**

Ensure that the voltage applied to REFIN does not exceed V<sub>DD</sub> at any time. If proper power sequencing is not possible, connect an external Schottky diode between REFIN and V<sub>DD</sub> to ensure compliance with the absolute maximum ratings.

#### Power-Supply Bypassing and Ground Management

Digital or AC transient signals on GND create noise at the analog output. Return GND to the highest-quality ground plane available. For extremely noisy environments, bypass REFIN and VDD to GND with 1 $\mu$ F and 0.1 $\mu$ F capacitors with the 0.1 $\mu$ F capacitor as close to the device as possible. Careful PC board ground layout minimizes crosstalk between the DAC outputs and digital inputs.

#### Pin Configuration



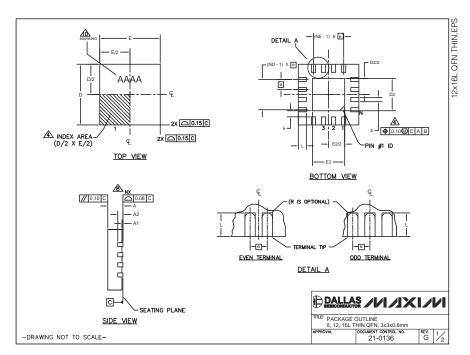
#### **Chip Information**

PROCESS: BICMOS

\_ /N/XI/N

#### Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to <a href="https://www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>.)



PKG	_	8L 3x3	_		2L 3x3		_	6L 3x3					EXF	POSE	D PAE	VAR	IATIC	ONS		
REF.	-	NOM.			NOM.	=	=	NOM.			PKG. CODES		D2			E2		PIN ID	JEDEC	DOWN BONDS
Α	0.70	0.75	0.80	0.70		0.80	0.70	0.75	0.80		CODES	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	PINID	JEDEC	ALLOWED
b	0.25	0.30	0.35	0.20	_	0.30	0.20	0.25	0.30		TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC	NO
D	2.90	3.00	3.10	2.90		3.10	2.90	3.00	3.10		T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
E	2.90	3.00 65 BS	3.10	2.90	3.00 50 BS	3.10	2.90	3.00 50 BS	3.10		T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
L	-	0.55	0.75	_		0.65	0.30	0.40	0.50		T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
N	0.33	8	0.75	0.45	12	0.00	0.30	16	0.50		T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
ND	-	2			3	_		4	-		T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
NF	_	2			3			4			T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
A1	0	0.02	0.05	0	_	0.05	0	0.02	0.05		T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
A2	-	20 RF		-	20 RF		-	20 RF			T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
2	2. ALI 3. N I 4. TH JE: WI MA 6. DIN 7. DE 6. CC	L DIME S THE E TER SD 95- THIN T RKED MENSI OM TE AND I POPU	ENSION TOTA MINAL 1 SPP THE ZO FEATO ON b A RMINA NE RE LATION ARITY	NS ARI L NUM #1 IDI 012. I DNE IN JRE. PPLIE AL TIP. FER TO N IS PO APPLI	E IN MI BER C ENTIFI DETAIL DICAT S TO I O THE DSSIBI ES TO	ILLIME F TER ER AN S OF ED. TH METAL NUME LE IN A	TERS. MINAL ID TER TERMI HE TER LIZED SER OF	. ANGI .S. MINAL # RMINA TERM TERM TERM ETERM	1 IDENTI L #1 IDEN IINAL AN MINALS C CAL FAS	ERING IFIER A INTIFIE IND IS M ON EAC SHION.	GREES. CONVENTION ARE OPTIONA R MAY BE EIT IEASURED BE	L, BUT THER A TWEEN	MUST E MOLD ( 1 0.20 m	BE LOC OR nm AND	ATED	m				

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