

## Programmable Single-/Dual-/Triple- Tone Gong

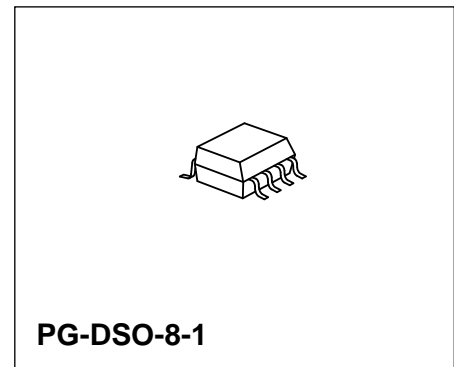
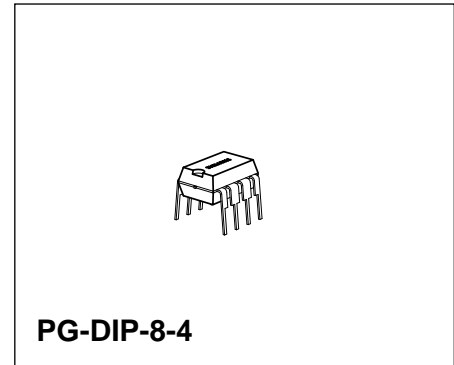
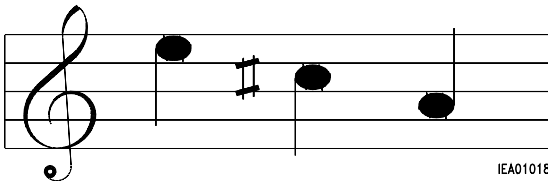
SAE 800

Pb-free lead plating; RoHS compliant

Bipolar IC

### Features

- Supply voltage range 2.8 V to 18 V
- Few external components (no electrolytic capacitor)
- 1 tone, 2 tones, 3 tones programmable
- Loudness control
- Typical standby current 1  $\mu$ A
- Constant current output stage (no oscillation)
- High-efficiency power stage
- Short-circuit protection
- Thermal shutdown



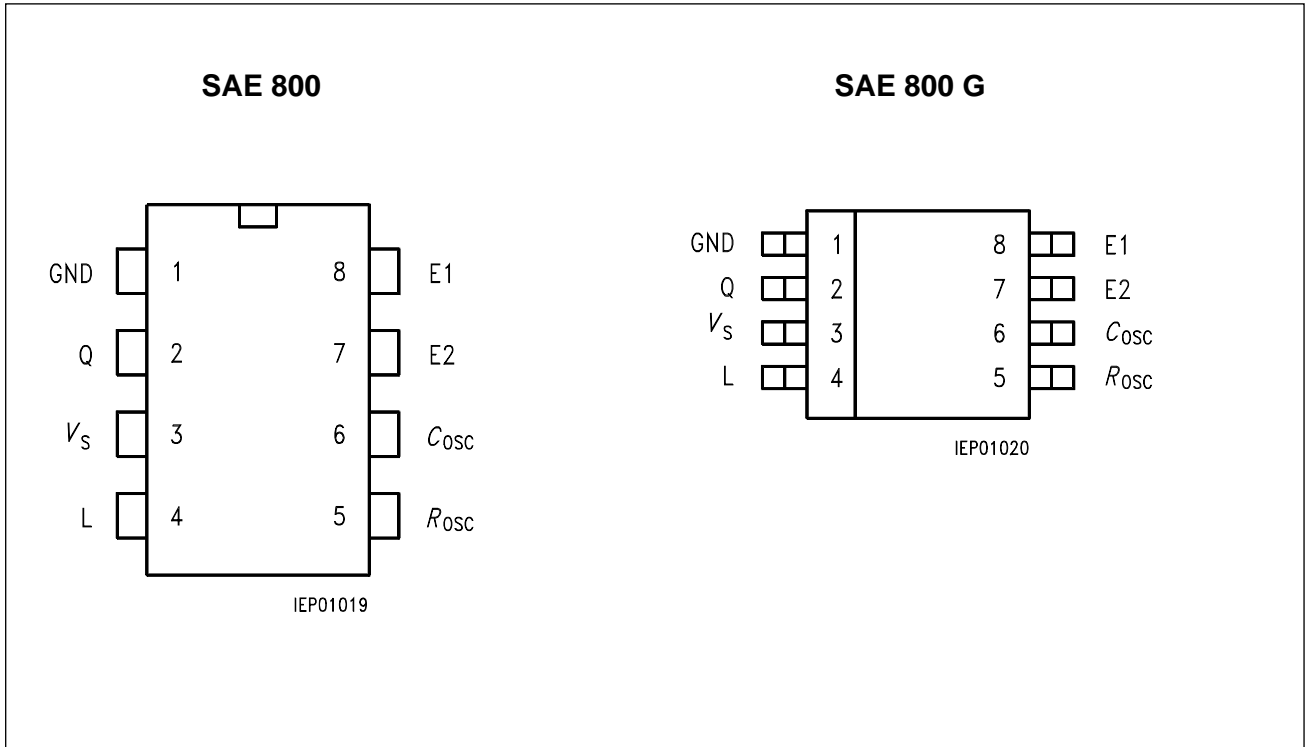
Type	Ordering Code	Package
▼ SAE 800	Q67000-A8339	PG-DIP-8-4
▼ SAE 800 G	Q67000-A8340	PG-DSO-8-1 (SMD)

▼ New type

### Functional Description

The SAE 800 is a single-tone, dual-tone or triple-tone gong IC designed for a very wide supply voltage range. If the oscillator is set to  $f_0 = 13.2$  kHz for example, the IC will issue in **triple-tone-mode** the minor and major third  $e^2 - C$  sharp – a, corresponding to 660 Hz – 550 Hz – 440 Hz, in **dual-tone-mode** the minor third  $e^2 - C$  sharp, and in **single-tone-mode** the tone  $e^2$  (derived from the fundamental frequency  $f_0$ ;  $f_1 = f_0 / 20$ ,  $f_2 = f_0 / 24$ ,  $f_3 = f_0 / 30$ ).

When it is not triggered, the IC is in a standby state and only draws a few  $\mu$ A. It comes in a compact P-DIP-8-1 or P-DSO-8-1 (SMD) package and only requires a few external components.



**Pin Configuration**  
(top view)

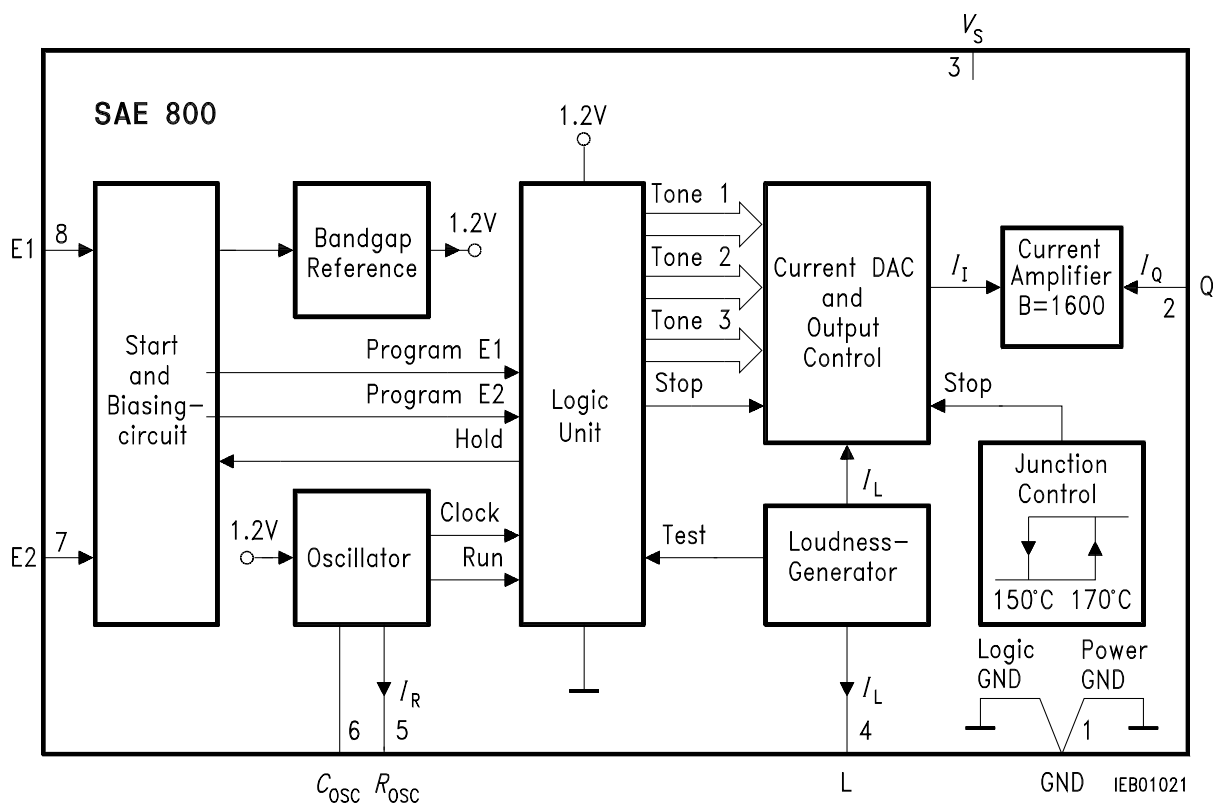
**Pin Definitions and Functions**

Pin	Symbol	Function
1	GND	Ground
2	Q	Output
3	$V_s$	Supply Voltage
4	L	Loudness Control
5	$R_{osc}$	Oscillator Resistor
6	$C_{osc}$	Oscillator Capacitor
7	E2	Trigger 2 (dual tone)
8	E1	Trigger 1 (single tone)

**Functional Description** (cont'd)

An RC combination is needed to generate the fundamental frequency (pin  $R_{osc}$ ,  $C_{osc}$ ). The volume can be adjusted with another resistor (pin L). The loudspeaker must be connected directly between the output Q and the power supply  $V_s$ . The current-sink principle combined with an integrated thermal shutdown (with hysteresis) makes the IC overload-protected and shortcircuit-protected.

There are two trigger pins (E1, E2) for setting single-tone, dual-tone or triple-tone mode.



Block Diagram

**Circuit Description**

**Trigger**

Positive pulses on inputs E1 and/or E2 trigger the IC. The hold feedback in the logic has a delay of several milliseconds. After this delay has elapsed, the tone sequence is started. This prevents parasitic spikes from producing any effect on the trigger pins.

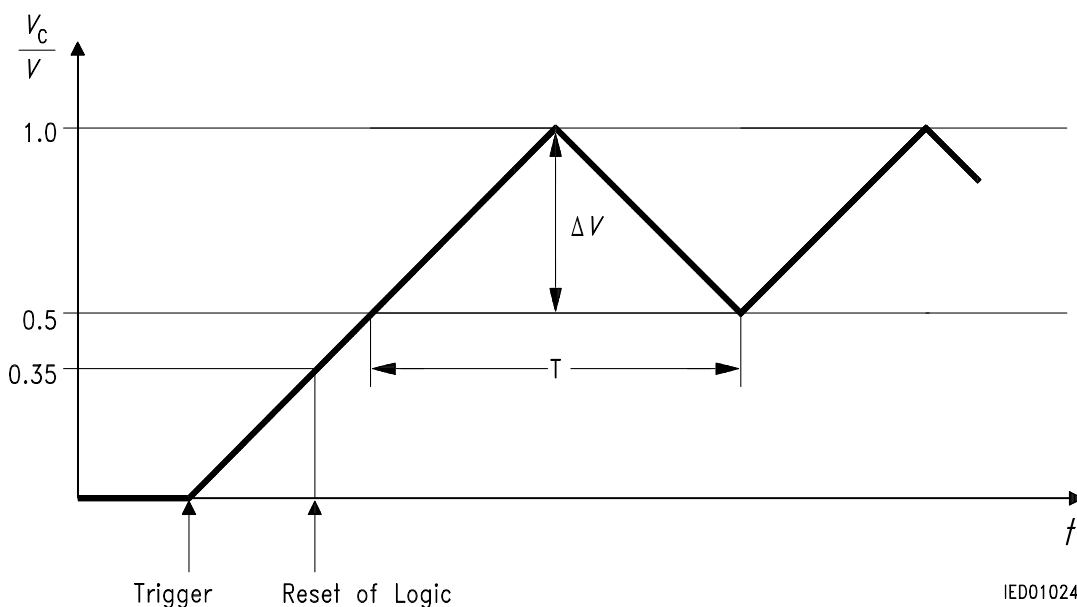
The following **table** shows the trigger options:

E1	E2	Mode	Issued Sequence
Triggered	Triggered	Triple-tone	Minor and major third
Grounded/open	Triggered	Dual-tone	Minor third
Triggered	Grounded/open	Single-tone	1st tone of minor third

**Oscillator**

This is a precision triangle oscillator with an external time constant ( $R \times C$ ). Capacitor  $C_C$  on pin  $C_{OSC}$  is charged by constant current to 1 V and then discharged to 0.5 V. The constant current is obtained on pin  $R_{OSC}$  with an external resistor  $R_R$  to ground.

When the voltage on  $C_{OSC}$  is building up, the logic is reset at 350 mV. This always ensures that a complete tone sequence is issued. If the oscillator pin is short-circuited to GND during operation, the sequence is repeated.



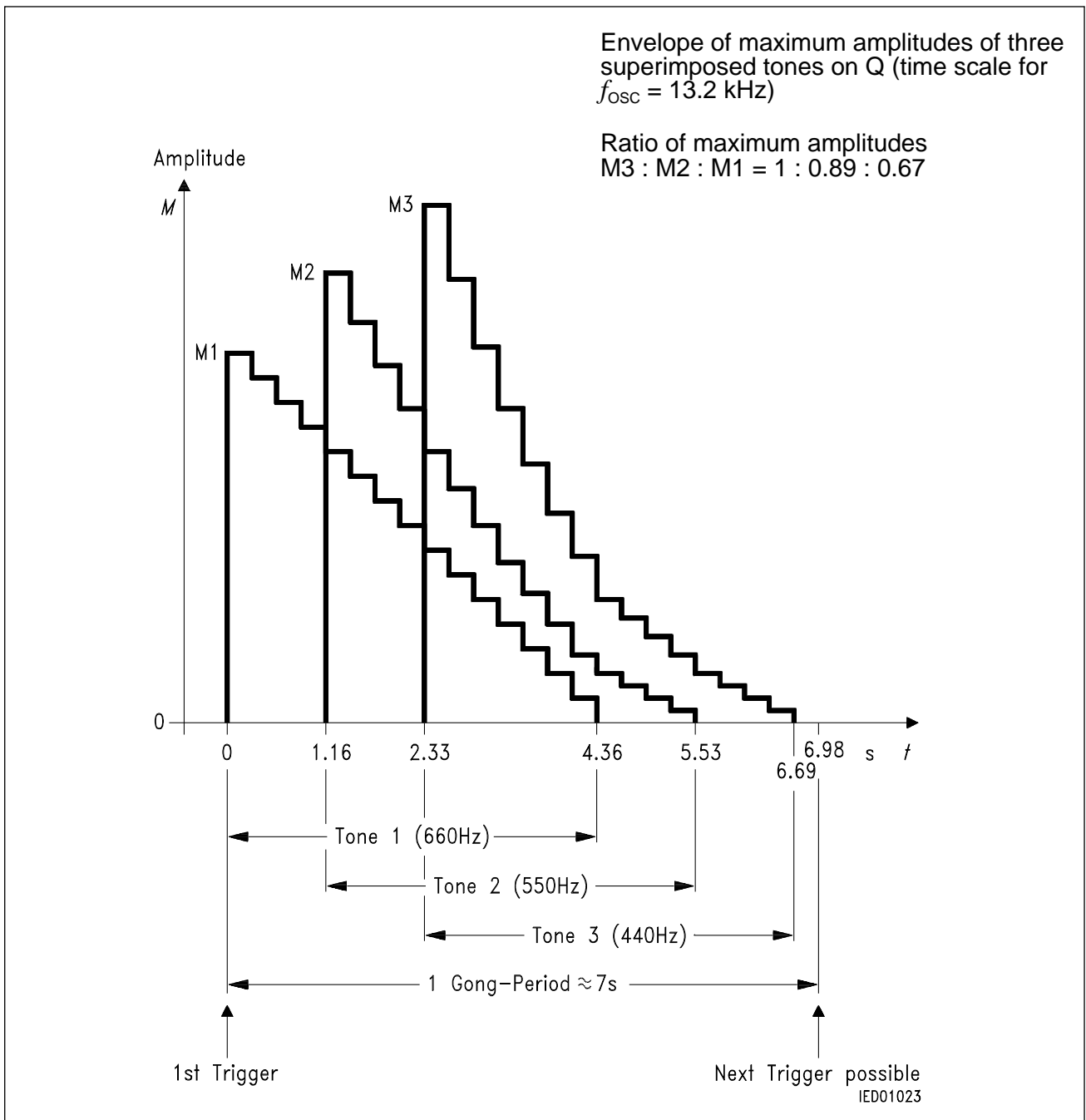
The following applies:  $\Delta V_C \times C_C = I_C \times T/2$  with  $I_C = V_R/2R_R = 1.2 \text{ V}/2R_R$   
 $f_0 = 5/8 \times 1/(R_R \times C_C)$

**Voltages on Pin  $C_{osc}$**

**Logic**

The logic unit contains the complete sequence control. The oscillator produces the power-on reset and the clock frequency. Single-tone, dual-tone or triple-tone operation is programmed on inputs E1 and E2. The 4-bit digital/analog converters are driven in parallel. In the event of oscillator disturbance, and after the sequence, the dominant stop output is set. By applying current to pin L, the sequence can be shortened by a factor of 30 for test purposes.

The following figure shows the envelope of the triple-tone sequence:



**Envelope of the Triple-Tone Sequence**

## Digital / Analog Converter, Loudness and Junction Control

The DAC converts the 4-bit words from the logic into the appropriate staircase currents with the particular tone frequency. The sum current  $I_I$  drives the following current amplifier. The loudness generator produces the DAC reference current  $I_L$  for all three tones. This requires connecting an external resistor to ground. The chip temperature is monitored by the junction control. At temperatures of more than approx. 170 °C the stop input will switch the output current  $I_I$  to zero. The output current is enabled again once the chip has cooled down to approx. 150 °C.

### Current Amplifier

The current amplifier with a gain of 1600 boosts the current  $I_I$  from approx. 470  $\mu$ A maximum to approx. 750 mA maximum. The output stage consists of an NPN transistor with its emitter on power GND and collector on pin Q.

The current control insures that the output stage only conducts defined currents. In conjunction with the integrated thermal shutdown, this makes the configuration shortcircuit-protected within wide limits. Because of the absence of feedback the circuit is also extremely stable and therefore uncritical in applications. Resistor  $R_L$  on pin L sets the output voltage swing. This assumes that the resistive component of the loudspeaker impedance  $R_Q$  responds similarly as the resistance  $R_L$ .

The output amplitude of the current  $I_I$  reaches the maximum  $I_{I_{max}} \cong 3 \times V_L / R_L$  at a time  $t$  of 2.33 s (only 3 tone mode), so  $R_L$  has to be scaled for this point.

The following applies:

$$I_Q = I_{I_{max}} \times B = (V_S - V_{sat}) / R_Q \approx 0.8 V_S / R_Q$$

$$3 \times B \times (V_L / R_L) \approx 0.8 V_S / R_Q$$

the result is:

$$R_L = R_Q \times 3 \times B \times (V_L / 0.8 V_S)$$

with: B = 1600

$$R_L = R_Q \times K \times (V_L / 0.8 V_S)$$

with: K = 4800

## Application Hints and Application Circuit

### 1) Loudness Resistor (max. Load Current of 3-Tone Signal with Ensured Ratio of Amplitudes)

$$0.8 V_S / R_Q \approx (V_L / R_L) \times K$$

$$R_L = (V_L / 0.8 V_S) \times R_Q \times K; K = 4800$$

Example:  $R_Q = 8 \Omega$ ;  $V_S = 5 V$ ;  $V_L = 1.2 V$

$$R_L = (1.2 / 4) \times 8 \Omega \times 4800 \approx 12 k\Omega$$

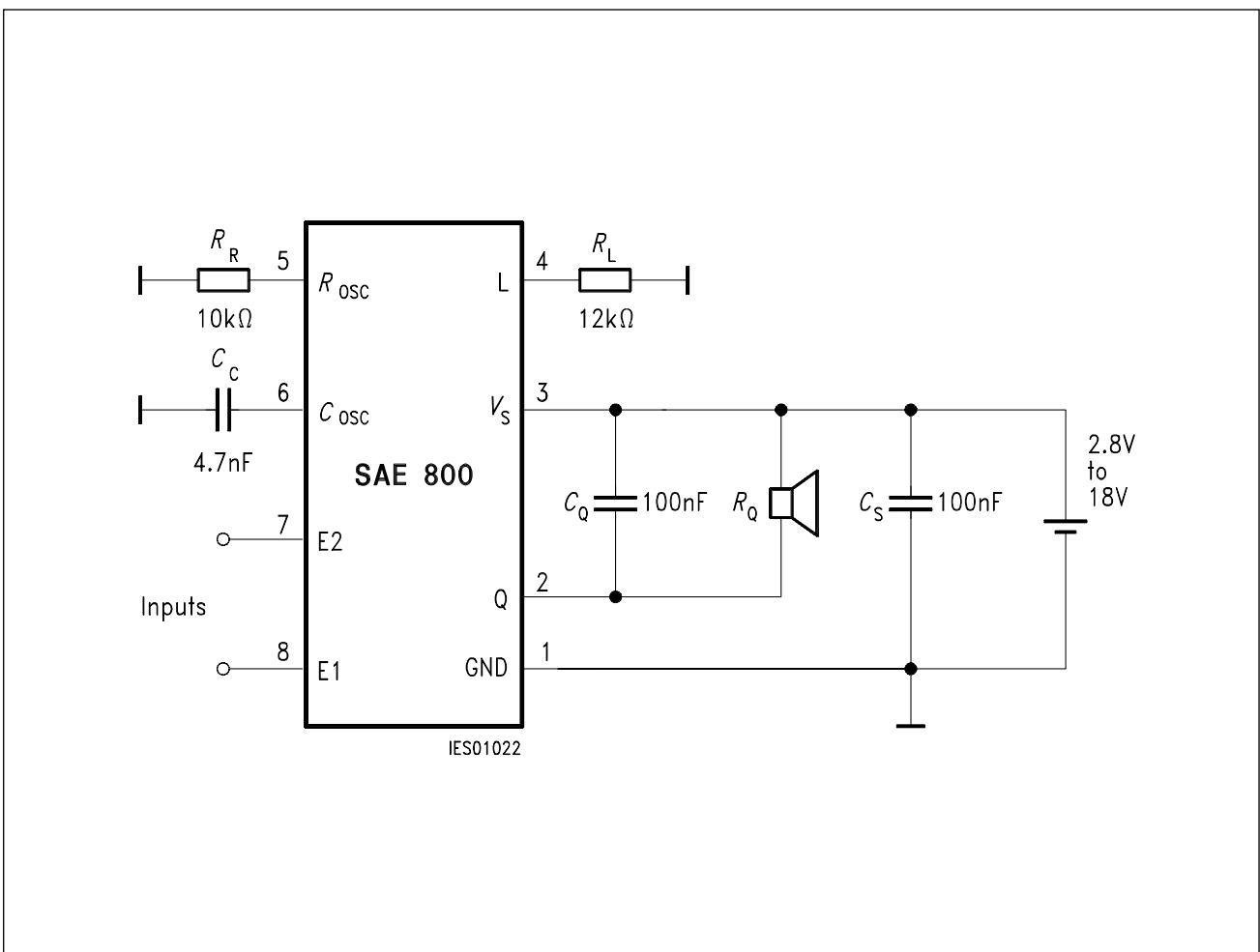
### 2) Oscillator Elements $R_R$ , $C_C$

$$f = 5 / 8 \times 1 / (R_R \times C_C)$$

Example:  $f = 13.2 kHz$ ;  $C_C = 4.7 nF$

$$R_R = 5 / (8 \times 13.2 \times 4.7) \times 10^6 \Omega \approx 10 k\Omega$$

The following is a typical application circuit



## Application Circuit

## Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_S$	- 0.3	24	V
Input voltage at E1, E2	$V_{E1, E2}$	- 5	24	V
Current at output Q	$I_Q$	- 50	750	mA
Current at input pins E1, E2	$I_{E1, E2}$	- 2	3	mA
Current at pin $R_{OSC}$	$I_R$	- 300	200	$\mu$ A
Current at pin L	$I_L$	- 300	200	$\mu$ A
Current at pin $C_{OSC}$	$I_C$	- 200	200	$\mu$ A
Junction temperature	$T_j$	- 50	150	$^{\circ}$ C
Storage temperature	$T_{stg}$	- 50	150	$^{\circ}$ C

## Operating Range

Supply voltage	$V_S$	2.8	18	V
Junction temperature	$T_j$	- 25	125	$^{\circ}$ C
Oscillator frequency at $C_{OSC}$	$f_C$		100	kHz
Current at pin $R_{OSC}$	$I_R$	- 200	- 10	$\mu$ A
Current for test mode at pin L	$I_R$	90	110	$\mu$ A
Current at pin L	$I_L$	- 200	- 10	$\mu$ A
Input voltage at E1, E2	$V_{E1, E2}$	- 4	18	V
Thermal resistance junction-air (PG-DIP-8-4)	$R_{th JA}$		100	K/W
junction-air (PG-DSO-8-1)	$R_{th JA}$		180	K/W



## Characteristics

$T_j = -25$  to  $125^\circ\text{C}$ ;  $V_S = 2.8$  to  $18$  V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

## Supply Section

Standby current	$I_{St}$		1	10	$\mu\text{A}$	
Quiescent current; pin L open	$I_{Qu}$		5	10	mA	

## Output Section

Peak output power (tone 3)						
$V_S = 2.8$ V; $R_Q = 4$ $\Omega$ ; $R_L = 8.2$ k $\Omega$	$P_Q$	250	330		mW	A
$V_S = 2.8$ V; $R_Q = 8$ $\Omega$ ; $R_L = 18$ k $\Omega$	$P_Q$	125	165		mW	
$V_S = 5.0$ V; $R_Q = 8$ $\Omega$ ; $R_L = 10$ k $\Omega$	$P_Q$	450	600		mW	
$V_S = 5.0$ V; $R_Q = 16$ $\Omega$ ; $R_L = 18$ k $\Omega$	$P_Q$	225	300		mW	
$V_S = 12$ V; $R_Q = 50$ $\Omega$ ; $R_L = 33$ k $\Omega$	$P_Q$	450	600		mW	
Output level differences:						
tone 1 to 3	$a_{13}$	- 1		1	dB	A <sup>1)</sup>
tone 2 to 3	$a_{23}$	- 1		1	dB	A <sup>2)</sup>

## Biasing Section

Voltage at pin $R_{OSC}$ ; $R_R = 10$ k $\Omega$	$V_R$		1.2		V	
Voltage at pin L; $R_L = 10$ k $\Omega$	$V_L$		1.2		V	

## Oscillator Section

Amplitude	$\Delta V_C$		0.5		V	
Frequency $R_R = 10$ k $\Omega$ ; $C_C = 4.7$ nF	$f_0$		13.2		kHz	
Oscill. drift vs. temperature	$D_T$	- 3		+ 3	$10^{-4}/\text{K}$	
Oscill. drift vs. supply voltage	$D_V$		1		$10^{-3}/\text{K}$	

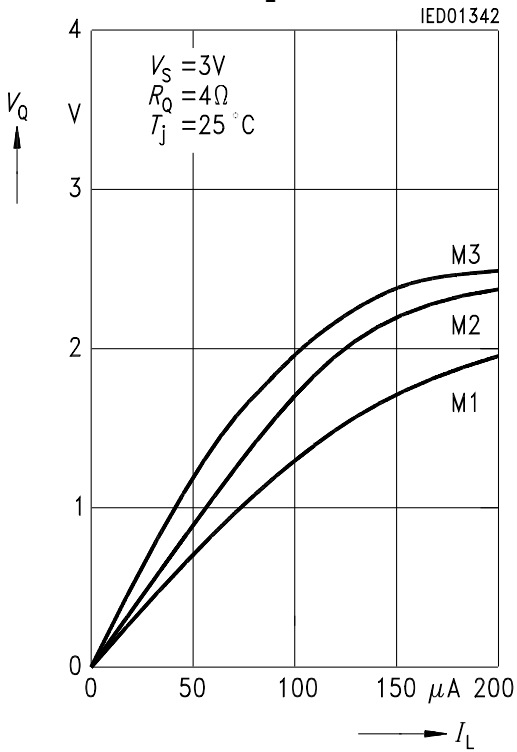
## Input Section

Triggering voltage at E1, E2	$V_{E1, E2}$	1.6			V	
Triggering current at E1, E2	$I_{E1, E2}$	100			$\mu\text{A}$	
Noise voltage immunity at E1, E2	$V_{E1, E2}$			0.3	V	
Triggering delay at $f_0 = 13.2$ kHz	$t_{dT}$	2		10	ms	

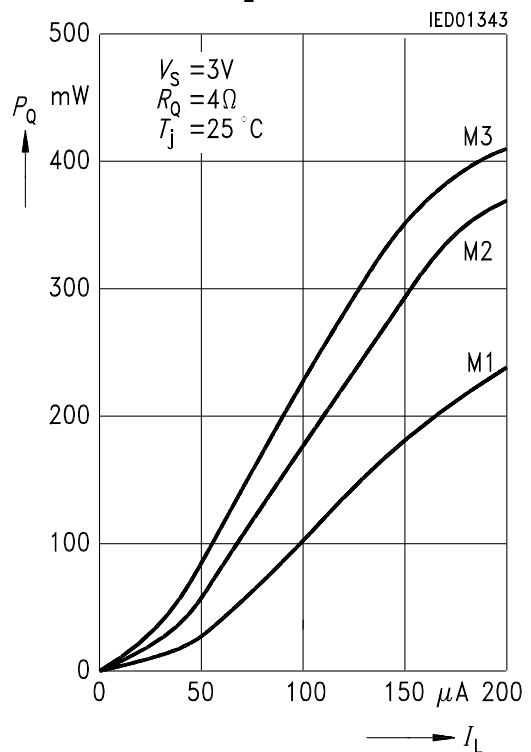
1)  $a_{13} = 20 \times \log (M1 / (0.67 \times M3))$

2)  $a_{23} = 20 \times \log (M2 / (0.89 \times M3))$

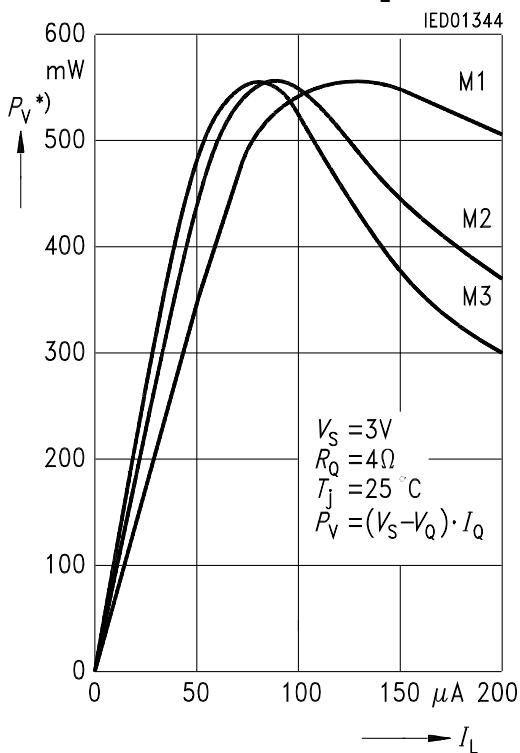
Output Peak Voltage  $V_Q$  versus Loudness-Current  $I_L$



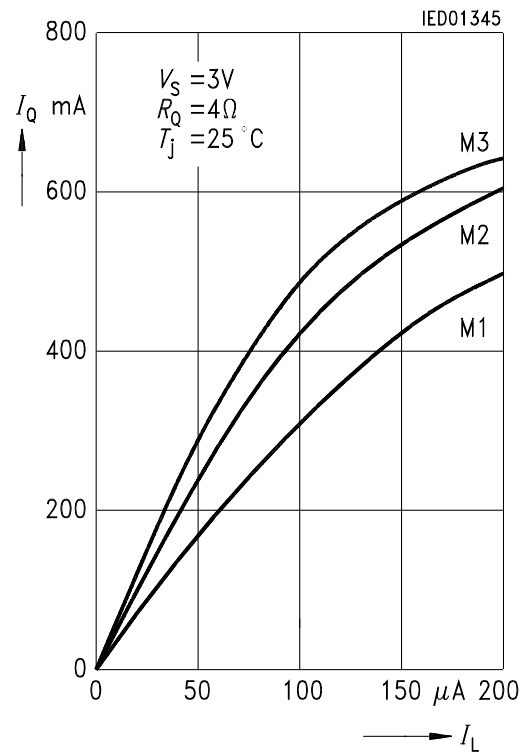
Max. Output Power  $P_Q$  versus Loudness-Current  $I_L$



Power Dissipation  $P_V$  of Output Stage versus Loudness-Current  $I_L$

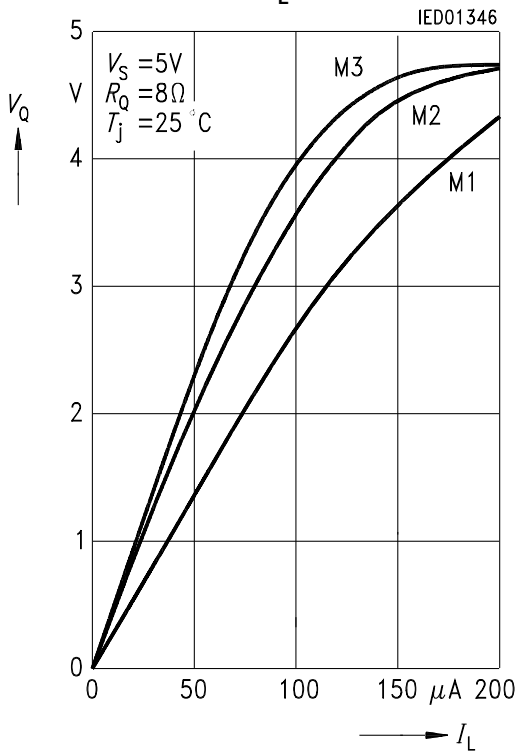


Peak Current  $I_Q$  versus Loudness-Current  $I_L$

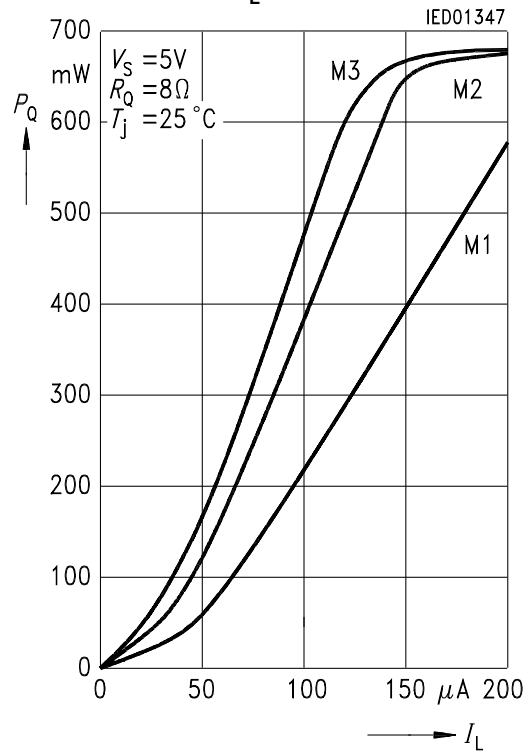


\*) Note that  $I_Q = f(I_L)$  varies between 0 and  $K \cdot I_L$  during tone sequence. Thereby the maximum of the power dissipation during the tone sequence is the maximum of  $P_V$  (in diagram) between  $I_L = 0$  and chosen  $I_L = V_L/R_L$ .

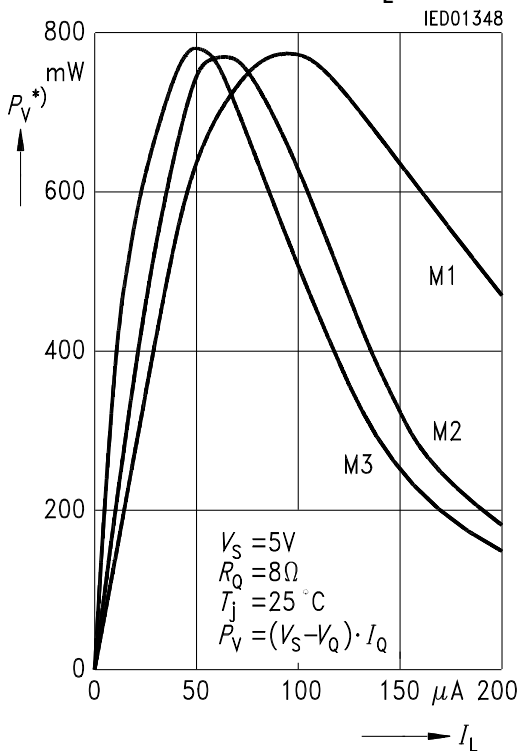
Output Peak Voltage  $V_Q$  versus Loudness-Current  $I_L$



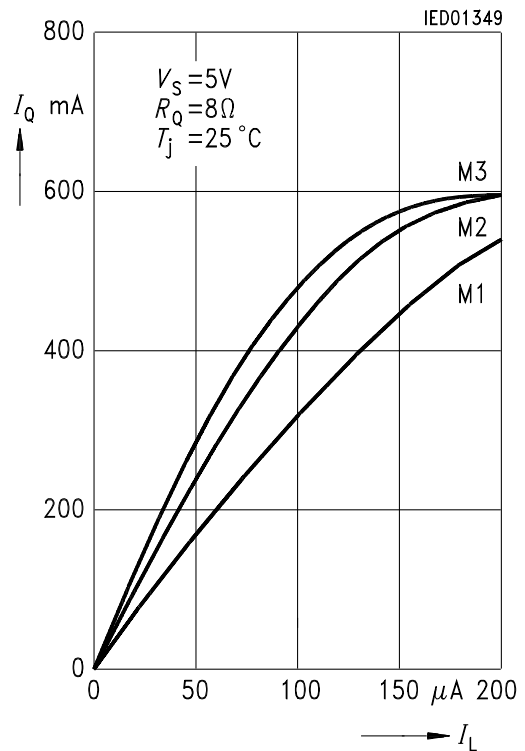
Max. Output Power  $P_Q$  versus Loudness-Current  $I_L$



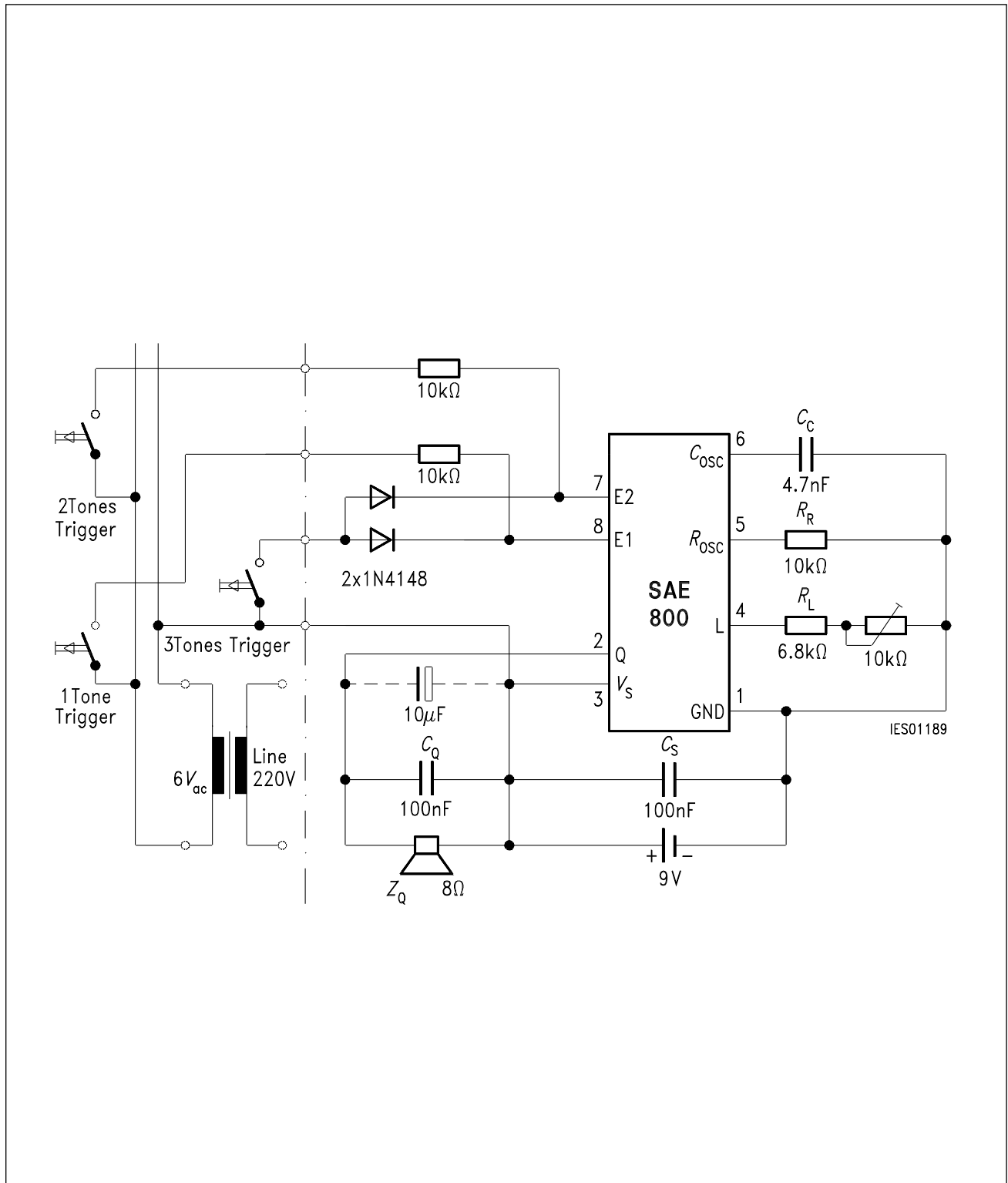
Power Dissipation  $P_V$  of Output Stage versus Loudness-Current  $I_L$



Peak Current  $I_Q$  versus Loudness-Current  $I_L$

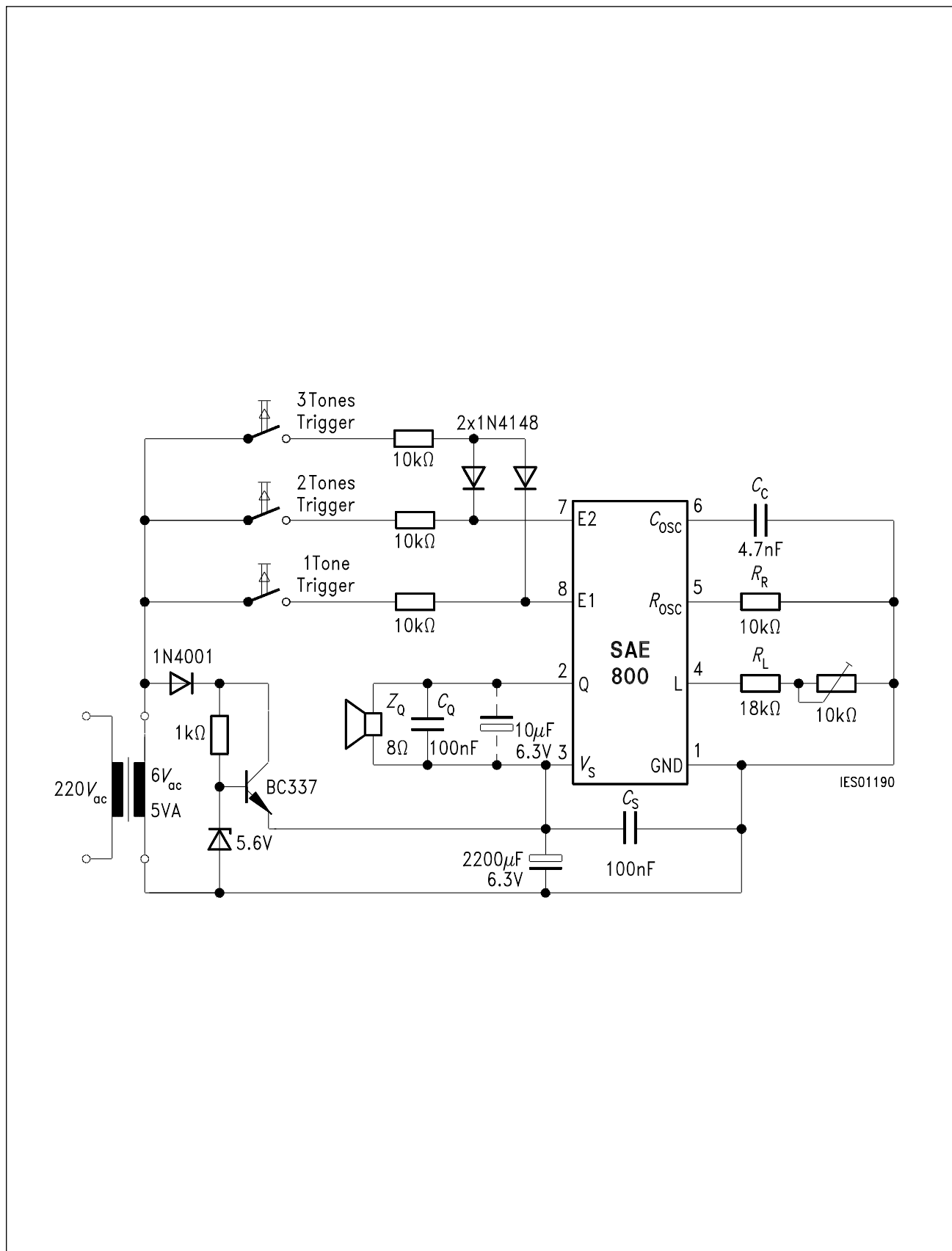


\*) Note that  $I_Q = f(I_L)$  varies between 0 and  $K \cdot I_L$  during tone sequence. Thereby the maximum of the power dissipation during the tone sequence is the maximum of  $P_V$  (in diagram) between  $I_L = 0$  and chosen  $I_L = V_L/R_L$ .



**Circuit for SAE 800 Application in Home Chime Installation Utilizing AC and DC Triggering for 1, 2 or 3 Tone Chime; Adjustable Volume**

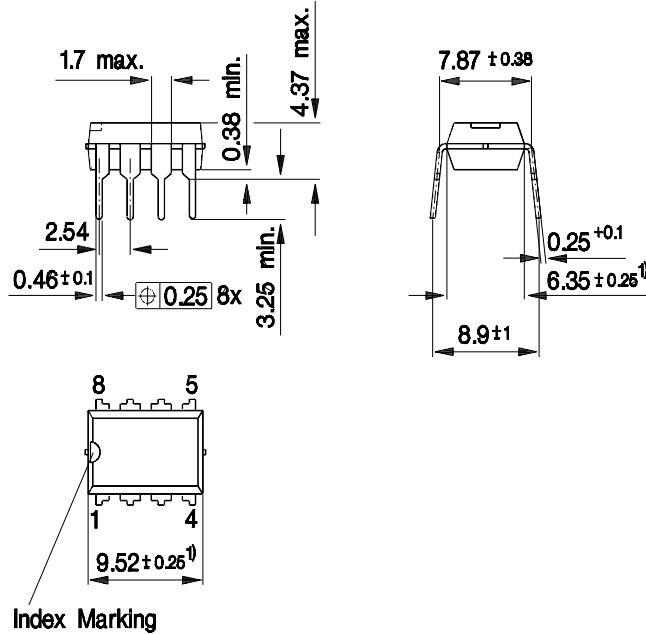
PCB layout information: Because of the peak currents at  $V_s$ , Q and GND the lines should be designed in a flatspread way or as star pattern.



Circuit for SAE 800 Application in Home Chime Installation for Operation without Battery

Package Outlines

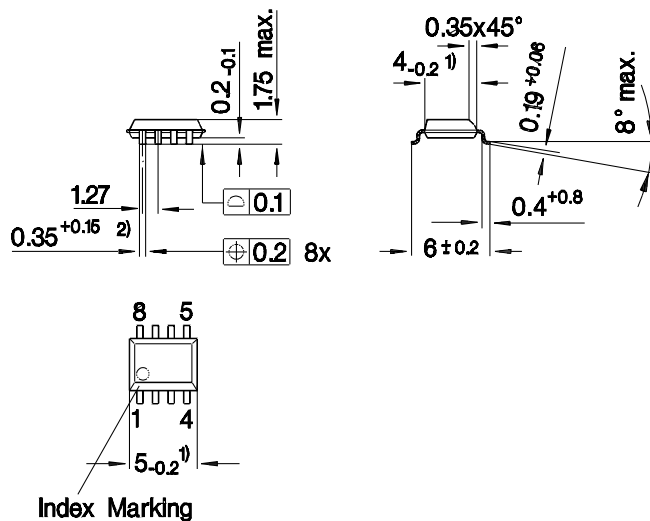
**Plastic-Package, PG-DIP-8-4**  
(Plastic Dual In-Line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05583

**Plastic-Package, PG-DSO-8-1 (SMD)**  
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side  
2) Does not include dambar protrusion

GPS05121

SMD = Surface Mounted Device

Dimensions in mm

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