

64K x 16 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

NOVEMBER 2005

FEATURES

- High-speed access time: 8, 10, 12 ns
- CMOS low power operation
 - 61LV6416:
 - 75 mW (typical) operating current
 - 0.5 mW (typical) standby current
 - 61LV6416L:
 - 65 mW (typical) operating current
 - 50 μ W (typical) standby current
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

DESCRIPTION

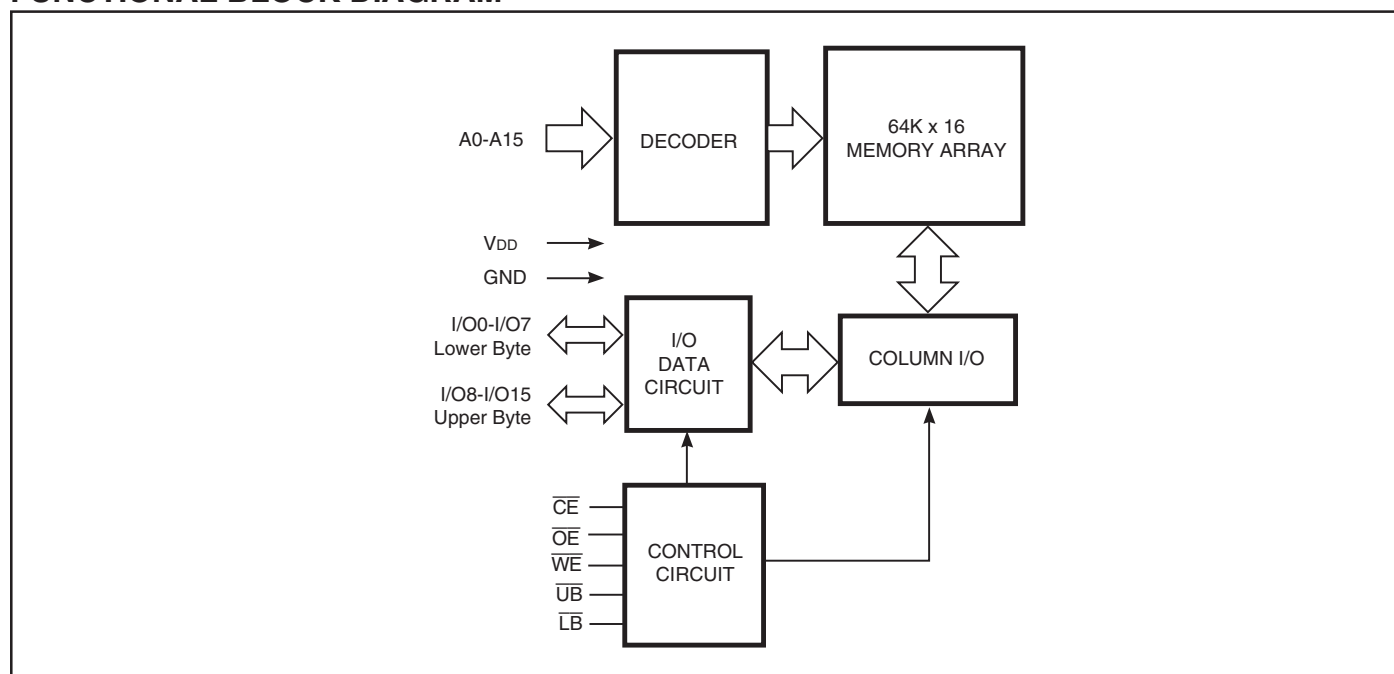
The *ISSI* IS61LV6416/IS61LV6416L is a high-speed, 1,048,576-bit static RAM organized as 65,536 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS61LV6416/IS61LV6416L is packaged in the JEDEC standard 44-pin 400-mil SOJ, 44-pin TSOP-II, and 48-pin mini BGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATIONS

44-Pin SOJ (K)



44-Pin TSOP-II (T)



48-Pin mini BGA (6mm x 8mm) (B)



PIN DESCRIPTIONS

| | |
|-----------------|---------------------------------|
| A0-A15 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{LB} | Lower-byte Control (I/O0-I/O7) |
| \overline{UB} | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| VDD | Power |
| GND | Ground |

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | \overline{LB} | \overline{UB} | I/O PIN | | V _{DD} Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------|------------|-------------------------------------|
| | | | | | | I/O0-I/O7 | I/O8-I/O15 | |
| Not Selected | X | H | X | X | X | High-Z | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | H | L | H | X | X | High-Z | High-Z | I _{CC} |
| | X | L | X | H | H | High-Z | High-Z | |
| Read | H | L | L | L | H | DOUT | High-Z | I _{CC} |
| | H | L | L | H | L | High-Z | DOUT | |
| | H | L | L | L | L | DOUT | DOUT | |
| Write | L | L | X | L | H | DIN | High-Z | I _{CC} |
| | L | L | X | H | L | High-Z | DIN | |
| | L | L | X | L | L | DIN | DIN | |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{DD} +0.5 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.5 | W |
| I _{OUT} | DC Output Current (LOW) | 20 | mA |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

| Range | Ambient Temperature | V _{DD} (8,10 ns) | V _{DD} (12 ns) |
|------------|---------------------|---------------------------|-------------------------|
| Commercial | 0°C to +70°C | 3.3V+10%,-5% | 3.3V ± 10% |
| Industrial | -40°C to +85°C | 3.3V+10%,-5% | 3.3V ± 10% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|----------------------------------|-------------------------------------------------------------|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -4.0 mA | 2.4 | — | V |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 8.0 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | -2 | 2 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | -2 | 2 | μA |

Notes:

1. V_{IL} (min.) = -2.0V for pulse width less than 10 ns.

IS61LV6416

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -8 ns | | -10 ns | | -12 ns | | Unit |
|------------------|--------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------|------|--------|------|--------|------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. | — | 140 | — | 120 | — | 100 | mA |
| | | | Ind. | — | 150 | — | 130 | — | 110 | |
| | | | typ. ⁽²⁾ | — | 105 | — | 95 | — | 75 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} CE ≥ V _{IH} , f = 0 | Com. | — | 15 | — | 15 | — | 15 | mA |
| | | | Ind. | — | 20 | — | 20 | — | 20 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., CE ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 5 | — | 5 | — | 5 | mA |
| | | | Ind. | — | 10 | — | 10 | — | 10 | |
| | | | typ. ⁽²⁾ | — | 0.5 | — | 0.5 | — | 0.5 | |

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD}=3.3V, T_A=25°C. Not 100% Tested.

IS61LV6416L

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -8 ns | | -10 ns | | Unit |
|------------------|--------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------|------|--------|------|------|
| | | | | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. | — | 100 | — | 95 | mA |
| | | | Ind. | — | 110 | — | 105 | |
| | | | typ. ⁽²⁾ | — | 75 | — | 70 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} CE ≥ V _{IH} , f = 0 | Com. | — | 15 | — | 15 | mA |
| | | | Ind. | — | 20 | — | 20 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., CE ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 1 | — | 1 | mA |
| | | | Ind. | — | 1.5 | — | 1.5 | |
| | | | typ. ⁽²⁾ | — | 0.05 | — | 0.05 | |

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD}=3.3V, T_A=25°C. Not 100% Tested.

CAPACITANCE⁽¹⁾

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Note:

- Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

| Parameter | Unit |
|---------------------------------------------|-----------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1a and 1b |

AC TEST LOADS



Figure 1a.



Figure 1b.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

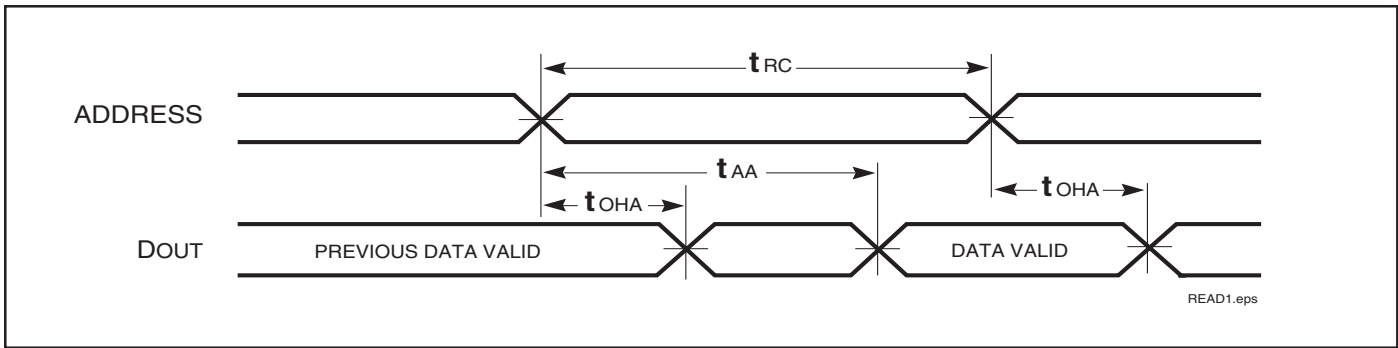
| Symbol | Parameter | -8 ns | | -10 ns | | -12 ns | | Unit |
|---------------------------------|----------------------------------------------------|-------|------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | 12 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | — | 12 | ns |
| t _{OH} | Output Hold Time | 3 | — | 3 | — | 3 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 8 | — | 10 | — | 12 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 5 | — | 5 | — | 6 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | — | 5 | — | 5 | — | 6 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 0 | — | 0 | — | 0 | — | ns |
| t _{HZCE⁽²⁾} | \overline{CE} to High-Z Output | 0 | 4 | 0 | 5 | 0 | 6 | ns |
| t _{LZCE⁽²⁾} | \overline{CE} to Low-Z Output | 3 | — | 3 | — | 3 | — | ns |
| t _{BA} | \overline{LB} , \overline{UB} Access Time | — | 6 | — | 6 | — | 6 | ns |
| t _{HZB} | \overline{LB} , \overline{UB} to High-Z Output | 0 | 4 | 0 | 5 | 0 | 6 | ns |
| t _{LZB} | \overline{LB} , \overline{UB} to Low-Z Output | 0 | — | 0 | — | 0 | — | ns |

Notes:

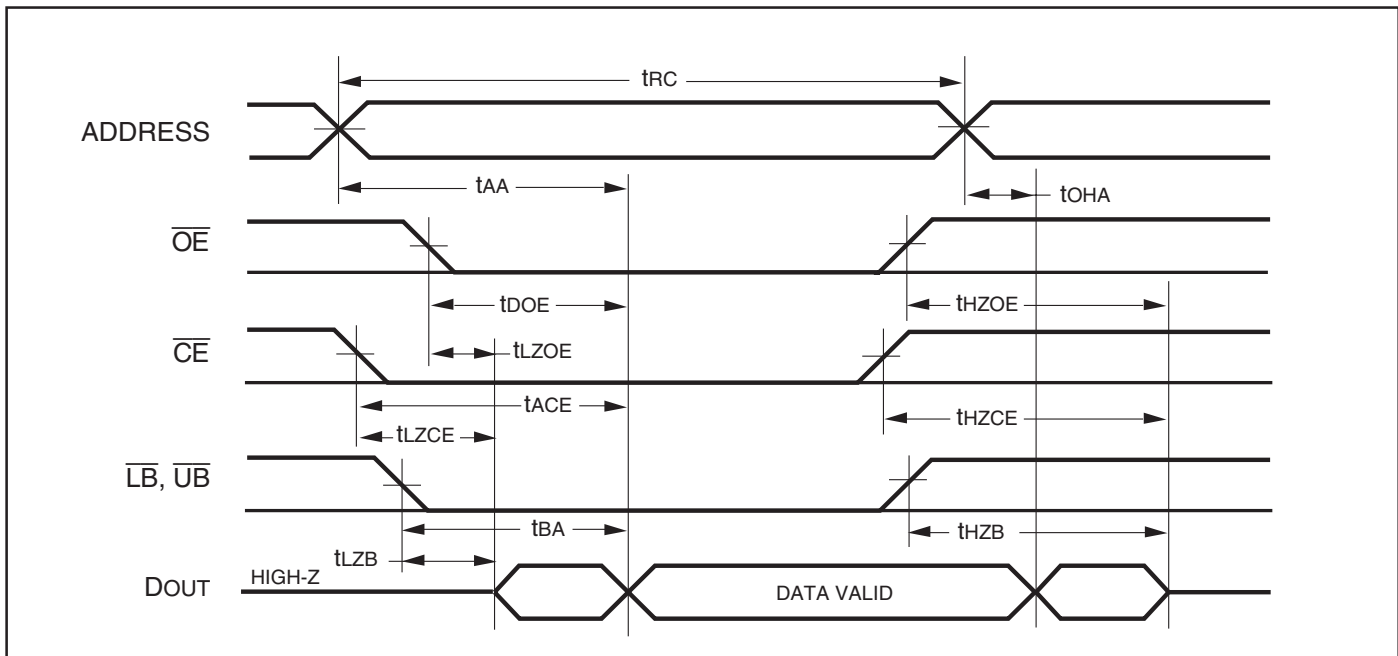
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CS} = \overline{OE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

| Symbol | Parameter | -8 ns | | -10 ns | | -12 ns | | Unit |
|--------------------------------------|-----------------------------------------------------------|-------|------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | 12 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 6 | — | 8 | — | 9 | — | ns |
| t _{AW} | Address Setup Time to Write End | 8 | — | 8 | — | 9 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | 0 | — | ns |
| t _{PBW} | \overline{LB} , \overline{UB} Valid to End of Write | 7 | — | 8 | — | 9 | — | ns |
| t _{PWE1} /t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = HIGH/LOW) | 6 | — | 8 | — | 9 | — | ns |
| t _{SD} | Data Setup to Write End | 6 | — | 6 | — | 6 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{HZWE⁽²⁾} | \overline{WE} LOW to High-Z Output | — | 4 | — | 5 | — | 6 | ns |
| t _{LZWE⁽²⁾} | \overline{WE} HIGH to Low-Z Output | 3 | — | 3 | — | 3 | — | ns |

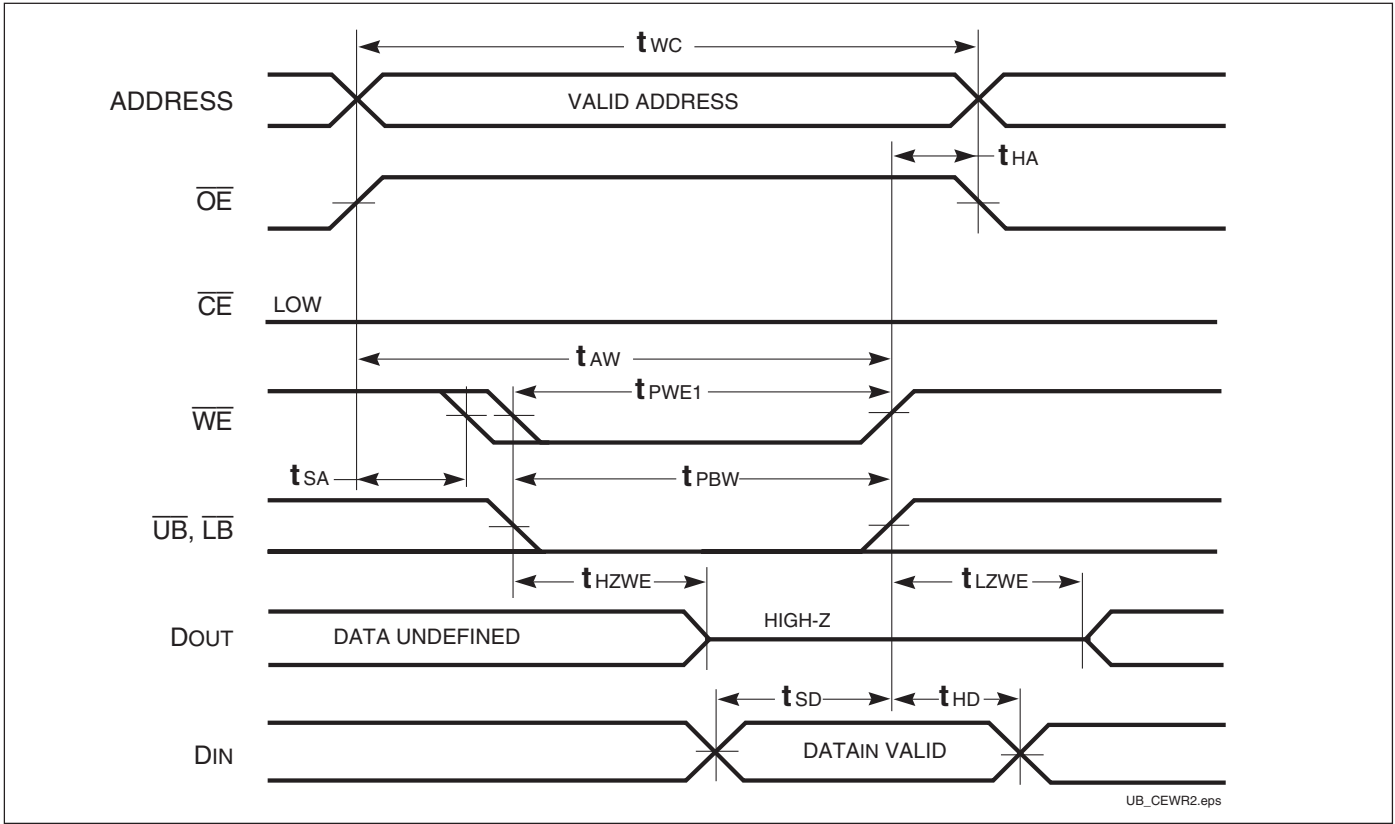
Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{UB} or \overline{LB} , and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

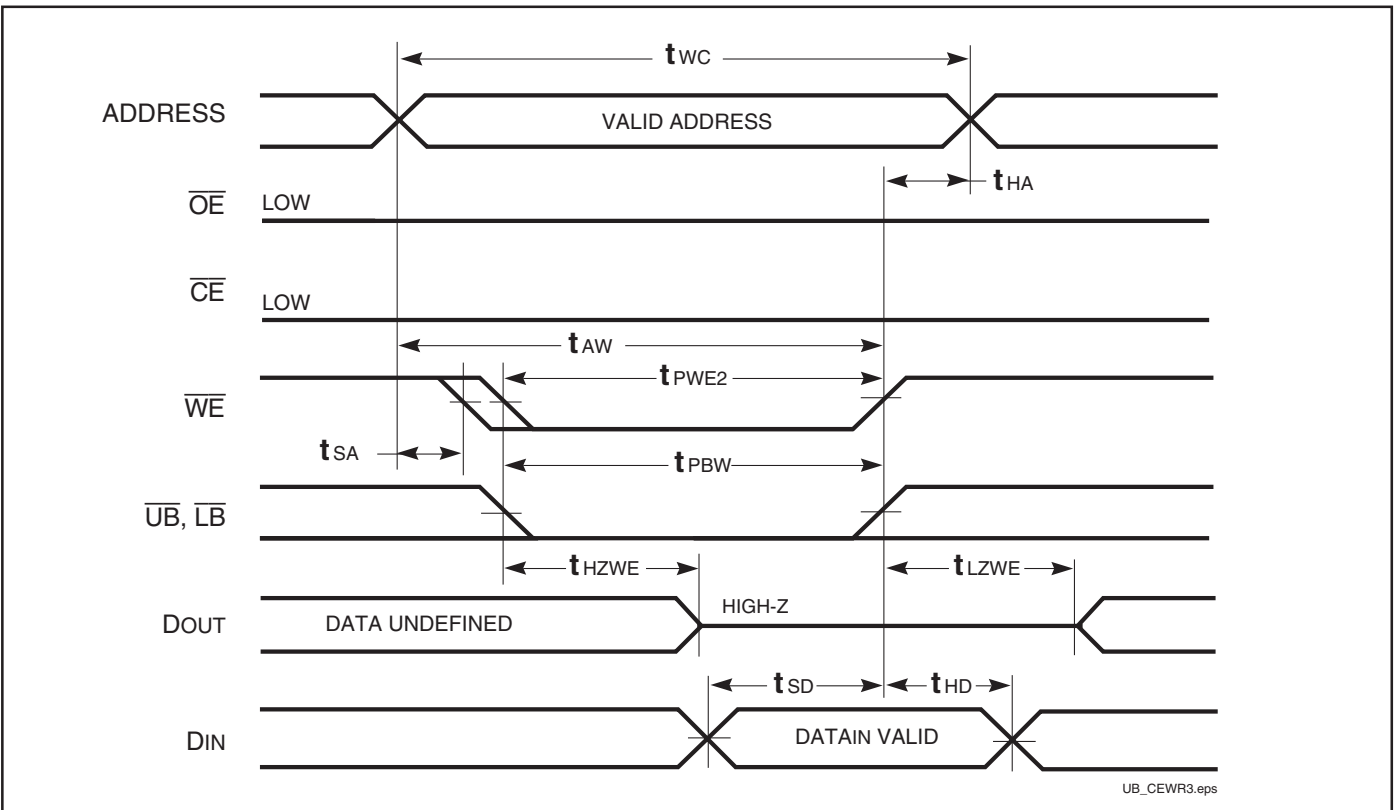
WRITE CYCLE NO. 1^(1,2) (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)



WRITE CYCLE NO. 2⁽¹⁾ (\overline{WE} Controlled, \overline{OE} = HIGH during Write Cycle)



WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled, Back-to-Back Write)^(1,3)



Notes:

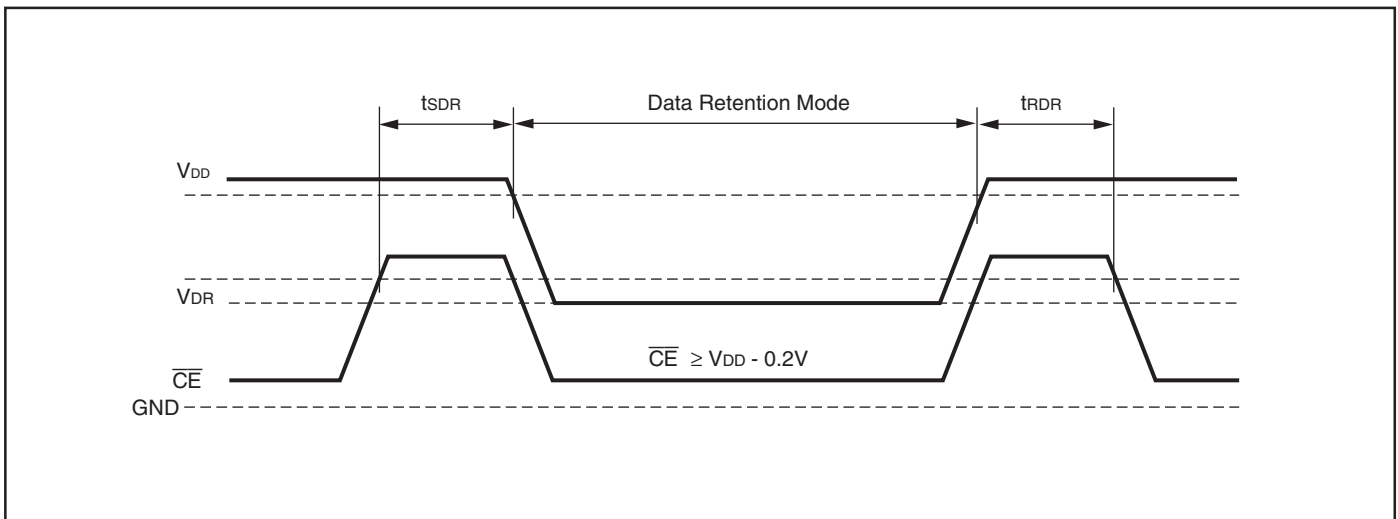
1. The internal Write time is defined by the overlap of $\overline{\text{CE}} = \text{LOW}$, $\overline{\text{UB}}$ and/or $\overline{\text{LB}} = \text{LOW}$, and $\overline{\text{WE}} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{\text{OE}}$ HIGH for a minimum of 4 ns before $\overline{\text{WE}} = \text{LOW}$ to place the I/O in a HIGH-Z state.
3. $\overline{\text{WE}}$ may be held LOW across many address cycles and the $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins can be used to control the Write function.

DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Options | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|------------------|------------------------------------|------------------------------------------------------------|---------------------------|-----------------|---------------------|-----------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | | 2.0 | — | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | IS61LV6416 IS61LV6416L | — | 0.5 0.05 | 10 1.5 | mA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | | t _{rc} | — | — | ns |

Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



IS61LV6416

ORDERING INFORMATION

| Speed (ns) | Order Part No. | Package | Temperature Range |
|-------------------|-----------------------|----------------------|----------------------------------------|
| 8 | IS61LV6416-8T | Plastic TSOP | Commercial (0°C to +70°C) |
| 8 | IS61LV6416-8TL | Plastic TSOP | Commercial (0°C to +70°C), Lead-free |
| 8 | IS61LV6416-8BI | mini BGA (6mm x 8mm) | Industrial (-40°C to +85°C) |
| 8 | IS61LV6416-8TI | Plastic TSOP | Industrial (-40°C to +85°C) |
| 8 | IS61LV6416-8KL | 400-mil Plastic SOJ | Commercial (0°C to +70°C), Lead-free |
| 10 | IS61LV6416-10T | Plastic TSOP | Commercial (0°C to +70°C) |
| 10 | IS61LV6416-10TL | Plastic TSOP | Commercial (0°C to +70°C), Lead-free |
| 10 | IS61LV6416-10K | 400-mil Plastic SOJ | Commercial (0°C to +70°C) |
| 10 | IS61LV6416-10BI | mini BGA (6mm x 8mm) | Industrial (-40°C to +85°C) |
| 10 | IS61LV6416-10BLI | mini BGA (6mm x 8mm) | Industrial (-40°C to +85°C), Lead-free |
| 10 | IS61LV6416-10TI | Plastic TSOP | Industrial (-40°C to +85°C) |
| 10 | IS61LV6416-10TLI | Plastic TSOP | Industrial (-40°C to +85°C), Lead-free |
| 10 | IS61LV6416-10KI | 400-mil Plastic SOJ | Industrial (-40°C to +85°C) |
| 10 | IS61LV6416-10KLI | 400-mil Plastic SOJ | Industrial (-40°C to +85°C), Lead-free |
| 12 | IS61LV6416-12T | Plastic TSOP | Commercial (0°C to +70°C) |
| 12 | IS61LV6416-12K | 400-mil Plastic SOJ | Commercial (0°C to +70°C) |
| 12 | IS61LV6416-12KL | 400-mil Plastic SOJ | Commercial (0°C to +70°C), Lead-free |
| 12 | IS61LV6416-12BI | mini BGA (6mm x 8mm) | Industrial (-40°C to +85°C) |

IS61LV6416L

ORDERING INFORMATION

| Speed (ns) | Order Part No. | Package | Temperature Range |
|-------------------|-----------------------|----------------------|-----------------------------|
| 8 | IS61LV6416L-8T | Plastic TSOP | Commercial (0°C to +70°C) |
| 8 | IS61LV6416L-8BI | mini BGA (6mm x 8mm) | Industrial (-40°C to +85°C) |
| 8 | IS61LV6416L-8TI | Plastic TSOP | Industrial (-40°C to +85°C) |
| 8 | IS61LV6416L-8KI | 400-mil Plastic SOJ | Industrial (-40°C to +85°C) |
| 10 | IS61LV6416L-10T | Plastic TSOP | Commercial (0°C to +70°C) |
| 10 | IS61LV6416L-10BI | mini BGA (6mm x 8mm) | Industrial (-40°C to +85°C) |
| 10 | IS61LV6416L-10TI | Plastic TSOP | Industrial (-40°C to +85°C) |
| 10 | IS61LV6416L-10KI | 400-mil Plastic SOJ | Industrial (-40°C to +85°C) |

PACKAGING INFORMATION

400-mil Plastic SOJ

Package Code: K



Notes:

1. Controlling dimension: millimeters.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Reference document: JEDEC MS-027.

| Symbol | Millimeters | | Inches | | Millimeters | | Inches | | Millimeters | | Inches | |
|---------------|-------------|-------|-----------|-------|-------------|-------|-----------|-------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| No. Leads (N) | 28 | | | | 32 | | | | 36 | | | |
| A | 3.25 | 3.75 | 0.128 | 0.148 | 3.25 | 3.75 | 0.128 | 0.148 | 3.25 | 3.75 | 0.128 | 0.148 |
| A1 | 0.64 | — | 0.025 | — | 0.64 | — | 0.025 | — | 0.64 | — | 0.025 | — |
| A2 | 2.08 | — | 0.082 | — | 2.08 | — | 0.082 | — | 2.08 | — | 0.082 | — |
| B | 0.38 | 0.51 | 0.015 | 0.020 | 0.38 | 0.51 | 0.015 | 0.020 | 0.38 | 0.51 | 0.015 | 0.020 |
| b | 0.66 | 0.81 | 0.026 | 0.032 | 0.66 | 0.81 | 0.026 | 0.032 | 0.66 | 0.81 | 0.026 | 0.032 |
| C | 0.18 | 0.33 | 0.007 | 0.013 | 0.18 | 0.33 | 0.007 | 0.013 | 0.18 | 0.33 | 0.007 | 0.013 |
| D | 18.29 | 18.54 | 0.720 | 0.730 | 20.82 | 21.08 | 0.820 | 0.830 | 23.37 | 23.62 | 0.920 | 0.930 |
| E | 11.05 | 11.30 | 0.435 | 0.445 | 11.05 | 11.30 | 0.435 | 0.445 | 11.05 | 11.30 | 0.435 | 0.445 |
| E1 | 10.03 | 10.29 | 0.395 | 0.405 | 10.03 | 10.29 | 0.395 | 0.405 | 10.03 | 10.29 | 0.395 | 0.405 |
| E2 | 9.40 BSC | | 0.370 BSC | | 9.40 BSC | | 0.370 BSC | | 9.40 BSC | | 0.370 BSC | |
| e | 1.27 BSC | | 0.050 BSC | | 1.27 BSC | | 0.050 BSC | | 1.27 BSC | | 0.050 BSC | |

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| Symbol | Millimeters | | Inches | | Millimeters | | Inches | | Millimeters | | Inches | |
|---------------|-------------|-------|-----------|-------|-------------|-------|-----------|-------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| No. Leads (N) | 40 | | | | 42 | | | | 44 | | | |
| A | 3.25 | 3.75 | 0.128 | 0.148 | 3.25 | 3.75 | 0.128 | 0.148 | 3.25 | 3.75 | 0.128 | 0.148 |
| A1 | 0.64 | — | 0.025 | — | 0.64 | — | 0.025 | — | 0.64 | — | 0.025 | — |
| A2 | 2.08 | — | 0.082 | — | 2.08 | — | 0.082 | — | 2.08 | — | 0.082 | — |
| B | 0.38 | 0.51 | 0.015 | 0.020 | 0.38 | 0.51 | 0.015 | 0.020 | 0.38 | 0.51 | 0.015 | 0.020 |
| b | 0.66 | 0.81 | 0.026 | 0.032 | 0.66 | 0.81 | 0.026 | 0.032 | 0.66 | 0.81 | 0.026 | 0.032 |
| C | 0.18 | 0.33 | 0.007 | 0.013 | 0.18 | 0.33 | 0.007 | 0.013 | 0.18 | 0.33 | 0.007 | 0.013 |
| D | 25.91 | 26.16 | 1.020 | 1.030 | 27.18 | 27.43 | 1.070 | 1.080 | 28.45 | 28.70 | 1.120 | 1.130 |
| E | 11.05 | 11.30 | 0.435 | 0.445 | 11.05 | 11.30 | 0.435 | 0.445 | 11.05 | 11.30 | 0.435 | 0.445 |
| E1 | 10.03 | 10.29 | 0.395 | 0.405 | 10.03 | 10.29 | 0.395 | 0.405 | 10.03 | 10.29 | 0.395 | 0.405 |
| E2 | 9.40 BSC | | 0.370 BSC | | 9.40 BSC | | 0.370 BSC | | 9.40 BSC | | 0.370 BSC | |
| e | 1.27 BSC | | 0.050 BSC | | 1.27 BSC | | 0.050 BSC | | 1.27 BSC | | 0.050 BSC | |

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PACKAGING INFORMATION



Mini Ball Grid Array Package Code: B (48-pin)



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01/15/03

PACKAGING INFORMATION

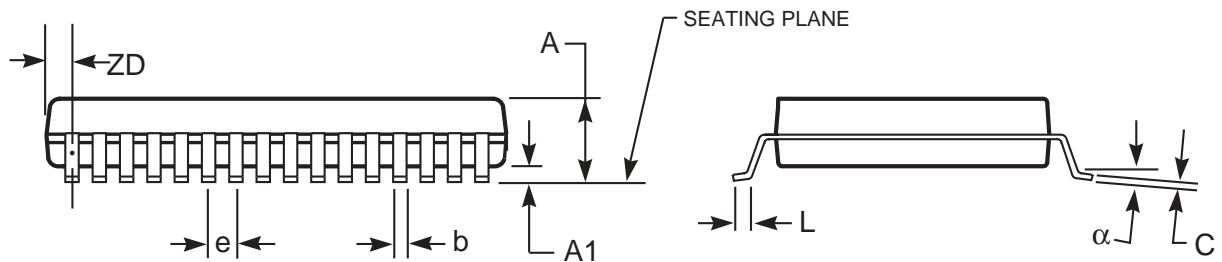


Plastic TSOP Package Code: T (Type II)



Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

| Symbol | Millimeters | | Inches | | Millimeters | | Inches | | Millimeters | | Inches | |
|---------------|-------------|-------|-----------|-------|-------------|-------|-----------|-------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| Ref. Std. | | | | | | | | | | | | |
| No. Leads (N) | 32 | | | | 44 | | | | 50 | | | |
| A | — | 1.20 | — | 0.047 | — | 1.20 | — | 0.047 | — | 1.20 | — | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 |
| b | 0.30 | 0.52 | 0.012 | 0.020 | 0.30 | 0.45 | 0.012 | 0.018 | 0.30 | 0.45 | 0.012 | 0.018 |
| C | 0.12 | 0.21 | 0.005 | 0.008 | 0.12 | 0.21 | 0.005 | 0.008 | 0.12 | 0.21 | 0.005 | 0.008 |
| D | 20.82 | 21.08 | 0.820 | 0.830 | 18.31 | 18.52 | 0.721 | 0.729 | 20.82 | 21.08 | 0.820 | 0.830 |
| E1 | 10.03 | 10.29 | 0.391 | 0.400 | 10.03 | 10.29 | 0.395 | 0.405 | 10.03 | 10.29 | 0.395 | 0.405 |
| E | 11.56 | 11.96 | 0.451 | 0.466 | 11.56 | 11.96 | 0.455 | 0.471 | 11.56 | 11.96 | 0.455 | 0.471 |
| e | 1.27 BSC | | 0.050 BSC | | 0.80 BSC | | 0.032 BSC | | 0.80 BSC | | 0.031 BSC | |
| L | 0.40 | 0.60 | 0.016 | 0.024 | 0.41 | 0.60 | 0.016 | 0.024 | 0.40 | 0.60 | 0.016 | 0.024 |
| ZD | 0.95 REF | | 0.037 REF | | 0.81 REF | | 0.032 REF | | 0.88 REF | | 0.035 REF | |
| α | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° |

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- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
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JONHON

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«FORSTAR» (основан в 1998 г.)

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кабельные сборки и микроволновые компоненты:

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