MAX11900

16-Bit, 1Msps, Low-Power, Fully Differential SAR ADC

General Description

The MAX11900 is a 16-bit, 1Msps, single-channel, fully differential SAR ADC with internal reference buffers. The MAX11900 provides excellent static and dynamic performance with best-in-class power consumption that directly scales with throughput. The device has a unipolar differential $\pm V_{REF}$ input range. Supplies include a 3.3V supply for the reference buffers, a 1.8V analog supply, a 1.8V digital supply, and a 1.5V to 3.6V digital interface supply.

This ADC achieves 95.6dB SNR and -115dB THD, guarantees 16-bit resolution with no-missing codes and 0.5 LSB INL (max).

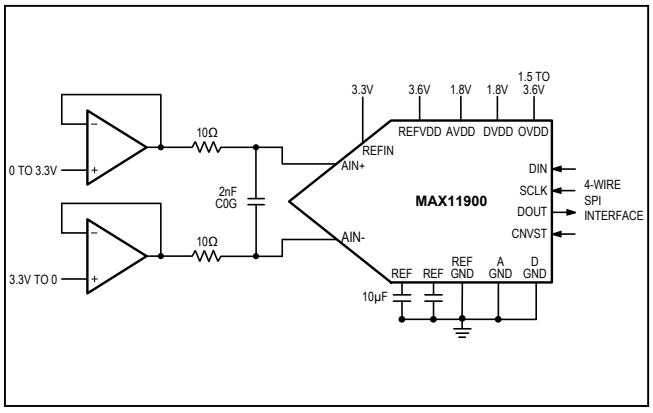
The MAX11900 communicates data using a SPI-compatible serial interface. The MAX11900 is offered in a 20-pin, 4mm x 4mm, TQFN package and is specified over the -40°C to +85°C operating temperature range.

Applications

- Test and Measurement
- Automatic Test Equipment
- Medical Instrumentation
- Process Control and Industrial Automation
- Data Acquisition Systems
- Telecommunications
- Battery-Powered Equipment

***Ordering Information* and *Selector Guide* appears at end of data sheet.**

Application Diagram



Benefits and Features

- High DC/AC Accuracy Improves Measurement Quality
  - 16-Bit Resolution with No Missing Codes
  - 1Msps Throughput Rates Without Pipeline Delay/Latency
  - 95.6dB SNR and -115dB THD at 10kHz
  - 0.4 LSB_{RMS} Transition Noise
  - ±0.25 LSB DNL (max) and ±0.5 LSB INL (max)
- Highly Integrated ADC Saves Cost and Space
  - Internal Reference Buffer
- Wide Supply Range and Low Power Simplify Power-Supply Design
  - 1.8V Analog Supply
  - 1.5V to 3.6V Digital Supply
  - 6.7mW Power Consumption at 1Msps
  - 6.7µW Power Consumption at 1ksps
  - 1µA in Shutdown Mode
- Multi-Industry Standard Serial Interface and Small Package Reduces Size
  - SPI/QSPI™/MICROWIRE®/DSP-Compatible Serial Interface
  - 4mm x 4mm 20-Pin TQFN Package

QSPI is a trademark of Motorola, Inc.

MICROWIRE is a registered trademark of National Semiconductor Corporation.

16-Bit to 20-Bit SAR ADC Family

	16-BIT	18-BIT	20-BIT
1.6Msps	MAX11901	MAX11903	MAX11905
1Msps	MAX11900	MAX11902	MAX11904

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX11900.related.

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TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Application Diagram . . . 1
16-Bit to 20-Bit SAR ADC Family . . . 1
Absolute Maximum Ratings . . . 4
Package Thermal Characteristics . . . 4
Electrical Characteristics . . . 4
Typical Operating Characteristics . . . 8
Pin Configuration . . . 12
Pin Description . . . 12
Functional Diagram . . . 13
Detailed Description . . . 14
- Analog Inputs . . . 14
- Input Settling . . . 16
- Input Filtering . . . 16
- Voltage Reference Configurations . . . 17
- Transfer Function . . . 17

Digital Interface . . . 19
- SPI Timing Diagram . . . 20
- Register Write . . . 22
- Register Read . . . 22

Register Map . . . 23
- Mode Register . . . 23
- Conversion Result Register . . . 24
- Chip ID Register . . . 24

Typical Application Circuit . . . 24
- Single-Ended Unipolar Input to Differential Unipolar Output . . . 24
- Single-Ended Bipolar Input to Differential Unipolar Output . . . 24

Layout, Grounding, and Bypassing . . . 24
Definitions . . . 27
- Integral Nonlinearity . . . 27
- Differential Nonlinearity . . . 27
- Offset Error . . . 27
- Gain Error . . . 27
- Signal-to-Noise Ratio . . . 27
- Signal-to-Noise Plus Distortion . . . 27

TABLE OF CONTENTS (continued)

Effective Number of Bits . . . 27
Total Harmonic Distortion . . . 27
Spurious-Free Dynamic Range . . . 27
Aperture Delay . . . 27
Aperture Jitter . . . 27
Full-Power Bandwidth . . . 27
Selector Guide . . . 28
Ordering Information . . . 28
Chip Information . . . 28
Package Information . . . 28
Revision History . . . 29

LIST OF FIGURES

Figure 1. Signal Ranges . . . 14
Figure 2. Simplified Model of Input Sampling Circuit . . . 15
Figure 3. Conversion Frame, SAR Conversion, Track and Read Operation . . . 15
Figure 4. Ideal Transfer Characteristic . . . 18
Figure 5. Read During Track Phase . . . 19
Figure 6. Read During SAR Conversion Phase . . . 19
Figure 7. Split Read Mode . . . 20
Figure 8. SPI Interface Connection . . . 20
Figure 9. DIN Timing for Register Write Operations . . . 21
Figure 10. Timing Diagram for Data Out Reading After Conversion . . . 21
Figure 11. Mode Register Write . . . 22
Figure 12. Register Read . . . 22
Figure 13. Unipolar Single-Ended Input . . . 25
Figure 14. Bipolar Single-Ended Input . . . 25
Figure 15. Top-Layer Sample Layout . . . 26

LIST OF TABLES

Table 1. ADC Driver Amplifier Recommendation . . . 16
Table 2. Voltage Reference Configurations . . . 17
Table 3. MAX11900 External Reference Recommendations . . . 17
Table 4. Transfer Characteristic . . . 18
Table 5. DOUT Driver Strength . . . 23

Absolute Maximum Ratings

REFVDD, REF, REFIN, OVDD to GND .....-0.3V to +4V
AVDD, DVDD to GND .....-0.3V to +2V
DGND to AGND, REFGND .....-0.3V to +0.3V
AIN+, AIN- to GND ..... -0.3V to the lower of (V_{REF} + 0.3V) and +4V or ±130mA
SCLK, DIN, DOUT, CNVST, to GND.....-0.3V to the lower of (V_{OVDD} + 0.3V) and +4V
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 30.30mW/°C above +70°C).....2424.2mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).... .....33°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(f_{SAMPLE} = 1Msps, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{OVDD} = 1.5V to 3.6V, V_{REFVDD} = 3.6V, V_{REF} = 3.3V, Internal Ref Buffers On, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Input Voltage Range (Note 3)		(AIN+) - (AIN-)	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage Range		AIN+, AIN- relative to AGND	-0.1		V_{REF} + 0.1	V
Common-Mode Input Range		[(AIN+) + (AIN-)]/2	$V_{REF}/2$ - 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	V
Input Leakage Current		Acquisition phase	-1	0.001	+1	µA
Input Capacitance				32		pF
STATIC PERFORMANCE (Note 4)						
Resolution	N		16			Bits
Resolution	LSB	V_{REF} = 3.3V		100.7		µV
No Missing Codes			16			Bits
Offset Error (Note 4)			-1	±0.1	+1	LSB
Offset Temperature Coefficient				±0.001		LSB/°C
Gain Error		Referred to REFIN reference input	-12	±2	+12	LSB
Gain Error Temperature Coefficient (Note 5)		Referred to REFIN reference input		±0.02		LSB/°C
Gain Error		Referred to REF pins	-3	±1	+3	LSB
Gain Error Temperature Coefficient (Note 5)		Referred to REF pins		±0.01		LSB/°C
Integral Nonlinearity	INL		-0.5	±0.1	+0.5	LSB

Electrical Characteristics (continued)

(f_{SAMPLE} = 1Msps, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{OVDD} = 1.5V to 3.6V, V_{REFVDD} = 3.6V, V_{REF} = 3.3V, Internal Ref Buffers On, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Nonlinearity (Note 6)	DNL		-0.25	±0.1	+0.25	LSB
Analog Input CMR	CMR	DC		1		LSB/V
Power-Supply Rejection (Note 7)	PSR	PSR vs. AVDD		0.2		LSB/V
Power-Supply Rejection (Note 7)	PSR	PSR vs. REFVDD		0.3		LSB/V
Transition Noise				0.4		LSB_{RMS}
EXTERNAL REFERENCE						
REF Voltage Input Range	V_{REF}		2.5	3.3	3.6	V
Load Current	I_{REF}	1Msps, V_{REF} = 3.3V		600		µA
REF Input Capacitance				1		nF
REFERENCE BUFFER						
REFIN Input Voltage Range	V_{REFIN}	V_{REF} < (V_{REFVDD} - 200mV)	2.5	3	V_{REFVDD} - 200mV	V
REFIN Input Current	I_{REFIN}			1		nA
Turn-On Settling Time		C_{EXT} = 10µF on REF pin, C_{REFIN} = 0.1µF on REFIN pin		20		ms
External Compensation Capacitor	C_{EXT}	REF pins	4.7	10		µF
DYNAMIC PERFORMANCE (Note 8)						
Dynamic Range		Internal RefBuffer, -60dBFS input		95.6		dB
Signal-to-Noise Ratio	SNR	Internal RefBuffer, f_{IN} = 10kHz	95	95.6		dB
Signal-to-Noise Plus Distortion	SINAD	Internal RefBuffer, f_{IN} = 10kHz, -0.1dBFs	95	95.6		dB
Spurious-Free Dynamic Range	SFDR	Internal RefBuffer, f_{IN} = 10kHz		117		dB
Total Harmonic Distortion	THD	Internal RefBuffer, f_{IN} = 10kHz		-115		dB
Total Harmonic Distortion	THD	Internal RefBuffer, f_{IN} = 100kHz		-110		dB
Total Harmonic Distortion	THD	Internal RefBuffer, f_{IN} = 250kHz		-100		dB
SAMPLING DYNAMICS						
Throughput			0		1.0	Msps
Full-Power Bandwidth		-3dB point (targeting 20MHz)		20		MHz
		-0.1dB point		3		
Acquisition Time	t_{ACQ}		150			ns
Aperture Delay		Time delay from CNVST rising edge to time at which sample is taken for conversion		1		ns
Aperture Jitter				3		ps_{RMS}

Electrical Characteristics (continued)

(f_{SAMPLE} = 1Msps, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{OVDD} = 1.5V to 3.6V, V_{REFVDD} = 3.6V, V_{REF} = 3.3V, Internal Ref Buffers On, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	AVDD		1.7	1.8	1.9	V
Digital Supply Voltage	DVDD		1.7	1.8	1.9	V
Reference Buffer Supply Voltage	REFVDD		2.7	3.3	3.6	V
Interface Supply Voltage	OVDD		1.5		3.6	V
Analog Supply Current	I_{AVDD}	V_{AVDD} = 1.8V		1.75	2.3	mA
Digital Supply Current	I_{DVDD}	V_{DVDD} = 1.8V		1.5	1.9	mA
Reference Buffer Supply Current	I_{REFVDD}	V_{REFVDD} = 3.6V, internal buffers enabled		3.3	3.55	mA
Reference Buffer Supply Current	I_{REFVDD}	V_{REFVDD} = 3.6V, internal buffers powered down		0.2		mA
Interface Supply Current (Note 9)	I_{OVDD}	V_{OVDD} = 1.5V		0.27		mA
		V_{OVDD} = 3.6V		1		
Shutdown Current		For AVDD, DVDD, REFVDD		1		µA
Shutdown Current		For DVDD		1		µA
Power Dissipation		V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{REFVDD} = 3.3V, internal reference buffers disabled		6.7	8.4	mW
DIGITAL INPUTS (DIN, SCLK, CNVST)						
Input Voltage High	V_{IH}	V_{OVDD} = 1.5V to 3.6V	0.7 x V_{OVDD}			V
Input Voltage Low	V_{IL}	V_{OVDD} = 1.5V to 3.6V			0.3 x V_{OVDD}	V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	V_{IN} = 0V or V_{OVDD}		1		µA
DIGITAL OUTPUTS (DOUT)						
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V

Electrical Characteristics (continued)

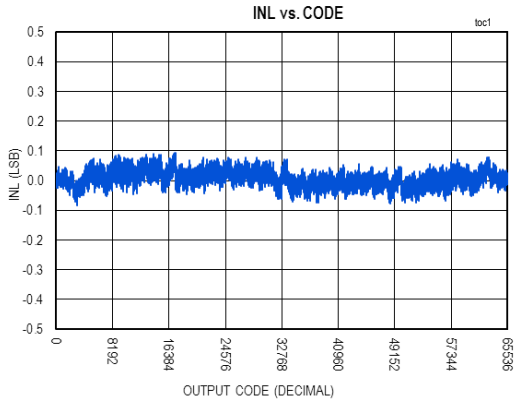
(f_{SAMPLE} = 1Msps, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{OVDD} = 1.5V to 3.6V, V_{REFVDD} = 3.6V, V_{REF} = 3.3V, Internal Ref Buffers On, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

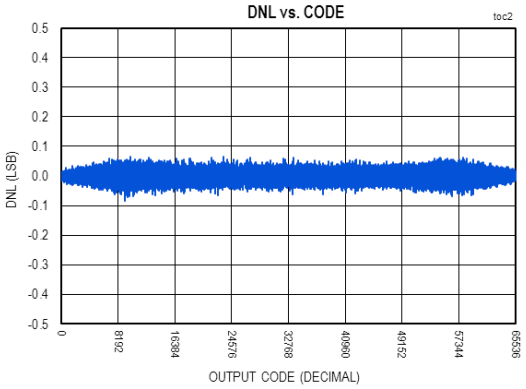
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING						
DIN to SCLK Rising Edge Setup	t_1				4	ns
DIN to SCLK Rising Edge Hold	t_2		1			ns
DOUT End-Of-Conversion Low Time	t_3		15			ns
DOUT to SCLK Rising Edge Hold	t_4		2.5			ns
DOUT to SCLK Rising Edge Setup	t_5	100MHz SCLK	1.5			ns
SCLK High	t_6		4.5			ns
SCLK Period	t_7		10			ns
SCLK Low	t_8		4.5			ns
CNVST Rising Edge To SCLK Rising Edge	t_9		0			ns
SCLK Rising Edge to CNVST Rising Edge	t_{10}		25			ns
CNVST High	t_{11}		25			ns
CNVST High to EOC	t_{12}				850	ns
Conversion Period	t_{13}		1000			ns

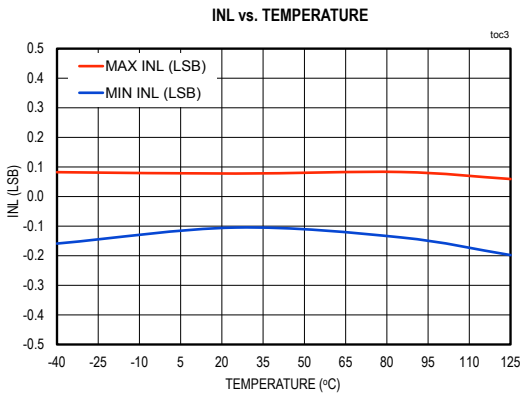
Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and device characterization.
Note 3: See the *Analog Inputs* section.
Note 4: See the *Definitions* section at the end of the data sheet.
Note 5: See the *Definitions* section at the end of the data sheet. Error contribution from the external reference not included.
Note 6: Parameter is guaranteed by design.
Note 7: Defined as the change in positive full-scale code transition caused by a ±5% variation in the supply voltage.
Note 8: Sine wave input, f_{IN} = 10kHz, A_{IN} = -0.5dB below full scale.
Note 9: C_{LOAD} = 10pF on DOUT. f_{CONV} = 1Msps. All data is read out.

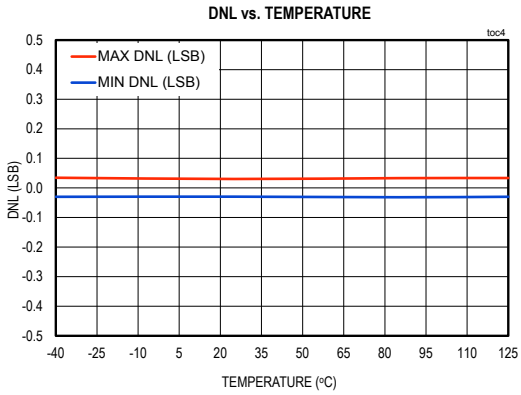
Typical Operating Characteristics

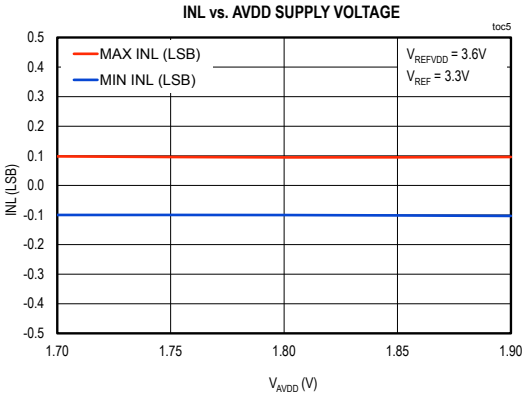
(V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{OVDD} = 1.8V, V_{REFVDD} = 3.6V, f_{SAMPLE} = 1Msps, V_{REF} = 3.3V, Internal Ref Buffer On, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

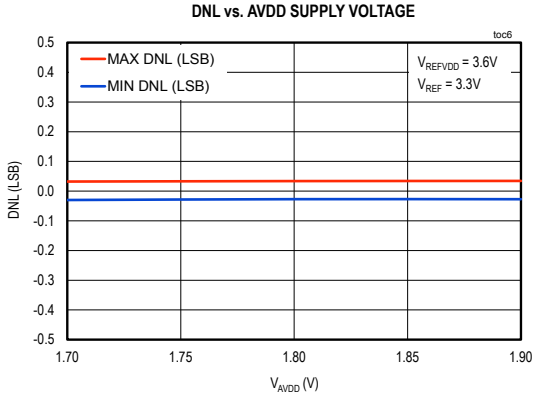








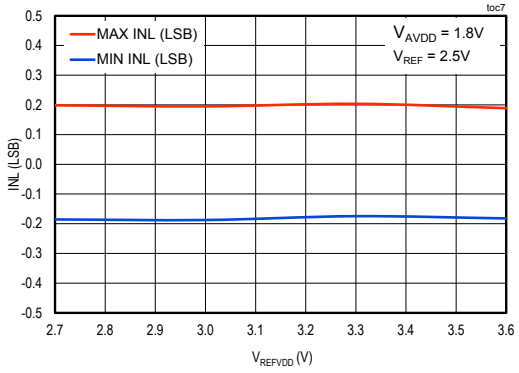




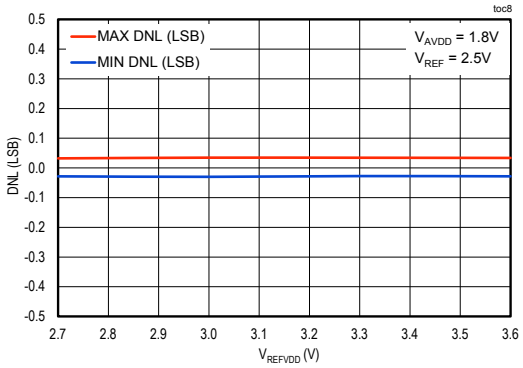
Typical Operating Characteristics (continued)

(V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{OVDD} = 1.8V, V_{REFVDD} = 3.6V, f_{SAMPLE} = 1Msps, V_{REF} = 3.3V, Internal Ref Buffer On, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

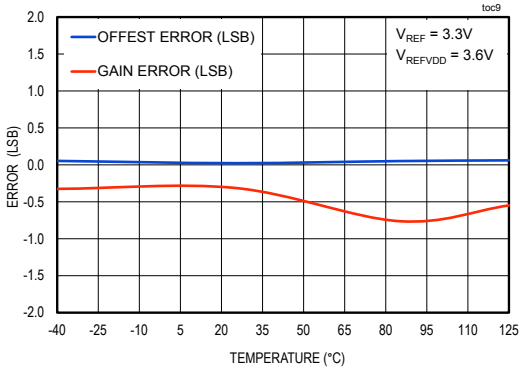
INL vs. REFVDD SUPPLY VOLTAGE



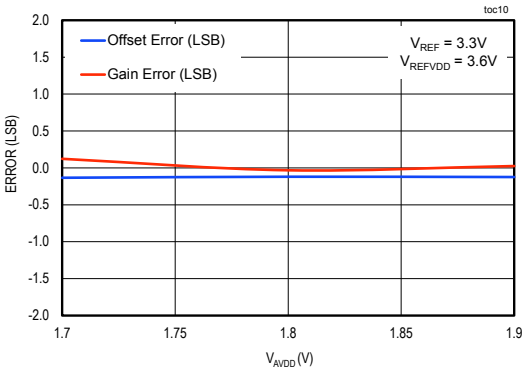
DNL vs. REFVDD SUPPLY VOLTAGE



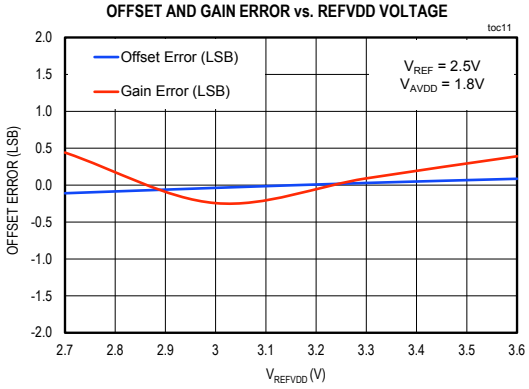
OFFSET AND GAIN ERROR vs. TEMPERATURE



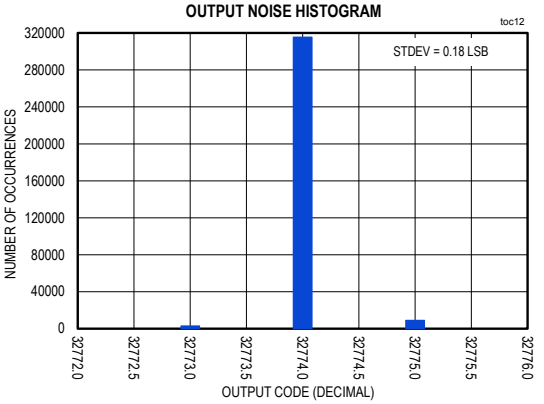
OFFSET AND GAIN ERROR vs. AVDD SUPPLY VOLTAGE



OFFSET AND GAIN ERROR vs. REFVDD VOLTAGE

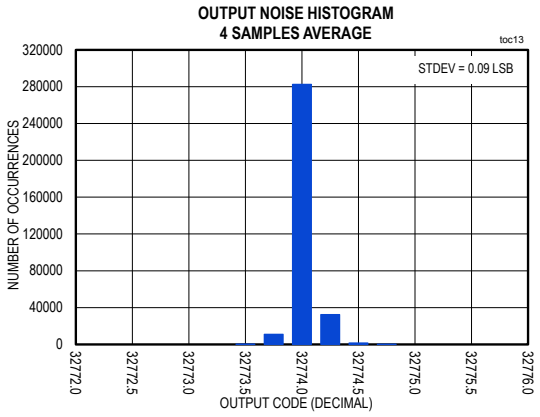


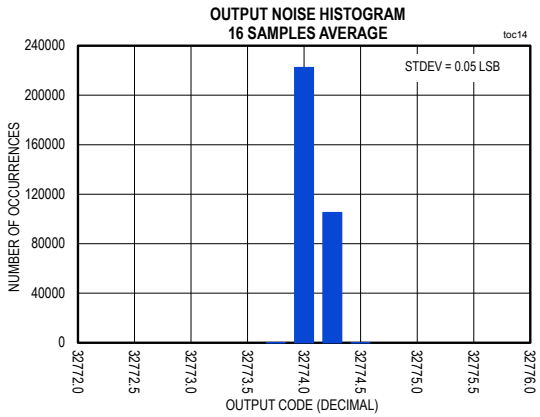
OUTPUT NOISE HISTOGRAM

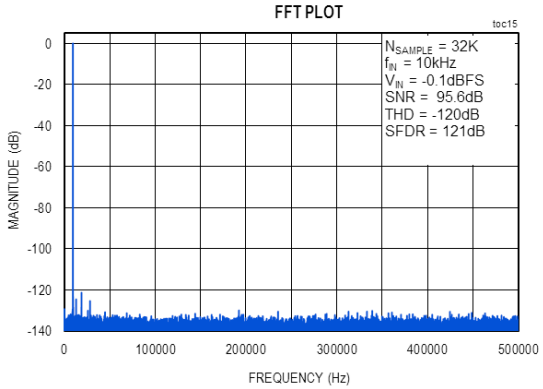


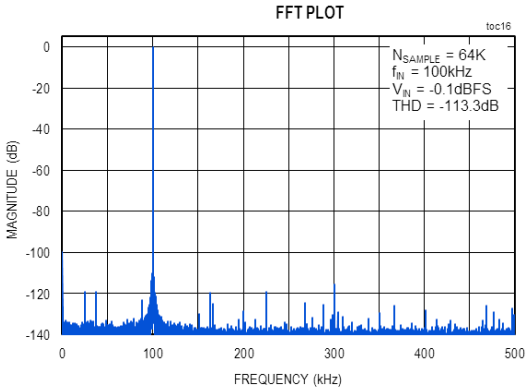
Typical Operating Characteristics (continued)

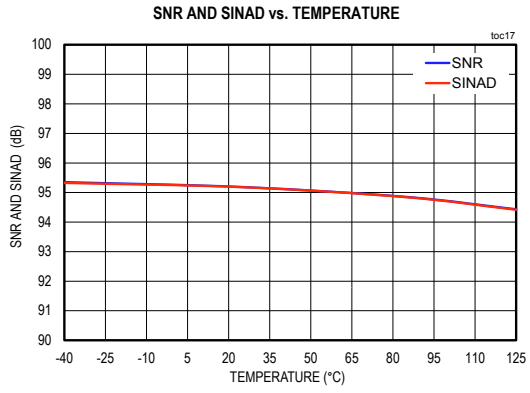
(V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{OVDD} = 1.8V, V_{REFVDD} = 3.6V, f_{SAMPLE} = 1Msps, V_{REF} = 3.3V, Internal Ref Buffer On, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

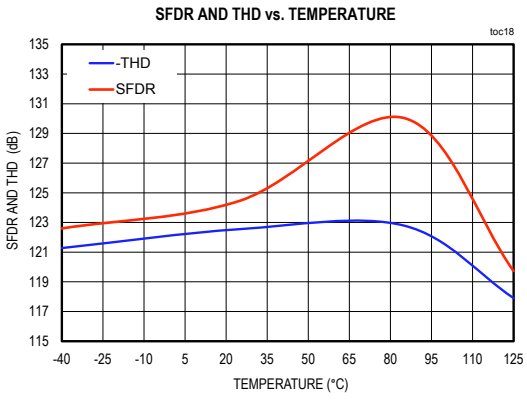








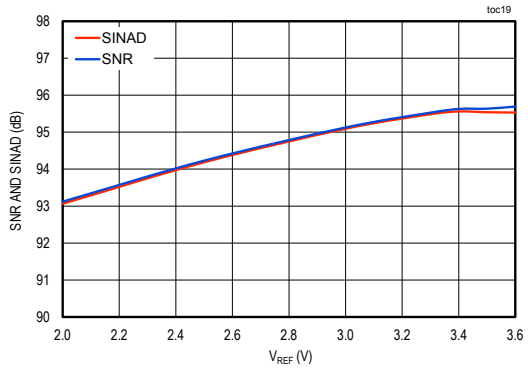




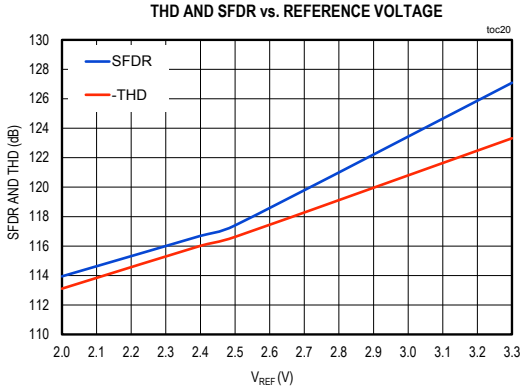
Typical Operating Characteristics (continued)

(V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{OVDD} = 1.8V, V_{REFVDD} = 3.6V, f_{SAMPLE} = 1Msps, V_{REF} = 3.3V, Internal Ref Buffer On, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

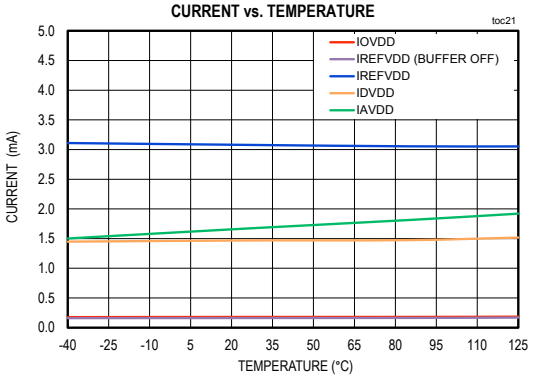
SNR AND SINAD vs. REFERENCE VOLTAGE



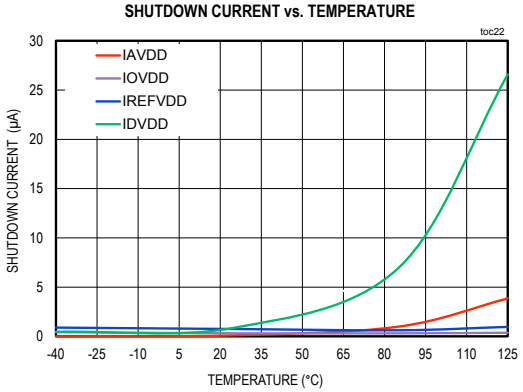
THD AND SFDR vs. REFERENCE VOLTAGE



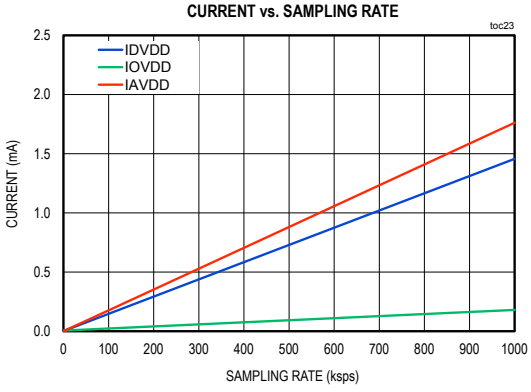
CURRENT vs. TEMPERATURE



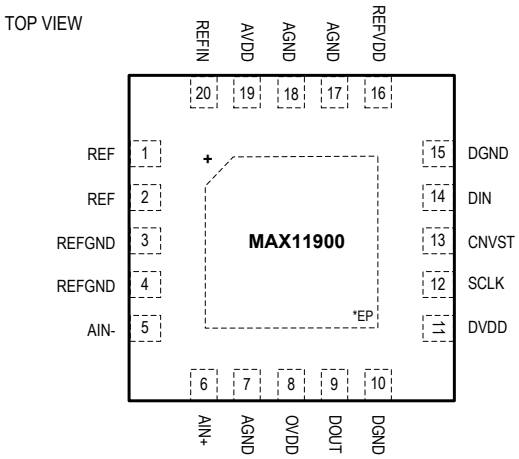
SHUTDOWN CURRENT vs. TEMPERATURE



CURRENT vs. SAMPLING RATE



Pin Configuration



TQFN
4mm × 4mm

*EXPOSED PAD IS GROUND. IT MUST BE SOLDERED TO PCB.

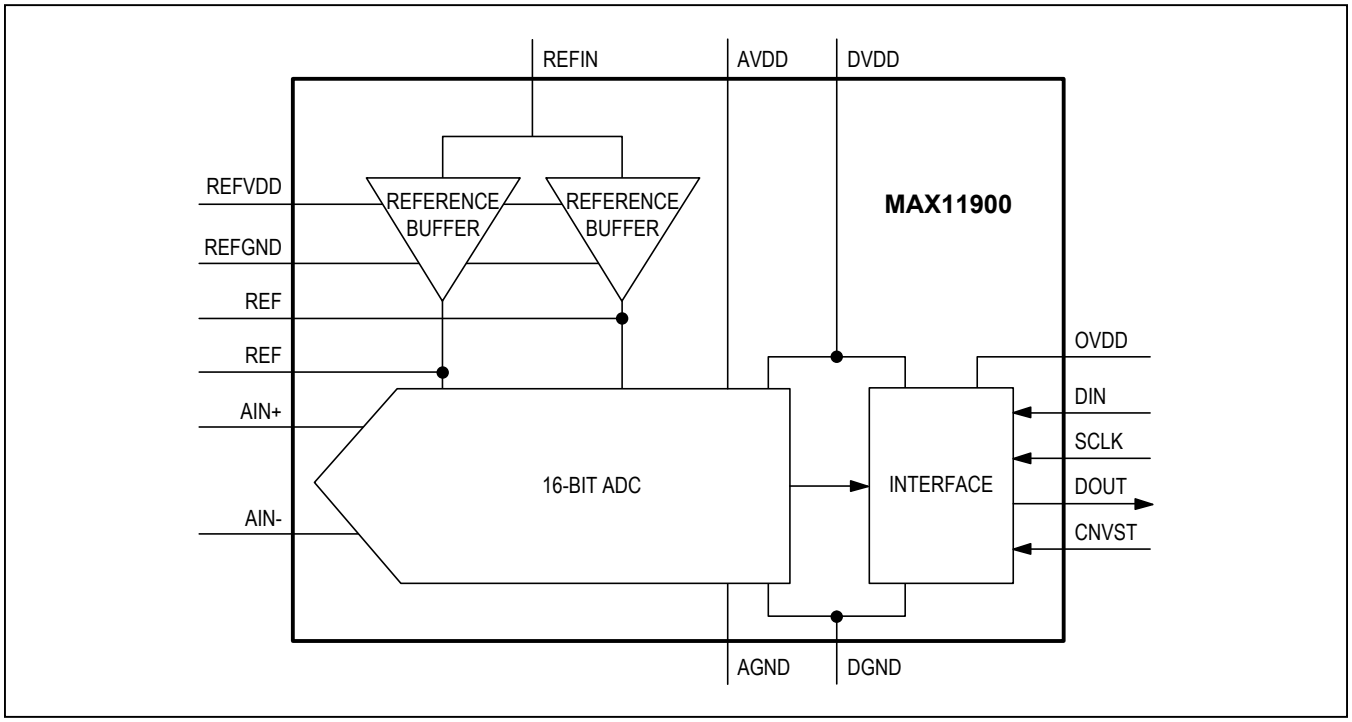
Pin Description

PIN	NAME	I/O	FUNCTION
1, 2	REF	I/O	Reference. REF is a bypass pin for the reference either driven by the internal reference buffers or the external reference directly. Bypass these pins with 10µF capacitors to REFGND.
3, 4	REFGND	I	Reference Ground
5	AIN-	I	Negative Analog Input
6	AIN+	I	Positive Analog Input
7	AGND	I	Analog Ground
8	OVDD	I	Digital Interface Supply. Nominally at 1.8V. Bypass to DGND with a 10µF capacitor in parallel with a 0.1µF capacitor (10µF || 0.1µF).
9	DOUT	O	Digital Output Data
10	DGND	I	Digital Ground
11	DVDD	I	Digital Supply. Nominally at 1.8V. Bypass with a 10µF capacitor in parallel with a 0.1µF capacitor (10µF || 0.1µF).
12	SCLK	I	Serial Clock Input
13	CNVST	I	Conversion Start. The analog inputs (AIN+, AIN-) are sampled at the rising edge and conversion process is started.
14	DIN	I	Serial Data Input. DIN data is latched into the serial interface on the rising edge of SCLK.
15	DGND	I	Digital Ground

Pin Description (continued)

PIN	NAME	I/O	FUNCTION
16	REFVDD	I	Reference Buffer Supply. Nominally at 3V. Bypass to AGND with a 10µF capacitor in parallel with a 0.1µF capacitor (10µF || 100nF).
17, 18	AGND	I	Analog Ground. Bypass to AGND with a 10µF capacitor in parallel with a 0.1µF capacitor (10µF || 100nF).
19	AVDD	I	Analog Supply. Nominally at 1.8V.
20	REFIN	I	Input for the Internal Reference Buffer. Voltage must be at least 300mV lower than REFVDD voltage. If REFIN = 0V, reference buffer will be disabled.
—	EP	—	Exposed Pad. Must be connected to the same plane as AGND.

Functional Diagram



Detailed Description

The MAX11900 is a 16-bit, 1Msps maximum sampling rate, fully differential input, single-channel SAR ADC with SPI interface. This part features industry-leading sample rate and resolution, while consuming very low power. The MAX11900 has an integrated reference buffer to minimize board space, component count, and system cost. An internal oscillator drives the conversion and sets conversion time, easing external timing considerations.

Analog Inputs

Both analog inputs, AIN+ and AIN-, range from 0V to V_{REF}. Thus, the differential input interval V_{DIFF} = (AIN+) - (AIN-) ranges from $-V_{REF}$ to $+V_{REF}$, and the full-scale range is:

$$FSR = 2 \times V_{REF}$$

The nominal resolution step width of the least significant bit (LSB) is:

$$LSB = \frac{FSR}{2^N}, N = 16$$

The differential analog input must be centered around a signal common mode of $V_{REF}/2$, with a tolerance of ±100mV.

The reference voltage can range from 2.5V to the reference supply, REFVDD, if an external reference buffer is used. When using the on-board reference buffer the reference voltage can range from 2.5V to 200mV below reference supply REFVDD. This will guarantee adequate headroom for the internal reference buffers.

Figure 1 illustrates signal ranges for AIN+/AIN-, reference voltage V_{REF} and reference supply voltage REFVDD.

Figure 2 shows the input equivalent circuit of MAX11900. The ADC samples both inputs, AIN+ and AIN-, with a fully differential on-chip track-and-hold exhibiting no pipeline delay or latency.

The MAX11900 has dedicated input clamps to protect the inputs from overranging. Diodes D1 and D2 provide ESD protection and act as a clamp for the input voltages. Diodes D1/D2 can sustain a maximum forward current of 100mA. The sampling switches connect inputs to the sampling capacitors.

Figure 3 shows the timing of the digitizing cycle: Conversion frame, SAR conversion, Track and Read operations.

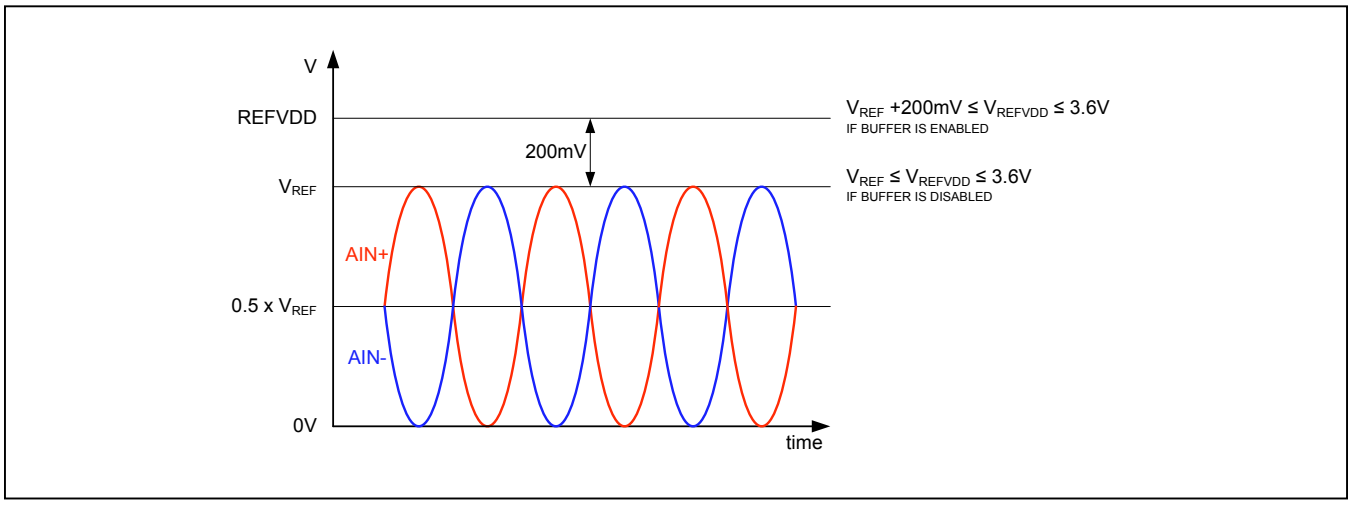


Figure 1. Signal Ranges

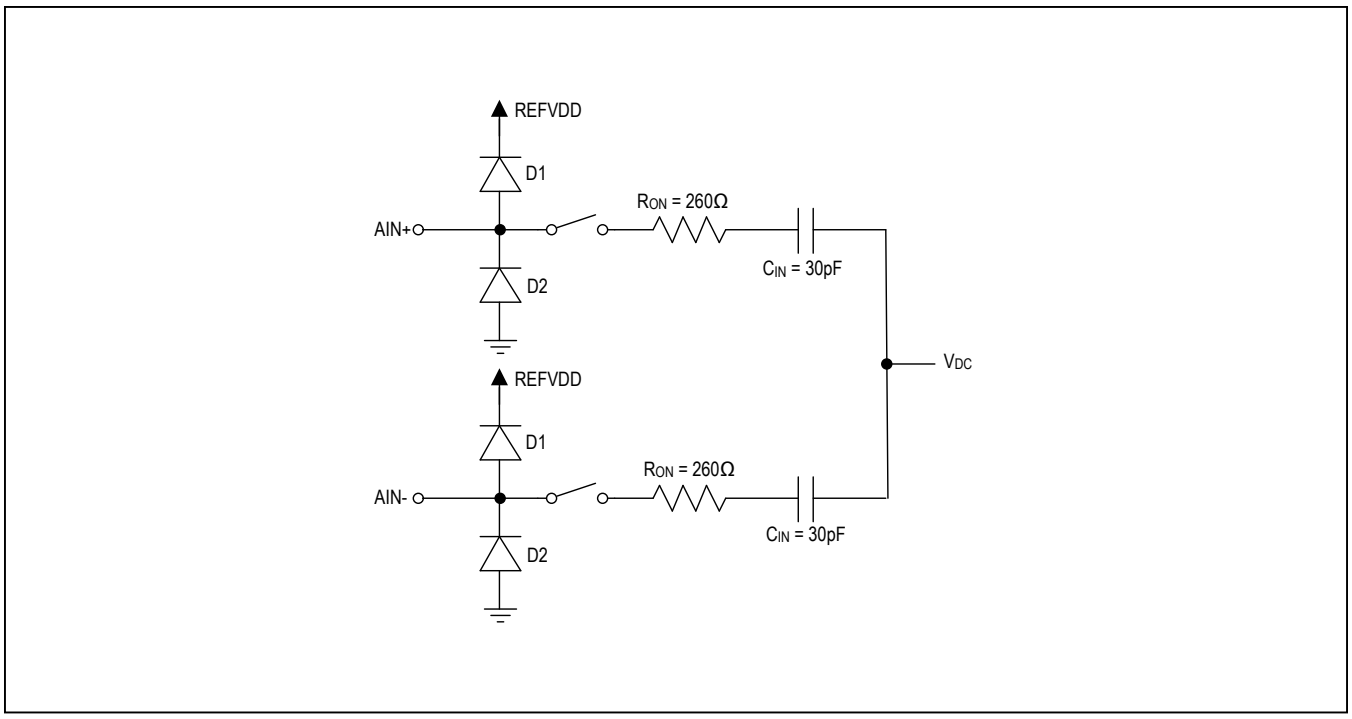


Figure 2. Simplified Model of Input Sampling Circuit

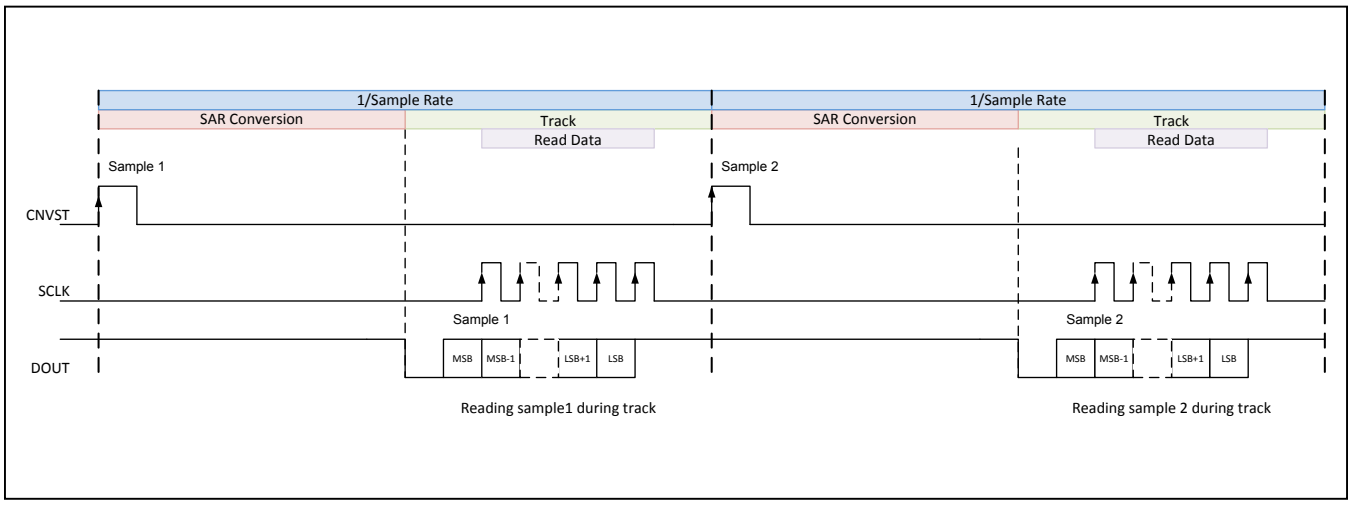


Figure 3. Conversion Frame, SAR Conversion, Track and Read Operation

Input Settling

During track phase (Figure 3), the sample switches are closed and the analog inputs are directly connected to the sample capacitors. The charging of the sample capacitor to the input voltage is determined by the source resistance and sampling capacitor size. The rising edge of CNVST is the sampling instant for the ADC. At this instant, the track phase ends, the sample switch opens, and the device enters into the successive approximation (SAR) conversion phase. In the conversion phase, a differential comparator compares the voltage on the sample capacitor against the CDAC value, which cycles through values between $V_{REF}/2$ and $V_{REF}/2^{16}$ using the successive approximation technique. The final result can be read via the SPI bus. The ADC automatically goes back into track phase at the end of SAR conversion and powers down its active circuits. That is, the ADC consumes no static power in track mode.

The conversion results will be accurate if the ADC tracks the input signal for an interval longer than the input signal's settling time. If the signal cannot settle within the track time due to excessive source resistance, external ADC drivers are required to achieve faster settling. Since the MAX11900 has a fixed conversion time set by an internal oscillator, track time can be increased by lowering the sample rate for better settling.

The settling behavior is determined by the time constant in the sampling network. The time constant depends upon the total resistance (source resistance + switch resistance) and total capacitance (sampling capacitor, external input capacitor, PCB parasitic capacitors).

Modeling the input circuit with a single pole network, the time constant, $R_{TOTAL} \times C_{LOAD}$, of the input should not exceed $t_{TRACK}/15$, where R_{TOTAL} is the total resistance (source resistance + switch resistance), C_{LOAD} is the total capacitance (sampling capacitor, external input capacitor, PCB parasitic capacitor), and t_{TRACK} is the track time.

When an ADC driver is used, it is recommended to use a series resistance (typically 5Ω to 50Ω) between the amplifier and the ADC input, as shown in the *Application Diagram*. Below are some of the requirements for the ADC driver amplifier:

1) Fast settling time: For a multichannel multiplexed circuit the ADC driver amplifier must be able to settle with an error less than 0.5 LSB during the minimum track time when a full-scale step is applied.
2) Low noise: It is important to ensure that the ADC driver has a sufficiently low-noise density in the bandwidth of interest of the application. When the MAX11900 is used with its full bandwidth of 20MHz, it is preferable to use an amplifier with an output noise spectral density of less than $3nV/\sqrt{Hz}$, to ensure that the overall SNR is not degraded significantly. It is recommended to insert an external RC filter at the ADC input to attenuate out-of-band input noise.
3) To take full advantage of the ADC's excellent dynamic performance, Maxim recommends the use of an ADC driver with equal or even better THD performance. This will ensure that the ADC driver does not limit distortion performance in the signal path. Table 1 summarizes the most important features of the MAX9632 when used as an ADC driver.

Input Filtering

Noisy input signals should be filtered prior to the ADC driver amplifier input with an appropriate filter to minimize noise. The RC network shown in the *Application Diagram* is mainly designed to reduce the load transient seen by the amplifier when the ADC starts the track phase. This network also has to satisfy the settling time requirement and provides the benefit of limiting the noise bandwidth.

Table 1. ADC Driver Amplifier Recommendation

AMPLIFIER	INPUT-NOISE DENSITY ($nV/\sqrt{Hz}$)	SMALL-SIGNAL BANDWIDTH (MHz)	SLEW RATE (V/µs)	THD (dB)	I_{CC} (mA)	COMMENTS
MAX9632	1	55	30	-128	3.9mA	Low noise, THD at 10kHz

Voltage Reference Configurations

The MAX11900 features internal reference buffers, helping to reduce component count and board space. Alternatively, the user may drive the reference nodes REF with an external reference. To use the internal reference buffers, drive the REFIN pin with an external reference voltage source. It will appear on the REF pin as a buffered reference output. The internal reference buffers can be disabled by writing to a register (see the *Mode Register* section) or tying REFIN to 0V. Once the on-chip reference buffers are disabled, REF pins can be directly driven by external reference buffers. A simplified diagram is shown to clarify the required connections for external reference.

A low-noise, low-temperature drift reference is required to achieve high system accuracy. The MAX6126 and MAX6325 are particularly well suited for use with the MAX11900. The MAX6126 and MAX6325 offer, respectively, 0.02% and 0.04% initial accuracy and 3ppm/°C and 1ppm/°C (max) temperature coefficient for high-precision applications. Maxim recommends bypassing REFIN and REF with a 2.2µF capacitor close to the ADC pins.

Transfer Function

Figure 4 shows the ideal transfer characteristics for the MAX11900.

The default data format is two's complement. However, offset binary format can be chosen by setting mode register BIT 1 (see the *Mode Register* section).

Table 4 shows the codes in terms of input voltage applied. The data reported is with V_{REF} of 3.0V, that gives a full-scale range of 6V.

Table 2. Voltage Reference Configurations

REFERENCE CONFIGURATION	INTERNAL REFERENCE BUFFERS	REFIN	V_{REF}	V_{REFVDD}
Internal Reference Buffer	ON	2.5V to V_{REFVDD} - 0.2V	2.5V to V_{REFVDD} - 0.2V	2.7V to 3.6V
External Reference Buffer	OFF	Tie to 0V or disable through serial interface	2.5V to V_{REFVDD}	2.5V to 3.6V

Table 3. MAX11900 External Reference Recommendations

PART	V_{OUT} (V)	TEMPERATURE COEFFICIENT (ppm/°C, max)	INITIAL ACCURACY (%)	NOISE (0.1Hz TO 10Hz) (μV_{P-P})	PACKAGE
MAX6126	2.5, 3	3	0.02	1.45	µMAX-8, SO-8
MAX6325	2.5	1	0.04	1.5	SO-8

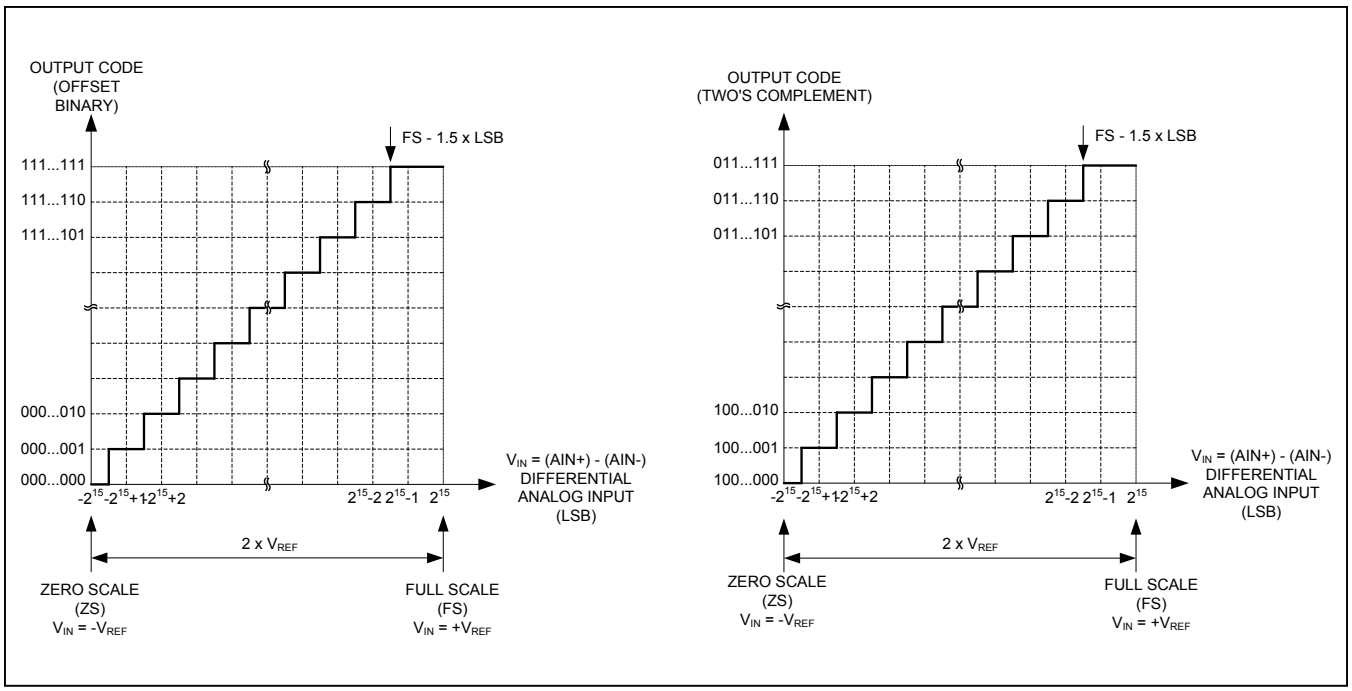


Figure 4. Ideal Transfer Characteristic

Table 4. Transfer Characteristic

MIDCODE VALUE	DIFFERENTIAL ANALOG INPUT FULL-SCALE RANGE = 6V (V)	HEXADECIMAL TWO'S COMPLEMENT	HEXADECIMAL OFFSET BINARY
FS - 1 LSB	2.99990845	7FFF	FFFF
Midscale + 1 LSB	0.00009155	0001	8001
Midscale	0.00000000	0000	8000
Midscale - 1 LSB	-0.00009155	FFFF	7FFF
-FS + 1 LSB	-2.99990845	8001	0001
-FS	-3.00000000	8000	0000

Digital Interface

The MAX11900 has a SPI interface with CNVST controlling the sampling, and SCLK, DOUT, DIN forming the standard SPI signals. The SAR conversion begins with the rising edge of CNVST. The minimum CNVST high time is 25ns and CNVST should be brought low before DOUT goes low, which signals the completion of a SAR conversion. The DOUT goes low for 15ns, followed by the output of the MSB on the DOUT pin. The 16-bit conversion result can then be read via the SPI interface by sending 16 SCLK pulses. DOUT going low also signals the start of the track phase. The ADC stays in track phase until the next rising edge of CNVST.

The MAX11900 has three different modes to read the data:

- Reading during track phase (Figure 5)
- Reading during SAR conversion phase (Figure 6)
- Split reading (Figure 7)

When reading during track phase mode, the data is read only while the ADC is in track mode. Figure 5 shows the SPI signal for this reading mode.

In the reading during SAR conversion phase mode, the data is read only in the SAR conversion phase. Figure 6 illustrates all SPI signals for this mode. Note that the data being read only during the SAR conversion phase corresponds to the previous conversion frame.

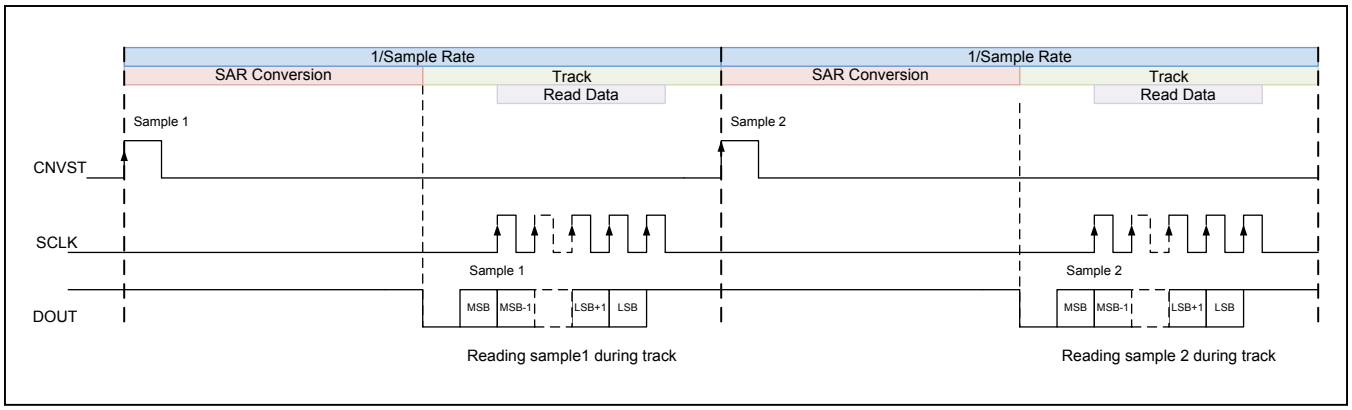


Figure 5. Read During Track Phase

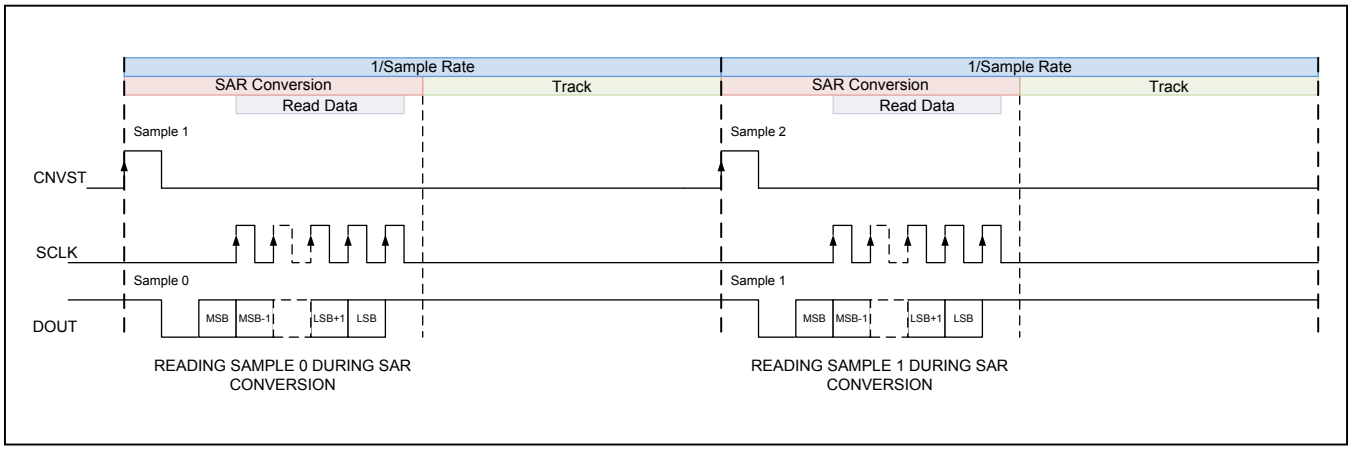


Figure 6. Read During SAR Conversion Phase

In the split reading mode, the data is read during the track phase and the following SAR conversion phase. Figure 7 shows the descriptive timing diagram.

At higher sampling rates, the track time may not be long enough to allow reading all 16 bits of data. In this case, the data read can be started in track mode, and then continued in the subsequent SAR conversion phase. Note that the read operation must be completed before DOUT goes low, signaling the end of the SAR conversion phase. Also note that no SCLK pulses should be applied close to the sampling edge (rising edge of CNVST), to safeguard the sampling edge from digital noise (see the Quiet Time specification t_{10}). This split reading feature can be used to accommodate slower SPI clocks.

SPI Timing Diagram

Figure 8 shows the typical digital SPI interface connection between the MAX11900 and host processor.

The dashed connections are optional.

Figure 9 shows the timing diagram for configuration registers.

Figure 10 shows the timing diagram for data output reading after conversion.

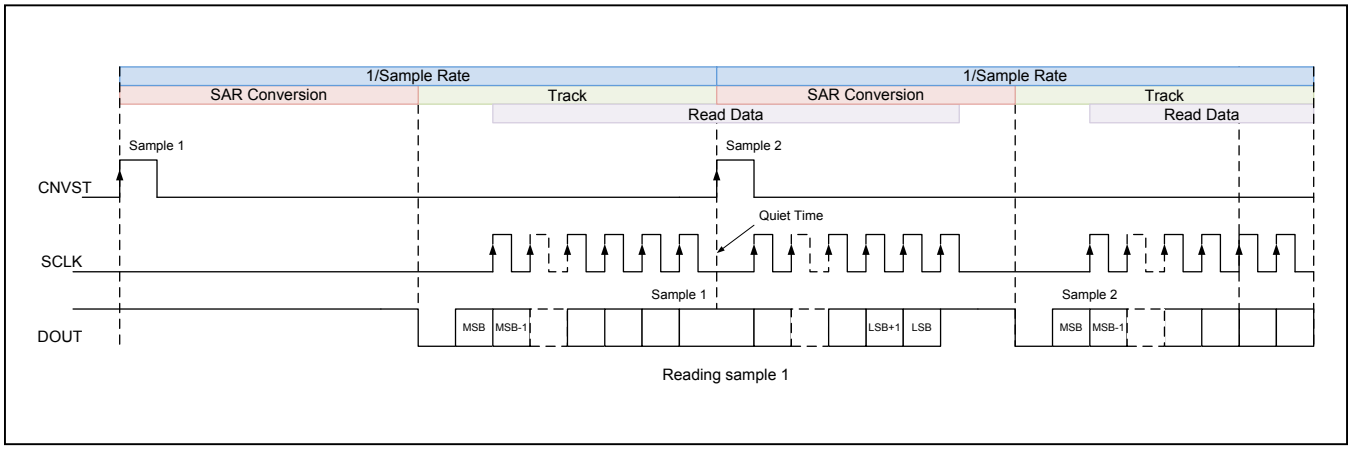


Figure 7. Split Read Mode

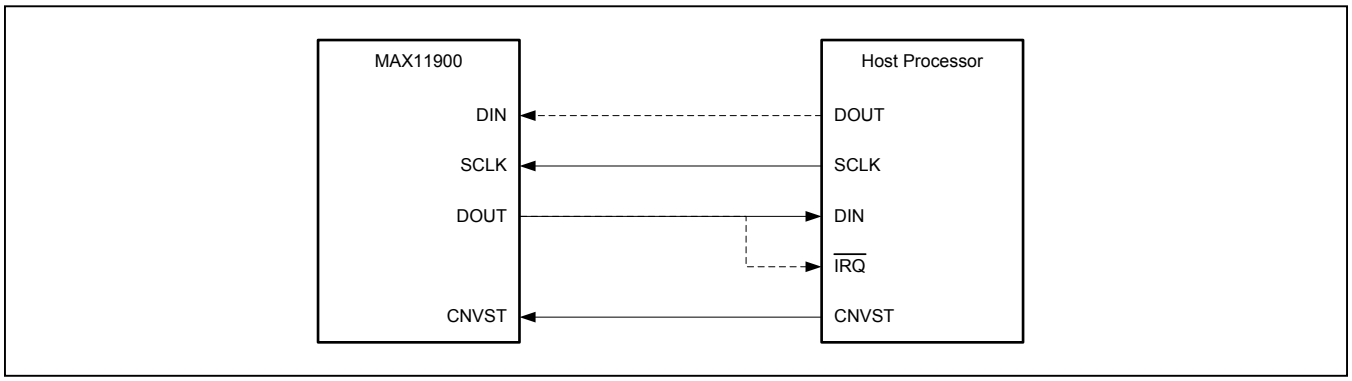


Figure 8. SPI Interface Connection

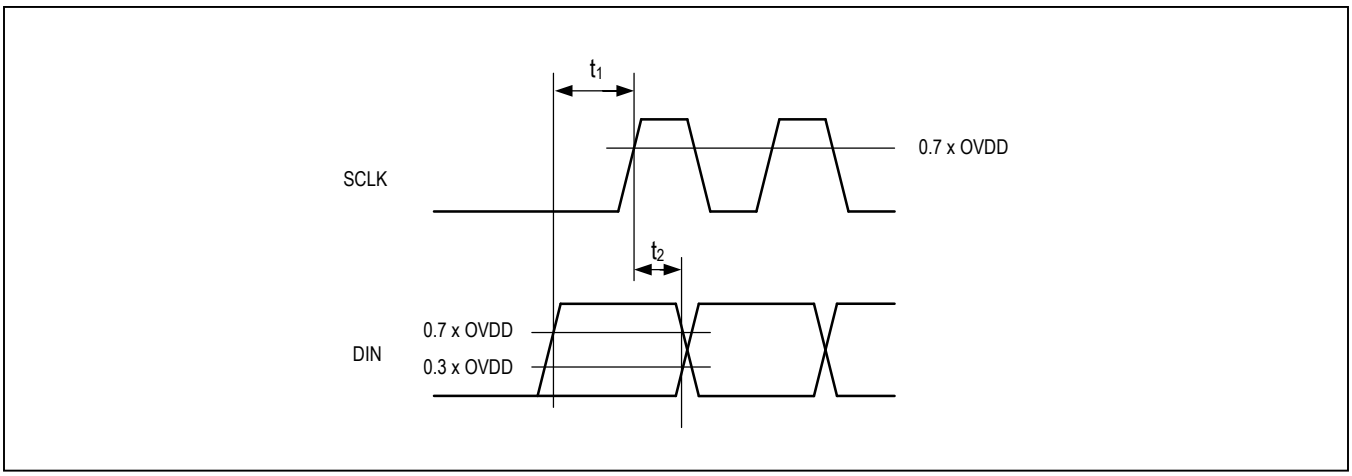


Figure 9. DIN Timing for Register Write Operations

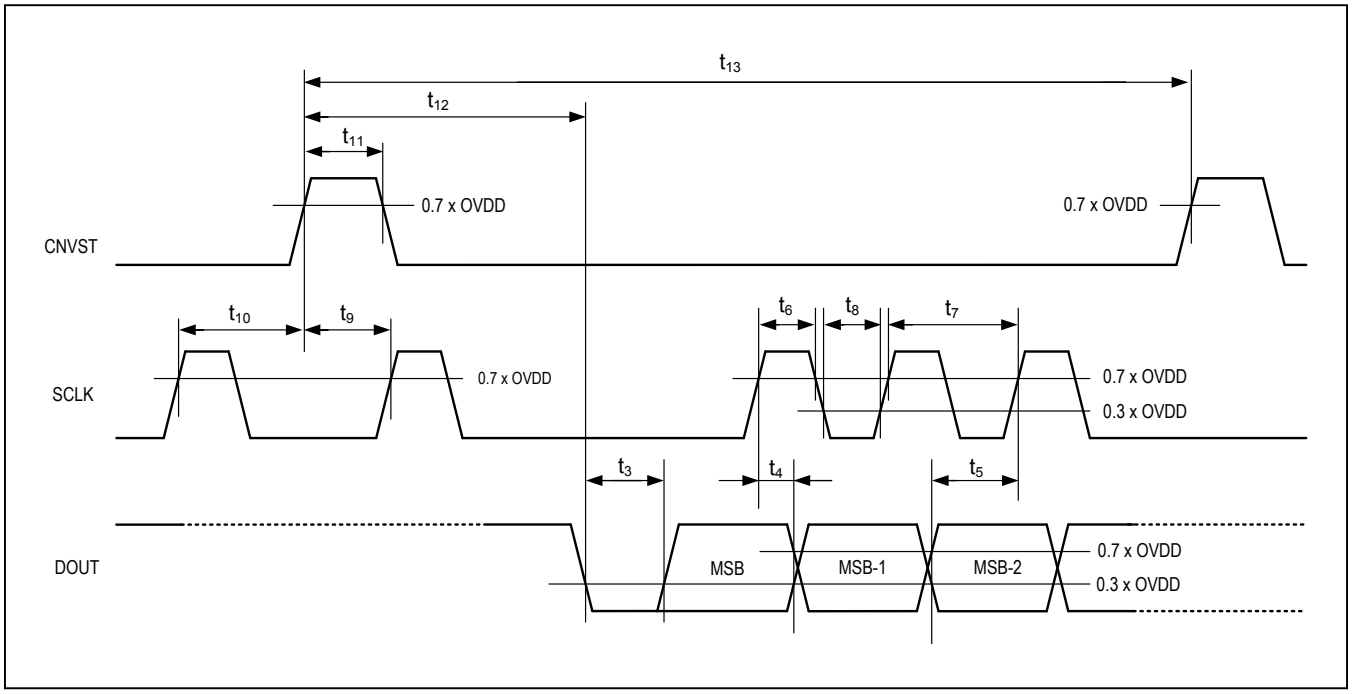


Figure 10. Timing Diagram for Data Out Reading After Conversion

Register Write

All SPI operations start with a command word. The structure of the command word is shown below. If there is no start bit, i.e. DIN is low, the part will output the conversion result and then go idle (see Figures 5, 6, and 7). The 16-bit mode register is the only register that can be written to. Figure 11 shows the waveform for a mode register write operation.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Start	0	Adr 3	Adr 2	Adr 1	Adr 0	R/$\overline{W}$	0

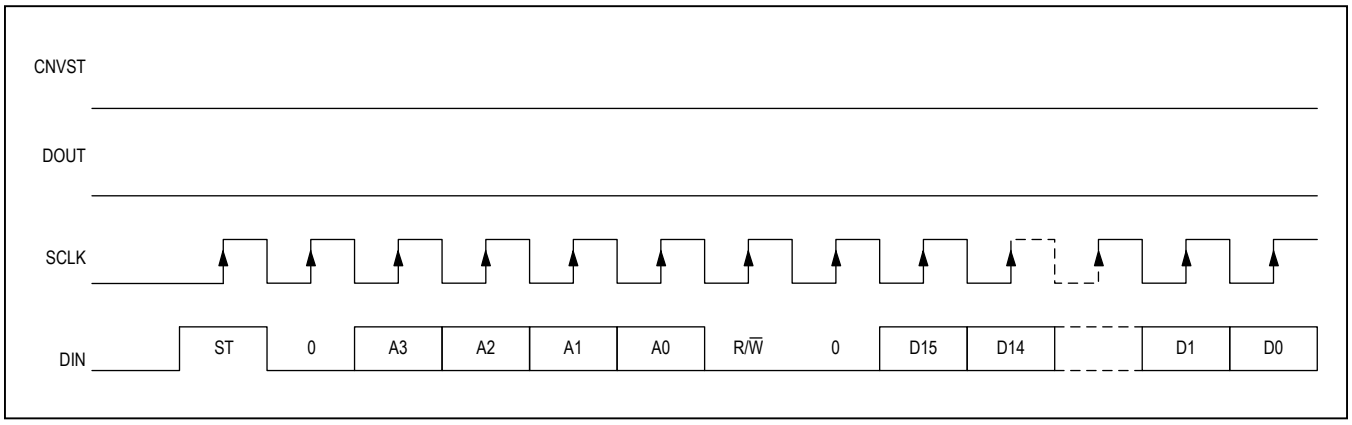


Figure 11. Mode Register Write

Register Read

A read operation is specified by setting the R/$\overline{W}$ bit high. Data will be output by the MAX11900 after the 8th rising SCLK edge. Figure 12 shows the waveform for a mode register read.

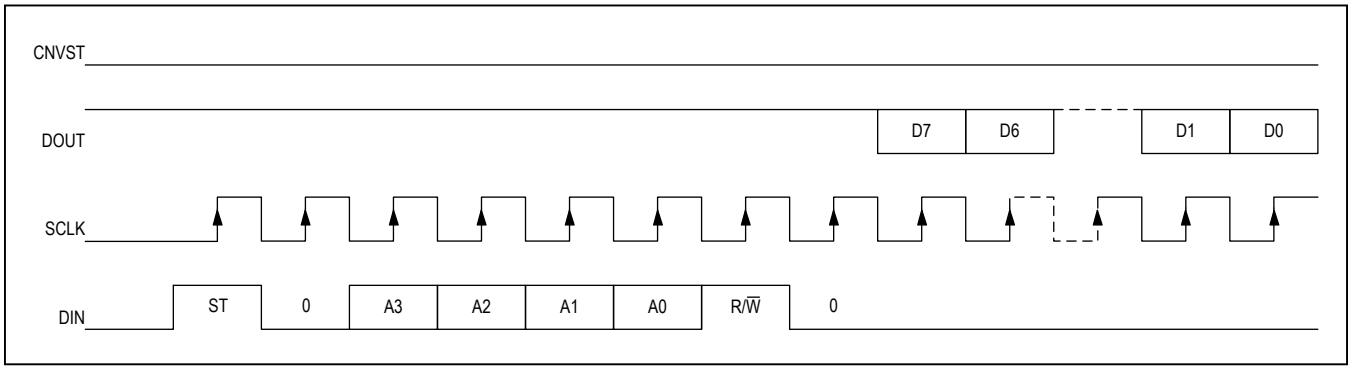


Figure 12. Register Read

Register Map

FUNCTION	ADDRESS	R/$\overline{W}$ BITS	DATA WIDTH	DATA
Read or Write Mode Register	0001	1 or 0	16	Mode Register
Read Conversion Result*	0010	1	16	Conversion Result
Read Chip ID	0100	1	8	Chip ID
Reserved, Do Not Use	All other	—	—	Reserved, Do Not Use

*Conversion result can also be read as shown in Figures 5, 6, and 7.

Mode Register

The reset state is: 0x0000. That is, the reference buffers are enabled if a valid reference voltage is applied at the REFIN pin. If external reference buffers are used, tie REFIN low and the buffers will be automatically powered down.

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset	—	—	—	—	—	DD2	DD1	DD0	—	—	PD REF1	POR pass	OTP busy	OB	PD REF2

Reset:	Reset the part when high.
DD[2:0]:	Program the driver strength on DOUT.
PD REF1:	Power down the first reference buffer when set.
POR pass:	High to indicate that POR was successful. If this bit is low, RESET should be asserted.
OTP busy:	High to indicate that the device is powering up.
OB:	Output data format is offset binary when high. two's complement when low.
PD REF2:	Power down the second reference buffer when set.

DD[2:0] program the driver strength on DOUT pin. Higher driver strengths are for systems that have larger capacitive loads on DOUT. The lowest driver strength that works should be chosen to save power and improve performance.

The driver strength is ordered from 1 to 6. The driver strength 1 is the weakest while the driver strength 6 is the strongest. Table 5 shows the mapping between the register value D[2:0] and the correspondent driver strength.

Table 5. DOUT Driver Strength

DD[2:0]	DRIVER STRENGTH
000	4
001	5
010	6
011	Not Valid
100	1
101	2
110	3
111	Not Valid

Conversion Result Register

A 16-bit read-only register, can be read directly or via a command read sequence.

Chip ID Register

This register holds a 4-bit code that can be used to verify the silicon revision. The ID = 1001b.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	—	—	—	ID3	ID2	ID1	ID0

Typical Application Circuit

Real-world signals usually require conditioning before they can be digitized by an ADC. The following outlines common examples of analog signal processing circuits for shifting, gaining, attenuating, and filtering signals.

Single-Ended Unipolar Input to Differential Unipolar Output

The circuit in Figure 13 shows how a single-ended, unipolar signal can interface with the MAX11900. This signal conditioning circuit transforms a 0V to +V_{REF} single-ended input signal to a fully differential output signal with a signal peak-to-peak amplitude of 2 x V_{REF} and common-mode voltage (V_{REF}/2). In this case, the single-ended signal source drives the high-impedance input of the first amplifier. This amplifier drives the AIN+ input of ADC and the second stage amplifier with peak-to-peak amplitude of V_{REF} and common-mode output voltage of V_{REF}/2. The second amplifier inverts this input signal and adds an offset to generate an inverted signal with peak-to-peak amplitude of V_{REF} and common-mode output voltage of V_{REF}/2, which drives the AIN- input of ADC.

Single-Ended Bipolar Input to Differential Unipolar Output

The MAX11900 is a differential input ADC that accepts a differential input signal with unipolar common mode. Figure 14 shows a signal conditioning circuit that transforms a -2 x V_{REF} to +2 x V_{REF} single-ended bipolar input signal to a fully differential output signal with amplitude peak-to-peak 2 x V_{REF} and common-mode voltage V_{REF}/2.

The single-ended bipolar input signal drives the inverting input of the first amplifier. This amplifier inverts and adds an offset to the input signal. It also drives the AIN- input of ADC and the second stage amplifier with peak-to-peak amplitude of V_{REF} and common-mode output voltage of V_{REF}/2. The second amplifier is also in inverting configuration and drives the AIN+ input of the ADC. This amplifier adds an offset to generate a signal with peak-to-peak amplitude of V_{REF} and common-mode output voltage of V_{REF}/2. The input impedance, seen by the signal source, depends on the input resistor of the first-stage inverting amplifier. Input impedance must be chosen carefully based on the output source impedance of the signal source.

Layout, Grounding, and Bypassing

For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect the GND pin on the MAX11900 to this ground plane. Keep the ground return to the power supply for this ground low impedance and as short as possible for noise-free operation.

A 2nF C0G ceramic chip capacitor should be placed between AIN+ and AIN- as close as possible to the MAX11900. This capacitor reduces the voltage transient seen by the input source circuit.

For best performance, connect the REF output to the ground plane with a 16V, 10µF ceramic-chip capacitor with a X5R dielectric in a 1210 or smaller case size. Ensure that all bypass capacitors are connected directly into the ground plane with an independent via.

Bypass AVDD, DVDD, and OVDD to the ground plane with 10µF ceramic chip capacitors on each pin as close as possible to the device to minimize parasitic inductance. For best performance, bring the AVDD and DVDD power plane in from the analog interface side of the MAX11900 and the OVDD power plane from the digital interface side of the device. Figure 15 shows the top layer of a sample layout.

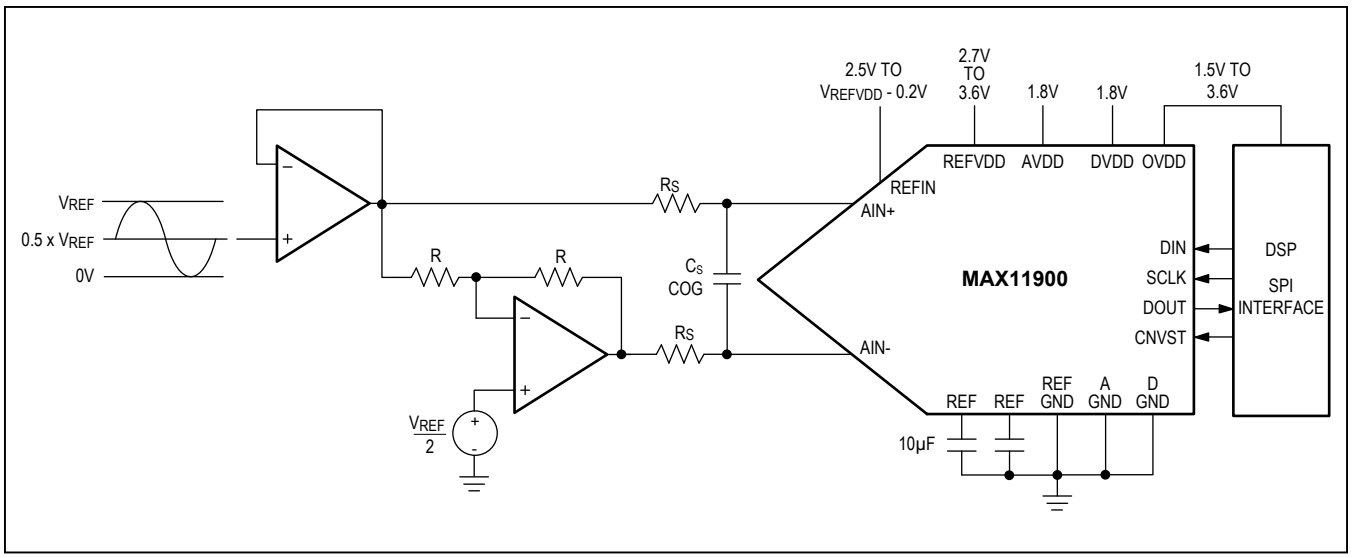


Figure 13. Unipolar Single-Ended Input

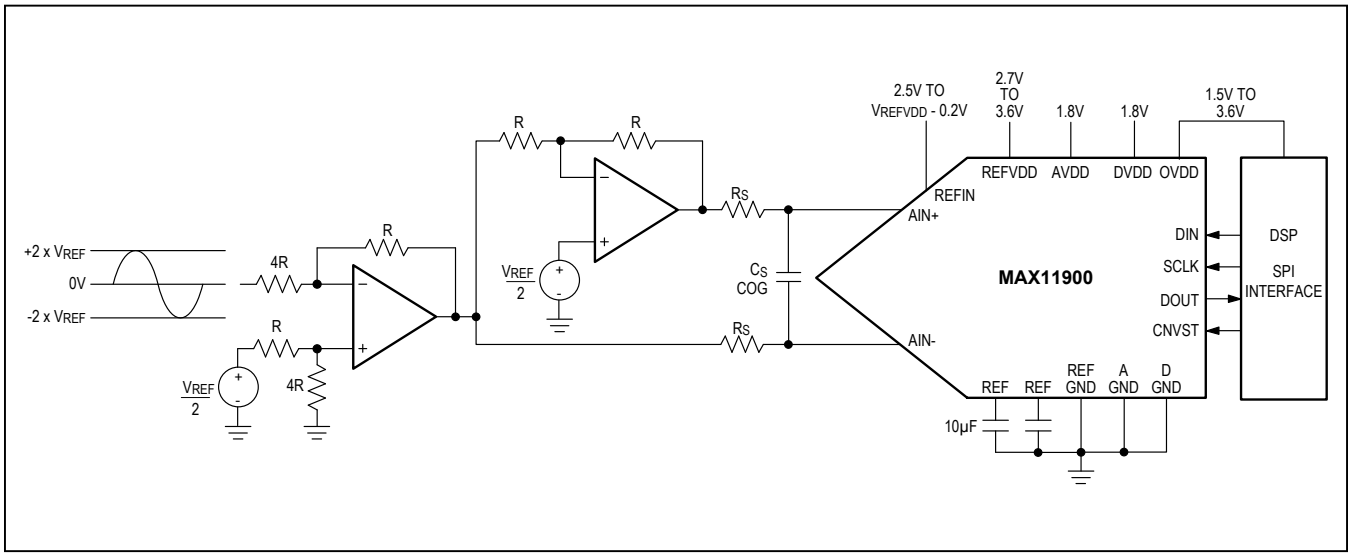


Figure 14. Bipolar Single-Ended Input

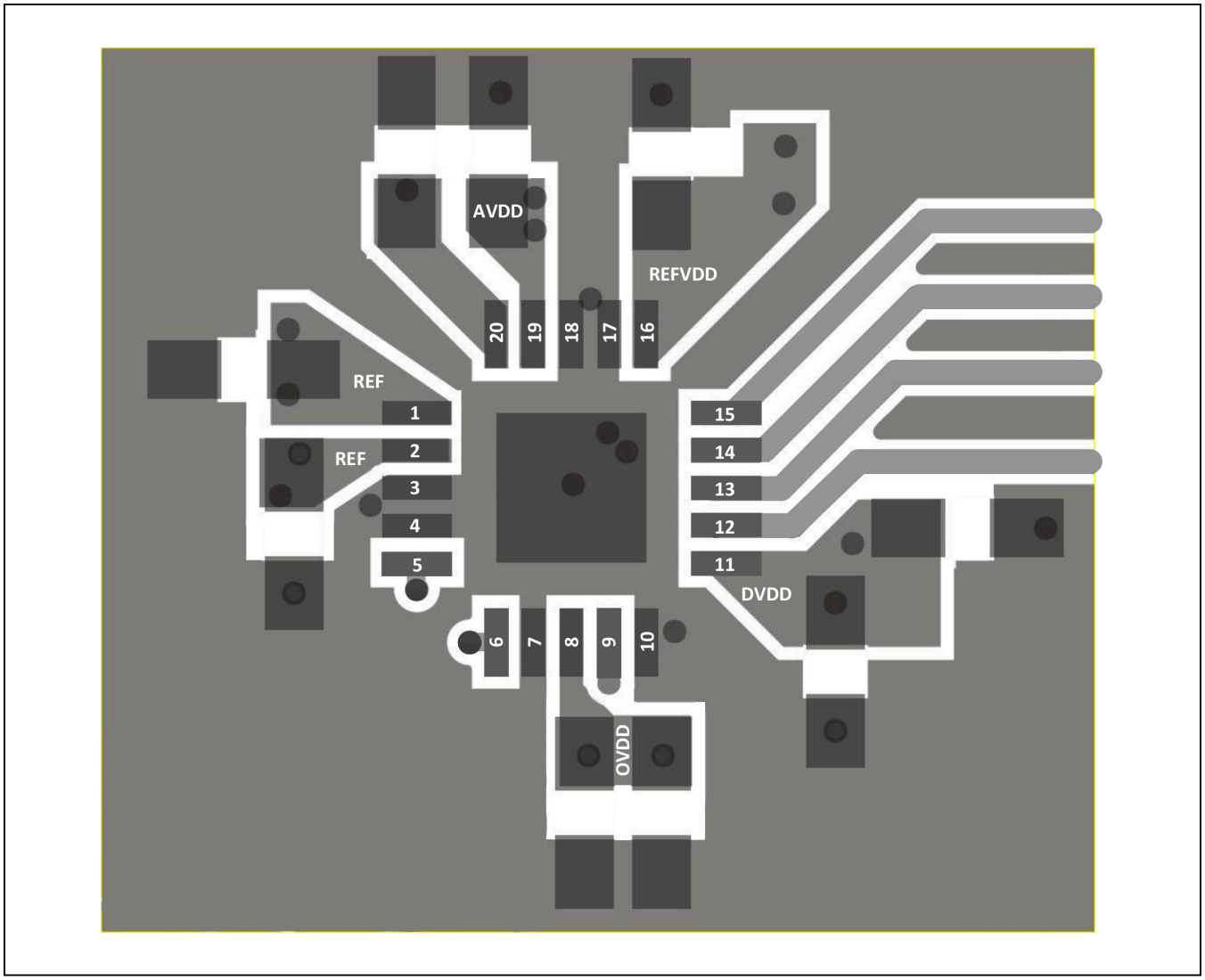


Figure 15. Top-Layer Sample Layout

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of less than ±1 LSB guarantees no missing codes.

Offset Error

The offset error is defined as the deviation between the actual output and ideal output measured with 0V differential analog input voltage.

Gain Error

Gain error is defined as the difference between the actual output range measured and the ideal output range expected. It is measured with signal applied at the input with an amplitude close to full-scale range.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input power to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the signal power to the noise power, which includes all spectral components not including the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's power to the power of all the other ADC output signals:

$$SINAD(dB) = 10 \times LOG\left[\frac{Signal}{Noise + Distortion}\right]$$

Effective Number of Bits

The effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the power contained in the first five harmonics of the converted data to the power of the fundamental. This is expressed as:

$$THD = 10 \times \log\left[\frac{P_2 + P_3 + P_4 + P_5}{P_1}\right]$$

where P1 is the fundamental power and P2 through P5 is the power of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the power of the fundamental (maximum signal component) to the power of the next-largest frequency component.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

Selector Guide

PART	BITS	SPEED (ksps)	FULLY DIFFERENTIAL INPUT (MAX) (V)	REFERENCE BUFFERS	PACKAGE
MAX11900	16	1000	±3.6	Internal/External	4mm x 4mm TQFN-20
MAX11901	16	1600	±3.6	Internal/External	4mm x 4mm TQFN-20
MAX11902	18	1000	±3.6	Internal/External	4mm x 4mm TQFN-20
MAX11903	18	1600	±3.6	Internal/External	4mm x 4mm TQFN-20
MAX11904	20	1000	±3.6	Internal/External	4mm x 4mm TQFN-20
MAX11905	20	1600	±3.6	Internal/External	4mm x 4mm TQFN-20

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11900ETP+	-40°C to +85°C	20 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2044+5	21-0139	90-0429

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/15	Initial release	—

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