TOSHIBA CMOS Integrated Circuit Silicon Monolithic

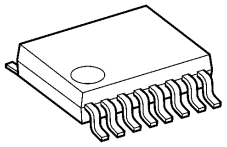
TC78B002FNG

Single Phase Full-wave Driver for Fan Motor

TC78B002FNG is a single phase full-wave driver for fan motor. It has a DMOS device in an output transistor.

A highly effective drive is possible by adopting a DMOS output driver with low ON resistance and a PWM drive system.

TC78B002FNG



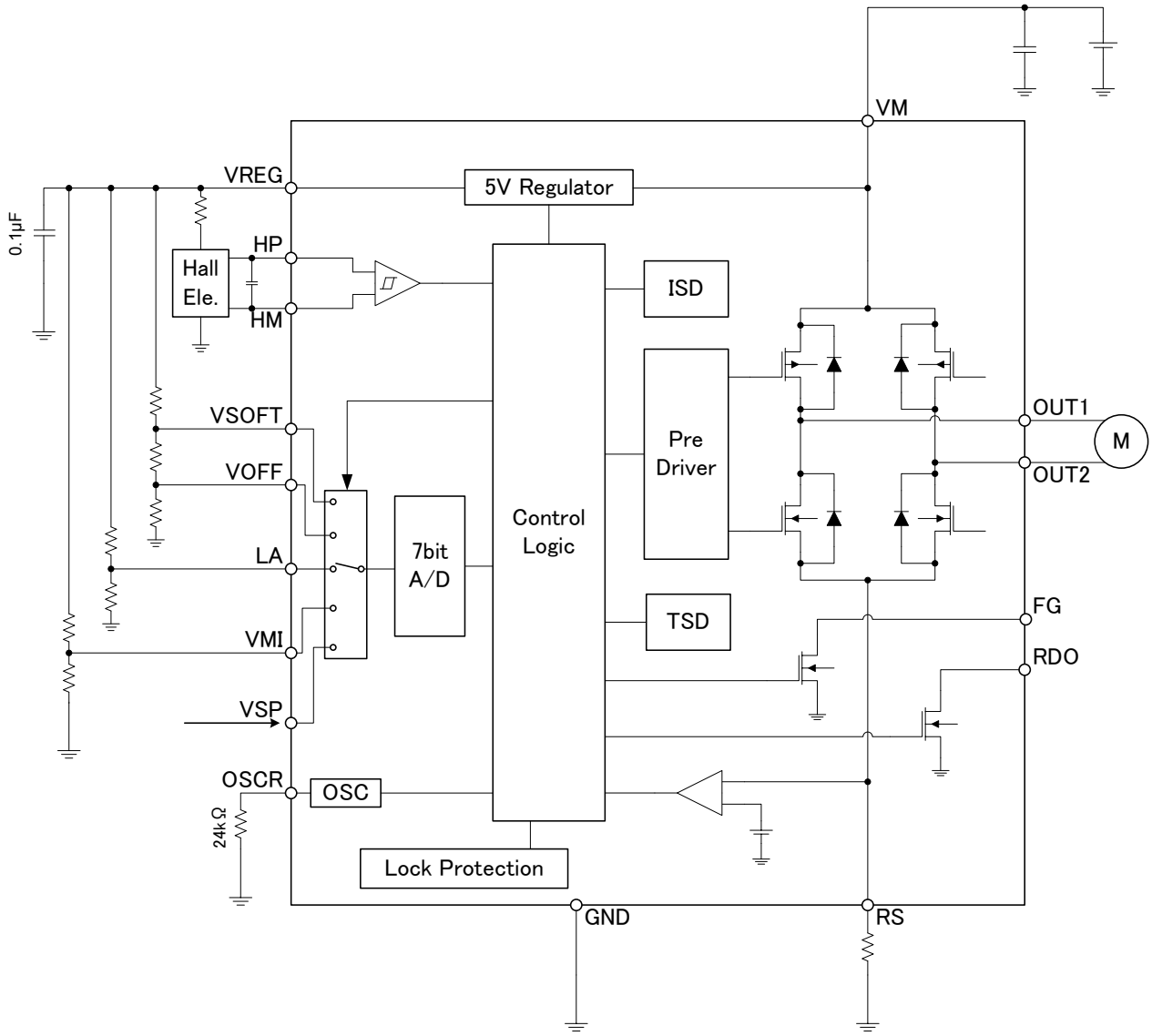
SSOP16-P-225-0.65B

Weight: 0.07g (typ)

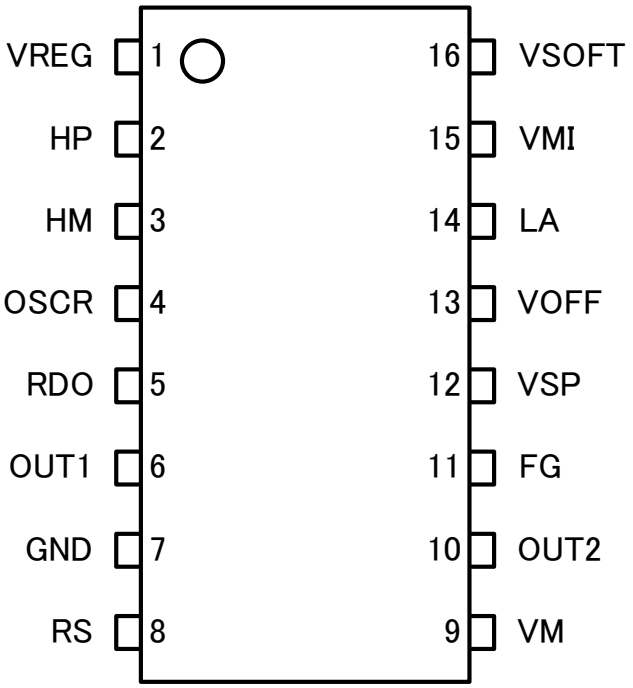
Features

- Single-phase full-wave drive
- Motor power supply voltage: VM =16V (maximum operating range)
- Output current: Iout = 1.5A (max.)
- PWM control
- Built-in oscillation circuit (External resistor)
- Soft switching drive
- Lock protection, Automatic recovery
- Quick start
- Built in hall bias
- Rotation Speed Detection (FG) and Lock Detection (RDO) Output
- Current limit function
- Built in over current protection
- Built in thermal shut down circuit

Block Diagram (Application circuit)



Pin Assignment



Pin Description

Pin No.	Pin name	Description
1	VREG	Output pin for reference voltage of 5 V
2	HP	Hall signal input pin +
3	HM	Hall signal input pin−
4	OSCR	Connection pin for resistor of oscillation circuit
5	RDO	Output pin for lock detection
6	OUT1	Motor output pin 1
7	GND	Connection pin for ground
8	RS	Connection pin for detecting resistor of output current
9	VM	Power supply pin
10	OUT2	Motor output pin 2
11	FG	Rotating output pin
12	VSP	Setting pin for output duty
13	VOFF	Setting pin for OFF term in switching conducting phase
14	LA	Setting pin for lead angle
15	VMI	Setting pin for minimum output duty
16	VSOFT	Setting pin for soft switching term

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Power supply voltage		VM	18	V
Input voltage		V_{IN}	-0.3~6 (Note 1)	V
Output voltage		V_{OUT}	18 (Note 2)	V
Output current	OUT1,OUT2	I_{OUT}	1.5 (Note 3)	A
	VREG	I_{OUT}	10	mA
FG pin sink current		I_{FG}	10	mA
RDO pin sink current		I_{RDO}	10	mA
Power dissipation		P_D	0.96 (Note 4)	W
Operating temperature		T_{opr}	-40 to 105	°C
Storage temperature		T_{stg}	-55 to 150	°C

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

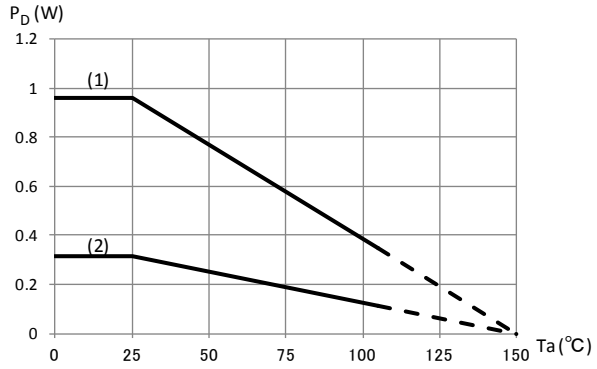
Note 1: VMI, VSP, VSOFT, VOFF, and LA pins

Note 2: OUT1, OUT2, FG and RDO pins

Note 3: Power dissipation must not be exceed

Note 4: Mounted on a glass epoxy board

Package Power Dissipation



(1) When mounted on the board (40mm×30mm×1.6mm 2 layers, FR-4 board) Rth(j-a)=130°C/W

(2) IC only Rth(j-a)=400°C/W

Operating Ranges (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Power supply voltage	VM_{opr1}	5.5	12	16	V
Power supply for low voltage operation	VM_{opr2}	3.5	4.5	5.5	V
Internal oscillation frequency (Note 1)	f_{OSC}	8	10	12	MHz
PWM frequency	f_{PWM}	20	25	30	kHz
Input voltage (Note 2)	V_{IN}	0	—	V_{REG}	V

Note 1: In low-voltage operation, operation with frequency more than 10MHz is not covered under guarantee.

Note 2: VMI, VSOFT, VOFF, and LA pins

Electrical Characteristics (Ta = 25°C and VM = 12 V, unless otherwise specified.)

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
Power supply current		I_{VM}	VM = 12 V, V_{REG} = OPEN Hall input=100Hz, output OPEN	—	3	5	mA
Hall signal input	Common mode input voltage range	V_{CMRH}		0	—	V_{REG} -1.5	V
	Input voltage swing	V_H		40	—	—	mV
	Input current	I_H	$\|V_{HP}-V_{HM}\| \geqq 100mV$	—	—	1	μA
	Hysteresis＋Voltage	V_{HHYS+}	(Design target value) (Note 1)	5	10	15	mV
	Hysteresis－Voltage	V_{HHYS-}	(Design target value) (Note 1)	-15	-10	-5	mV
VREG pin voltage		V_{REG}	VREG pin output source current=10mA	4.5	5.0	5.5	V
Maximum voltage of ADC convertor		V_{ADC}	(Design target value) (Note 1)	—	V_{REG} -0.75	—	V
Output On Duty (Note 1)		Duty(20)	R_{OSC}=24kΩ, output load:1kΩ V_{SP}=1.2V, VMI=0V or VMI=1.2V, V_{SP}=0V	15	20	25	%
		Duty(50)	R_{OSC}=24kΩ, output load:1kΩ V_{SP}=2.2V, VMI=0V or VMI=2.2V, V_{SP}=0V	43	50	57	%
		Duty(80)	R_{OSC}=24kΩ, output load:1kΩ V_{SP}=3.2V, VMI=0V or VMI=3.2V, V_{SP}=0V	70	80	90	%
VSP threshold		$V_{AD\ (L)}$	Threshold voltage of stopping output	0.5	0.55	—	V
		$V_{AD\ (H)}$	Threshold voltage of full output	—	3.9	4.3	
VSP response time		T_{VSP}	(Design target value) (Note 1)	—	—	10	ms
Internal oscillation frequency		f_{OSC}	R_{OSC}=24kΩ Measured by internal divided frequency	8	10	12	MHz
PWM frequency		f_{PWM}	R_{OSC}=24kΩ	20	25	30	kHz
Pin input current		I_{IN}	VSP,VMI,VSOFT,VOFF, and LA pins input voltage 0~V_{REG}	—	—	1	μA
Output ON resistance		Ron(H+L)	I_{OUT} = 0.2A	—	1.6	2.5	Ω
Soft switching time (Note 1)		T_{SOFT}(0)	R_{OSC}=24kΩ, Hall input=100Hz VOFF=0V , VSOFT=0V	—	—	0	°
		T_{SOFT}(45)	R_{OSC}=24kΩ, Hall input=100Hz VOFF=0V , VSOFT=V_{REG}*0.45	43	—	47	
		T_{SOFT}(90)	R_{OSC}=24kΩ, Hall input=100Hz VOFF=0V , VSOFT= V_{REG}	84	—	90	
OFF term (Note 1)		T_{OFF}(0)	R_{OSC}=24kΩ, Hall input=100Hz VSOFT=0V, VOFF=0V	—	—	0	°
		T_{OFF}(45)	R_{OSC}=24kΩ, Hall input=100Hz VSOFT=0V, VOFF= V_{REG}*0.45	43	—	47	
		T_{OFF}(90)	R_{OSC}=24kΩ, Hall input=100Hz VSOFT=0V, VOFF= V_{REG}	84	—	90	
Lead angle correction (Note 1)		T_{LA}(0)	R_{OSC}=24kΩ, Hall input=100Hz LA=0V	—	—	0	°
		T_{LA}(11.25)	R_{OSC}=24kΩ, Hall input=100Hz LA= V_{REG}*0.23	10	—	12	
		T_{LA}(22.5)	R_{OSC}=24kΩ, Hall input=100Hz LA= V_{REG}	21	—	24	

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
FG RDO pin	Output low voltage	$V_{OUT}(L)$	$I_{FG/RDO}$=5mA	—	—	0.3	V
	Output leakage current	$I_{OUT}(H)$	$V_{FG/RDO}$=5V	—	—	1	μA
Current limit detecting voltage for RS pin		V_{RS}		0.27	0.3	0.33	V
Masking time of current limit detection		T_{mask}	(Design target value) (Note 1)	1.2	1.5	1.8	μs
Operating current of over current protection		I_{LIM}	(Design target value) (Note 1)	—	2.5	—	A
Masking time of over current protection		$T_{ISDMASK}$	(Design target value) (Note 1)	—	2	—	μs
OFF time of over current protection		T_{ISDOFF}	(Design target value) (Note 1)	—	100	—	ms
Operating temperature of thermal shutdown circuit		T_{SD}	Junction temperature (Design target value) (Note 1)	—	170	—	℃
Hysteresis of thermal shutdown circuit		ΔT_{SD}	(Design target value) (Note 1)	—	40	—	℃
ON time of lock detection		T_{ON}	R_{OSC}=24kΩ (Design target value) (Note 1)	0.32	0.4	0.48	s
OFF time of lock detection		T_{OFF}	R_{OSC}=24kΩ (Design target value) (Note 1)	3.2	4	4.8	s
Detecting voltage for low voltage		V_{UVLO}	Operation voltage (Design target value) (Note 1)	2.6	2.9	3.2	V
		V_{PORRL}	Recovery voltage (Design target value) (Note 1)	2.9	3.2	3.5	V
Output switching characteristics		t_r	(Design target value) (Note 1)	—	100	—	ns
		t_f	(Design target value) (Note 1)	—	100	—	

Note 1: Pre-shipment testing is not performed.

Reference Data

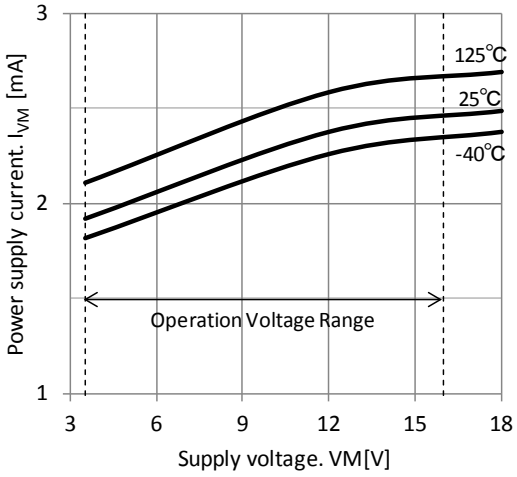


Fig.1 Power supply current

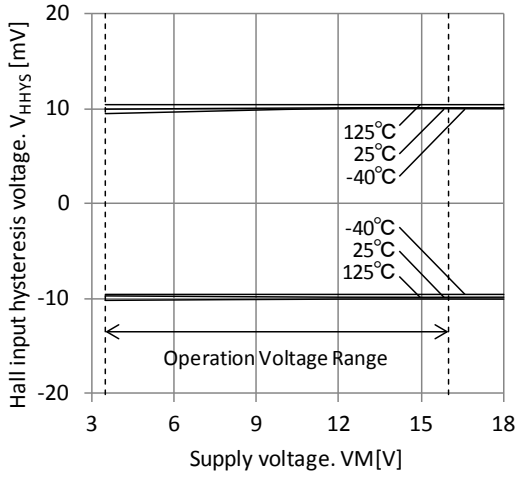


Fig.2 Hall input Hysteresis voltage

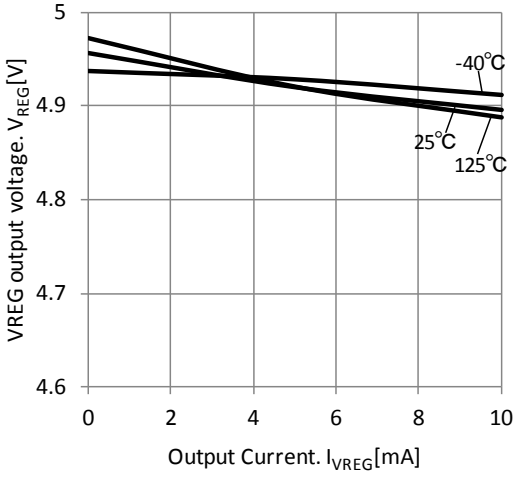


Fig.3 VREG pin voltage (VM=12V)

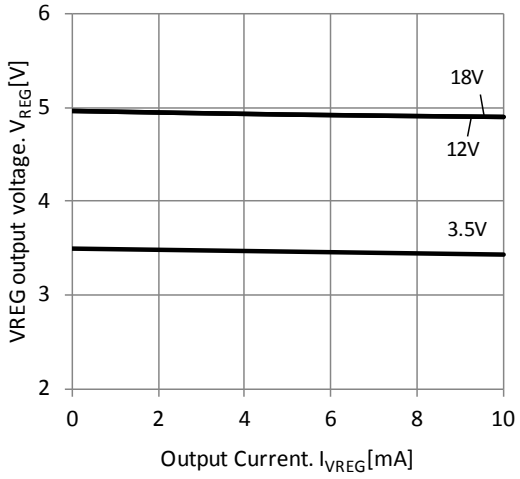


Fig.4 VREG pin voltage (Ta=25℃)

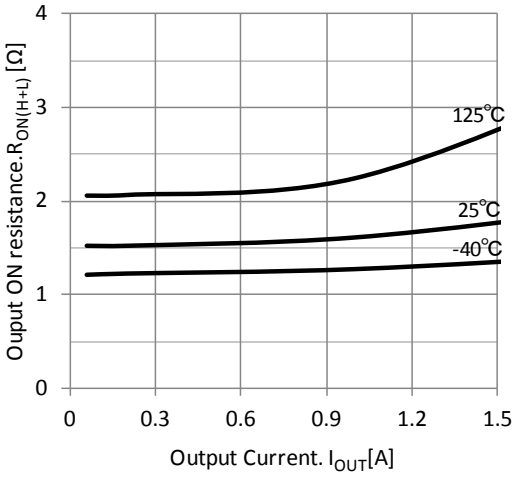


Fig.5 Output ON resistance (VM=12V)

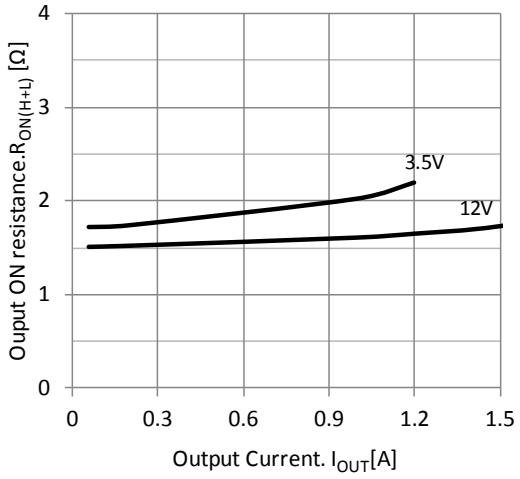


Fig.6 Output ON resistance (Ta=25℃)

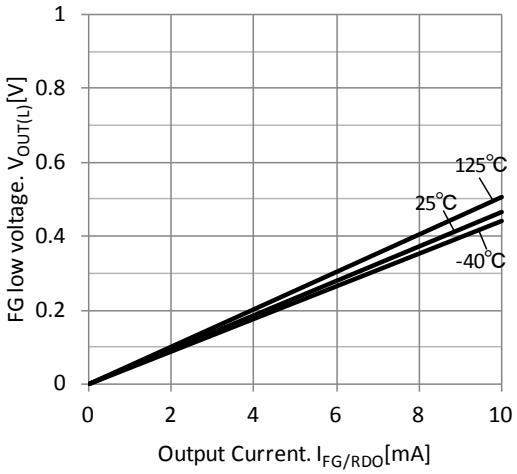


Fig.7 FG/RDO pin Output low voltage (VM=12V)

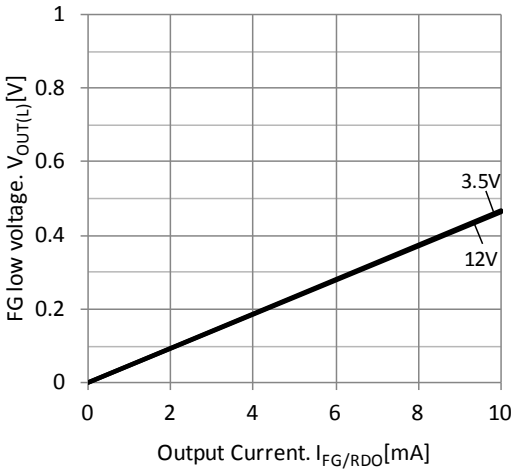


Fig.8 FG/RDO pin Output low voltage (Ta=25°C)

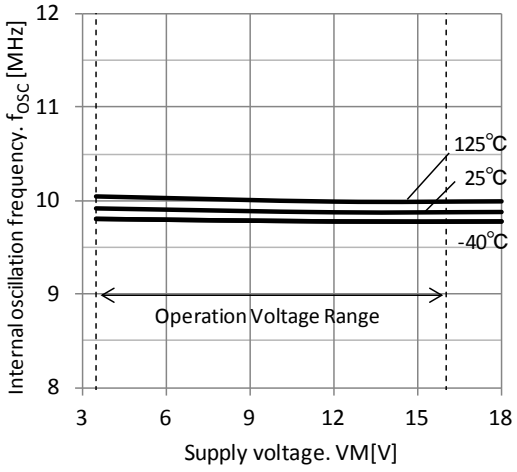


Fig.9 Internal oscillation frequency

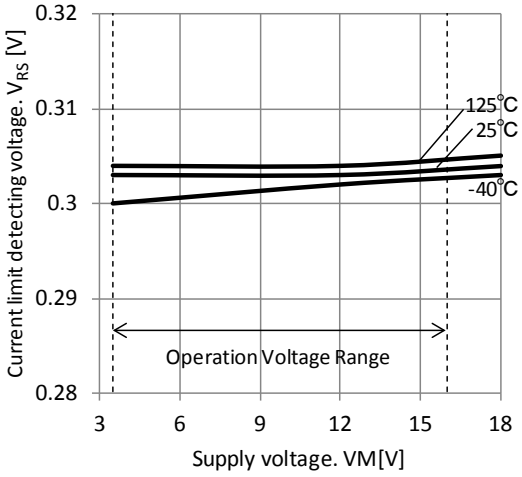
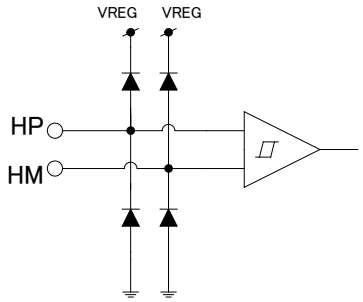
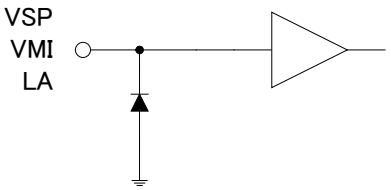
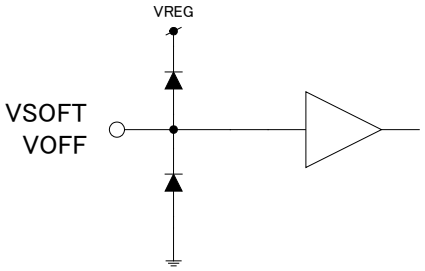
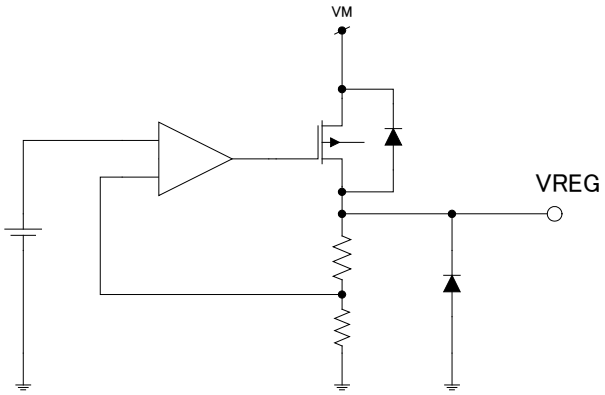
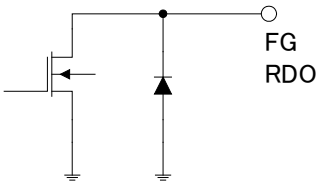
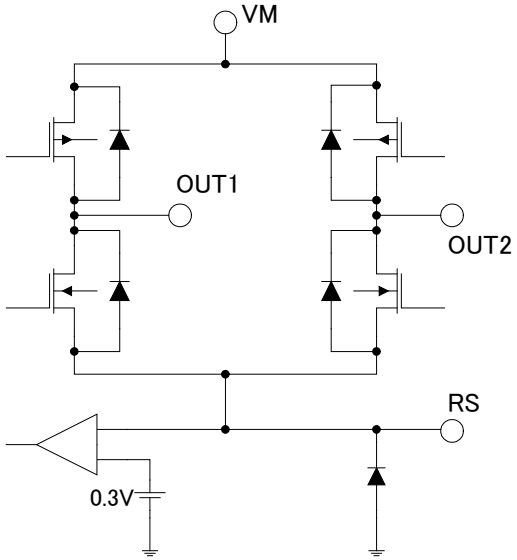
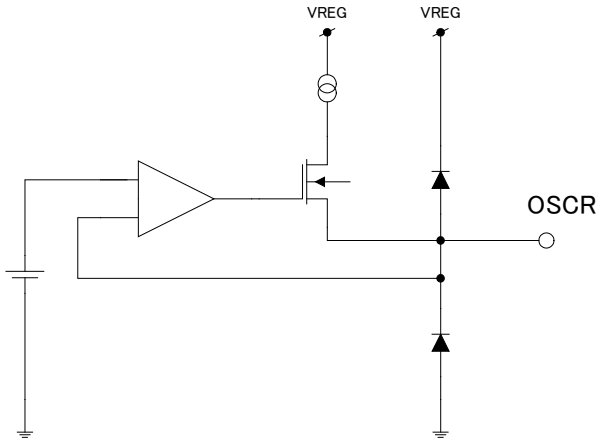


Fig.10 Current limit detecting voltage for RS pin

I/O Equivalent Circuits

Pin name	I/O signal	Equivalent circuit
HP HM	Hall signal input pin In-phase input voltage range 0V to V_{REG}-1.5V	
VSP VMI LA	Control voltage input pin	
VSOFT VOFF	Control voltage input pin	
VREG	Voltage output pin V_{REG} = 5V (typ)	
FG RDO	Digital output pin Open drain output It should be pulled up externally to output High.	

Pin name	I/O signal	Equivalent circuit
VM OUT1 OUT2 RS	Motor output pin	
OSCR	Connection pin for resistor of oscillation circuit	

Functional Description

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes. Timing charts may be simplified for explanatory purposes.

1. Basic Operation

At startup, the motor is driven by a square-wave drive by determining the conducting phase with hall input signal.

When hall signal frequency reaches 5Hz (typ) or more, the motor is driven by the conducting pattern which is generated by estimating the next conducting timing from the hall input signal.

<I/O function table>

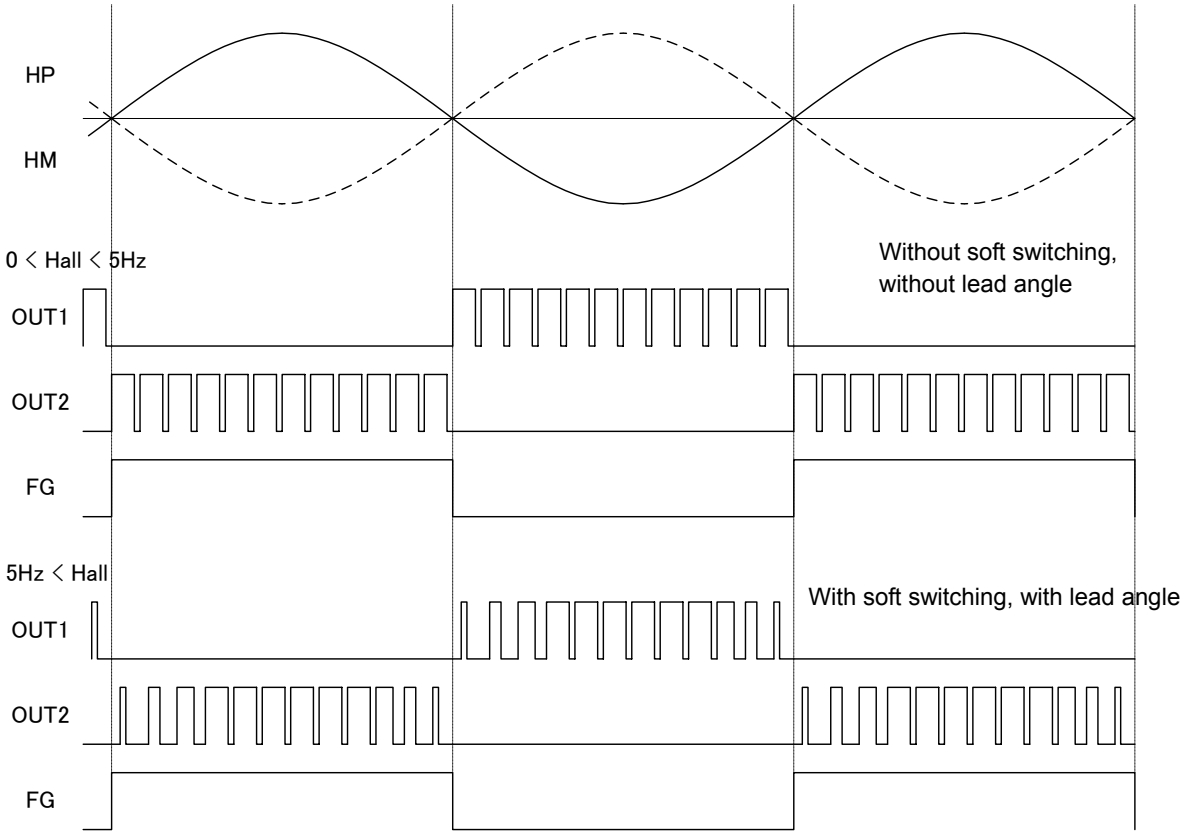
HP	HM	OUT1	OUT2	FG	RDO	Mode
H	L	L	PWM	OFF	L	Rotating (Note 1)
L	H	PWM	L	L	L	
H	L	L	OFF	OFF	—	Current limit drive (Note 2)
L	H	OFF	L	L	—	
—	—	OFF	OFF	—	OFF	Lock protection (Note 3)
—	—	OFF	OFF	—	—	Thermal shutdown

Note 1 : Conducting phase is switched by the hall input signal. FG signal is outputted according to the phase-switching. Conducting timing may be preceded depending on the lead angle set.

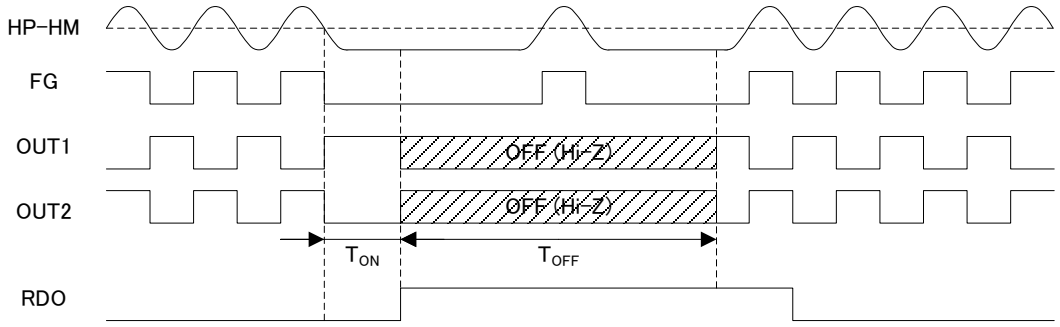
Note 2 : Upper power transistor is turned off during current limitation. It recovers automatically every PWM frequency.

Note 3 : FG output changes depending on the rotor position in the lock protection mode the same as rotating mode.

Timing chart (Normal rotation)



Timing chart (Lock protection)



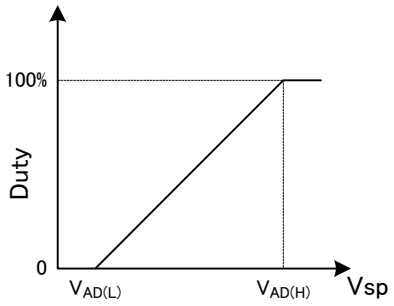
2. VSP/ VMI Input Pin

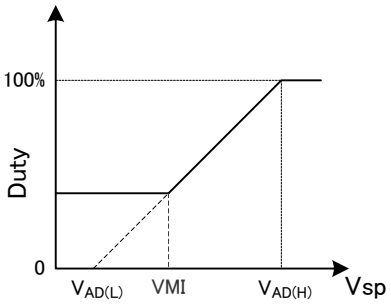
Output starts when VSP pin at the voltage of more than $V_{AD(L)}$. And it turns off at the voltage of $V_{AD(L)}$ or less. Minimum voltage of VSP pin is clipped by the voltage of VMI pin.

In case the minimum duty setting by VMI pin is not used, connect the VMI pin to the GND pin.

Analog voltage which is input to VSP pin and VMI pin is converted by AD convertor of 7 bit, and the output PWM duty is controlled.

0	≤	VSP, VMI	≤	$V_{AD\ (L)}$	→	Duty = 0%
$V_{AD\ (L)}$	<	VSP, VMI	≤	$V_{AD\ (H)}$	→	Below figure (17/127 to 116/127)
$V_{AD\ (H)}$	<	VSP, VMI	≤	V_{REG}	→	Duty = 100% (117/127 to 127/127)

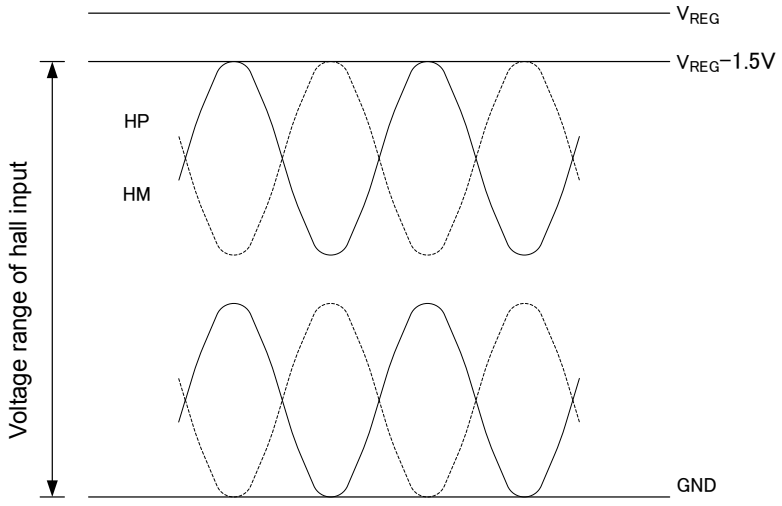


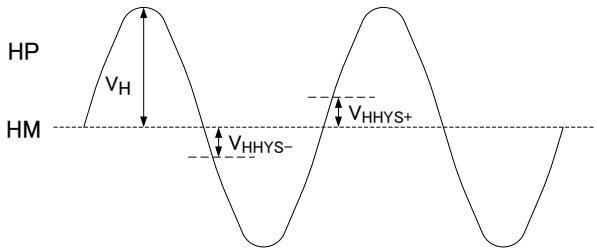


(PWM duty indicates the peak value of output because this circuit has a soft switching function.)

3. Hall Input Signal

Characteristics of hall signal shown below are inputted to the hall input pin.





V_H: 40mV or more
V_{HHYS+}=10mV, V_{HHYS-}=-10mV

*Though hall amplifier operates when V_H is 40mV or more, please widen the oscillation as possible to stabilize the time width.
(200mV or more is recommended.)

4. OSC Frequency and PWM Frequency

Oscillation frequency is approximated by below formula.

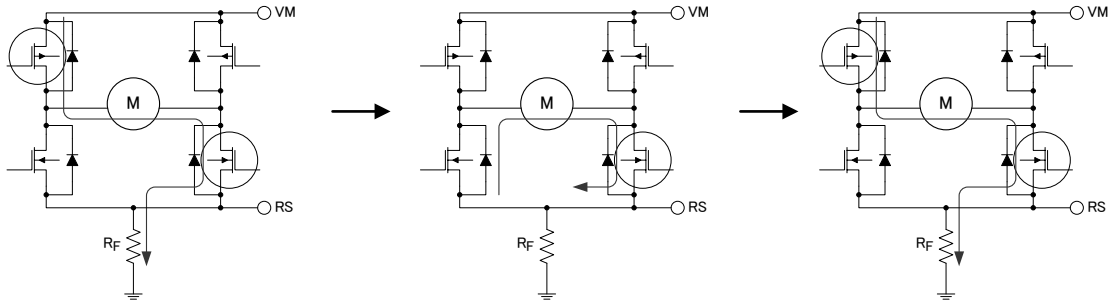
$f_{OSC} = 1/(2C[F] \times R_{OSC}[\Omega])$ [Hz]= $1/(2 \times 2.08e\text{-}12[F] \times R_{OSC}[\Omega])$ [Hz]

Oscillation frequency f_{OSC} is 10MHz(typ) when external resistor ROSC is 24kΩ

PWM frequency $f_{PWM}=f_{OSC}/400$.

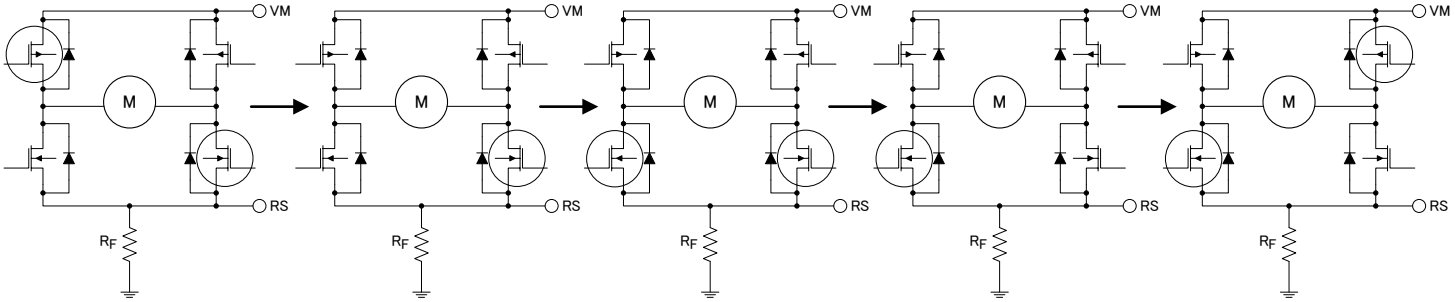
5. PWM Output Drive

In PWM drive, upper power transistor is turned on and off repeatedly.



PWM ON → PWM ON → OFF → PWM ON

In switching phase, power transistor operates in below order.



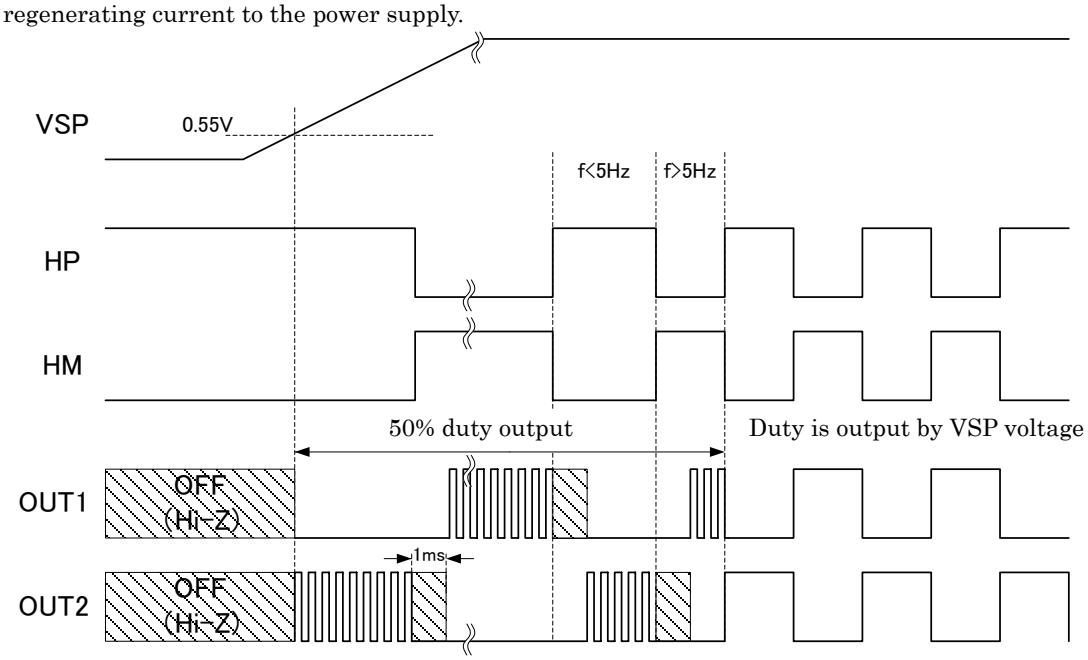
PWM ON → PWM OFF → Short brake → PWM OFF → PWM ON

200ns (Design target value)

6. Startup Sequence

Output starts when VSP pin at the voltage of $V_{AD(L)}$ or more. In order to ensure the starting torque, PWM output is 50% duty when the motor rotating speed is lower than 5Hz (typ).

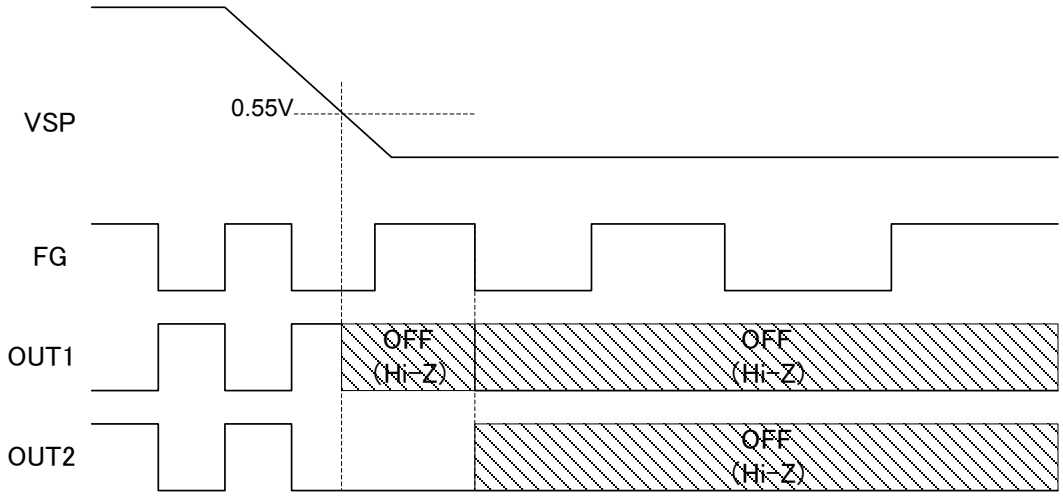
When output phase is switched during startup sequence, PWM OFF term of 1ms (typ) is inserted to reduce the regenerating current to the power supply.

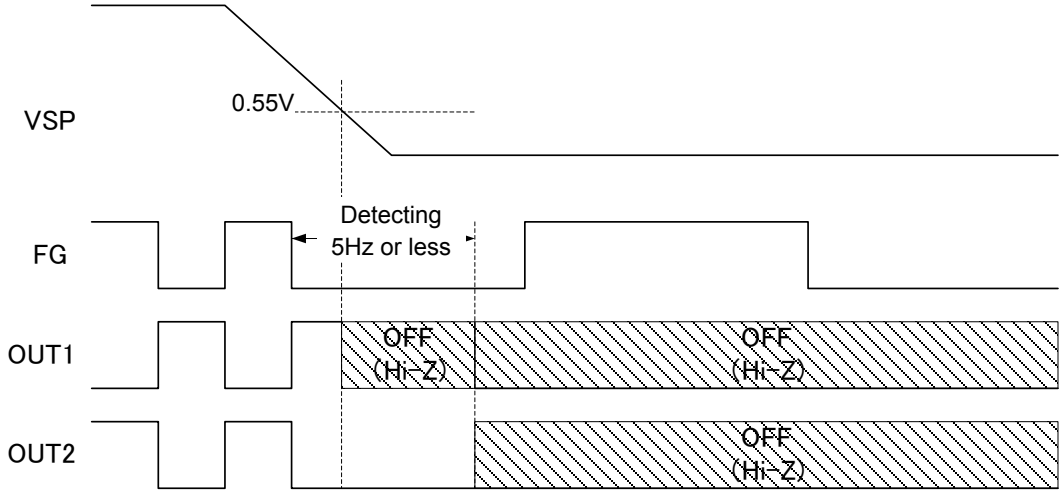


7. Turning Off

Output turns off when the voltage of VSP pin is $V_{AD(L)}$ or less.

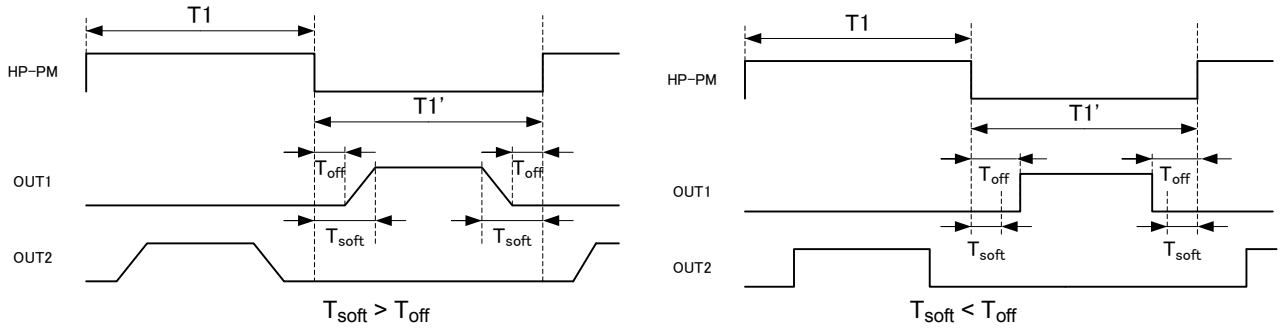
Before all output power transistors are turned off, the time, until the edge of FG signal is detected twice or the frequency of 5 Hz or less is detected, is defined PWM OFF term.





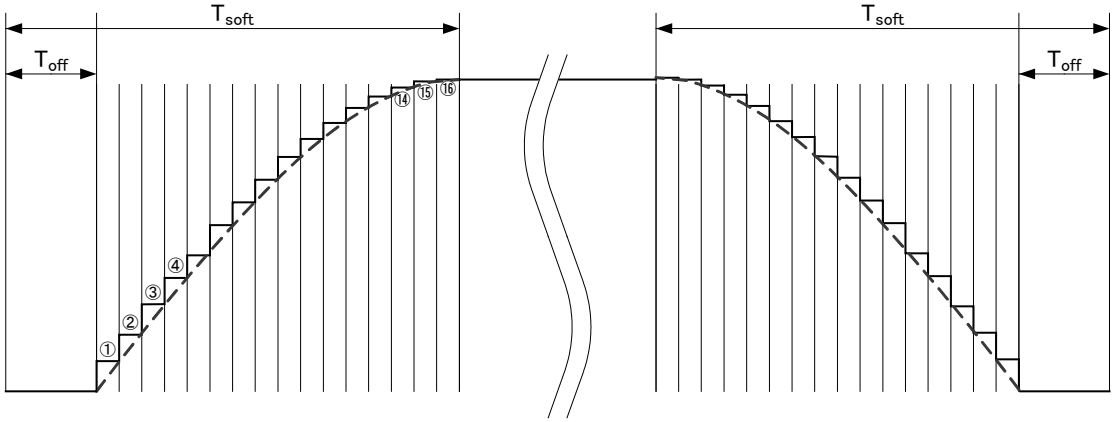
8. Soft Switching

Soft switching is performed by changing the output PWM duty gradually when conducting phase switches. The time of soft switching is determined by the voltage of VSOFT pin and that of VOFF pin.



Voltage of VSOFT > Voltage of VOFF:

Total term of soft switching (Tsoft) is determined by the time of prior hall signal (180°) and the voltage of VSOFT pin. OFF term is provided during soft switching. The time of OFF term (Toff) is determined by the prior hall signal (180°) and the voltage of VOFF pin. During OFF term, the state of the power transistor is in the PWM OFF mode. Soft switching operates in the period other than the OFF term, and output PWM duty changes by 16 steps in maximum.



Voltage of VSOFT < Voltage of VOFF:

It does not have the term of soft switching operation which changes the duty, but it has the OFF term. OFF term (Toff) is determined by the time of the prior hall signal (180°) and the voltage of VOFF pin. During OFF term, the sate of the power transistor is in the PWM OFF mode.

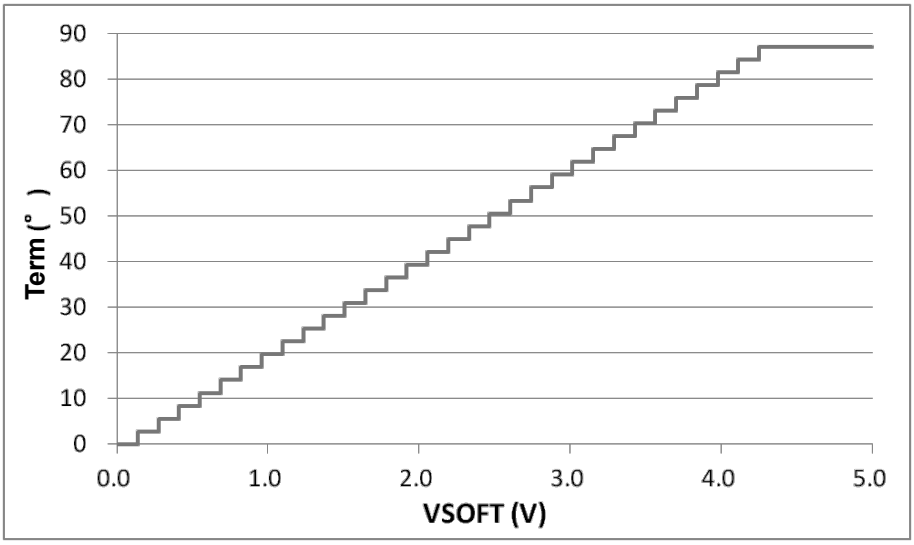
When next edge does not occur though time of T1' passes, last output state continues.
Conducting pattern is reset in synchronization with the up edge and the down edge of the hall signal.
So, waveform indicates non-contiguous every reset when hall signal is offset and in speed up/slow down mode.

<Relation between the voltage of VSOFT pin and the term of soft switching>

VSOFT = 0V → 0°

VSOFT = V_{ADC} → 87.2° (In case voltage of V_{ADC} or more is input, it is set to 87.2°.)

Step	VSOFT (V)	Term (°)	Step	VSOFT (V)	Term (°)	Step	VSOFT (V)	Term (°)
1	0.00	0.0	12	1.51	30.9	23	3.02	61.9
2	0.14	2.8	13	1.65	33.8	24	3.15	64.7
3	0.27	5.6	14	1.78	36.6	25	3.29	67.5
4	0.41	8.4	15	1.92	39.4	26	3.43	70.3
5	0.55	11.3	16	2.06	42.2	27	3.56	73.1
6	0.69	14.1	17	2.19	45.0	28	3.70	75.9
7	0.82	16.9	18	2.33	47.8	29	3.84	78.8
8	0.96	19.7	19	2.47	50.6	30	3.98	81.6
9	1.10	22.5	20	2.60	53.4	31	4.11	84.4
10	1.23	25.3	21	2.74	56.3	32	4.25	87.2
11	1.37	28.1	22	2.88	59.1			



< Relation between the voltage of VOFF pin and the term of turning off>

VOFF = 0V → 0°

VOFF = V_{ADC} → 87.2° (In case voltage of V_{ADC} or more is input, it is set to 87.2°)

Step	VOFF (V)	Term (°)	Step	VOFF (V)	Term (°)	Step	VOFF (V)	Term (°)
1	0.00	0.0	12	1.51	30.9	23	3.02	61.9
2	0.14	2.8	13	1.65	33.8	24	3.15	64.7
3	0.27	5.6	14	1.78	36.6	25	3.29	67.5
4	0.41	8.4	15	1.92	39.4	26	3.43	70.3
5	0.55	11.3	16	2.06	42.2	27	3.56	73.1
6	0.69	14.1	17	2.19	45.0	28	3.70	75.9
7	0.82	16.9	18	2.33	47.8	29	3.84	78.8
8	0.96	19.7	19	2.47	50.6	30	3.98	81.6
9	1.10	22.5	20	2.60	53.4	31	4.11	84.4
10	1.23	25.3	21	2.74	56.3	32	4.25	87.2
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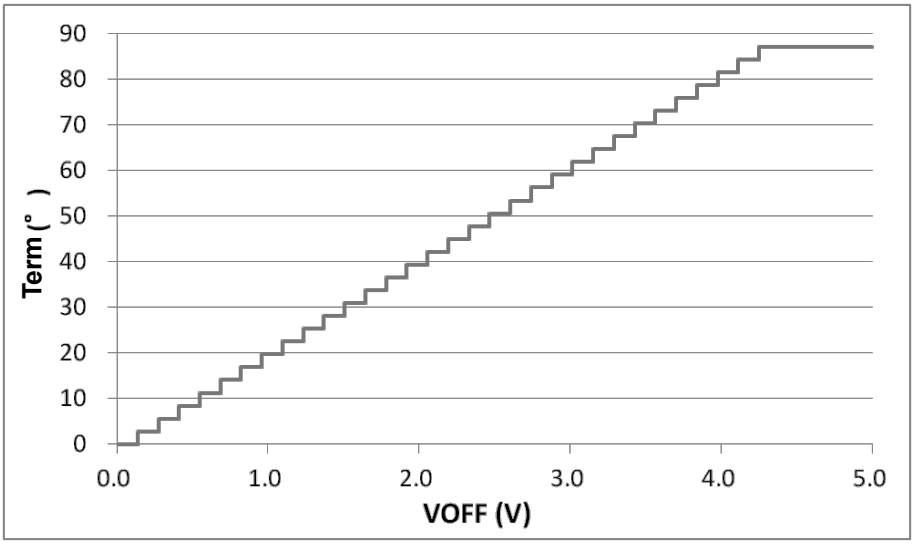


<PWM change during soft switching>

Soft switching after conducting phase switch:

It changes gradually from 4% to 100% of output PWM duty determined by the voltage of VSP pin. Its number of steps is 16 in maximum.

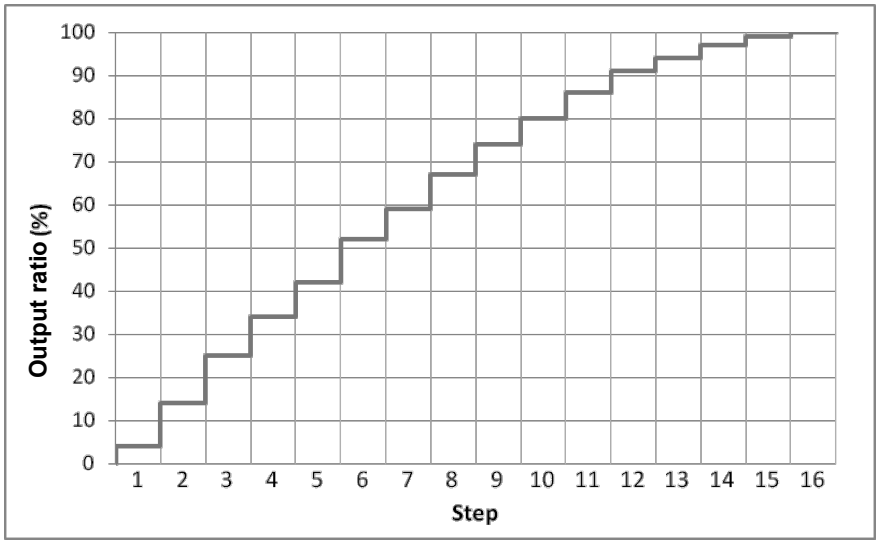
Soft switching before conducting phase switch:

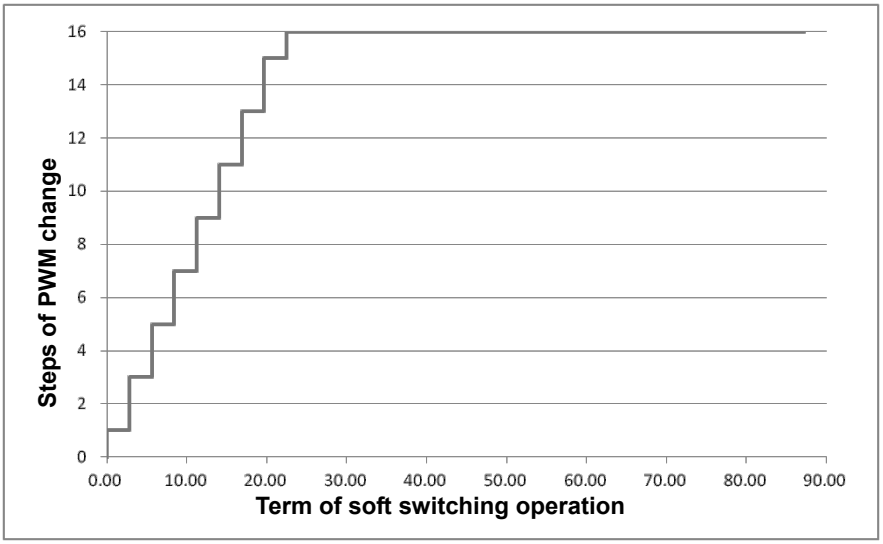
It changes gradually from 100% to 4% of output PWM duty determined by the voltage of VSP pin. Its number of steps is 16 in maximum.

In case the term of soft switching operation is 22.5° or less, number of steps is less than16 in the soft switching term.

The relation of steps of soft switching and the output PWM duty ratio is shown below.

Step	Output ratio (%)	Step	Output ratio (%)	Step	Output ratio (%)
1	4	7	59	13	94
2	14	8	67	14	97
3	25	9	74	15	99
4	34	10	80	16	100
5	42	11	86		
6	52	12	91		





9. Lead Angle

Lead angle of the conducting signal can be set in the range of 0 to 22.5° against the hall signal.

Lead angle is set by analog input of LA pin (The range of 0 to V_{ADC} is divided into 32 steps and lower 17 steps are used.)

LA = 0V → Lead angle 0°

LA = V_{ADC} → Lead angle 22.5° (In case of inputting the voltage of V_{ADC} or more.)

Step	LA (V)	Lead angle (°)	Step	LA (V)	Lead angle (°)	Step	LA (V)	Lead angle (°)
0	0.00	0.0	6	0.82	8.4	12	1.65	16.9
1	0.14	1.4	7	0.96	9.8	13	1.78	18.3
2	0.27	2.8	8	1.10	11.3	14	1.92	19.7
3	0.41	4.2	9	1.23	12.7	15	2.06	21.1
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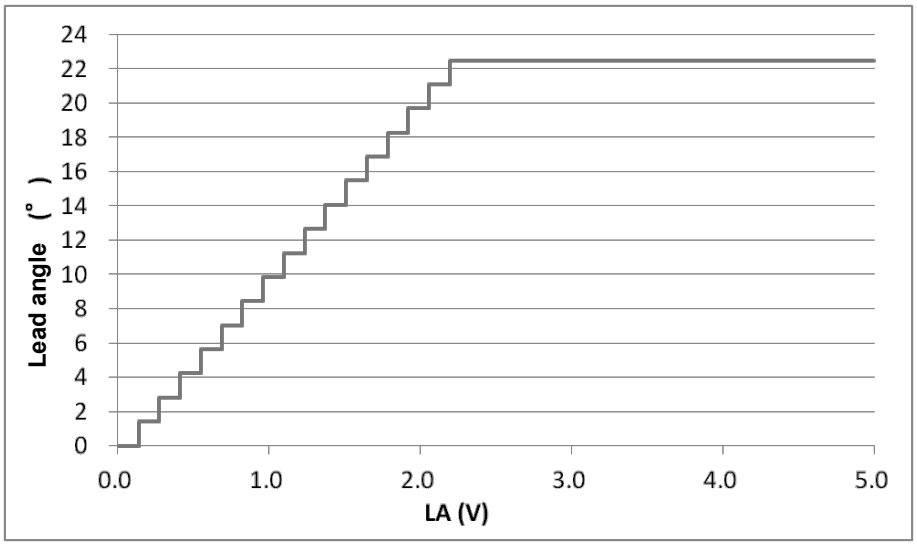
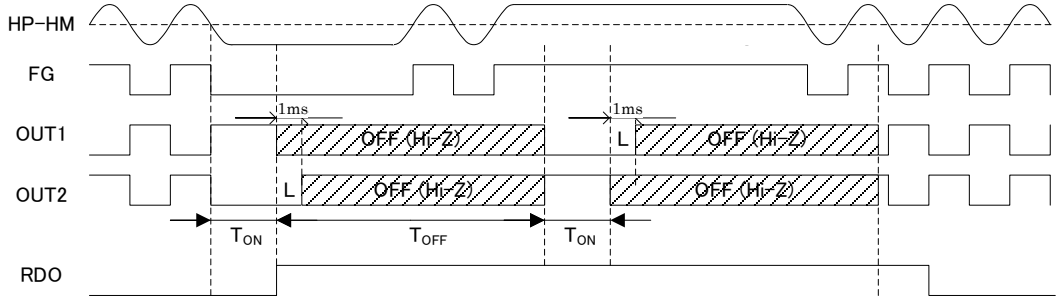


10. Lock protection

It monitors the motor rotation by the hall signal and operates when the zero cross of the hall signal can not be detected for certain time (T_{ON}) or more. When lock protection operates, the upper output transistor is turned off for 1ms(typ) and then all output power transistors are turned off. The motor drive resumes certain time (T_{OFF}) after the lock protection operates.

T_{ON} = 0.4s (typ)
T_{OFF} = 4s (typ)

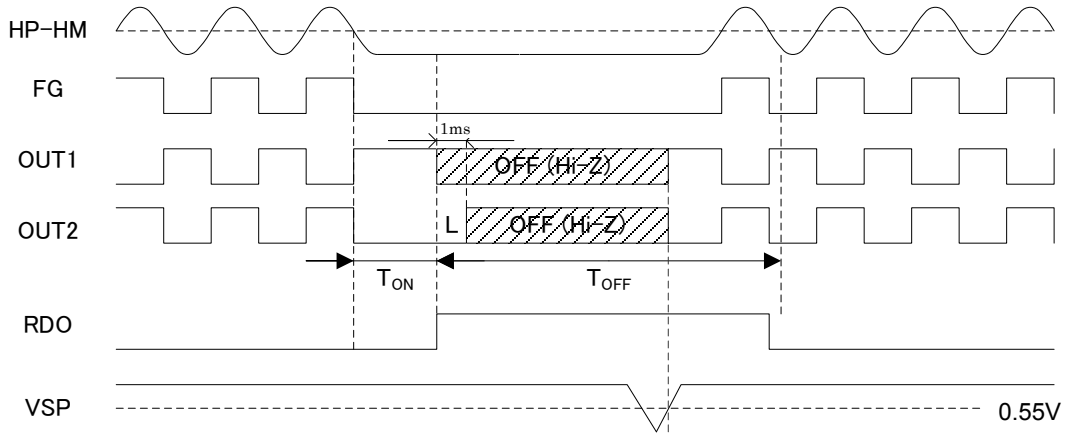


FG is outputted by the hall signal even while the lock protection is operating.

In case the zero cross of the hall signal is detected twice in re-startup, the lock protection is cleared and the RDO signal outputs low again.

11. Quick Start

During T_{OFF} of lock protection, lock protection is cleared when the voltage of VSP pin is set to $V_{AD(L)}$ or less. When $V_{AD(L)}$ or more is applied to the VSP pin again, the motor restarts operating quickly without waiting for the end of the T_{OFF} term.



Because the voltage of VSP pin is detected through A/D circuit, the voltage of VSP pin should be kept at $V_{AD(L)}$ or less for VSP response time (T_{VSP}) or more in order to clear the lock protection.

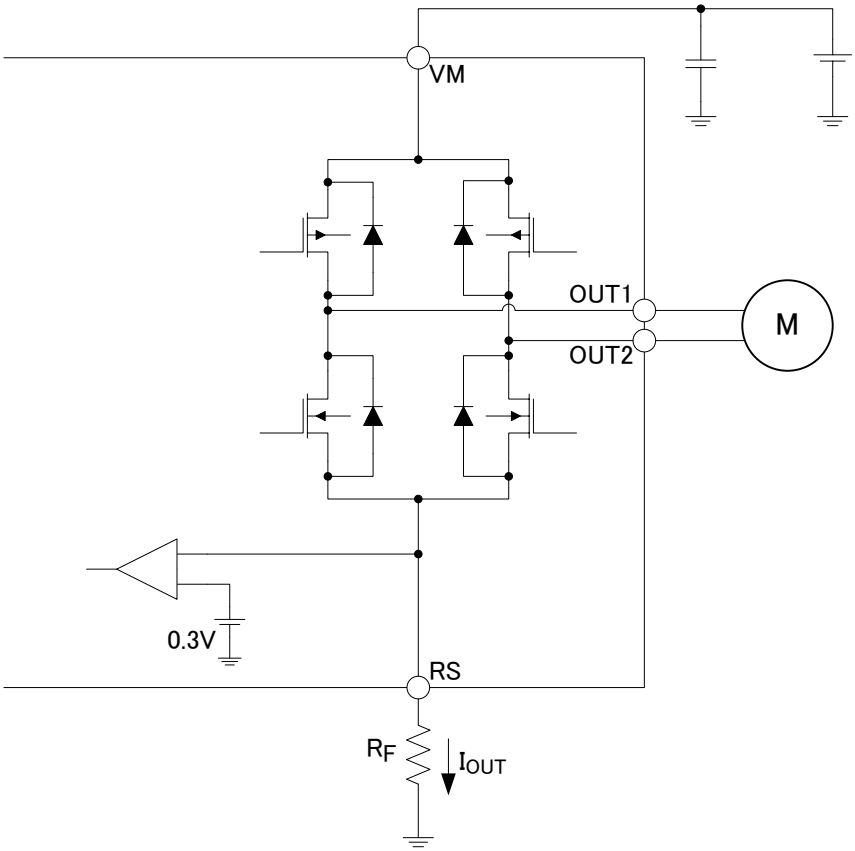
Quick start is disabled when the minimum of the duty is configured by applying the voltage of $V_{AD(L)}$ or more to VMI pin.

12. Current Limit

This function operates when the output voltage reaches the current limit detection voltage (V_{RS} = 0.3 V (typ)). It is detected by the resistor R_F.

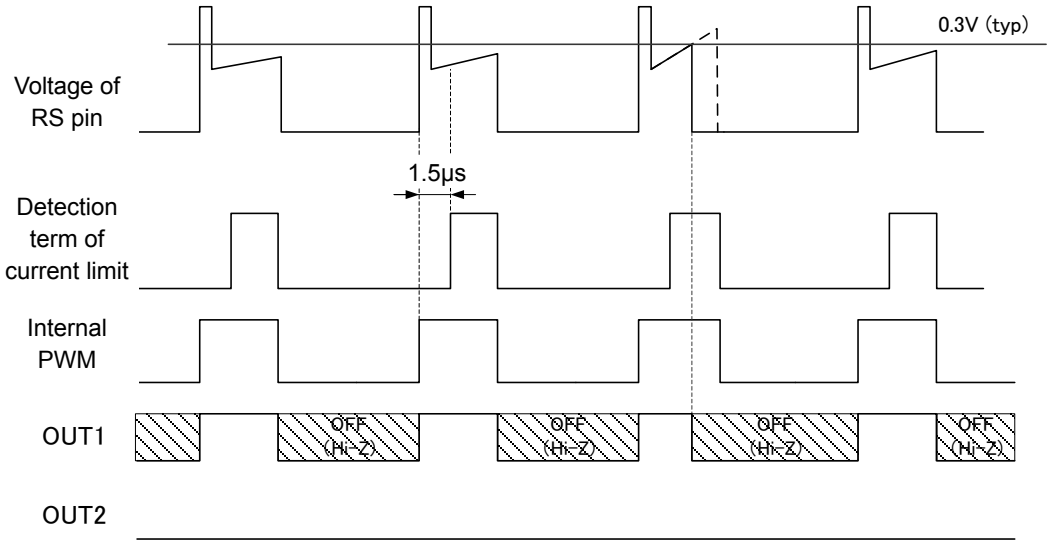
$$\text{Current value which over current protection operates } (I_{OUT}) = \frac{\text{Over current detection voltage } (V_{RS})}{\text{Detection resistance } (R_F)}$$

When R_F=0.51Ω, I_{OUT}=0.3V (typ)/0.51Ω=588mA



During the current limit operation, the operation mode is moved to PWM OFF state by turning off the upper output power transistor. The operation resumes at the next PWM ON timing.

Masking time is configured to avoid malfunction by noise.



(In case HP = L and HM = H)

13. Over Current Protection (ISD)

Detection of current of the output power transistor is incorporated.

Each current flowing through four power transistors is detected individually. When the current exceeds the detection value, the related output power transistor is turned off. Then all output power transistors are turned off 1ms(typ) after this related output power transistor is turned off.

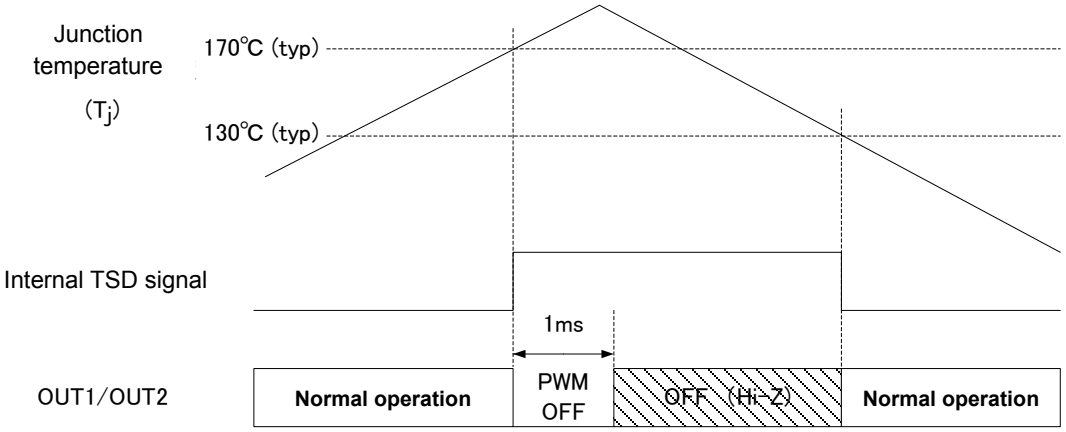
Timer is incorporated in this circuit. The motor operation resumes OFF time of 100ms (typ) after the over current is detected. When state of over current continues, over current protection operates repeatedly. In case this protection operates 8 times repeatedly, the motor operation does not resume automatically. The output power transistor keeps turned off. In order to clear this state, VSP or the power supply should be applied again.

Design target value of current limit for over current protection is 2.5A. Masking term of 2 μs (typ) is configured to avoid malfunction by noisy pulse current.

14. Thermal Shutdown Circuit (TSD)

Thermal shutdown circuit (TSD) operates when T_j rises to 170℃(typ) or more. All output power transistors are turned off after a 1ms(typ) PWM OFF term during which upper output power transistor is turned off.

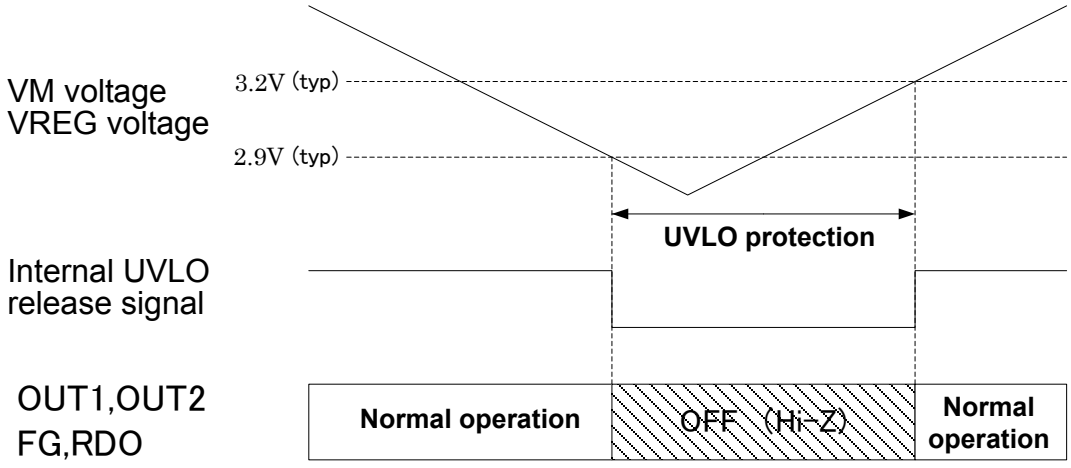
The operation resumes when the temperature falls to 130℃(typ) or less.



15. Under Voltage Lockout Protection (UVLO)

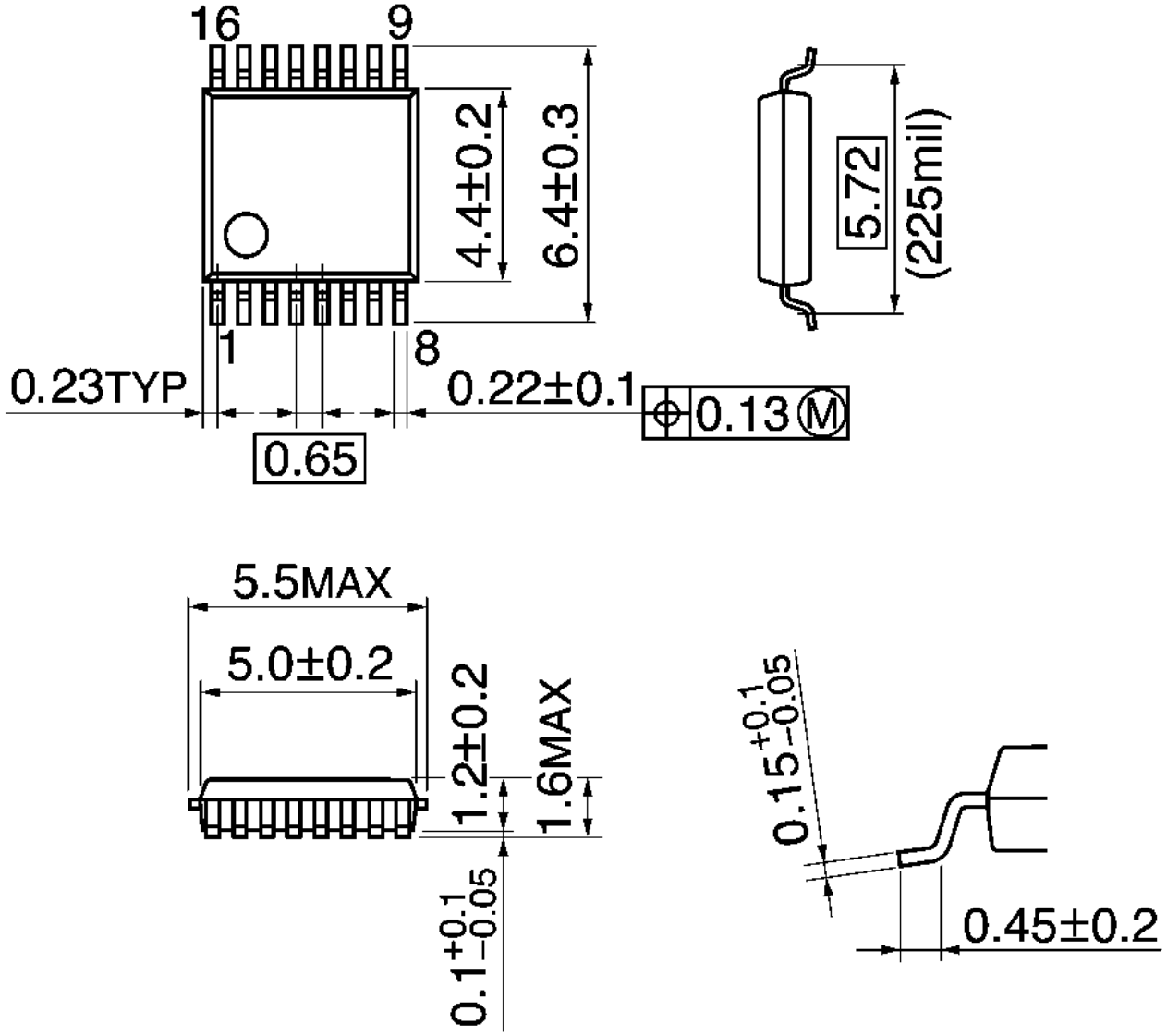
This IC has an under voltage lockout protection (UVLO).

The power supply voltage of VM and the voltage of VREG are monitored. When each of them falls to 2.9 V (typ) or less, it is recognized as low voltage and the circuit is turned off. The normal operation resumes when both voltage recovers to 3.2V (typ) or more.



Package Dimensions

SSOP16-P-225-0.65B Unit: mm



Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.

Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.

Make sure that the positive and negative terminals of power supplies are connected properly.

Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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