Wideband Dual-Channel Linear Multiplier/Divider

AD539

FEATURES

2-quadrant multiplication/division
2 independent signal channels
Signal bandwidth of 60 MHz (I_{OUT})
Linear control channel bandwidth of 5 MHz
Low distortion (to 0.01%)
Fully calibrated, monolithic circuit

APPLICATIONS

Precise high bandwidth AGC and VCA systems
Voltage-controlled filters
Video signal processing
High speed analog division
Automatic signal-leveling
Square-law gain/loss control

FUNCTIONAL BLOCK DIAGRAM

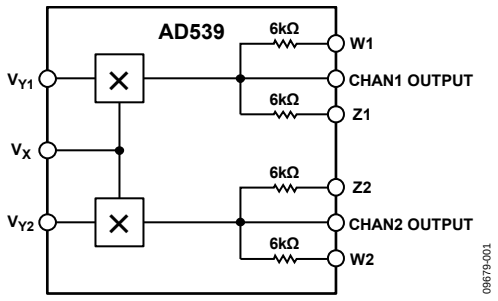

Figure 1.

GENERAL DESCRIPTION

The AD539 is a low distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X input providing linear control of gain. Excellent ac characteristics up to video frequencies and a −3 dB bandwidth of over 60 MHz are provided. Although intended primarily for applications where speed is important, the circuit exhibits good static accuracy in computational applications. Scaling is accurately determined by a band-gap voltage reference and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100 Ω. Output voltage is restricted to a few hundred millivolts under these conditions.

The two channels provide flexibility. In single-channel applications, they can be used in parallel to double the output current, in series to achieve a square-law gain function with a control range of over 100 dB, or differentially to reduce distortion. Alternatively, they can be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the state-variable approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15 MHz.

Power consumption is only 135 mW using the recommended ±5 V supplies. The AD539 is available in three versions: the J and K grades are specified for 0 to 70°C operation and S grade is guaranteed over the extended range of −55°C to +125°C. The J and K grades are available in either a hermetic ceramic SBDIP (D-16) or a low cost PDIP (N-16), whereas the S grade is available in ceramic SBDIP (D-16) or LCC (E-20-1). The S grade is available in MIL-STD-883 and Standard Military Drawing (DESC) Number 5962-8980901EA versions.

Rev. B

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TABLE OF CONTENTS

REVISION HISTORY

4/11—Rev. A to Rev. B

Updated Format ... Universal
Changed Pin Configuration to Functional Block Diagram ... 1
Changes to General Description Section ... 1
Added Pin Configurations and Function Descriptions Section ... 5
Added Table 2; Renumbered Sequentially ... 5
Added Table 3 ... 6
Added Typical Performance Characteristics Section ... 7
Added Figure 6 and Figure 9; Renumbered Sequentially ... 7
Changes to Figure 18 ... 10
Moved Dual Signal Channels Section, Common Control Channel Section, and Flexible Scaling Section ... 11
Changes to Figure 20 ... 12
Changes to Table 4, Figure 21, and Table 5 ... 13
Changes to Figure 22 and Figure 23 ... 14
Changes to Figure 24 ... 15
Changes to Figure 25 ... 16
Updated Outline Dimensions ... 17
Changes to Ordering Guide ... 18

12/91—Rev. 0 to Rev. A

SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, unless otherwise specified. $V_Y = V_{Y1} - V_{Y2}$, $V_X = V_{X1} - V_{X2}$. All minimum and maximum specifications are guaranteed.

Table 1.

		AD539J			AD539K			AD539S			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL CHANNEL DYNAMICS											
Minimal Configuration	See Figure 22										
Bandwidth, −3 dB	R_L = 50 Ω, C_C = 0.01 µF	30	60		30	60		30	60		MHz
Maximum Output	0.1 V < V_X < 3 V, V_Y ac = 1 V rms		−10			−10			−10		dBm
Feedthrough	V_X = 0 V, V_Y ac = 1.5 V rms										
f < 1 MHz			−75			−75			−75		dBm
f = 20 MHz			−55			−55			−55		dBm
Differential Phase Linearity											
−1 V < V_Y dc < +1 V	f = 3.58 MHz, V_X = 3 V, V_Y ac = 100 mV		±0.2			±0.2			±0.2		Degrees
−2 V < V_Y dc < +2 V	f = 3.58 MHz, V_X = 3 V, V_Y ac = 100 mV		±0.5			±0.5			±0.5		Degrees
Group Delay	V_X = 3 V, V_Y ac = 1 V rms, f = 1 MHz		4			4			4		ns
Standard 2-Channel Multiplier	See Figure 20										
Maximum Output	V_X = 3 V, V_Y ac = 1.5 V rms		4.5			4.5			4.5		V
Feedthrough, f < 100 kHz	V_X = 0 V, V_Y ac = 1.5 V rms		1			1			1		mV rms
Crosstalk (Channel 1 to Channel 2)	V_{Y1} = 1 V rms, V_{Y2} = 0 V, V_X = 3 V, f < 100 kHz		−40			−40			−40		dB
RTO Noise, 10 Hz to 1 MHz	V_X = 1.5 V, V_Y = 0 V		200			200			200		nV/√Hz
THD + Noise											
V_X = 1 V	f = 10 kHz, V_Y ac = 1 V rms		0.02			0.02			0.02		%
V_Y = 3 V	f = 10 kHz, V_Y ac = 1 V rms		0.04			0.04			0.04		%
Wideband 2-Channel Multiplier	See Figure 20										
Bandwidth, −3 dB (LH0032)	0.1 V < V_X < 3 V, V_Y ac = 1 V rms		25			25			25		MHz
Maximum Output V_X = 3 V	V_Y ac = 1.5 V rms, f = 3 MHz		4.5			4.5			4.5		V rms
Feedthrough V_X = 0 V	V_Y ac = 1.0 V rms, f = 3 MHz		14			14			14		mV rms
Wideband Single-Channel VCA	See Figure 24										
Bandwidth, −3 dB	0.1 V < V_X < 3 V, V_Y ac = 1 V rms		50			50			50		MHz
Maximum Output	75 Ω load		±1			±1			±1		V
Feedthrough	V_X = −0.01 V, f = 5 MHz		−54			−54			−54		dB
CONTROL CHANNEL DYNAMICS											
Bandwidth, −3 dB	C_C = 3000 pF, V_X dc = 1.5 V, V_X ac = 100 mV rms		5			5			5		MHz
SIGNAL INPUTS, V_{Y1} AND V_{Y2}											
Nominal Full-Scale Input			±2			±2			±2		V
Operational Range, Degraded Performance	$-V_S \le 7$ V	±4.2[1]			±4.2[1]			±4.2[1]			V
Input Resistance			400			400			400		kΩ
Bias Current			10	30[1]		10	20[1]		10	30[1]	µA
Offset Voltage	V_X = 3 V, V_Y = 0 V		5	20[1]		5	10[1]		5	20[1]	mV
T_{MIN} to T_{MAX}			10			5			15	35	mV
Power Supply Sensitivity	V_X = 3 V, V_Y = 0 V		2			2			2		mV/V

Parameter	Test Conditions/Comments	AD539J			AD539K			AD539S			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CONTROL INPUT, V_X											
Nominal Full-Scale Input			3.0			3.0			3.0		V
Operational Range, Degraded Performance		+3.2			+3.2			+3.2			V
Input Resistance[2]			500			500			500		Ω
Offset Voltage			1	4[1]		1	2[1]		1	4[1]	mV
T_{MIN} to T_{MAX}			3			2			2	5[1]	mV
Power Supply Sensitivity			30			30			30		μV/V
Gain	See Figure 20										
Absolute Gain Error	V_X = 0.1 V to 3.0 V, V_Y = ±2 V		0.2	0.4[1]		0.1	0.2[1]		0.2	0.4[1]	dB
T_{MIN} to T_{MAX}	V_X = 0.1 V to 3.0 V, V_Y = ±2 V		0.3			0.15			0.25	0.5[1]	dB
CURRENT OUTPUT[2]											
Full-Scale Output Current	V_X = 3 V, V_Y = ±2 V		±1			±1			±1		mA
Peak Output Current	V_X = 3.3 V, V_Y = ±5 V, V_S = ±7.5 V	±2	±2.8		±2	±2.8		±2	±2.8		mA
Output Offset Current	V_X = 0 V, V_Y = 0 V		0.2	1.5[1]		0.2	1.5[1]		0.2	1.5[1]	μA
Output Offset Voltage[3]	See Figure 20, V_X = 0 V, V_Y = 0 V		3	10[1]		3	10[1]		3	10[1]	mV
Output Resistance			1.2			1.2			1.2		kΩ
Scaling Resistors											
Channel 1	Z1, W1 to CH1		6			6			6		kΩ
Channel 2	Z2, W2 to CH2		6			6			6		kΩ
VOLTAGE OUTPUTS, V_{W1} AND V_{W2}[3]	See Figure 20										
Multiplier Transfer Function											
Either Channel			$V_W = -V_X \times V_Y/V_U$			$V_W = -V_X \times V_Y/V_U$			$V_W = -V_X \times V_Y/V_U$		
Multiplier Scaling Voltage, V_U		0.98[1]	1.0	1.02[1]	0.99[1]	1.0	1.01[1]	0.98[1]	1.0	1.02[1]	V
Accuracy			0.5	2[1]		0.5	1[1]		0.5	2	%
T_{MIN} to T_{MAX}			1			0.5			1.0	3[1]	%
Power Supply Sensitivity			0.04			0.04			0.04		%/V
Total Multiplication Error[4]	$V_X \le 3$ V, −2 V < V_Y < +2 V		1	2.5		0.6	1.5		1	2.5	% FSR
T_{MIN} to T_{MAX}			2			1			2	4[1]	%
Control Feedthrough	V_X = 0 V to 3 V, V_Y = 0 V		25	60[1]		15	30[1]		15	60[1]	mV
T_{MIN} to T_{MAX}			30			15			60	120[1]	mV
TEMPERATURE RANGE											
Rated Performance		0		+70	0		+70	−55		+125	°C
POWER SUPPLIES											
Operational Range		±4.5		±15	±4.5		±15	±4.5		±15	V
Current Consumption											
$+V_S$			8.5	10.2[1]		8.5	10.2[1]		8.5	10.2[1]	mA
$-V_S$			18.5	22.2[1]		18.5	22.2[1]		18.5	22.2[1]	mA

[1] Tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
[2] Resistance value and absolute current outputs subject to 20% tolerance.
[3] Specification assumes the external op amp is trimmed for negligible input offset.
[4] Includes all errors.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

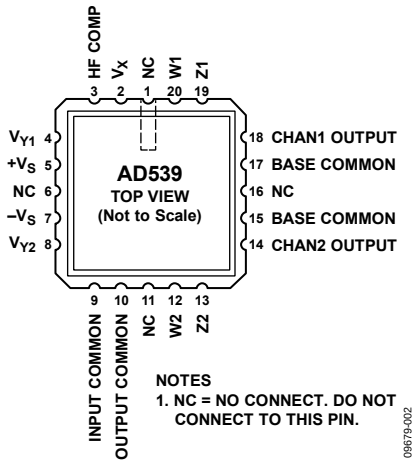


Figure 2. 20-Lead LLC Pin Configuration (E-20-1)

Table 2. 20-Lead LLC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. Do not connect to this pin.
2	V_X	Control Channel Input.
3	HF COMP	High Frequency Compensation.
4	V_{Y1}	Channel 1 Input.
5	$+V_S$	Positive Supply Rail.
6	NC	No Connect. Do not connect to this pin.
7	$–V_S$	Negative Supply Rail.
8	V_{Y2}	Channel 2 Input.
9	INPUT COMMON	Internal Common Connection for the Input Amplifier Circuitry.
10	OUTPUT COMMON	Internal Common Connection for the Output Amplifier Circuitry.
11	NC	No Connect.
12	W2	6 kΩ Feedback Resistor for Channel 2.
13	Z2	6 kΩ Feedback Resistor for Channel 2.
14	CHAN2 OUTPUT	Channel 2 Product of V_X and V_{Y2}.
15	BASE COMMON	Increases Negative Output Compliance.
16	NC	No Connect. Do not connect to this pin.
17	BASE COMMON	Increases Negative Output Compliance.
18	CHAN1 OUTPUT	Channel 1 Product of V_X and V_{Y1}.
19	Z1	6 kΩ Feedback Resistor for Channel 1.
20	W1	6 kΩ Feedback Resistor for Channel 1.

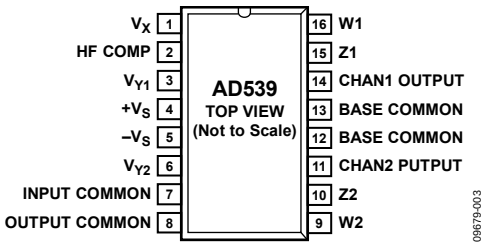


Figure 3. 16-Lead PDIP and SBDIP Pin Configurations (N-16, D-16)

Table 3. 16-Lead PDIP and SBDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_X	Control Channel Input.
2	HF COMP	High Frequency Compensation.
3	V_{Y1}	Channel 1 Input.
4	$+V_S$	Positive Supply Rail.
5	$-V_S$	Negative Supply Rail.
6	V_{Y2}	Channel 2 Input.
7	INPUT COMMON	Internal Common Connection for the Input Amplifier Circuitry.
8	OUTPUT COMMON	Internal Common Connection for The Output Amplifier Circuitry.
9	W2	6 kΩ Feedback Resistor for Channel 2.
10	Z2	6 kΩ Feedback Resistor for Channel 2.
11	CHAN2 OUTPUT	Channel 2 Product of V_X and V_{Y2}.
12	BASE COMMON	Increases Negative Output Compliance.
13	BASE COMMON	Increases Negative Output Compliance.
14	CHAN1 OUTPUT	Channel 1 Product of V_X and V_{Y1}.
15	Z1	6 kΩ Feedback Resistor for Channel 1.
16	W1	6 kΩ Feedback Resistor for Channel 1.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_Y = V_{Y1} - V_{Y2}$, $V_X = V_{X1} - V_{X2}$, unless otherwise noted.

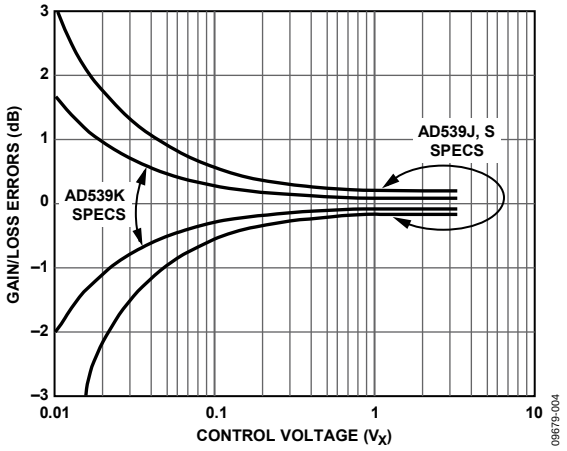


Figure 4. Maximum AC Gain Error Boundaries

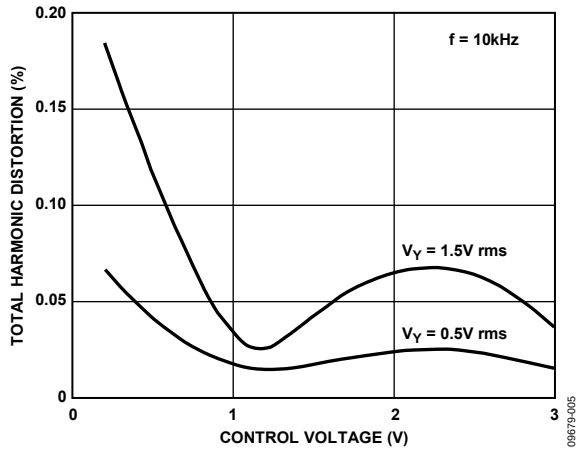


Figure 5. Total Harmonic Distortion vs. Control Voltage

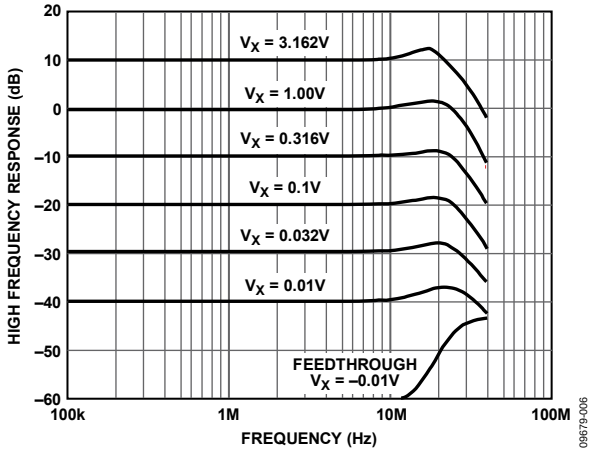


Figure 6. Multiplier High Frequency Response Using LH0032 Op Amps

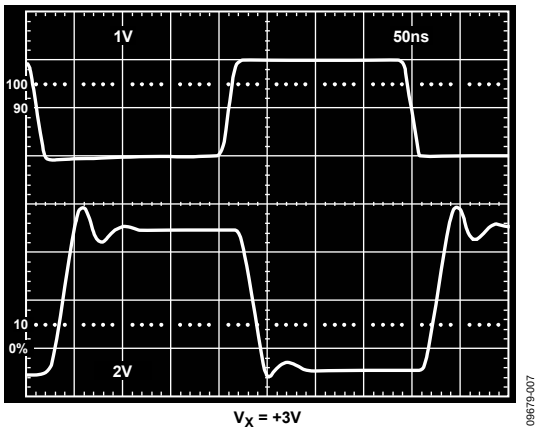


Figure 7. Multiplier Pulse Response Using LH0032 Op Amp, V_X = 3 V

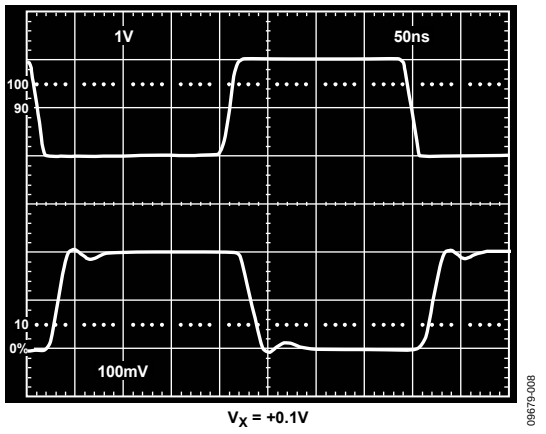


Figure 8. Multiplier Pulse Response Using LH0032 Op Amp, V_X = 0.1 V

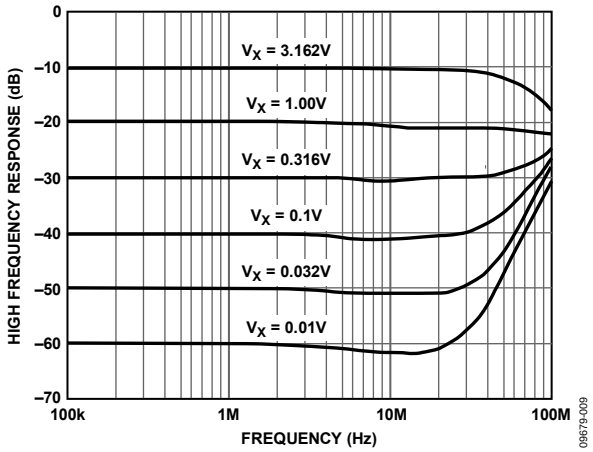


Figure 9. High Frequency Response in Minimal Configuration

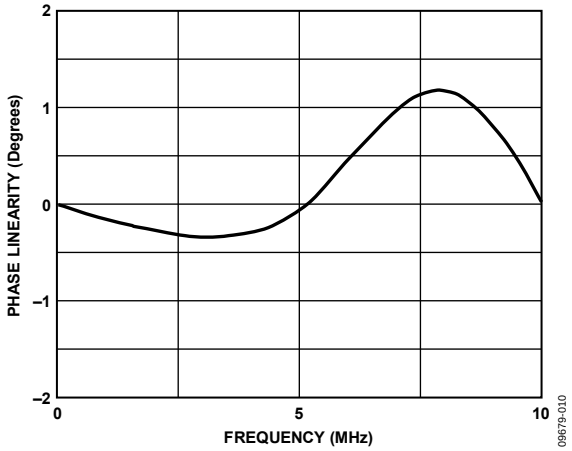


Figure 10. Phase Linearity Error in Minimal Configuration

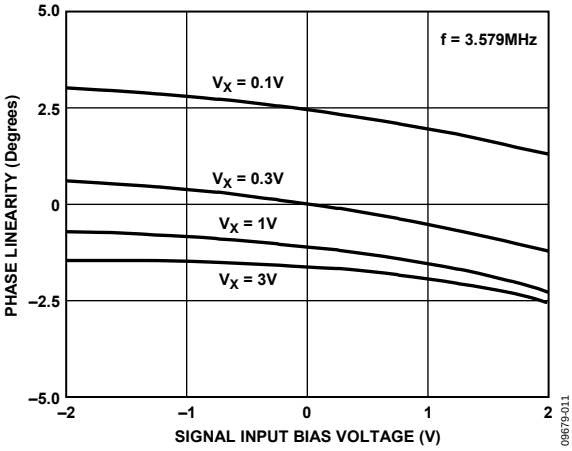


Figure 11. Differential Phase Linearity in Minimal Configuration for a Typical Device

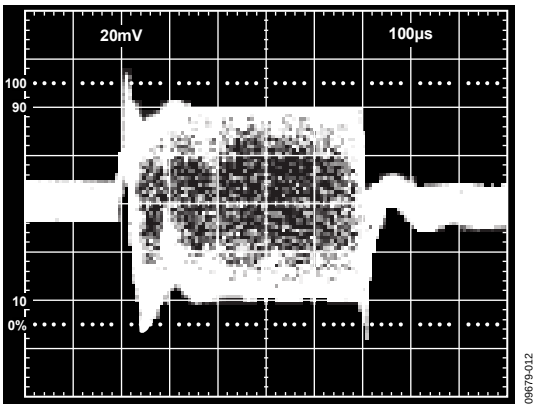


Figure 12. Control Feedthrough One Channel of Figure 22

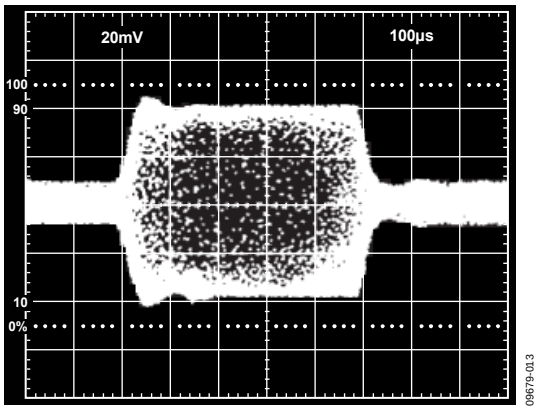


Figure 13. Control Feedthrough Differential Mode of Figure 22

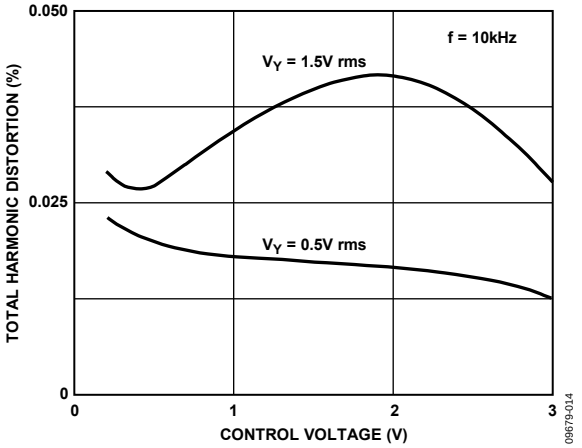


Figure 14. Distortion in Differential Mode Using LH0032 Op Amp

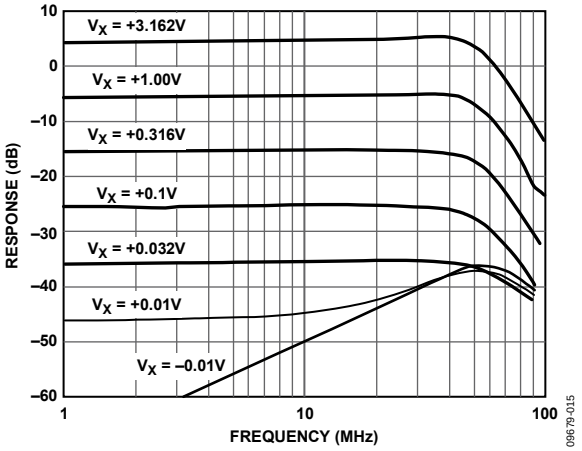


Figure 15. AC Response of the VCA at Different Gains, V_Y = 0.5 V RMS

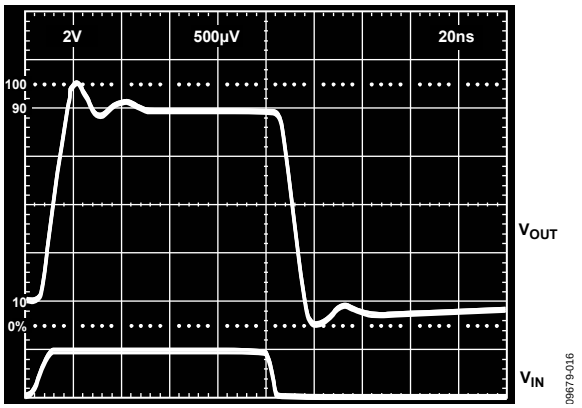


Figure 16. Transient Response of the Voltage-Controlled Amplifier, $V_X = +2$ V, $V_Y = \pm 1$ V

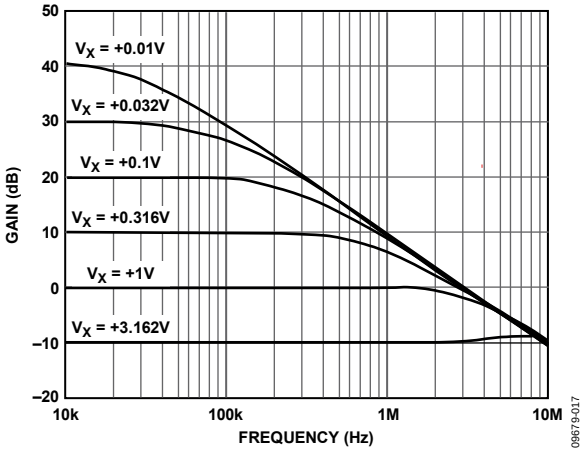


Figure 17. High Frequency Response of Divider in Figure 25

THEORY OF OPERATION

CIRCUIT DESCRIPTION

Figure 18 shows a simplified schematic of the AD539. Q1 to Q6 are large-geometry transistors designed for low distortion and low noise. Emitter-area scaling further reduces distortion: Q1 is three times larger than Q2; Q4 and Q5 are each three times larger than Q3 and Q6 and are twice as large as Q1 and Q2. A stable reference current of I_{REF} = 1.375 mA is produced by a band gap reference circuit and applied to the common emitter node of a controlled cascode formed by Q1 and Q2. When V_X = 0 V, all of I_{REF} flows in Q1 due to the action of the high gain control amplifier, which lowers the voltage on the base of Q2. As V_X is raised, the fraction of I_{REF} flowing in Q2 is forced to balance the control current, V_X/2.5 kΩ. At the full-scale value of V_X (3 V) this fraction is 0.873. Because the base of Q1, Q4, and Q5 are at ground potential and the bases of Q2, Q3, and Q6 are commoned, all three controlled cascodes divide the current applied to their emitter nodes in the same proportion. The control loop is stabilized by the external capacitor, C_C.

The signal voltages, V_{Y1} and V_{Y2} (generically referred to as V_Y), are first converted to currents by voltage-to-current converters with a g_m of 575 µmhos. Thus, the full-scale input of ±2 V becomes a current of ±1.15 mA, which is superimposed on a bias of 2.75 mA and applied to the common emitter node of controlled cascode Q3/Q4 or Q5/Q6. As previously explained, the proportion of this current steered to the output node is linearly dependent on V_X. Therefore, for full-scale V_X and V_Y inputs, a signal of ±1 mA (0.873 × ±1.15 mA) and a bias component of 2.4 mA (0.873 × 2.75 mA) appear at the output. The bias component absorbed by the 1.25 kΩ resistors also connected to V_X and the resulting signal current can be applied to an external load resistor (in which case scaling is not accurate) or can be forced into either or both of the 6 kΩ feedback resistors (to the Z and W nodes) by an external op amp. In the latter case, scaling accuracy is guaranteed.

GENERAL RECOMMENDATIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high quality ground plane should be used with the device either soldered directly into the board or mounted in a low profile socket. In Figure 18, an open triangle denotes a direct, short connection to this ground plane; the BASE COMMON pins (Pin 12 and Pin 13) are especially prone to unwanted signal pickup. Power supply decoupling capacitors of 0.1 µF to 1 µF should be connected from the $+V_S$ and $-V_S$ pins (Pin 4 and Pin 5) to the ground plane. In applications using external high speed op amps, use separate supply decoupling. It is good practice to insert small (10 Ω) resistors between the primary supply and the decoupling capacitor.

The control amplifier compensation capacitor, C_C, should likewise have short leads to ground and a minimum value of 3 nF. Unless maximum control bandwidth is essential, it is advisable to use a larger value of 0.01 µF to 0.1 µF to improve the signal channel phase response, high frequency crosstalk, and high frequency distortion. The control bandwidth is inversely proportional to this capacitance, typically 2 MHz for C_C = 0.01 µF, V_X = 1.7 V. The bandwidth and pulse response of the control channel can be improved by using a feedforward capacitor of 5% to 20% the value of C_C between the V_X and HF COMP pins (Pin 1 and Pin 2). Optimum transient response results when the rise/fall time of V_X are commensurate with the control channel response time.

V_X should not exceed the specified range of 0 V to 3 V. The ac gain is zero for V_X < 0 V but there remains a feedforward path (see Figure 18) causing control feedthrough. Recovery time from negative values of V_X can be improved by adding a small signal Schottky diode with its cathode connected to HF COMP (Pin 2) and its anode grounded. This constrains the voltage swing on C_C. Above V_X = 3.2 V, the ac gain limits at its maximum value, but any overdrive appears as control feedthrough at the output.

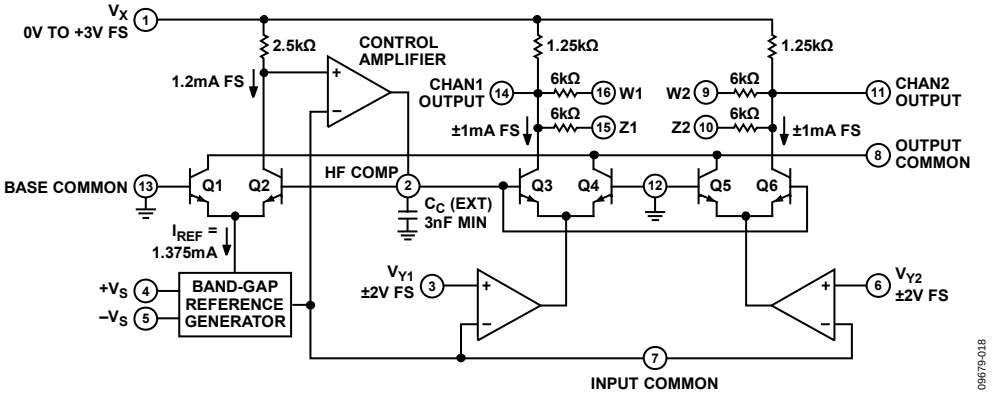


Figure 18. Simplified Schematic of AD539 Multiplier (16-Lead SBDIP and PDIP Shown)

The power supplies to the AD539 can be as low as ±4.5 V and as high as ±16.5 V. The maximum allowable range of the signal inputs, V_Y, is approximately 0.5 V above $+V_S$; the minimum value is 2.5 V above $-V_S$. To accommodate the peak specified inputs of ±4.2 V the supplies should be nominally +5 V and −7.5 V. Although there is no performance advantage in raising supplies above these values, it may often be convenient to use the same supplies as for the op amps. The AD539 can tolerate the excess voltage with only a slight effect on dc accuracy but dissipation at ±16.5 V can be as high as 535 mW, and some form of heat sink is essential in the interests of reliability.

TRANSFER FUNCTION

In using any analog multiplier or divider, careful attention must be paid to the matter of scaling, particularly in computational applications. To be dimensionally consistent, a scaling voltage must appear in the transfer function, which, for each channel of the AD539 in the standard multiplier configuration (see Figure 20), is

$$V_W = -V_X V_Y / V_U$$

where the V_X and V_Y inputs, the V_W output, and the scaling voltage, V_U, are expressed in a consistent unit, usually volts. In this case, V_U is fixed by the design to be 1 V and it is often acceptable in the interest of simplification to use the less rigorous expression

$$V_W = -V_X V_Y$$

where it is understood that all signals must be expressed in volts, that is, they are rendered dimensionless by division by 1 V.

The accuracy specifications for V_U allow the use of either of the two feedback resistors supplied with each channel, because these are very closely matched, or they can be used in parallel to halve the gain (double the effective scaling voltage), when

$$V_W = -V_X V_Y / 2$$

When an external load resistor, R_L, is used, the scaling is no longer exact because the internal thin film resistors, although trimmed to high ratiometric accuracy, have an absolute tolerance of 20%. However, the nominal transfer function is

$$V_W = -V_X V_Y / V_U'$$

where the effective scaling voltage, V_U', can be calculated for each channel using the formula

$$V_U' = V_U (5R_L + 6.25)/R_L$$

where R_L is expressed in kilohms. For example, when R_L = 100 Ω, V_U' = 67.5 V. Table 5 provides more detailed data for the case where both channels are used in parallel. The AD539 can also be used with no external load (CHAN2 OUTPUT, Pin 11, or CHAN1 OUTPUT, Pin 14, open circuit), when VU' is precisely 5 V.

DUAL SIGNAL CHANNELS

The signal voltage inputs, V_{Y1} and V_{Y2}, have nominal full-scale (FS) values of ±2 V with a peak range to ±4.2 V (using a negative supply of 7.5 V or greater). For video applications where differential phase is critical, a reduced input range of ±1 V is recommended, resulting in a phase variation of typically ±0.2° at 3.579 MHz for full gain. The input impedance is typically 400 kΩ shunted by 3 pF. Signal channel distortion is typically well under 0.1% at 10 kHz and can be reduced to 0.01% by using the channels differentially.

COMMON CONTROL CHANNEL

The control channel accepts positive inputs, V_X, from 0 V to 3 V FS, ±3.3 V peak. The input resistance is 500 Ω. An external, grounded capacitor determines the small-signal bandwidth and recovery time of the control amplifier; the minimum value of 3 nF allows a bandwidth at midgain of about 5 MHz. Larger compensation capacitors slow the control channel but improve the high frequency performance of the signal channels.

FLEXIBLE SCALING

Using either one or two external op amps in conjunction with the on-chip 6 kΩ scaling resistors (see Figure 19), the output currents (nominally ±1 mA FS, ±2.25 mA peak) can be converted to voltages with accurate transfer functions of $V_W = -V_X V_Y/2$, $V_W = -V_X V_Y$, or $V_W = -2V_X V_Y$ (where the V_X and V_Y inputs and V_W output are expressed in volts), with corresponding full-scale outputs of ±3 V, ±6 V, and ±12 V. Alternatively, low impedance grounded loads can be used to achieve the full signal bandwidth of 60 MHz, in which mode the scaling is less accurate.

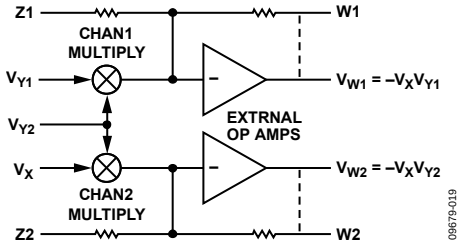


Figure 19. Block Diagram Showing Scaling Resistors and External Op Amps

APPLICATIONS INFORMATION

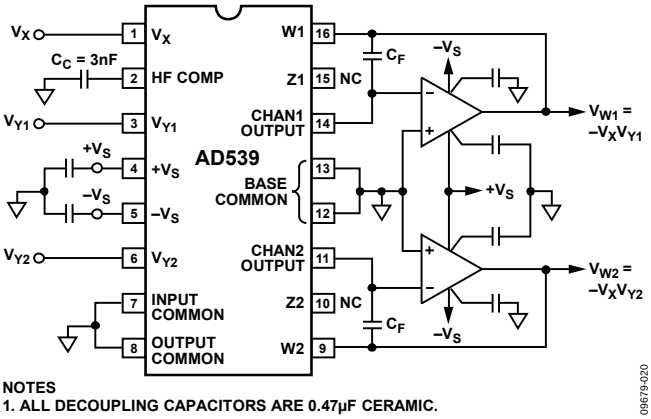
BASIC MULTIPLIER CONNECTIONS

Figure 20 shows the connections for the standard dual-channel multiplier, using op amps to provide useful output power and the AD539 feedback resistors to achieve accurate scaling. The transfer function for each channel is

$$V_W = -V_X V_Y$$

where the inputs and outputs are expressed in volts (see the Transfer Function section).

At the nominal full-scale inputs of V_X = 3 V and V_Y = ±2 V, the full-scale outputs are ±6 V. Depending on the choice of op amp, their supply voltages may need to be about 2 V more than the peak output. Thus, supplies of at least ±8 V are required; the AD539 can share these supplies. Higher outputs are possible if V_X and V_Y are driven to their peak values of +3.2 V and ±4.2 V, respectively, when the peak output is ±13.4 V. This requires operating the op amps at supplies of ±15 V. Under these conditions, it is advisable to reduce the supplies to the AD539 to ±7.5 V to limit its power dissipation; however, with some form of heat-sinking, it is permissible to operate the AD539 directly from ±15 V supplies.



NOTES
1. ALL DECOUPLING CAPACITORS ARE 0.47µF CERAMIC.

Figure 20. Standard Dual-Channel Multiplier (16-Lead SBDIP and PDIP Shown)

Viewed as a voltage-controlled amplifier, the decibel gain is simply

$$G = 20 \log V_X$$

where V_X is expressed in volts. This results in a gain of 10 dB at V_X = 3.162 V, 0 dB at V_X = 1 V, −20 dB at V_X = 0.1 V, and so on. In many ac applications, the output offset voltage (for V_X = 0 V or V_Y = 0 V) is not a major concern; however, it can be eliminated using the offset nulling method recommended for the particular op amp, with V_X = V_Y = 0 V.

At small values of V_X, the offset voltage of the control channel degrades the gain/loss accuracy. For example, a ±1 mV offset uncertainty causes the nominal 40 dB attenuation at V_X = 0.01 V to range from 39.2 dB to 40.9 dB. Figure 4 shows the maximum gain error boundaries based on the guaranteed control channel offset voltages of ±2 mV for the AD539K and ±4 mV for the AD539J. These curves include all scaling errors and apply to all configurations using the internal feedback resistors (W1 and W2 or, alternatively, Z1 and Z2).

Distortion is a function of the signal input level (V_Y) and the control input (V_X). It is also a function of frequency, although in practice, the op amp generates most of the distortion at frequencies above 100 kHz. Figure 5 shows typical results at f = 10 kHz as a function of V_X with V_Y = 0.5 V rms and 1.5 V rms.

In some cases, it may be desirable to alter the scaling. This can be achieved in several ways. One option is to use both the Z and W feedback resistors (see Figure 18) in parallel, in which case $V_W = -V_X V_Y/2$. This may be preferable where the output swing must be held at ±3 V FS (±6.75 peak), for example, to allow the use of reduced supply voltages for the op amps. Alternatively, the gain can be doubled by connecting both channels in parallel and using only a single feedback resistor, in which case $V_W = -2V_X Y_Y$ and the full-scale output is ±12 V. Another option is to insert a resistor in series with the control channel input, permitting the use of a large (for example, 0 V to 10 V) control voltage. A disadvantage of this scheme is the need to adjust this resistor to accommodate the tolerance of the nominal 500 Ω input resistance at Pin 1, V_X. The signal channel inputs can also be resistively attenuated to permit operation at higher values of V_Y, in which case it may often be possible to partially compensate for the response roll-off of the op amp by adding a capacitor across the upper arm of this attenuator.

Signal Channel AC and Transient Response

The HF response is dependent almost entirely on the op amp. Note that the noise gain for the op amp in Figure 20 is determined by the value of the feedback resistor (6 kΩ) and the 1.25 kΩ control-bias resistors (see Figure 18). Op amps with provision for external frequency compensation should be compensated for a closed-loop gain of 6.

The layout of the circuit components is very important if low feedthrough and flat response at low values of V_X is to be maintained (see the General Recommendations section).

For wide bandwidth applications requiring an output voltage swing greater than ±1 V, the LH0032 hybrid op amp is recommended. Figure 6 shows the HF response of the circuit of Figure 20 using this amplifier with V_Y = 1 V rms and other conditions as shown in Table 4. C_F was adjusted for 1 dB peaking at V_X = 1 V; the −3 dB bandwidth exceeds 25 MHz. The effect of signal feedthrough on the response becomes apparent at V_X = 0.01 V. The minimum feedthrough results when V_X is taken slightly negative to ensure that the residual control channel offset is exceeded and the dc gain is reliably zero. Measurements show that the feedthrough can be held to −90 dB relative to full output at low frequencies and to −60 dB up to 20 MHz with careful board layout. The corresponding pulse response is shown in Figure 7 for a signal input of V_Y of ±1 V and two values of V_X (3 V and 0.1 V).

Table 4. Summary of Operating Conditions and Performance for the AD539 When Used with Various External Op Amp Output Amplifiers

Operating Conditions	AD711[1]	LH0032[1]
Op Amp Supply Voltages	±15 V	±10 V
Op Amp Compensation Capacitor	None	1 pF to 5 pF
Feedback Capacitor, C_F	None	1 pF to 4 pF
−3 dB Bandwidth, V_X = 1 V	900 kHz	25 MHz
Load Capacitance	<1 nF	<10 pF
HF Feedthrough		
V_X = −0.01 V, f = 5 MHz	N/A	−70 dB
RMS Output Noise		
V_X = 1 V, BW 10 Hz to10 kHz	50 µV	30 µV
V_X = 1 V, BW 10 Hz to 5 MHz	120 µV	500 µV

[1] For the circuit of Figure 20.

In all cases, 0.47 µF ceramic supply decoupling capacitors were used at each IC pin, the AD539 supplies were ±5 V, and the control compensation capacitor C_C was 3 nF.

Minimal Wideband Configurations

The maximum bandwidth can be achieved using the AD539 with simple resistive loads to convert the output currents to voltages. These currents (nominally ±1 mA FS, ±2.25 mA peak, into short-circuit loads) are shunted by their source resistance of 1.25 kΩ (each channel). Calculations of load power and effective scaling-voltage must allow for this shunting effect when using resistive loads. The output power is quite low in this mode, and the device behaves more like a voltage-controlled attenuator than a classical multiplier. The matching of gain and phase between the two channels is excellent. From dc to 10 MHz, the gains are typically within ±0.025 dB (measured using precision 50 Ω load resistors) and the phase difference within ±0.1°.

For a given load resistance, the output power can be quadrupled by using both channels in parallel, as shown in Figure 21. The small signal silicon diode, D, connected between ground and BASE COMMON (Pin 12 and Pin 13) provides extra voltage compliance at the output nodes in the negative direction (to −1 V at 25°C); it is not required if the output swing does not exceed −300 mV. Table 5 compares performance for various load resistances, using this configuration.

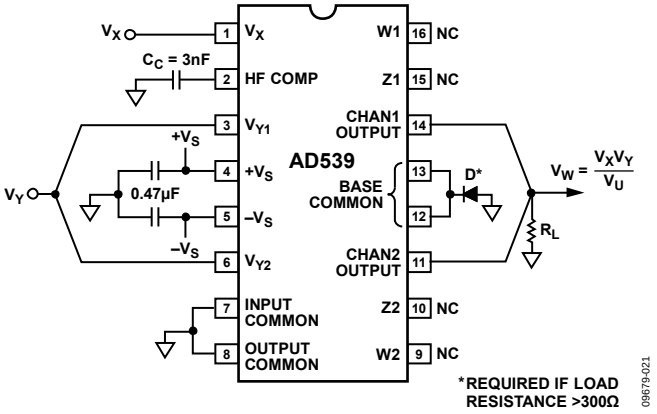


Figure 21. Minimal Single-Channel Multiplier (16-Lead SBDIP and PDIP Shown)

Figure 9 shows the high frequency response for Figure 21 with the AD539 in a carefully shielded 50 Ω test environment; the test system response was first characterized and this background removed by digital signal processing to show the inherent circuit response.

In many applications phase linearity over frequency is important. Figure 10 shows the deviation from an ideal linear-phase response for a typical AD539 over the frequency range dc to 10 MHz, for V_X = 3 V; the peak deviation is slightly more than 1°. Differential phase linearity (the stability of phase over the signal window at a fixed frequency) is shown in Figure 11 for f = 3.579 MHz and various values of V_X. The most rapid variation occurs for V_Y above 1 V; in applications where this characteristic is critical, it is recommended that a ground-referenced, negative-going signal be used.

Table 5. Summary of Performance for Minimal Configuration

Load Resistance	50 Ω	75 Ω	100 Ω	150 Ω	600 Ω	Open Circuit
FS Output Voltage						
DC	±92.6 mV	±134 mV	±172 mV	±242 mV	±612 mV	±1 V
AC (RMS)	65.5 mV rms	94.7 mV rms	122 mV rms	171 mV rms	433 mV rms	Note[1]
FS Output	0.086 mW	0.12 mW	0.15 mW	0.195 mW	0.312 mW	N/A[2]
Power in Load	−10.5 dBm	−9.2 dBm	−8.3 dBm	−7.1 dBm	−5.05 dBm	N/A
Peak Output Voltage						
DC	±210 mV	±300 mV	±388 mV	±544 mV	±1 mV	±1 V
AC (RMS)	148 mV rms	212 mV rms	274 mV rms	385 mV rms	Note[1]	Note[1]
Peak Output	0.44 mW	0.6 mW	0.75 mW	1 mW	±1 V	±1 V
Power in Load	−7 dBm	−4.4 dBm	−2.5 dBm	0 dBm	Note[1]	Note[1]
Effective Scaling Voltage, V_U′	67.5 V	46.7 V	36.3 V	25.8 V	10.2 V	5 V

[1] Peak negative voltage swing limited by output compliance.
[2] N/A means not applicable.

Differential Configurations

When only one signal channel must be handled, it is often advantageous to use the channels differentially. By subtracting the Channel 1 and Channel 2 outputs, any residual transient control feedthrough is virtually eliminated. Figure 22 shows a minimal configuration where it is assumed that the host system uses differential signals and a 50 Ω environment throughout. This figure also shows a recommended control feedforward network to improve large-signal response time. The control feedthrough glitch is shown in Figure 12, where the input was applied to Channel 1 and only the output of Channel 1 was displayed on the oscilloscope. The improvement obtained when CH1 and CH2 outputs are viewed differentially is clear in Figure 13. The envelope rise time is of the order of 40 ns.

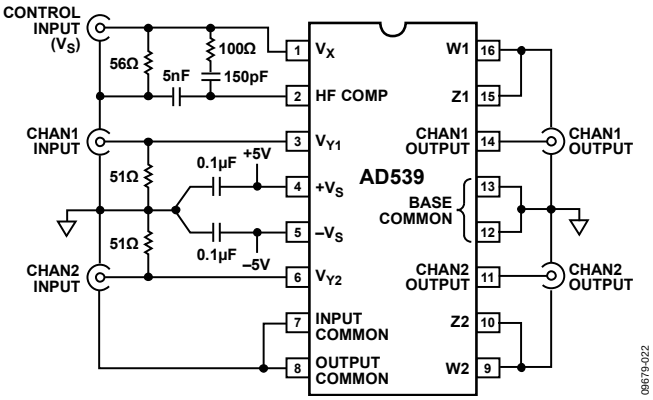


Figure 22. High Speed Differential Configuration (16-Lead SBDIP and PDIP Shown)

Lower distortion results when Channel 1 and Channel 2 are driven by complementary inputs and the outputs are utilized differentially, using a circuit such as the one shown in Figure 23. Resistors R1 and R2 minimize a secondary distortion mechanism caused by a collector modulation effect in the controlled cascode stages (see the Theory of Operation section) by keeping the voltage swing at the outputs to an acceptable level and should have a value in the range of 100 Ω to 1000 Ω. Figure 14 shows the improvement in distortion over the standard configuration (compare with Figure 5). Note that the Z nodes (Pin 10 and Pin 15) are returned to the control input; this prevents the early onset of output transistor saturation.

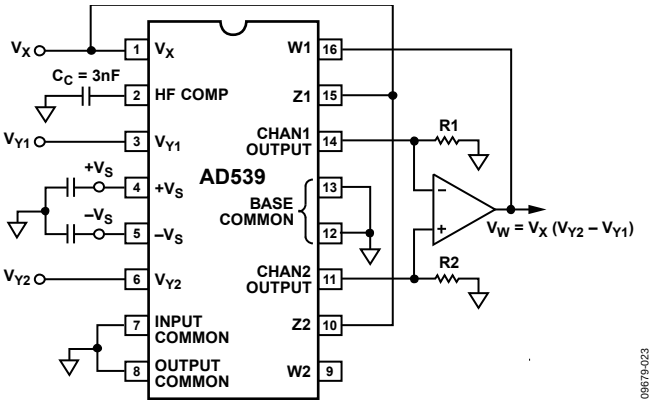


Figure 23. Low Distortion Differential Configuration (16-Lead SBDIP and PDIP Shown)

Even lower distortion (0.01%, or −80 dB) has been measured using two output op amps in a configuration similar to that shown in Figure 20 connected as virtual ground current summers (to prevent the modulation effect). Note that to generate the difference output it is merely necessary to connect the output of the Channel 1 op amp to the Z node of Channel 2. In this way, the net input to the Channel 2 op amp is the difference signal, and the low distortion resultant appears as its output.

A 50 MHZ VOLTAGE-CONTROLLED AMPLIFIER

Figure 24 is a circuit for a 50 MHz voltage-controlled amplifier (VCA) suitable for use in high quality video-speed applications. The outputs from the two signal channels of the AD539 are applied to the op amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when overdriven ($V_X < 0$ V or $V_X > 3.3$ V). Secondly, it provides a choice of either noninverting or inverting response, using either input, V_{Y1} or V_{Y2}, respectively. In this circuit, the output of the op amp equals

$$V_{OUT} = \frac{V_X (V_{Y1} - V_{Y2})}{2\,\text{V}} \text{ for } V_X > 0\,\text{V}$$

Therefore, the gain is unity at $V_X = 2$ V. Because V_X can overrange to 3.3 V, the maximum gain in this configuration is about 4.3 dB.

The −3 dB bandwidth of this circuit is over 50 MHz at a full gain and is not substantially affected at lower gains. When V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, extreme care is required in laying out the PC board to minimize this effect. In addition, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 15 shows the ac response from the noninverting input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions include $V_{Y1} = 0.5$ V rms for values of V_X from 10 mV to 3.16 V; this is with a 75 Ω load on the output. The feedthrough at $V_X = -10$ mV is also shown.

With the VCA driving a 75 Ω load and the transient response of the signal channel at $V_X = 2$ V, $V_Y = V_{OUT} = \pm 1$ V is shown in Figure 16. The rise and fall times are approximately 7 ns.

A more detailed description of this circuit, including differential gain and phase characteristics, is given in the AN-213 Application Note, *Low Cost, Two Chip Voltage-Controlled Amplifier and Video Switch*, available from Analog Devices.

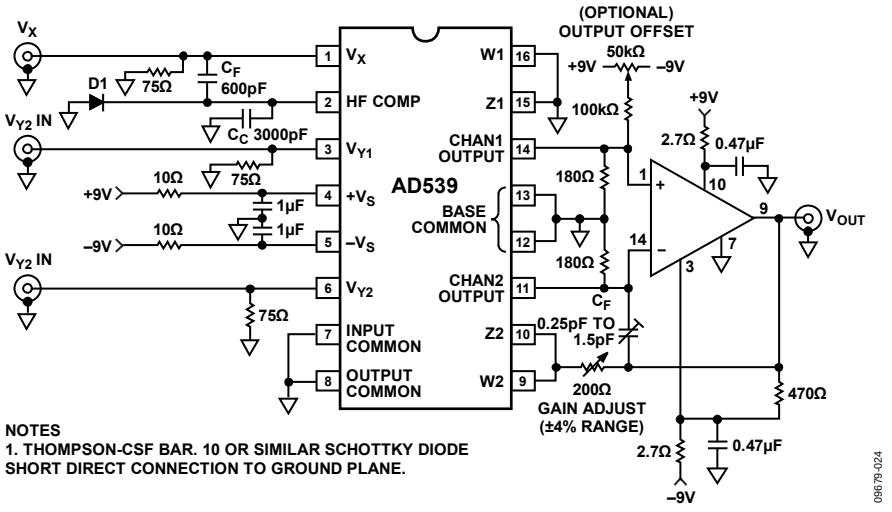


Figure 24. A Wide Bandwidth Voltage-Controlled Amplifier (16-Lead SBDIP and PDIP Shown)

BASIC DIVIDER CONNECTIONS

Standard Scaling

The AD539 provides excellent operation as a two-quadrant analog divider in wideband, wide gain-range applications, with the advantage of dual-channel operation. Figure 25 shows the simplest connections for division with a transfer function of

$$V_Y = -V_U V_W / V_X$$

Recalling that the nominal value of V_U is 1 V, this can be simplified to

$$V_Y = -V_W / V_X$$

where all signals are expressed in volts. The circuit thus exhibits unity gain for V_X = 1 V and a gain of 40 dB when V_X = 0.01 V.

The output swing is limited to ±2 V nominal full scale and ±4.2 V peak (using a $-V_S$ supply of at least 7.5 V for the AD539). Because the maximum loss is 10 dB (at V_X = 3.162 V), it follows that the maximum input to V_W should be ±6.3 V (4.4 V rms) for low distortion applications and no more than ±13.4 V (9.5 V rms) to avoid clipping. Note that offset adjustment is needed for the op amps to maintain accurate dc levels at the output in high gain applications: the noise gain is 6 V/V_X, or 600 at V_X = 0.01 V.

The gain magnitude response for this configuration using the LH0032 op amps with nominally 12 pF compensation (HF COMP, Pin 2, to V_{Y1}, Pin 3) and C_F = 7 pF is shown in Figure 17; however, other amplifiers can also be used. Because there is some manufacturing variation in the HF response of the op amps and load conditions also affect the response, these capacitors should be adjustable: 5 pF to 15 pF is recommended for both positions. The bandwidth in this configuration is nominally 17 MHz at V_X = 3.162 V, 4.5 MHz at V_X = 1 V, 350 kHz at V_X = 0.1 V, and 35 kHz at V_X = 0.01 V. The general recommendations regarding the use of a good ground plane and power supply decoupling should be carefully observed. Other suitable high speed op amps include: AD844, AD827, and AD811. Consult these data sheets for suitable applications circuits.

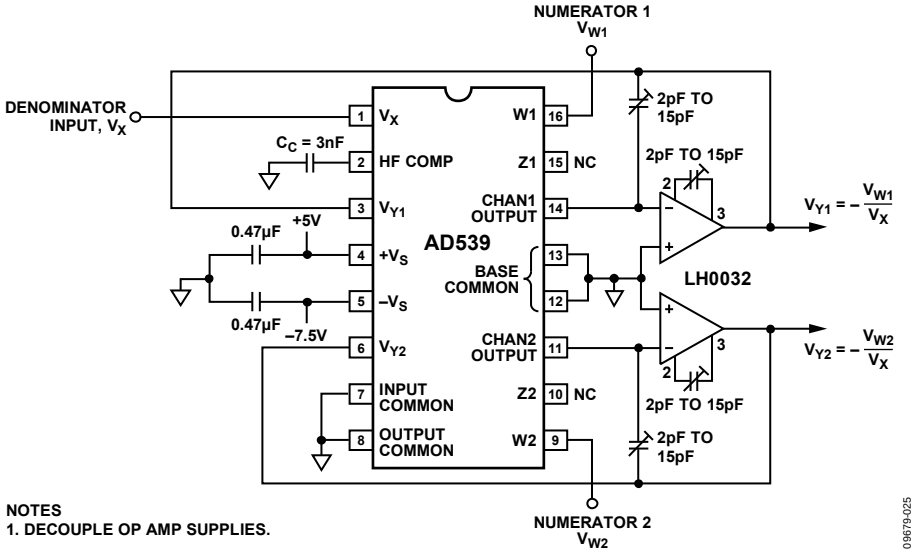
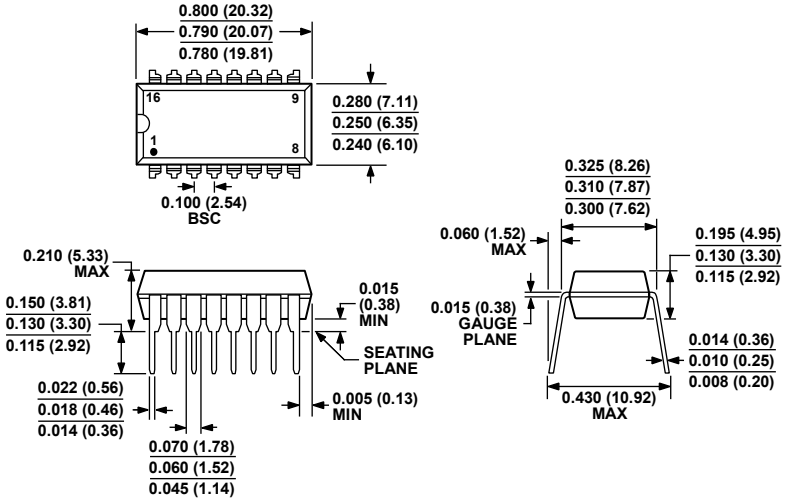


Figure 25. 2-Channel Divider with 1 V Scaling (16-Lead SBDIP and PDIP Shown)

OUTLINE DIMENSIONS

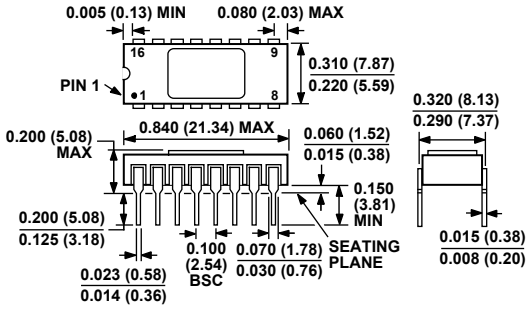


COMPLIANT TO JEDEC STANDARDS MS-001-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

073106-B

Figure 26. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 27. 16-Lead Side-Brazed Ceramic Dual In-Line Package (SBDIP]
(D-16)
Dimensions shown in inches and (millimeters)

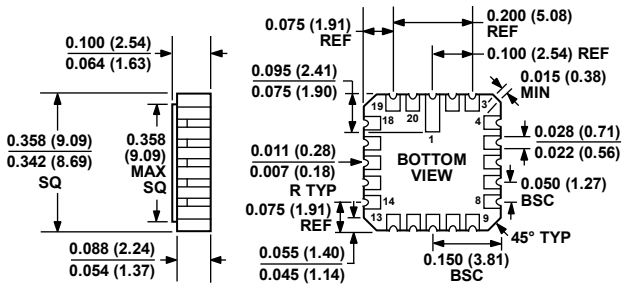


Figure 28. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20-1)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option
AD539JN		0°C to 70°C	16-Lead PDIP	N-16
AD539JNZ		0°C to 70°C	16-Lead PDIP	N-16
AD539JDZ		0°C to 70°C	16-Lead SBDIP	D-16
AD539KN		0°C to 70°C	16-Lead PDIP	N-16
AD539KNZ		0°C to 70°C	16-Lead PDIP	N-16
AD539KDZ		0°C to 70°C	16-Lead SBDIP	D-16
AD539SD		−55°C to +125°C	16-Lead SBDIP	D-16
AD539SD/883B		−55°C to +125°C	16-Lead SBDIP	D-16
5962-8980901EA	[2]	−55°C to +125°C	16-Lead SBDIP	D-16
AD539SE/883B		−55°C to +125°C	20-Terminal LCC	E-20-1

[1] Z = RoHS Compliant Part.
[2] The standard military drawing version of the AD539 (5962-8980901EA) is now available.

NOTES

NOTES

D09679-0-4/11(B)

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