THCV241A

SerDes transmitter with bi-directional transceiver

1 General Description

THCV241A is designed to support 1080p60 2Mpixel uncompressed video data over 15m 100ohm differential STP or single-end 50ohm Coaxial cable with 4 in-line connectors between camera and processor by V-by-One® HS.

THCV241A supports a MIPI CSI-2. Each CSI-2 data lane can transmit up to 1.2Gbps/lane. Virtual channel is supported.

One high-speed V-by-One® HS lane can transmit up to 1080p60fps. The maximum serial data rate is 4Gbps/lane. 2nd output lane supports HDR large amount of data or data copy-and-distribution experience.

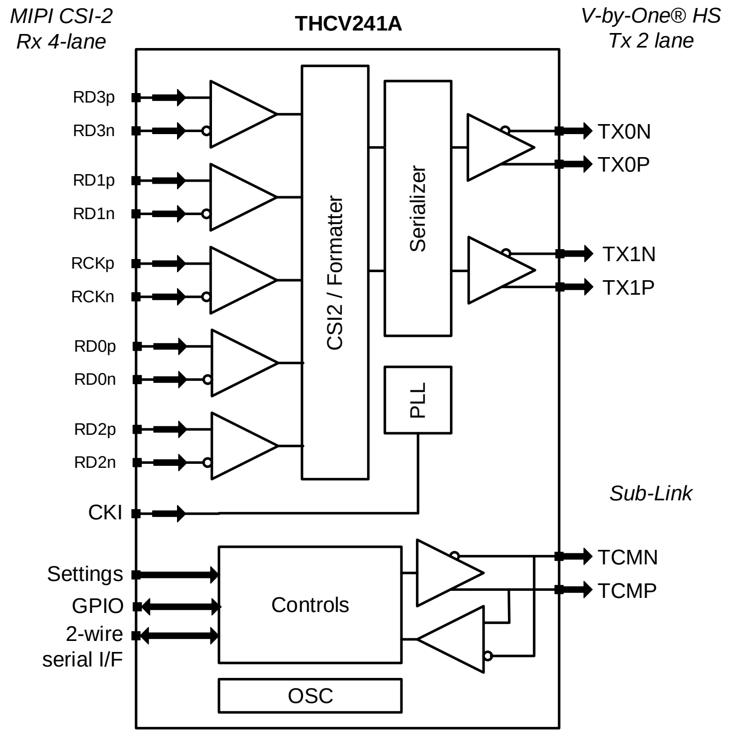
THCV241A is capable to control and monitor camera module from remote ECU via GPIO, UART or 1Mbps 2-wire serial interface.

Several fault and error detection function including CRC provides hardware functional safety design.

2 Features

- MIPI CSI-2 with 1,2 or 4-lane input
- MIPI D-PHY supports 80Mbps~1.2Gbps
- MIPI Virtual channel supported
- Video formats: RAW8/10/12/14/16/20, YUV422/420, RGB888/666/565, JPEG, User-defined generic 8-bit
- V-by-One® HS 400Mbps~4Gbps x2lane
- V-by-One® HS standard version1.5
- Reference clock input CKI range 10~40MHz shareable with video source CMOS sensor
- Wide range IO voltage from 1.7V to 3.6V
- Additional spread spectrum to reduce EMI
- 2-wire serial interface 1Mbps bridge function
- Remote GPIO/UART control and monitoring
- Error detection including CRC and notification
- QFN40 5x5mm 0.4mm pitch Exp-pad package

3 Block Diagram



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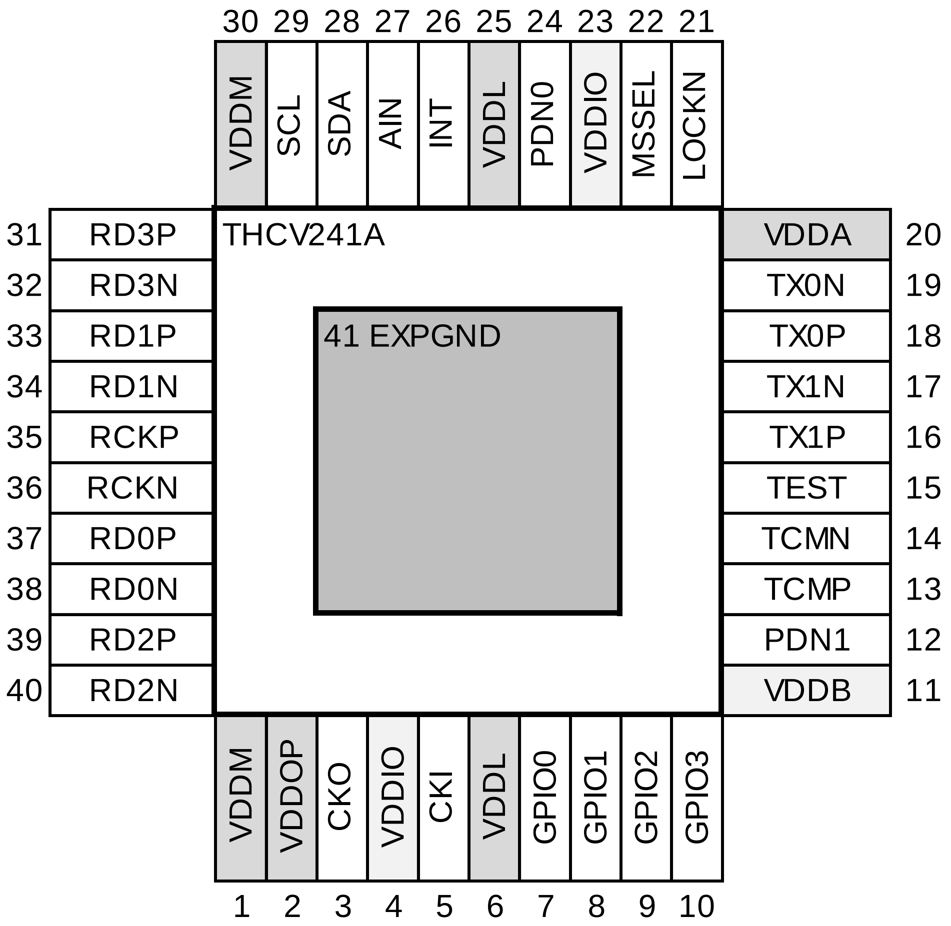
4 Pin Configuration



5 Pin Description

Pin Name	Pin #	type*	Description
RD3P/N	31,32	MI	MIPI lane3 differential data input
RD1P/N	33,34	MI	MIPI lane1 differential data input
RCKP/N	35,36	MI	MIPI differential clock inputs
RD0P/N	37,38	MI	MIPI lane0 differential data input
RD2P/N	39,40	MI	MIPI lane2 differential data input
TX0P/N	18,19	CO	V-by-One® HS lane0 High-speed CML signal output
TX1P/N	16,17	CO	V-by-One® HS lane1 High-speed CML signal output
TCMP/N	13,14	CB/B	TCMP/N (PDN1=1): CML Bi-directional Input/Output(Sub-Link). NC (PDN1=0): Not Connected. Must be open.
SCL	29	B	2-wire serial Master/Slave SCL
SDA	28	B	2-wire serial Master/Slave SDA
PDN0	24	I	Whole IC Power Down 0 : Power Down 1 : Normal Operation
PDN1	12	I	Sub-Link Power Down 0 : Sub-Link Power Down 1 : Sub-Link Normal Operation
TEST	15	I	Test pin. Must be tied to Ground for normal operation.
CKI	5	I	Reference Clock Input
CKO	3	O	Reference Clock Output
LOCKN	21	I	LOCK detect input Negative polarity If external LOCKN connection is used, it is supposed to be connected to Rx LOCKN with a 30kΩ pull-up resistor.
GPIO0	7	B	GPIO0
GPIO1	8	B	GPIO1
GPIO2	9	B	GPIO2
GPIO3	10	B	GPIO3
MSSEL	22	I	MSSEL (PDN1=1): Sub-Link Master/Slave Select 0 : Sub-Link Master side(inside 2-wire serial I/F is slave) 1 : Sub-Link Slave side(inside 2-wire serial I/F is master) Sub-Link Master is connected to HOST MCU. HTPDN (PDN1=0): HoT Plug Detect input Negative polarity Must be connected to Rx HTPDN with a 30kΩ pull-up resistor.
AIN	27	I	Select Slave Address 0 : 2wire serial Address = 7'b000_1011 1 : 2wire serial Address = 7'b011_0100
INT	26	O	Interrupt signal output. It must be connected with a pull-up resistor. 0 : Interrupt occurred 1 : Steady state
VDDOP	2	P	PLL Power supply Pin 1.2V
VDDM	1,30	P	MIPI Power supply Pin 1.2V
VDDA	20	P	Analog Power supply Pin 1.2V
VDDL	6,25	P	Digital Power supply Pins 1.2V
VDDB	11	P	Analog Power supply Pin 1.8~3.3V
VDDIO	4,23	P	IO Power supply Pin 1.8~3.3V
EXPGND	41	G	Exposed Pad Ground : Must be tied to Ground

*type symbol
MI=MIPI Input, CO=CML Output
CB=CML Bi-directional input/output
B=1.8~3.3V CMOS Bi-directional input/output, I=1.8~3.3v CMOS Input, O=1.8~3.3v CMOS Output
P=Power, G=Ground

6 Functional Description

6.1 Functional Overview

THCV241A can receive MIPI CSI-2 video and transmit it to over 15m length. With High Speed CML SerDes, high reliability and robustness encoding scheme and CDR (Clock and Data Recovery) architecture, the THCV241A enables to transmit RAW/YUV/RGB/JPEG/Generic8bit data through Main-Link by single 100ohm differential pair or 50ohm Coax cable with minimal external components. Maximum supported resolution is horizontal active 3840 pixels format. In addition, the THCV241A has Sub-Link which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for Main-Link through the other 1-pair of CML-Line. The THCV241A system is able to watch peripheral devices and to control them via 2-wire serial interface or GPIOs. They also can report interrupt events caused by change of GPIO inputs and internal statuses such as CRC error.

6.2 Reference clock supply

Reference clock supply CKI is required since MIPI CSI-2 clock stream will not always be continuous.
CKI frequency examples are 24MHz, 27MHz and 37.125MHz.
To supply the same oscillator clock as CMOS sensor to THCV241A is recommended.
See Figure 1.
Physical layout artwork of oscillator clock trace is supposed to be designed to shorten stub branch as possible.

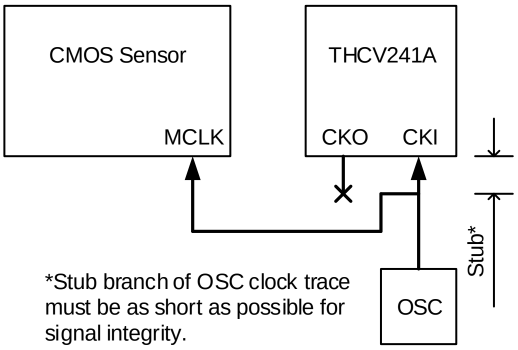


Figure 1. Reference clock supply basic method

Another alternative is to make use of THCV241A CKO internal clock buffer function.
CKO clock buffer may strengthen clock drive ability in order to compensate clock signal loss in large structure.
On the other hand, additional clock buffer may become another EMI emission source as trade-off.

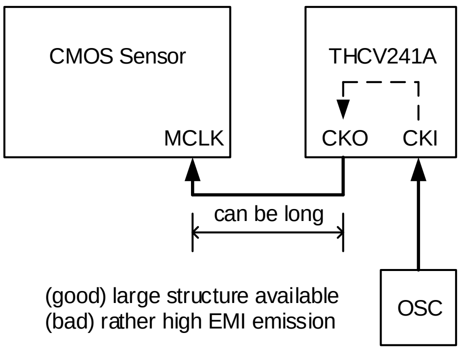


Figure 2. Reference clock supply clock buffer method (optional)

6.3 MIPI input setting

Setting of MIPI input can be configurable by 2-wire access to internal register.
Lane0 of MIPI input must always be used regardless of configuration as an obligation.

Table 1. MIPI input setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1025	[0]	R_RX_PN_SW	1	R/W	MIPI P/N swap	1'h0
0x1026	[7:6]	R_RX_LANE_SEL0	2	R/W	MIPI Data Lane RX0P/RX0N pin input mapping/swap select MIPI standard format lane# assignment used on RX0P/RX0N input The same setting as R_RX_LANE_SEL1/2/3 is prohibited.	2'h0
0x1026	[5:4]	R_RX_LANE_SEL1	2	R/W	MIPI Data Lane RX1P/RX1N pin input mapping/swap select MIPI standard format lane# assignment used on RX1P/RX1N input The same setting as R_RX_LANE_SEL0/2/3 is prohibited.	2'h1
0x1026	[3:2]	R_RX_LANE_SEL2	2	R/W	MIPI Data Lane RX2P/RX2N pin input mapping/swap select MIPI standard format lane# assignment used on RX2P/RX2N input The same setting as R_RX_LANE_SEL0/1/3 is prohibited.	2'h2
0x1026	[1:0]	R_RX_LANE_SEL3	2	R/W	MIPI Data Lane RX3P/RX3N pin input mapping/swap select MIPI standard format lane# assignment used on RX3P/RX3N input The same setting as R_RX_LANE_SEL0/1/2 is prohibited.	2'h3
0x102C	[0]	R_RX_CLKLANE_EN	1	R/W	MIPI Clock Lane Enable 0:Disable 1:Enable	1'h0
0x102D	[4]	R_RX_DATALANE_EN	1	R/W	MIPI Data Lane Enable 0:Disable 1:Enable, following R_RX_LANE_SEL_EN	1'h0
0x102D	[1:0]	R_RX_LANE_SEL_EN	2	R/W	MIPI Valid Data Lane number select 00:1Lane (lane0 Enable) 01,10:2Lane (lane<1:0> Enable) 11:4Lane (lane<3:0> Enable)	2'h3

6.4 HTPDN/LOCKN

Hot-Plug Function

HTPDN indicates Main-Link connect condition between Transmitter and Receiver. HTPDN of Transmitter side is high when Receiver is not active or not connected. Then Transmitter can enter into power down mode. HTPDN is set to Low by the Receiver when Receiver is active and connects to the Transmitter, and then Transmitter must start up and transmit CDR training pattern for link training. HTPDN is open drain output at the receiver side. Transmitter side needs Pull-up resistor.

There is an application option to omit HTPDN connection between Transmitter and Receiver. In this case, HTPDN at Transmitter side should always be at Low.

Lock Detect Function

LOCKN indicates whether CDR PLL of Main-Link is in lock status or not. LOCKN at Transmitter input is set to High by pull-up resistor when Receiver is not active or in CDR PLL training. LOCKN is set to Low by Receiver when CDR lock is completed. After that the CDR training mode finishes and then Transmitter shifts to the normal mode. LOCKN of Receiver is open drain. Transmitter side needs pull-up resistor.

When an application omits HTPDN, LOCKN signal should only be considered with HTPDN pulled low by Receiver.

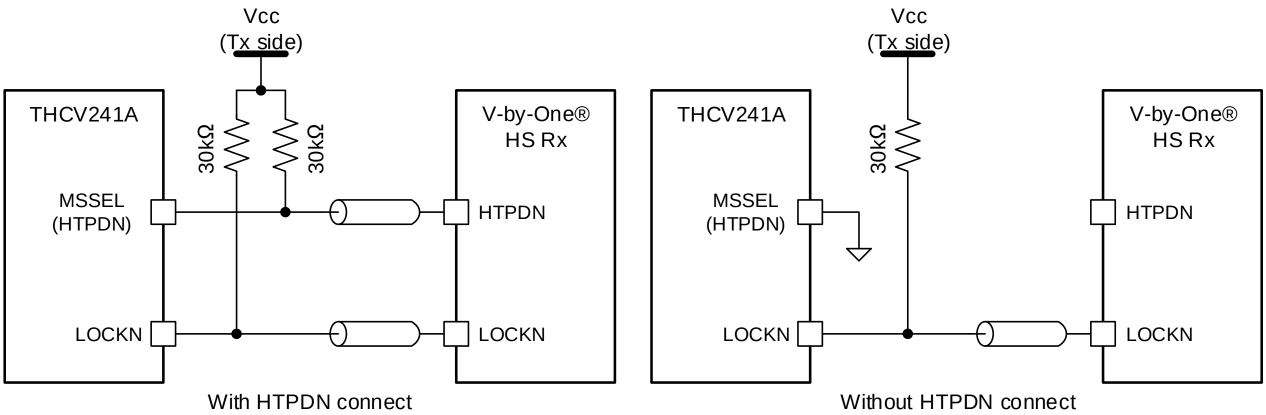


Figure 3. Physical wire connection for wired Hot-plug and Lock detect scheme

It will need same GND potential reference between transmitter and receiver device to connect HTPDN and LOCKN pins directly like above. HTPDN and LOCKN can also be transmitted via Sub-Link without physical wire connection. Assignment can be configurable by 2-wire access to internal register.

Table 2. HTPDN/LOCKN register

Addr(h)	Bits	Register	width	R/W	Description	Default
0x101D	[1:0]	R_HTPDN_SEL	2	R/W	V-by-One® HS HTPDN assignment 00:Sub-Link at PDN1=1 / HTPDN pin input at PDN1=0, 01:Reserved, 10:forced Low (Must be set at V-by-One® HS Distribution Enable), 11:forced High	2'h0
0x101E	[5:4]	R_LOCKN0_SEL	2	R/W	V-by-One® HS LOCKN for lane0 assignment 00:Sub-Link, 01:LOCKN pin input, 10:forced Low , 11:forced High	2'h0
0x101E	[1:0]	R_LOCKN1_SEL	2	R/W	V-by-One® HS LOCKN for lane1 assignment 00:Sub-Link, 01:LOCKN pin input, 10:forced Low , 11:forced High	2'h0

6.5 V-by-One® HS output setting

Setting of V-by-One® HS output format can be configurable by 2-wire access to internal register.

Table 3. V-by-One® HS output format setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1000	[0]	R_VX1_LANE	1	R/W	V-by-One® HS output lane number setting 0:1lane 1:2lanes	1'h1
0x1001	[6:4]	R_OUTPUT_FMT	3	R/W	V-by-One® HS output format setting 000:Main-Link PRivate Format (MPRF) 001:V-by-One® HS Standard YUV422(16bit)/RAW8 010:V-by-One® HS Standard RGB888 011:V-by-One® HS Standard RGB565 100:V-by-One® HS Standard RAW10 Mode1 101:V-by-One® HS Standard RAW12 Mode1 110: V-by-One® HS Standard RAW10 Mode2 111: V-by-One® HS Standard RAW12 Mode2	3'h0
0x1002	[5]	R_HFSEL	1	R/W	V-by-One® HS HFSEL (High Freq. SELect) mode Enable 0:HF Mode Disable 1:HF Mode Enable	1'h0
0x1055	[1:0]	R_BITMAP_SEL	2	R/W	V-by-One® HS output data mapping select 00:MAP1, 01:MAP2, 10:MAP3, 11:MAP4	2'h0

6.5.1 MPRF (Main-Link PRivate Format)

MPRF format encoding preserves original data packet input to THCV241A and output the data packet from counterpart V-by-One® HS receiver. The counterpart receiver must have installed MPRF format decoder like THCV242 because MPRF is not standard format.

Output V-by-One® HS Byte Mode is 4Byte Mode.

Video formats: RAW8/10/12/14/16/20, YUV422/420, RGB888/666/565, JPEG, and User-defined generic 8-bit are all supported with MPRF.

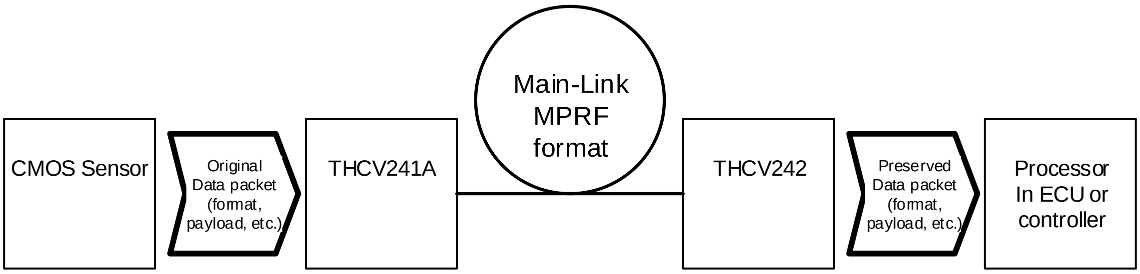


Figure 4. MPRF (Main-Link PRivate Format)

6.5.2 V-by-One® HS standard format

THCV241A output format capabilities as transmitter are shown as follows. D[31:0] indicates V-by-One® HS standard version1.5 Packer packet definition. Data can be transmitted normally only when both transmitter and receiver are set to the same available format. Some of the THCV241A format may not be supported by particular counterpart receiver because THCV241A prepares multiple formats that suit to multiple receiver devices alternatives.

Table 4. V-by-One® HS 1lane output data mapping format 1/3

R_OUTPUT_FMT	1						
R_HFSEL	0					1	
R_BITMAP_SEL	0	1	2	0	3	0	1
default V-by-One®HS Byte Mode	3	3	3	3	3	4	4
Format Name Vx1HS std. Packer Packet ref.	YUV422 Map1	YUV422 Map2	YUV422 Map3	RAW8	RAW8 Map4	YUV422HF Map1	YUV422HF Map2
V-by-One®HS_D[31]	-	-	-	-	-	Y[7](1st)	Cb(U)[7]
V-by-One®HS_D[30]	-	-	-	-	-	Y[6](1st)	Cb(U)[6]
V-by-One®HS_D[29]	-	-	-	-	-	Y[5](1st)	Cb(U)[5]
V-by-One®HS_D[28]	-	-	-	-	-	Y[4](1st)	Cb(U)[4]
V-by-One®HS_D[27]	-	-	-	-	-	Y[3](1st)	Cb(U)[3]
V-by-One®HS_D[26]	-	-	-	-	-	Y[2](1st)	Cb(U)[2]
V-by-One®HS_D[25]	-	-	-	-	-	Y[1](1st)	Cb(U)[1]
V-by-One®HS_D[24]	-	-	-	-	-	Y[0](1st)	Cb(U)[0]
V-by-One®HS_D[23]	Cb(U)[7]/Cr(V)[7]	Y[7](1st)/Y[7](2nd)	0	RAW[7] (1st)	RAW[7] (1st)	Cb(U)[7]	Y[7](1st)
V-by-One®HS_D[22]	Cb(U)[6]/Cr(V)[6]	Y[6](1st)/Y[6](2nd)	0	RAW[6] (1st)	RAW[6] (1st)	Cb(U)[6]	Y[6](1st)
V-by-One®HS_D[21]	Cb(U)[5]/Cr(V)[5]	Y[5](1st)/Y[5](2nd)	0	RAW[5] (1st)	RAW[5] (1st)	Cb(U)[5]	Y[5](1st)
V-by-One®HS_D[20]	Cb(U)[4]/Cr(V)[4]	Y[4](1st)/Y[4](2nd)	0	RAW[4] (1st)	RAW[4] (1st)	Cb(U)[4]	Y[4](1st)
V-by-One®HS_D[19]	Cb(U)[3]/Cr(V)[3]	Y[3](1st)/Y[3](2nd)	0	RAW[3] (1st)	RAW[3] (1st)	Cb(U)[3]	Y[3](1st)
V-by-One®HS_D[18]	Cb(U)[2]/Cr(V)[2]	Y[2](1st)/Y[2](2nd)	0	RAW[2] (1st)	RAW[2] (1st)	Cb(U)[2]	Y[2](1st)
V-by-One®HS_D[17]	Cb(U)[1]/Cr(V)[1]	Y[1](1st)/Y[1](2nd)	0	RAW[1] (1st)	RAW[1] (1st)	Cb(U)[1]	Y[1](1st)
V-by-One®HS_D[16]	Cb(U)[0]/Cr(V)[0]	Y[0](1st)/Y[0](2nd)	0	RAW[0] (1st)	RAW[0] (1st)	Cb(U)[0]	Y[0](1st)
V-by-One®HS_D[15]	0	0	Y[7](1st)/Y[7](2nd)	0	0	Y[7](2nd)	Cr(V)[7]
V-by-One®HS_D[14]	0	0	Y[6](1st)/Y[6](2nd)	0	0	Y[6](2nd)	Cr(V)[6]
V-by-One®HS_D[13]	0	0	Y[5](1st)/Y[5](2nd)	0	0	Y[5](2nd)	Cr(V)[5]
V-by-One®HS_D[12]	0	0	Y[4](1st)/Y[4](2nd)	0	0	Y[4](2nd)	Cr(V)[4]
V-by-One®HS_D[11]	0	0	Y[3](1st)/Y[3](2nd)	0	RAW[7] (2nd)	Y[3](2nd)	Cr(V)[3]
V-by-One®HS_D[10]	0	0	Y[2](1st)/Y[2](2nd)	0	RAW[6] (2nd)	Y[2](2nd)	Cr(V)[2]
V-by-One®HS_D[9]	0	0	Y[1](1st)/Y[1](2nd)	0	RAW[5] (2nd)	Y[1](2nd)	Cr(V)[1]
V-by-One®HS_D[8]	0	0	Y[0](1st)/Y[0](2nd)	0	RAW[4] (2nd)	Y[0](2nd)	Cr(V)[0]
V-by-One®HS_D[7]	Y[7](1st)/Y[7](2nd)	Cb(U)[7]/Cr(V)[7]	Cb(U)[7]/Cr(V)[7]	RAW[7] (2nd)	RAW[3] (2nd)	Cr(V)[7]	Y[7](2nd)
V-by-One®HS_D[6]	Y[6](1st)/Y[6](2nd)	Cb(U)[6]/Cr(V)[6]	Cb(U)[6]/Cr(V)[6]	RAW[6] (2nd)	RAW[2] (2nd)	Cr(V)[6]	Y[6](2nd)
V-by-One®HS_D[5]	Y[5](1st)/Y[5](2nd)	Cb(U)[5]/Cr(V)[5]	Cb(U)[5]/Cr(V)[5]	RAW[5] (2nd)	RAW[1] (2nd)	Cr(V)[5]	Y[5(2nd)
V-by-One®HS_D[4]	Y[4](1st)/Y[4](2nd)	Cb(U)[4]/Cr(V)[4]	Cb(U)[4]/Cr(V)[4]	RAW[4] (2nd)	RAW[0] (2nd)	Cr(V)[4]	Y[4](2nd)
V-by-One®HS_D[3]	Y[3](1st)/Y[3](2nd)	Cb(U)[3]/Cr(V)[3]	Cb(U)[3]/Cr(V)[3]	RAW[3] (2nd)	0	Cr(V)[3]	Y[3](2nd)
V-by-One®HS_D[2]	Y[2](1st)/Y[2](2nd)	Cb(U)[2]/Cr(V)[2]	Cb(U)[2]/Cr(V)[2]	RAW[2] (2nd)	0	Cr(V)[2]	Y[2](2nd)
V-by-One®HS_D[1]	Y[1](1st)/Y[1](2nd)	Cb(U)[1]/Cr(V)[1]	Cb(U)[1]/Cr(V)[1]	RAW[1] (2nd)	0	Cr(V)[1]	Y[1](2nd)
V-by-One®HS_D[0]	Y[0](1st)/Y[0](2nd)	Cb(U)[0]/Cr(V)[0]	Cb(U)[0]/Cr(V)[0]	RAW[0] (2nd)	0	Cr(V)[0]	Y[0](2nd)

Table 5. V-by-One® HS 1lane output data mapping format 2/3

R_OUTPUT_FMT	1	2	3		4		
R_HFSEL	1	-	0	1	0	1	1
R_BITMAP_SEL	2	-	0	0	0	0	2
default V-by-One®HS Byte Mode	4	3	3	4	3	4	4
Format Name Vx1HS std. Packer Packet ref.	RAW8HF	RGB888	RGB565	RGB565HF	RAW10	RAW10HF Map1	RAW10HF Map3
V-by-One®HS_D[31]	RAW[7] (2nd)	-	-	B[4] (1st)	-	0	0
V-by-One®HS_D[30]	RAW[6] (2nd)	-	-	B[3] (1st)	-	0	0
V-by-One®HS_D[29]	RAW[5] (2nd)	-	-	B[2] (1st)	-	0	0
V-by-One®HS_D[28]	RAW[4] (2nd)	-	-	B[1] (1st)	-	0	0
V-by-One®HS_D[27]	RAW[3] (2nd)	-	-	B[0] (1st)	-	0	RAW[9] (1st)
V-by-One®HS_D[26]	RAW[2] (2nd)	-	-	G[5] (1st)	-	0	RAW[8] (1st)
V-by-One®HS_D[25]	RAW[1] (2nd)	-	-	G[4] (1st)	-	RAW[1] (1st)	RAW[7] (1st)
V-by-One®HS_D[24]	RAW[0] (2nd)	-	-	G[3] (1st)	-	RAW[0] (1st)	RAW[6] (1st)
V-by-One®HS_D[23]	RAW[7] (1st)	B[7]	B[4]	G[2] (1st)	0	RAW[9] (1st)	RAW[5] (1st)
V-by-One®HS_D[22]	RAW[6] (1st)	B[6]	B[3]	G[1] (1st)	0	RAW[8] (1st)	RAW[4] (1st)
V-by-One®HS_D[21]	RAW[5] (1st)	B[5]	B[2]	G[0] (1st)	0	RAW[7] (1st)	RAW[3] (1st)
V-by-One®HS_D[20]	RAW[4] (1st)	B[4]	B[1]	R[4] (1st)	0	RAW[6] (1st)	RAW[2] (1st)
V-by-One®HS_D[19]	RAW[3] (1st)	B[3]	B[0]	R[3] (1st)	0	RAW[5] (1st)	RAW[1] (1st)
V-by-One®HS_D[18]	RAW[2] (1st)	B[2]	0	R[2] (1st)	0	RAW[4] (1st)	RAW[0] (1st)
V-by-One®HS_D[17]	RAW[1] (1st)	B[1]	0	R[1] (1st)	0	RAW[3] (1st)	0
V-by-One®HS_D[16]	RAW[0] (1st)	B[0]	0	R[0] (1st)	0	RAW[2] (1st)	0
V-by-One®HS_D[15]	RAW[7] (4th)	G[7]	G[5]	B[4] (2nd)	0	0	0
V-by-One®HS_D[14]	RAW[6] (4th)	G[6]	G[4]	B[3] (2nd)	0	0	0
V-by-One®HS_D[13]	RAW[5] (4th)	G[5]	G[3]	B[2] (2nd)	0	0	0
V-by-One®HS_D[12]	RAW[4] (4th)	G[4]	G[2]	B[1] (2nd)	0	0	0
V-by-One®HS_D[11]	RAW[3] (4th)	G[3]	G[1]	B[0] (2nd)	0	0	RAW[9] (2nd)
V-by-One®HS_D[10]	RAW[2] (4th)	G[2]	G[0]	G[5] (2nd)	0	0	RAW[8] (2nd)
V-by-One®HS_D[9]	RAW[1] (4th)	G[1]	0	G[4] (2nd)	RAW[1]	RAW[1] (2nd)	RAW[7] (2nd)
V-by-One®HS_D[8]	RAW[0] (4th)	G[0]	0	G[3] (2nd)	RAW[0]	RAW[0] (2nd)	RAW[6] (2nd)
V-by-One®HS_D[7]	RAW[7] (3rd)	R[7]	R[4]	G[2] (2nd)	RAW[9]	RAW[9] (2nd)	RAW[5] (2nd)
V-by-One®HS_D[6]	RAW[6] (3rd)	R[6]	R[3]	G[1] (2nd)	RAW[8]	RAW[8] (2nd)	RAW[4] (2nd)
V-by-One®HS_D[5]	RAW[5] (3rd)	R[5]	R[2]	G[0] (2nd)	RAW[7]	RAW[7] (2nd)	RAW[3] (2nd)
V-by-One®HS_D[4]	RAW[4] (3rd)	R[4]	R[1]	R[4] (2nd)	RAW[6]	RAW[6] (2nd)	RAW[2] (2nd)
V-by-One®HS_D[3]	RAW[3] (3rd)	R[3]	R[0]	R[3] (2nd)	RAW[5]	RAW[5] (2nd)	RAW[1] (2nd)
V-by-One®HS_D[2]	RAW[2] (3rd)	R[2]	0	R[2] (2nd)	RAW[4]	RAW[4] (2nd)	RAW[0] (2nd)
V-by-One®HS_D[1]	RAW[1] (3rd)	R[1]	0	R[1] (2nd)	RAW[3]	RAW[3] (2nd)	0
V-by-One®HS_D[0]	RAW[0] (3rd)	R[0]	0	R[0] (2nd)	RAW[2]	RAW[2] (2nd)	0

Table 6. V-by-One® HS 1lane output data mapping format 3/3

R_OUTPUT_FMT	5			6		7	
R_HFSEL	0	1	1	-	-	-	-
R_BITMAP_SEL	0	0	1	0	2	0	1
default V-by-One®HS Byte Mode	3	4	4	3	3	3	3
Format Name Vx1HS std. Packer Packet ref.	RAW12	RAW12HF Map1	RAW12HF Map2	RAW10HF2 Map1	RAW10HF2 Map3	RAW12HF2 Map1	RAW12HF2 Map2
V-by-One®HS_D[31]	-	0	0	-	-	-	-
V-by-One®HS_D[30]	-	0	0	-	-	-	-
V-by-One®HS_D[29]	-	0	0	-	-	-	-
V-by-One®HS_D[28]	-	0	0	-	-	-	-
V-by-One®HS_D[27]	-	RAW[3] (1st)	RAW[11] (1st)	-	-	-	-
V-by-One®HS_D[26]	-	RAW[2] (1st)	RAW[10] (1st)	-	-	-	-
V-by-One®HS_D[25]	-	RAW[1] (1st)	RAW[9] (1st)	-	-	-	-
V-by-One®HS_D[24]	-	RAW[0] (1st)	RAW[8] (1st)	-	-	-	-
V-by-One®HS_D[23]	0	RAW[11] (1st)	RAW[7] (1st)	0	RAW[9] (1st)	RAW[3] (1st)	RAW[11] (1st)
V-by-One®HS_D[22]	0	RAW[10] (1st)	RAW[6] (1st)	0	RAW[8] (1st)	RAW[2] (1st)	RAW[10] (1st)
V-by-One®HS_D[21]	0	RAW[9] (1st)	RAW[5] (1st)	RAW[1] (1st)	RAW[7] (1st)	RAW[1] (1st)	RAW[9] (1st)
V-by-One®HS_D[20]	0	RAW[8] (1st)	RAW[4] (1st)	RAW[0] (1st)	RAW[6] (1st)	RAW[0] (1st)	RAW[8] (1st)
V-by-One®HS_D[19]	0	RAW[7] (1st)	RAW[3] (1st)	RAW[9] (1st)	RAW[5] (1st)	RAW[11] (1st)	RAW[7] (1st)
V-by-One®HS_D[18]	0	RAW[6] (1st)	RAW[2] (1st)	RAW[8] (1st)	RAW[4] (1st)	RAW[10] (1st)	RAW[6] (1st)
V-by-One®HS_D[17]	0	RAW[5] (1st)	RAW[1] (1st)	RAW[7] (1st)	RAW[3] (1st)	RAW[9] (1st)	RAW[5] (1st)
V-by-One®HS_D[16]	0	RAW[4] (1st)	RAW[0] (1st)	RAW[6] (1st)	RAW[2] (1st)	RAW[8] (1st)	RAW[4] (1st)
V-by-One®HS_D[15]	0	0	0	RAW[5] (1st)	RAW[1] (1st)	RAW[7] (1st)	RAW[3] (1st)
V-by-One®HS_D[14]	0	0	0	RAW[4] (1st)	RAW[0] (1st)	RAW[6] (1st)	RAW[2] (1st)
V-by-One®HS_D[13]	0	0	0	RAW[3] (1st)	0	RAW[5] (1st)	RAW[1] (1st)
V-by-One®HS_D[12]	0	0	0	RAW[2] (1st)	0	RAW[4] (1st)	RAW[0] (1st)
V-by-One®HS_D[11]	RAW[3]	RAW[3] (2nd)	RAW[11] (2nd)	0	RAW[9] (2nd)	RAW[3] (2nd)	RAW[11] (2nd)
V-by-One®HS_D[10]	RAW[2]	RAW[2] (2nd)	RAW[10] (2nd)	0	RAW[8] (2nd)	RAW[2] (2nd)	RAW[10] (2nd)
V-by-One®HS_D[9]	RAW[1]	RAW[1] (2nd)	RAW[9] (2nd)	RAW[1] (2nd)	RAW[7] (2nd)	RAW[1] (2nd)	RAW[9] (2nd)
V-by-One®HS_D[8]	RAW[0]	RAW[0] (2nd)	RAW[8] (2nd)	RAW[0] (2nd)	RAW[6] (2nd)	RAW[0] (2nd)	RAW[8] (2nd)
V-by-One®HS_D[7]	RAW[11]	RAW[11] (2nd)	RAW[7] (2nd)	RAW[9] (2nd)	RAW[5] (2nd)	RAW[11] (2nd)	RAW[7] (2nd)
V-by-One®HS_D[6]	RAW[10]	RAW[10] (2nd)	RAW[6] (2nd)	RAW[8] (2nd)	RAW[4] (2nd)	RAW[10] (2nd)	RAW[6] (2nd)
V-by-One®HS_D[5]	RAW[9]	RAW[9] (2nd)	RAW[5] (2nd)	RAW[7] (2nd)	RAW[3] (2nd)	RAW[9] (2nd)	RAW[5] (2nd)
V-by-One®HS_D[4]	RAW[8]	RAW[8] (2nd)	RAW[4] (2nd)	RAW[6] (2nd)	RAW[2] (2nd)	RAW[8] (2nd)	RAW[4] (2nd)
V-by-One®HS_D[3]	RAW[7]	RAW[7] (2nd)	RAW[3] (2nd)	RAW[5] (2nd)	RAW[1] (2nd)	RAW[7] (2nd)	RAW[3] (2nd)
V-by-One®HS_D[2]	RAW[6]	RAW[6] (2nd)	RAW[2] (2nd)	RAW[4] (2nd)	RAW[0] (2nd)	RAW[6] (2nd)	RAW[2] (2nd)
V-by-One®HS_D[1]	RAW[5]	RAW[5] (2nd)	RAW[1] (2nd)	RAW[3] (2nd)	0	RAW[5] (2nd)	RAW[1] (2nd)
V-by-One®HS_D[0]	RAW[4]	RAW[4] (2nd)	RAW[0] (2nd)	RAW[2] (2nd)	0	RAW[4] (2nd)	RAW[0] (2nd)

Table 7. V-by-One® HS 2lane output data mapping format 1/3

	R_OUTPUT_FMT	1						
	R_HFSEL	0					1	
	R_BITMAP_SEL	0	1	2	0	3	0	1
	default V-by-One®HS Byte Mode	3	3	3	3	3	4	4
	Format Name	YUV422 Map1	YUV422 Map2	YUV422 Map3	RAW8	RAW8 Map4	YUV422HF Map1	YUV422HF Map2
TX0P/N V-by-One® HS lane0	V-by-One®HS_D[31]	-	-	-	-	-	Y[7](1st)	Cb(U)[7](1st)
	V-by-One®HS_D[30]	-	-	-	-	-	Y[6](1st)	Cb(U)[6](1st)
	V-by-One®HS_D[29]	-	-	-	-	-	Y[5](1st)	Cb(U)[5](1st)
	V-by-One®HS_D[28]	-	-	-	-	-	Y[4](1st)	Cb(U)[4](1st)
	V-by-One®HS_D[27]	-	-	-	-	-	Y[3](1st)	Cb(U)[3](1st)
	V-by-One®HS_D[26]	-	-	-	-	-	Y[2](1st)	Cb(U)[2](1st)
	V-by-One®HS_D[25]	-	-	-	-	-	Y[1](1st)	Cb(U)[1](1st)
	V-by-One®HS_D[24]	-	-	-	-	-	Y[0](1st)	Cb(U)[0](1st)
	V-by-One®HS_D[23]	Cb(U)[7]	Cr(V)[7]	0	RAW[7] (1st)	RAW[7] (1st)	Cb(U)[7](1st)	Y[7](1st)
	V-by-One®HS_D[22]	Cb(U)[6]	Cr(V)[6]	0	RAW[6] (1st)	RAW[6] (1st)	Cb(U)[6](1st)	Y[6](1st)
	V-by-One®HS_D[21]	Cb(U)[5]	Cr(V)[5]	0	RAW[5] (1st)	RAW[5] (1st)	Cb(U)[5](1st)	Y[5](1st)
	V-by-One®HS_D[20]	Cb(U)[4]	Cr(V)[4]	0	RAW[4] (1st)	RAW[4] (1st)	Cb(U)[4](1st)	Y[4](1st)
	V-by-One®HS_D[19]	Cb(U)[3]	Cr(V)[3]	0	RAW[3] (1st)	RAW[3] (1st)	Cb(U)[3](1st)	Y[3](1st)
	V-by-One®HS_D[18]	Cb(U)[2]	Cr(V)[2]	0	RAW[2] (1st)	RAW[2] (1st)	Cb(U)[2](1st)	Y[2](1st)
	V-by-One®HS_D[17]	Cb(U)[1]	Cr(V)[1]	0	RAW[1] (1st)	RAW[1] (1st)	Cb(U)[1](1st)	Y[1](1st)
	V-by-One®HS_D[16]	Cb(U)[0]	Cr(V)[0]	0	RAW[0] (1st)	RAW[0] (1st)	Cb(U)[0](1st)	Y[0](1st)
	V-by-One®HS_D[15]	0	0	Y[7](1st)	0	0	Y[7] (3rd)	Cb(U)[7] (3rd)
	V-by-One®HS_D[14]	0	0	Y[6](1st)	0	0	Y[6] (3rd)	Cb(U)[6] (3rd)
	V-by-One®HS_D[13]	0	0	Y[5](1st)	0	0	Y[5] (3rd)	Cb(U)[5] (3rd)
	V-by-One®HS_D[12]	0	0	Y[4](1st)	0	0	Y[4] (3rd)	Cb(U)[4] (3rd)
	V-by-One®HS_D[11]	0	0	Y[3](1st)	0	RAW[7] (3rd)	Y[3] (3rd)	Cb(U)[3] (3rd)
	V-by-One®HS_D[10]	0	0	Y[2](1st)	0	RAW[6] (3rd)	Y[2] (3rd)	Cb(U)[2] (3rd)
	V-by-One®HS_D[9]	0	0	Y[1](1st)	0	RAW[5] (3rd)	Y[1] (3rd)	Cb(U)[1] (3rd)
	V-by-One®HS_D[8]	0	0	Y[0](1st)	0	RAW[4] (3rd)	Y[0] (3rd)	Cb(U)[0] (3rd)
	V-by-One®HS_D[7]	Cr(V)[7]	Cb(U)[7]	Cb(U)[7]	RAW[7] (3rd)	RAW[3] (3rd)	Cb(U)[7] (3rd)	Y[7] (3rd)
	V-by-One®HS_D[6]	Cr(V)[6]	Cb(U)[6]	Cb(U)[6]	RAW[6] (3rd)	RAW[2] (3rd)	Cb(U)[6] (3rd)	Y[6] (3rd)
	V-by-One®HS_D[5]	Cr(V)[5]	Cb(U)[5]	Cb(U)[5]	RAW[5] (3rd)	RAW[1] (3rd)	Cb(U)[5] (3rd)	Y[5] (3rd)
	V-by-One®HS_D[4]	Cr(V)[4]	Cb(U)[4]	Cb(U)[4]	RAW[4] (3rd)	RAW[0] (3rd)	Cb(U)[4] (3rd)	Y[4] (3rd)
	V-by-One®HS_D[3]	Cr(V)[3]	Cb(U)[3]	Cb(U)[3]	RAW[3] (3rd)	0	Cb(U)[3] (3rd)	Y[3] (3rd)
	V-by-One®HS_D[2]	Cr(V)[2]	Cb(U)[2]	Cb(U)[2]	RAW[2] (3rd)	0	Cb(U)[2] (3rd)	Y[2] (3rd)
	V-by-One®HS_D[1]	Cr(V)[1]	Cb(U)[1]	Cb(U)[1]	RAW[1] (3rd)	0	Cb(U)[1] (3rd)	Y[1] (3rd)
	V-by-One®HS_D[0]	Cr(V)[0]	Cb(U)[0]	Cb(U)[0]	RAW[0] (3rd)	0	Cb(U)[0] (3rd)	Y[0] (3rd)
TX1P/N V-by-One® HS lane1	V-by-One®HS_D[31]	-	-	-	-	-	Y[7] (2nd)	Cr(V)[7] (2nd)
	V-by-One®HS_D[30]	-	-	-	-	-	Y[6] (2nd)	Cr(V)[6] (2nd)
	V-by-One®HS_D[29]	-	-	-	-	-	Y[5] (2nd)	Cr(V)[5] (2nd)
	V-by-One®HS_D[28]	-	-	-	-	-	Y[4] (2nd)	Cr(V)[4] (2nd)
	V-by-One®HS_D[27]	-	-	-	-	-	Y[3] (2nd)	Cr(V)[3] (2nd)
	V-by-One®HS_D[26]	-	-	-	-	-	Y[2] (2nd)	Cr(V)[2] (2nd)
	V-by-One®HS_D[25]	-	-	-	-	-	Y[1] (2nd)	Cr(V)[1] (2nd)
	V-by-One®HS_D[24]	-	-	-	-	-	Y[0] (2nd)	Cr(V)[0] (2nd)
	V-by-One®HS_D[23]	Y[7] (1st)	Y[7](2nd)	0	RAW[7] (2nd)	RAW[7] (2nd)	Cr(V)[7] (2nd)	Y[7] (2nd)
	V-by-One®HS_D[22]	Y[6] (1st)	Y[6](2nd)	0	RAW[6] (2nd)	RAW[6] (2nd)	Cr(V)[6] (2nd)	Y[6] (2nd)
	V-by-One®HS_D[21]	Y[5] (1st)	Y[5](2nd)	0	RAW[5] (2nd)	RAW[5] (2nd)	Cr(V)[5] (2nd)	Y[5] (2nd)
	V-by-One®HS_D[20]	Y[4] (1st)	Y[4](2nd)	0	RAW[4] (2nd)	RAW[4] (2nd)	Cr(V)[4] (2nd)	Y[4] (2nd)
	V-by-One®HS_D[19]	Y[3] (1st)	Y[3](2nd)	0	RAW[3] (2nd)	RAW[3] (2nd)	Cr(V)[3] (2nd)	Y[3] (2nd)
	V-by-One®HS_D[18]	Y[2] (1st)	Y[2](2nd)	0	RAW[2] (2nd)	RAW[2] (2nd)	Cr(V)[2] (2nd)	Y[2] (2nd)
	V-by-One®HS_D[17]	Y[1] (1st)	Y[1](2nd)	0	RAW[1] (2nd)	RAW[1] (2nd)	Cr(V)[1] (2nd)	Y[1] (2nd)
	V-by-One®HS_D[16]	Y[0] (1st)	Y[0](2nd)	0	RAW[0] (2nd)	RAW[0] (2nd)	Cr(V)[0] (2nd)	Y[0] (2nd)
	V-by-One®HS_D[15]	0	0	Y[7](2nd)	0	0	Y[7] (4th)	Cr(V)[7] (4th)
	V-by-One®HS_D[14]	0	0	Y[6](2nd)	0	0	Y[6] (4th)	Cr(V)[6] (4th)
	V-by-One®HS_D[13]	0	0	Y[5](2nd)	0	0	Y[5] (4th)	Cr(V)[5] (4th)
	V-by-One®HS_D[12]	0	0	Y[4](2nd)	0	0	Y[4] (4th)	Cr(V)[4] (4th)
	V-by-One®HS_D[11]	0	0	Y[3](2nd)	0	RAW[7] (4th)	Y[3] (4th)	Cr(V)[3] (4th)
	V-by-One®HS_D[10]	0	0	Y[2](2nd)	0	RAW[6] (4th)	Y[2] (4th)	Cr(V)[2] (4th)
	V-by-One®HS_D[9]	0	0	Y[1](2nd)	0	RAW[5] (4th)	Y[1] (4th)	Cr(V)[1] (4th)
	V-by-One®HS_D[8]	0	0	Y[0](2nd)	0	RAW[4] (4th)	Y[0] (4th)	Cr(V)[0] (4th)
	V-by-One®HS_D[7]	Y[7] (2nd)	Y[7](1st)	Cr(V)[7]	RAW[7] (4th)	RAW[3] (4th)	Cr(V)[7] (4th)	Y[7] (4th)
	V-by-One®HS_D[6]	Y[6] (2nd)	Y[6](1st)	Cr(V)[6]	RAW[6] (4th)	RAW[2] (4th)	Cr(V)[6] (4th)	Y[6] (4th)
	V-by-One®HS_D[5]	Y[5] (2nd)	Y[5](1st)	Cr(V)[5]	RAW[5] (4th)	RAW[1] (4th)	Cr(V)[5] (4th)	Y[5] (4th)
	V-by-One®HS_D[4]	Y[4] (2nd)	Y[4](1st)	Cr(V)[4]	RAW[4] (4th)	RAW[0] (4th)	Cr(V)[4] (4th)	Y[4] (4th)
	V-by-One®HS_D[3]	Y[3] (2nd)	Y[3](1st)	Cr(V)[3]	RAW[3] (4th)	0	Cr(V)[3] (4th)	Y[3] (4th)
	V-by-One®HS_D[2]	Y[2] (2nd)	Y[2](1st)	Cr(V)[2]	RAW[2] (4th)	0	Cr(V)[2] (4th)	Y[2] (4th)
	V-by-One®HS_D[1]	Y[1] (2nd)	Y[1](1st)	Cr(V)[1]	RAW[1] (4th)	0	Cr(V)[1] (4th)	Y[1] (4th)
	V-by-One®HS_D[0]	Y[0] (2nd)	Y[0](1st)	Cr(V)[0]	RAW[0] (4th)	0	Cr(V)[0] (4th)	Y[0] (4th)

Table 8. V-by-One® HS 2lane output data mapping format 2/3

	R_OUTPUT_FMT	1	2	3		4		
	R_HFSEL	1	-	0	1	0	1	
	R_BITMAP_SEL	2	-	0	0	0	0	2
	default V-by-One®HS Byte Mode	4	3	3	4	3	4	4
	Format Name	RAW8HF	RGB888	RGB565	RGB565HF	RAW10	RAW10HF Map1	RAW10HF Map3
TX0P/N V-by-One® HS lane0	V-by-One®HS_D[31]	RAW[7] (2nd)	-	-	B[4] (1st)	-	0	0
	V-by-One®HS_D[30]	RAW[6] (2nd)	-	-	B[3] (1st)	-	0	0
	V-by-One®HS_D[29]	RAW[5] (2nd)	-	-	B[2] (1st)	-	0	0
	V-by-One®HS_D[28]	RAW[4] (2nd)	-	-	B[1] (1st)	-	0	0
	V-by-One®HS_D[27]	RAW[3] (2nd)	-	-	B[0] (1st)	-	0	RAW[9] (1st)
	V-by-One®HS_D[26]	RAW[2] (2nd)	-	-	G[5] (1st)	-	0	RAW[8] (1st)
	V-by-One®HS_D[25]	RAW[1] (2nd)	-	-	G[4] (1st)	-	RAW[1] (1st)	RAW[7] (1st)
	V-by-One®HS_D[24]	RAW[0] (2nd)	-	-	G[3] (1st)	-	RAW[0] (1st)	RAW[6] (1st)
	V-by-One®HS_D[23]	RAW[7] (1st)	B[7] (1st)	B[4] (1st)	G[2] (1st)	0	RAW[9] (1st)	RAW[5] (1st)
	V-by-One®HS_D[22]	RAW[6] (1st)	B[6] (1st)	B[3] (1st)	G[1] (1st)	0	RAW[8] (1st)	RAW[4] (1st)
	V-by-One®HS_D[21]	RAW[5] (1st)	B[5] (1st)	B[2] (1st)	G[0] (1st)	0	RAW[7] (1st)	RAW[3] (1st)
	V-by-One®HS_D[20]	RAW[4] (1st)	B[4] (1st)	B[1] (1st)	R[4] (1st)	0	RAW[6] (1st)	RAW[2] (1st)
	V-by-One®HS_D[19]	RAW[3] (1st)	B[3] (1st)	B[0] (1st)	R[3] (1st)	0	RAW[5] (1st)	RAW[1] (1st)
	V-by-One®HS_D[18]	RAW[2] (1st)	B[2] (1st)	0	R[2] (1st)	0	RAW[4] (1st)	RAW[0] (1st)
	V-by-One®HS_D[17]	RAW[1] (1st)	B[1] (1st)	0	R[1] (1st)	0	RAW[3] (1st)	0
	V-by-One®HS_D[16]	RAW[0] (1st)	B[0] (1st)	0	R[0] (1st)	0	RAW[2] (1st)	0
	V-by-One®HS_D[15]	RAW[7] (6th)	G[7] (1st)	G[5] (1st)	B[4] (3rd)	0	0	0
	V-by-One®HS_D[14]	RAW[6] (6th)	G[6] (1st)	G[4] (1st)	B[3] (3rd)	0	0	0
	V-by-One®HS_D[13]	RAW[5] (6th)	G[5] (1st)	G[3] (1st)	B[2] (3rd)	0	0	0
	V-by-One®HS_D[12]	RAW[4] (6th)	G[4] (1st)	G[2] (1st)	B[1] (3rd)	0	0	0
	V-by-One®HS_D[11]	RAW[3] (6th)	G[3] (1st)	G[1] (1st)	B[0] (3rd)	0	0	RAW[9] (3rd)
	V-by-One®HS_D[10]	RAW[2] (6th)	G[2] (1st)	G[0] (1st)	G[5] (3rd)	0	0	RAW[8] (3rd)
	V-by-One®HS_D[9]	RAW[1] (6th)	G[1] (1st)	0	G[4] (3rd)	RAW[1] (1st)	RAW[1] (3rd)	RAW[7] (3rd)
	V-by-One®HS_D[8]	RAW[0] (6th)	G[0] (1st)	0	G[3] (3rd)	RAW[0] (1st)	RAW[0] (3rd)	RAW[6] (3rd)
	V-by-One®HS_D[7]	RAW[7] (5th)	R[7] (1st)	R[4] (1st)	G[2] (3rd)	RAW[9] (1st)	RAW[9] (3rd)	RAW[5] (3rd)
	V-by-One®HS_D[6]	RAW[6] (5th)	R[6] (1st)	R[3] (1st)	G[1] (3rd)	RAW[8] (1st)	RAW[8] (3rd)	RAW[4] (3rd)
	V-by-One®HS_D[5]	RAW[5] (5th)	R[5] (1st)	R[2] (1st)	G[0] (3rd)	RAW[7] (1st)	RAW[7] (3rd)	RAW[3] (3rd)
	V-by-One®HS_D[4]	RAW[4] (5th)	R[4] (1st)	R[1] (1st)	R[4] (3rd)	RAW[6] (1st)	RAW[6] (3rd)	RAW[2] (3rd)
	V-by-One®HS_D[3]	RAW[3] (5th)	R[3] (1st)	R[0] (1st)	R[3] (3rd)	RAW[5] (1st)	RAW[5] (3rd)	RAW[1] (3rd)
	V-by-One®HS_D[2]	RAW[2] (5th)	R[2] (1st)	0	R[2] (3rd)	RAW[4] (1st)	RAW[4] (3rd)	RAW[0] (3rd)
	V-by-One®HS_D[1]	RAW[1] (5th)	R[1] (1st)	0	R[1] (3rd)	RAW[3] (1st)	RAW[3] (3rd)	0
	V-by-One®HS_D[0]	RAW[0] (5th)	R[0] (1st)	0	R[0] (3rd)	RAW[2] (1st)	RAW[2] (3rd)	0
TX1P/N V-by-One® HS lane1	V-by-One®HS_D[31]	RAW[7] (4th)	-	-	B[4] (2nd)	-	0	0
	V-by-One®HS_D[30]	RAW[6] (4th)	-	-	B[3] (2nd)	-	0	0
	V-by-One®HS_D[29]	RAW[5] (4th)	-	-	B[2] (2nd)	-	0	0
	V-by-One®HS_D[28]	RAW[4] (4th)	-	-	B[1] (2nd)	-	0	0
	V-by-One®HS_D[27]	RAW[3] (4th)	-	-	B[0] (2nd)	-	0	RAW[9] (2nd)
	V-by-One®HS_D[26]	RAW[2] (4th)	-	-	G[5] (2nd)	-	0	RAW[8] (2nd)
	V-by-One®HS_D[25]	RAW[1] (4th)	-	-	G[4] (2nd)	-	RAW[1] (2nd)	RAW[7] (2nd)
	V-by-One®HS_D[24]	RAW[0] (4th)	-	-	G[3] (2nd)	-	RAW[0] (2nd)	RAW[6] (2nd)
	V-by-One®HS_D[23]	RAW[7] (3rd)	B[7] (2nd)	B[4] (2nd)	G[2] (2nd)	0	RAW[9] (2nd)	RAW[5] (2nd)
	V-by-One®HS_D[22]	RAW[6] (3rd)	B[6] (2nd)	B[3] (2nd)	G[1] (2nd)	0	RAW[8] (2nd)	RAW[4] (2nd)
	V-by-One®HS_D[21]	RAW[5] (3rd)	B[5] (2nd)	B[2] (2nd)	G[0] (2nd)	0	RAW[7] (2nd)	RAW[3] (2nd)
	V-by-One®HS_D[20]	RAW[4] (3rd)	B[4] (2nd)	B[1] (2nd)	R[4] (2nd)	0	RAW[6] (2nd)	RAW[2] (2nd)
	V-by-One®HS_D[19]	RAW[3] (3rd)	B[3] (2nd)	B[0] (2nd)	R[3] (2nd)	0	RAW[5] (2nd)	RAW[1] (2nd)
	V-by-One®HS_D[18]	RAW[2] (3rd)	B[2] (2nd)	0	R[2] (2nd)	0	RAW[4] (2nd)	RAW[0] (2nd)
	V-by-One®HS_D[17]	RAW[1] (3rd)	B[1] (2nd)	0	R[1] (2nd)	0	RAW[3] (2nd)	0
	V-by-One®HS_D[16]	RAW[0] (3rd)	B[0] (2nd)	0	R[0] (2nd)	0	RAW[2] (2nd)	0
	V-by-One®HS_D[15]	RAW[7] (8th)	G[7] (2nd)	G[5] (2nd)	B[4] (4th)	0	0	0
	V-by-One®HS_D[14]	RAW[6] (8th)	G[6] (2nd)	G[4] (2nd)	B[3] (4th)	0	0	0
	V-by-One®HS_D[13]	RAW[5] (8th)	G[5] (2nd)	G[3] (2nd)	B[2] (4th)	0	0	0
	V-by-One®HS_D[12]	RAW[4] (8th)	G[4] (2nd)	G[2] (2nd)	B[1] (4th)	0	0	0
	V-by-One®HS_D[11]	RAW[3] (8th)	G[3] (2nd)	G[1] (2nd)	B[0] (4th)	0	0	RAW[9] (4th)
	V-by-One®HS_D[10]	RAW[2] (8th)	G[2] (2nd)	G[0] (2nd)	G[5] (4th)	0	0	RAW[8] (4th)
	V-by-One®HS_D[9]	RAW[1] (8th)	G[1] (2nd)	0	G[4] (4th)	RAW[1] (2nd)	RAW[1] (4th)	RAW[7] (4th)
	V-by-One®HS_D[8]	RAW[0] (8th)	G[0] (2nd)	0	G[3] (4th)	RAW[0] (2nd)	RAW[0] (4th)	RAW[6] (4th)
	V-by-One®HS_D[7]	RAW[7] (7th)	R[7] (2nd)	R[4] (2nd)	G[2] (4th)	RAW[9] (2nd)	RAW[9] (4th)	RAW[5] (4th)
	V-by-One®HS_D[6]	RAW[6] (7th)	R[6] (2nd)	R[3] (2nd)	G[1] (4th)	RAW[8] (2nd)	RAW[8] (4th)	RAW[4] (4th)
	V-by-One®HS_D[5]	RAW[5] (7th)	R[5] (2nd)	R[2] (2nd)	G[0] (4th)	RAW[7] (2nd)	RAW[7] (4th)	RAW[3] (4th)
	V-by-One®HS_D[4]	RAW[4] (7th)	R[4] (2nd)	R[1] (2nd)	R[4] (4th)	RAW[6] (2nd)	RAW[6] (4th)	RAW[2] (4th)
	V-by-One®HS_D[3]	RAW[3] (7th)	R[3] (2nd)	R[0] (2nd)	R[3] (4th)	RAW[5] (2nd)	RAW[5] (4th)	RAW[1] (4th)
	V-by-One®HS_D[2]	RAW[2] (7th)	R[2] (2nd)	0	R[2] (4th)	RAW[4] (2nd)	RAW[4] (4th)	RAW[0] (4th)
	V-by-One®HS_D[1]	RAW[1] (7th)	R[1] (2nd)	0	R[1] (4th)	RAW[3] (2nd)	RAW[3] (4th)	0
	V-by-One®HS_D[0]	RAW[0] (7th)	R[0] (2nd)	0	R[0] (4th)	RAW[2] (2nd)	RAW[2] (4th)	0

Table 9. V-by-One® HS 2lane output data mapping format 3/3

	R_OUTPUT_FMT	5			6		7	
	R_HFSEL	0	1		-	-	-	-
	R_BITMAP_SEL	0	0	1	0	2	0	1
	default V-by-One®HS Byte Mode	3	4	4	3	3	3	3
	Format Name	RAW12	RAW12HF Map1	RAW12HF Map2	RAW10HF2 Map1	RAW10HF2 Map3	RAW12HF2 Map1	RAW12HF2 Map2
TX0P/N V-by-One® HS lane0	V-by-One®HS_D[31]	-	0	0	-	-	-	-
	V-by-One®HS_D[30]	-	0	0	-	-	-	-
	V-by-One®HS_D[29]	-	0	0	-	-	-	-
	V-by-One®HS_D[28]	-	0	0	-	-	-	-
	V-by-One®HS_D[27]	-	RAW[3] (1st)	RAW[11] (1st)	-	-	-	-
	V-by-One®HS_D[26]	-	RAW[2] (1st)	RAW[10] (1st)	-	-	-	-
	V-by-One®HS_D[25]	-	RAW[1] (1st)	RAW[9] (1st)	-	-	-	-
	V-by-One®HS_D[24]	-	RAW[0] (1st)	RAW[8] (1st)	-	-	-	-
	V-by-One®HS_D[23]	0	RAW[11] (1st)	RAW[7] (1st)	0	RAW[9] (1st)	RAW[3] (1st)	RAW[11] (1st)
	V-by-One®HS_D[22]	0	RAW[10] (1st)	RAW[6] (1st)	0	RAW[8] (1st)	RAW[2] (1st)	RAW[10] (1st)
	V-by-One®HS_D[21]	0	RAW[9] (1st)	RAW[5] (1st)	RAW[1] (1st)	RAW[7] (1st)	RAW[1] (1st)	RAW[9] (1st)
	V-by-One®HS_D[20]	0	RAW[8] (1st)	RAW[4] (1st)	RAW[0] (1st)	RAW[6] (1st)	RAW[0] (1st)	RAW[8] (1st)
	V-by-One®HS_D[19]	0	RAW[7] (1st)	RAW[3] (1st)	RAW[9] (1st)	RAW[5] (1st)	RAW[11] (1st)	RAW[7] (1st)
	V-by-One®HS_D[18]	0	RAW[6] (1st)	RAW[2] (1st)	RAW[8] (1st)	RAW[4] (1st)	RAW[10] (1st)	RAW[6] (1st)
	V-by-One®HS_D[17]	0	RAW[5] (1st)	RAW[1] (1st)	RAW[7] (1st)	RAW[3] (1st)	RAW[9] (1st)	RAW[5] (1st)
	V-by-One®HS_D[16]	0	RAW[4] (1st)	RAW[0] (1st)	RAW[6] (1st)	RAW[2] (1st)	RAW[8] (1st)	RAW[4] (1st)
	V-by-One®HS_D[15]	0	0	0	RAW[5] (1st)	RAW[1] (1st)	RAW[7] (1st)	RAW[3] (1st)
	V-by-One®HS_D[14]	0	0	0	RAW[4] (1st)	RAW[0] (1st)	RAW[6] (1st)	RAW[2] (1st)
	V-by-One®HS_D[13]	0	0	0	RAW[3] (1st)	0	RAW[5] (1st)	RAW[1] (1st)
	V-by-One®HS_D[12]	0	0	0	RAW[2] (1st)	0	RAW[4] (1st)	RAW[0] (1st)
	V-by-One®HS_D[11]	RAW[3] (1st)	RAW[3] (3rd)	RAW[11] (3rd)	0	RAW[9] (3rd)	RAW[3] (3rd)	RAW[11] (3rd)
	V-by-One®HS_D[10]	RAW[2] (1st)	RAW[2] (3rd)	RAW[10] (3rd)	0	RAW[8] (3rd)	RAW[2] (3rd)	RAW[10] (3rd)
	V-by-One®HS_D[9]	RAW[1] (1st)	RAW[1] (3rd)	RAW[9] (3rd)	RAW[1] (3rd)	RAW[7] (3rd)	RAW[1] (3rd)	RAW[9] (3rd)
	V-by-One®HS_D[8]	RAW[0] (1st)	RAW[0] (3rd)	RAW[8] (3rd)	RAW[0] (3rd)	RAW[6] (3rd)	RAW[0] (3rd)	RAW[8] (3rd)
	V-by-One®HS_D[7]	RAW[11] (1st)	RAW[11] (3rd)	RAW[7] (3rd)	RAW[9] (3rd)	RAW[5] (3rd)	RAW[11] (3rd)	RAW[7] (3rd)
	V-by-One®HS_D[6]	RAW[10] (1st)	RAW[10] (3rd)	RAW[6] (3rd)	RAW[8] (3rd)	RAW[4] (3rd)	RAW[10] (3rd)	RAW[6] (3rd)
	V-by-One®HS_D[5]	RAW[9] (1st)	RAW[9] (3rd)	RAW[5] (3rd)	RAW[7] (3rd)	RAW[3] (3rd)	RAW[9] (3rd)	RAW[5] (3rd)
	V-by-One®HS_D[4]	RAW[8] (1st)	RAW[8] (3rd)	RAW[4] (3rd)	RAW[6] (3rd)	RAW[2] (3rd)	RAW[8] (3rd)	RAW[4] (3rd)
	V-by-One®HS_D[3]	RAW[7] (1st)	RAW[7] (3rd)	RAW[3] (3rd)	RAW[5] (3rd)	RAW[1] (3rd)	RAW[7] (3rd)	RAW[3] (3rd)
	V-by-One®HS_D[2]	RAW[6] (1st)	RAW[6] (3rd)	RAW[2] (3rd)	RAW[4] (3rd)	RAW[0] (3rd)	RAW[6] (3rd)	RAW[2] (3rd)
	V-by-One®HS_D[1]	RAW[5] (1st)	RAW[5] (3rd)	RAW[1] (3rd)	RAW[3] (3rd)	0	RAW[5] (3rd)	RAW[1] (3rd)
	V-by-One®HS_D[0]	RAW[4] (1st)	RAW[4] (3rd)	RAW[0] (3rd)	RAW[2] (3rd)	0	RAW[4] (3rd)	RAW[0] (3rd)
TX1P/N V-by-One® HS lane1	V-by-One®HS_D[31]	-	0	0	-	-	-	-
	V-by-One®HS_D[30]	-	0	0	-	-	-	-
	V-by-One®HS_D[29]	-	0	0	-	-	-	-
	V-by-One®HS_D[28]	-	0	0	-	-	-	-
	V-by-One®HS_D[27]	-	RAW[3] (2nd)	RAW[11] (2nd)	-	-	-	-
	V-by-One®HS_D[26]	-	RAW[2] (2nd)	RAW[10] (2nd)	-	-	-	-
	V-by-One®HS_D[25]	-	RAW[1] (2nd)	RAW[9] (2nd)	-	-	-	-
	V-by-One®HS_D[24]	-	RAW[0] (2nd)	RAW[8] (2nd)	-	-	-	-
	V-by-One®HS_D[23]	0	RAW[11] (2nd)	RAW[7] (2nd)	0	RAW[9] (2nd)	RAW[3] (2nd)	RAW[11] (2nd)
	V-by-One®HS_D[22]	0	RAW[10] (2nd)	RAW[6] (2nd)	0	RAW[8] (2nd)	RAW[2] (2nd)	RAW[10] (2nd)
	V-by-One®HS_D[21]	0	RAW[9] (2nd)	RAW[5] (2nd)	RAW[1] (2nd)	RAW[7] (2nd)	RAW[1] (2nd)	RAW[9] (2nd)
	V-by-One®HS_D[20]	0	RAW[8] (2nd)	RAW[4] (2nd)	RAW[0] (2nd)	RAW[6] (2nd)	RAW[0] (2nd)	RAW[8] (2nd)
	V-by-One®HS_D[19]	0	RAW[7] (2nd)	RAW[3] (2nd)	RAW[9] (2nd)	RAW[5] (2nd)	RAW[11] (2nd)	RAW[7] (2nd)
	V-by-One®HS_D[18]	0	RAW[6] (2nd)	RAW[2] (2nd)	RAW[8] (2nd)	RAW[4] (2nd)	RAW[10] (2nd)	RAW[6] (2nd)
	V-by-One®HS_D[17]	0	RAW[5] (2nd)	RAW[1] (2nd)	RAW[7] (2nd)	RAW[3] (2nd)	RAW[9] (2nd)	RAW[5] (2nd)
	V-by-One®HS_D[16]	0	RAW[4] (2nd)	RAW[0] (2nd)	RAW[6] (2nd)	RAW[2] (2nd)	RAW[8] (2nd)	RAW[4] (2nd)
	V-by-One®HS_D[15]	0	0	0	RAW[5] (2nd)	RAW[1] (2nd)	RAW[7] (2nd)	RAW[3] (2nd)
	V-by-One®HS_D[14]	0	0	0	RAW[4] (2nd)	RAW[0] (2nd)	RAW[6] (2nd)	RAW[2] (2nd)
	V-by-One®HS_D[13]	0	0	0	RAW[3] (2nd)	0	RAW[5] (2nd)	RAW[1] (2nd)
	V-by-One®HS_D[12]	0	0	0	RAW[2] (2nd)	0	RAW[4] (2nd)	RAW[0] (2nd)
	V-by-One®HS_D[11]	RAW[3] (2nd)	RAW[3] (4th)	RAW[11] (4th)	0	RAW[9] (4th)	RAW[3] (4th)	RAW[11] (4th)
	V-by-One®HS_D[10]	RAW[2] (2nd)	RAW[2] (4th)	RAW[10] (4th)	0	RAW[8] (4th)	RAW[2] (4th)	RAW[10] (4th)
	V-by-One®HS_D[9]	RAW[1] (2nd)	RAW[1] (4th)	RAW[9] (4th)	RAW[1] (4th)	RAW[7] (4th)	RAW[1] (4th)	RAW[9] (4th)
	V-by-One®HS_D[8]	RAW[0] (2nd)	RAW[0] (4th)	RAW[8] (4th)	RAW[0] (4th)	RAW[6] (4th)	RAW[0] (4th)	RAW[8] (4th)
	V-by-One®HS_D[7]	RAW[11] (2nd)	RAW[11] (4th)	RAW[7] (4th)	RAW[9] (4th)	RAW[5] (4th)	RAW[11] (4th)	RAW[7] (4th)
	V-by-One®HS_D[6]	RAW[10] (2nd)	RAW[10] (4th)	RAW[6] (4th)	RAW[8] (4th)	RAW[4] (4th)	RAW[10] (4th)	RAW[6] (4th)
	V-by-One®HS_D[5]	RAW[9] (2nd)	RAW[9] (4th)	RAW[5] (4th)	RAW[7] (4th)	RAW[3] (4th)	RAW[9] (4th)	RAW[5] (4th)
	V-by-One®HS_D[4]	RAW[8] (2nd)	RAW[8] (4th)	RAW[4] (4th)	RAW[6] (4th)	RAW[2] (4th)	RAW[8] (4th)	RAW[4] (4th)
	V-by-One®HS_D[3]	RAW[7] (2nd)	RAW[7] (4th)	RAW[3] (4th)	RAW[5] (4th)	RAW[1] (4th)	RAW[7] (4th)	RAW[3] (4th)
	V-by-One®HS_D[2]	RAW[6] (2nd)	RAW[6] (4th)	RAW[2] (4th)	RAW[4] (4th)	RAW[0] (4th)	RAW[6] (4th)	RAW[2] (4th)
	V-by-One®HS_D[1]	RAW[5] (2nd)	RAW[5] (4th)	RAW[1] (4th)	RAW[3] (4th)	0	RAW[5] (4th)	RAW[1] (4th)
	V-by-One®HS_D[0]	RAW[4] (2nd)	RAW[4] (4th)	RAW[0] (4th)	RAW[2] (4th)	0	RAW[4] (4th)	RAW[0] (4th)

6.5.3 V-by-One® HS output Byte mode

Setting of V-by-One® HS output Byte mode follows format setting or register control.

When V-by-One® HS Self Pattern Generator (BIST) is active, R_BISTEN=1:Enable, Byte mode is 3Byte fixed.

Table 10. V-by-One® HS output Byte mode setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1036	[0]	R_COL_SEL	1	R/W	V-by-One® HS COL (COLor depth) Byte mode setting method 0:AUTO (COL_FMT defined by output format setting) 1:Manual (R_COL_MAN)	1'h0
0x1037	[5:4]	R_COL_MAN[1:0]	2	R/W	V-by-One® HS Manual Color Depth Select 00 : Reserved 01 : 8bit (3Byte mode) 10 : 10bit (4Byte mode) 11 : Reserved	2'h2

6.5.4 V-by-One® HS output Distribution mode

Output of V-by-One® HS lane0 is duplicated and distributed to lane1 output. When Distribution mode is Enabled, R_HTPDN_SEL, R_LOCKN0_SEL and R_LOCKN1_SEL are supposed to be set properly.

Table 11. V-by-One® HS output Distribution mode setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1053	[0]	R_DIST_EN	1	R/W	V-by-One® HS Distribution mode Enable 0:Disable 1:Enable	1'h0

6.5.5 V-by-One® HS Low Radiation Emission or High Immunity Resistance mode

V-by-One® HS Low Radiation Emission and High Immunity Resistance mode are available.

Immunity resistance strength is HS (2'b11) > HS (2'b10).

Radiated emission level is HS (2'b11) > HS (2'b10).

Table 12. V-by-One® HS Low Radiation Emission or High Immunity Resistance mode setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x101B	[5:4]	R_NHSEL	2	R/W	V-by-One® HS setting 00 : Reserved 01 : Reserved 10 : V-by-One® HS standard Low Radiation Emission mode 11 : V-by-One® HS standard High Immunity Resistance mode	2'h3

6.5.6 V-by-One® HS output Odd/Even swap

V-by-One® HS Odd/Even pixel assignment to output lane is adjustable.

Table 13. V-by-One® HS output Odd/Even swap setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1052	[0]	R_ML_OE_SWAP	1	R/W	V-by-One® HS 1st Pixel Start Timing Select 0:1st pixel assign on lane0 1:1st pixel assign on lane1	1'h0

6.5.7 V-by-One® HS output Drivability

V-by-One® HS driver emphasis and strength controls are adjustable.

Table 14. V-by-One® HS output Drivability setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1020	[7:6]	R_ML0_PRE	2	R/W	[VbyOne Transmitter] Pre-Emphasis ・when R_ML0_DRV=0 00:0% 10:100% ・when R_ML0_DRV=1 00:0% 01:50%	2'h0
0x1020	[5:4]	R_ML1_PRE	2	R/W	[VbyOne Transmitter] Pre-Emphasis ・when R_ML1_DRV=0 00:0% 10:100% ・when R_ML1_DRV=1 00:0% 01:50%	2'h0
0x1020	[3:2]	R_ML0_DRV	2	R/W	[VbyOne Transmitter] Drive Strength Select 00: VTOD=200mV 01: VTOD=300mV 10: VTOD=400mV	2'h2
0x1020	[1:0]	R_ML1_DRV	2	R/W	[VbyOne Transmitter] Drive Strength Select 00: VTOD=200mV 01: VTOD=300mV 10: VTOD=400mV	2'h2

6.5.8 V-by-One® HS output Low Frequency mode

V-by-One® HS Low Frequency Mode is available. For usage of Low Frequency mode, counterpart V-by-One® receiver must have installed Low Frequency mode format decoder like THCV236-Q.

Table 15. V-by-One® HS Low Frequency Mode setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x101B	[0]	R_LFQEN	1	R/W	V-by-One® HS Low FeqModeEnable 0:Normal 1:Low Frequency Mode	1'h0

6.5.9 Target Pixel clock

Target pixel clock for transmission is defined by a formula below.

Relationship between used packet and byte mode packet transfer potential is determined by output format (from Table 4) and whether Auto or Manual Byte-mode setting is used or not in Byte-mode setting (Table 10).

[dmp] = MIPI Data-rate

[nmp] = MIPI lane number

[bmvx1] = V-by-One® HS Byte Mode

[nvx1] = V-by-One® HS lane number

[PCLK.target] = Pixel clock target for V-by-One® HS per lane = [F(target)]

$$\text{Total pixel data-rate} = [\text{dmp}] \times [\text{nmp}]$$

$$= [\text{PCLK.target}] \times [\text{bmvx1}] \times 8 \times \frac{\text{Used packet in output format}}{\text{Byte mode packet total}} \times [\text{nvx1}]$$

$$[\text{PCLK.target}] = \frac{[\text{dmp}] \times [\text{nmp}]}{[\text{bmvx1}] \times 8 \times \dfrac{\text{Used packet in output format}}{\text{Byte mode packet total}} \times [\text{nvx1}]} = [\text{F(target)}]$$

6.6 Blanking period restriction under low MIPI data-rate environment

First of all, horizontal blanking period must meet minimum required length as MIPI standard defines to change MIPI data lane from Low Power mode to High Speed mode and from High Speed mode to Low Power mode.

In addition for THCV241A, when MIPI data-rate per lane is slower than 160Mbps, horizontal blanking period length must meet below rule.

$$\text{Horizontal blanking period (@[dmp]<160Mbps)} > \frac{168}{[\text{dmp}]}$$

Another alternative is simply to use 160Mbps and higher MIPI data-rate because cases to use below 160Mbps must be the cases of [nmp]=4 so that MIPI data-rate can be arranged to be higher by using [nmp]=1 or 2 configuration.

6.7 PLL setting

PLL setting is required. For manual setting, R_PLL_SET_MODE is supposed to be set 1 (Manual mode) from default value 0. PLL Manual mode setting set R_PLL_SETTING[47:0] is related with CKI frequency.

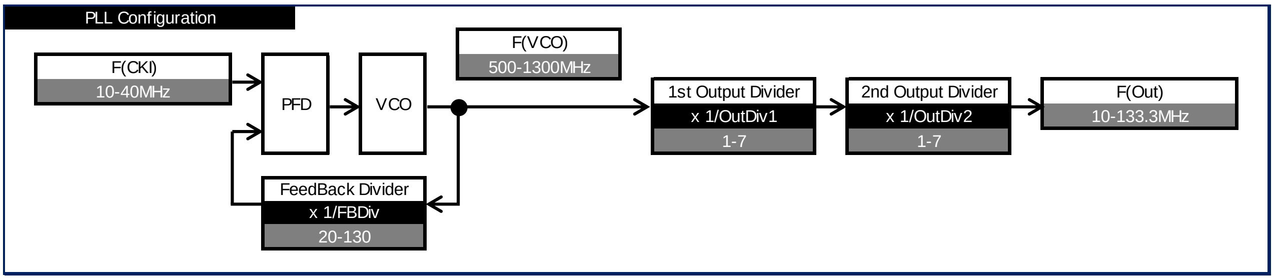


Figure 5. Reference clock supply basic method

PLL_SETTING[47:0] must be selected proper to meet below constraints.

Table 16. PLL constraints table

symbol	discription	condition	min	typ	max	unit
F(CKI)	CKI input frequency	-	10	-	40	MHz
FBDiv	FeedBack Divider value	-	20	-	130	-
OutDiv1	1st Output Divider value (OutDiv1 must be >= OutDiv2)	-	1	-	7	-
OutDiv2	2nd Output Divider value (OutDiv1 must be >= OutDiv2)	-	1	-	7	-
F(VCO)	VCO frequency	-	500	-	1300	MHz
F(OUT)	PLL output pixel clock frequency	-	10	-	133.3	MHz
ΔF	Allowed error between F(target) vs F(OUT)	Hactive=< 1280pixels and [dmp]x[nmp] < 500Mbps 1280 <Hactive=< 1920pixels and [dmp]x[nmp] < 800Mbps 1920 <Hactive=< 3840pixels and [dmp]x[nmp] <1500Mbps	|R_SPREAD|	-	8	%
		otherwise	0	0	8	%

Pixel clock frequency made by PLL is calculated as below.

[PCLK.actual] = Pixel clock actually used for V-by-One® HS per lane = [F(OUT)]

$$[\text{PCLK.actual}] = [\text{F(OUT)}] = \frac{[\text{F(CKI)}] \times [\text{FBDiv}]}{[\text{OutDiv1}] \times [\text{OutDiv2}]}$$

Actual Pixel clock, F(OUT) frequency must be equal or greater than ideal target Pixel clock, F(target) by 8% accuracy as below formula for most cases.

$$[\text{F(target)}] =< [\text{F(OUT)}] =< [\text{F(target)}] \times \frac{108}{100}$$

When transmitted camera image format horizontal active is rather large and total pixel data-rate is rather slow as described in previous table condition, minimum allowed F(OUT) setting is not equal to F(target) if Spread Spectrum function is activated. ΔF is supposed to be more than absolute value of applied SSCG modulation rate, |R_SPREAD|, under the condition specified on PLL constraints table.

$$\Delta F = \frac{[F(OUT)] - [F(target)]}{[F(target)]}$$

Table 17. PLL setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x100F	[0]	R_PLL_SET_MODE	1	R/W	PLL setting mode 0:PLL Auto setting mode 1:PLL Manual setting mode	1'h0
0x1011	[7:0]	R_PLL_SETTING[47:40]	8	R/W	PLL setting value, Feedback Divider value (integer part)	8'h00
0x1012	[7:0]	R_PLL_SETTING[39:32]	8	R/W	PLL setting value, Feedback Divider value (decimal part MSB)	8'h00
0x1013	[7:0]	R_PLL_SETTING[31:24]	8	R/W	PLL setting value, Feedback Divider value (decimal part)	8'h00
0x1014	[7:0]	R_PLL_SETTING[23:16]	8	R/W	PLL setting value, Feedback Divider value (decimal part LSB)	8'h00
0x1015	[7]	R_PLL_SETTING[15]	1	R/W	PLL setting value	1'h0
0x1015	[6:4]	R_PLL_SETTING[14:12]	3	R/W	PLL setting value, OutDiv1 (OutDiv1 must be >= OutDiv2)	3'h0
0x1015	[3]	R_PLL_SETTING[11]	1	R/W	PLL setting value	1'h0
0x1015	[2:0]	R_PLL_SETTING[10:8]	3	R/W	PLL setting value, OutDiv2 (OutDiv1 must be >= OutDiv2)	3'h0
0x1016	[7:0]	R_PLL_SETTING[7:0]	8	R/W	PLL setting value, Reserved (must be set to 8'h01)	8'h00

Below Table 18 is Look Up Table for typical cases.

Table 18. PLL setting Look Up Table

index	condition	input	output	f_CKI (MHz)	PLL[47:40]	PLL[39:32]	PLL[31:24]	PLL[23:16]	PLL[15:8]	PLL[7:0]
1	720p30fps RAW	594Mbps x1lane	1lane MPRF	27	0x18	0xC0	0x00	0x00	0x66	0x01
2				37.125	0x15	0x00	0x00	0x00	0x76	0x01
3	720p30fps YUV422	600Mbps x1lane	1lane MPRF	24	0x1C	0x20	0x00	0x00	0x66	0x01
4	720p60fps RAW	445.5Mbps x2lane	1lane MPRF	27	0x25	0x20	0x00	0x00	0x66	0x01
5	1080p30fps RAW			37.125	0x1B	0x00	0x00	0x00	0x66	0x01
6	720p60fps YUV422	594Mbps x2lane	1lane MPRF	27	0x21	0x00	0x00	0x00	0x64	0x01
7	1080p30fps YUV422			37.125	0x18	0x00	0x00	0x00	0x64	0x01
8	720p120fps RAW	891Mbps x2lane	1lane MPRF	27	0x21	0x00	0x00	0x00	0x44	0x01
9	1080p60fps RAW			37.125	0x18	0x00	0x00	0x00	0x44	0x01
10	720p120fps YUV422	594Mbps x4lane	1lane MPRF	27	0x2C	0x00	0x00	0x00	0x44	0x01
11	1080p60fps YUV422			37.125	0x20	0x00	0x00	0x00	0x44	0x01
12	1080p120fps RAW	891Mbps x4lane	2lane MPRF	27	0x21	0x00	0x00	0x00	0x44	0x01
13				37.125	0x18	0x00	0x00	0x00	0x44	0x01
14	1080p120fps YUV422	1200Mbps x4lane	2lane MPRF	24	0x32	0x00	0x00	0x00	0x44	0x01
15	720p30fps RAW	594Mbps x1lane	1lane RAW12HF Map2	27	0x21	0x00	0x00	0x00	0x66	0x01
16				37.125	0x18	0x00	0x00	0x00	0x66	0x01
17	720p30fps YUV422	600Mbps x1lane	1lane YUV422 Map1(4Byte) forced 4Byte	24	0x19	0x00	0x00	0x00	0x44	0x01
18	720p60fps RAW	445.5Mbps x2lane	1lane RAW12HF Map2	27	0x21	0x00	0x00	0x00	0x64	0x01
19	1080p30fps RAW			37.125	0x18	0x00	0x00	0x00	0x64	0x01
20	720p60fps YUV422	594Mbps x2lane	1lane YUV422 Map1(4Byte) forced 4Byte	27	0x2C	0x00	0x00	0x00	0x44	0x01
21	1080p30fps YUV422			37.125	0x20	0x00	0x00	0x00	0x44	0x01
22	720p120fps RAW	891Mbps x2lane	1lane RAW12HF Map2	27	0x2C	0x00	0x00	0x00	0x44	0x01
23	1080p60fps RAW			37.125	0x20	0x00	0x00	0x00	0x44	0x01
24	720p120fps YUV422	594Mbps x4lane	1lane YUV422HF Map1	27	0x2C	0x00	0x00	0x00	0x44	0x01
25	1080p60fps YUV422			37.125	0x20	0x00	0x00	0x00	0x44	0x01
26	1080p120fps RAW	891Mbps x4lane	2lane RAW12HF Map2	27	0x2C	0x00	0x00	0x00	0x44	0x01
27				37.125	0x20	0x00	0x00	0x00	0x44	0x01
28	1080p120fps YUV422	1200Mbps x4lane	2lane YUV422HF Map1	24	0x32	0x00	0x00	0x00	0x44	0x01

6.8 PLL Auto setting function

PLL auto setting function is available in case all the following conditions are met.

- ✓ V-by-One® HS output format setting (Address 0x1001) is MPRF.
- ✓ F(CKI) is 37.125MHz or 27MHz or 24MHz.
- ✓ MIPI input data-rate is equal to the integral multiple of F(CKI)

Under PLL auto setting function operation, it is sufficient only to control below resistors. No control on R_PLL_SETTING[47:0] is required.

Table 19. PLL Auto setting function control Resistors

Addr(h)	Bits	Register	width	R/W	Description	Default
0x100F	[0]	R_PLL_SET_MODE	1	R/W	PLL setting mode 0:PLL Auto setting mode 1:PLL Manual setting mode	1'h0
0x100E	[7:6]	R_CKI_FREQ	2	R/W	PLL Auto setting input frequency choice 2'h0: Reserved 2'h1: 37.125MHz 2'h2: 27MHz 2'h3: 24MHz	2'h0
0x100E	[5:0]	R_MIPI_MULT	6	R/W	PLL Auto setting multiplying ratio MIPI data-rate vs. F(CKI) Below formula must be met to application condition. MIPI Data-rate = F(CKI) *(R_MIPI_MULT+1)	6'hF
0x1000	[0]	R_VX1_LANE	1	R/W	See other Table for detail description	1'h1
0x1001	[6:4]	R_OUTPUT_FMT	3	R/W	Setting value 000:MPRF is required for PLL Auto setting function. See other Table for detail description	3'h0
0x1002	[5]	R_HFSEL	1	R/W	See other Table for detail description	1'h0
0x102D	[1:0]	R_RX_LANE_SEL_EN	2	R/W	See other Table for detail description	2'h3

If above PLL Auto setting control values are invalid and unmatched to application condition, C_PLL_SET_NG indicator is asserted.

Table 20. PLL Auto setting control invalid Indicator

Addr(h)	Bits	Register	width	R/W	Description	Default
0x112F	[0]	C_PLL_SET_NG	1	R	PLL Auto Setting control invalid indicator 0: PLL Auto Setting control valid or PLL Manual setting mode 1: PLL Auto Setting control invalid	-

6.9 V-by-One® HS output data-rate

V-by-One® HS output data-rate is made of actual Pixel clock frequency.

$$\text{V-by-One® HS physical Data-rate} = [\text{PCLK.actual}] \times [\text{bmvx1}] \times 8 \times \frac{10}{8}$$

At Low Frequency Mode, Data-rate is doubled.

$$\text{V-by-One® HS physical Data-rate on LowFreq.Mode} = [\text{PCLK.actual}] \times [\text{bmvx1}] \times 8 \times \frac{10}{8} \times 2$$

Supported Data-rate is from 400Mbps to 4Gbps.

6.10 V-by-One® HS output Spread Spectrum

Spread Spectrum Clock Generation (SSCG) modulation is available to apply on V-by-One® HS output.

$$[\text{PCLK.actual}]\,|_{\text{no SSCG}} \times \frac{(100 - |[\text{R\_SPREAD}]|)}{100} < [\text{PCLK.actual}]\,|_{\text{SSCG}} < [\text{PCLK.actual}]\,|_{\text{no SSCG}} \times \frac{(100 + |[\text{R\_SPREAD}]|)}{100}$$

Table 21. V-by-One® HS output Spread Spectrum settings

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1010	[7:4]	R_DIVVAL	4	R/W	SSCG modulation frequency setting fmod = F(CKI) / (128*R_DIVVAL)	4'h0
0x1019	[3:0]	R_SPREAD	4	R/W	SSCG modulation rate setting 4'h0 : modulation rate =0, 4'h1 : modulation rate =+/-0.1%, 4'h2 : modulation rate =+/-0.2%, …, 4'h5 : modulation rate =+/-0.5%, …, 4'hF : modulation rate =+/-1.5%	4'h3
0x101A	[0]	R_DISABLE_SSCG	1	R/W	SSCG modulation Enable/Disable setting 0:Enable 1:Disable	1'h1

SSCG modulation frequency divider setting values, R_DIVVAL on Address 0x1010, to meet V-by-One® HS standard 30kHz +/-0.5% are exemplified below.

Table 22. V-by-One® HS output SSCG R_DIVVAL setting examples

(MHz)	(hex.)	(dec.)	(kHz)
F(CKI)	R_DIVVAL	R_DIVVAL	fmod
37.125	4'hC(0xC)	12	24.2
27	4'h8(0x8)	8	26.4
24	4'h8(0x8)	8	23.4

6.11 V-by-One® HS CRC

V-by-One® HS transmission packet payload fault or error can be detected with CRC. THCV241A generates and sends check value to receiver. For usage of CRC function, the counterpart V-by-One® receiver must have installed CRC monitor like THCV242.

Table 23. V-by-One® HS CRC setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1054	[0]	R_CRC_OFF	1	R/W	V-by-One® HS CRC generator ON/OFF (ON default) 0:CRC output ON 1:CRC output OFF	1'h0

6.12 MIPI Packet Header V-by-One® HS output bridge mode

MIPI PH(Packet Header) can be bridge to V-by-One® HS output following selected schemes.

"R_PHMODE=2'b01" setting on THCV236-Q connection is only supported where HFSEL=0 setting is applied on THCV236-Q.

Table 24. V-by-One® HS output MIPI Packet Header bridge setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1001	[1:0]	R_PHMODE	2	R/W	V-by-One® HS output MIPI PH(Packet Header) timing setting 00:PH in normal data packet just after DE rise (THCV242-Q default) 01:PH in CTL packet of blanking period till 1pixel before DE rise 10,11:no PH	2'h0

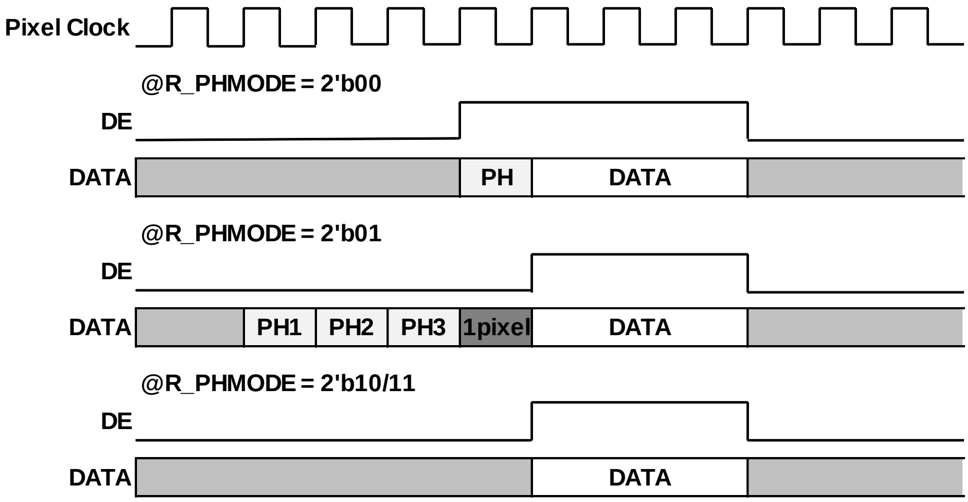


Figure 6. MIPI Packet Header V-by-One® HS output bridge timing alternative

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MIPI PH	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0
Vx1 PH *CTL packet	V-by-One®HS_D[31]*	V-by-One®HS_D[30]*	V-by-One®HS_D[29]*	V-by-One®HS_D[28]*	V-by-One®HS_D[27]*	V-by-One®HS_D[26]*	V-by-One®HS_D[25]*	V-by-One®HS_D[24]*	V-by-One®HS_D[23]*	V-by-One®HS_D[22]*	V-by-One®HS_D[21]*	V-by-One®HS_D[20]*	V-by-One®HS_D[19]*	V-by-One®HS_D[18]*	V-by-One®HS_D[17]*	V-by-One®HS_D[16]*
THCV236 HFSEL=0	THCV236 D[31]*	THCV236 D[30]*	THCV236 D[29]*	THCV236 D[28]*	THCV236 D[27]*	THCV236 D[26]*	THCV236 D[25]*	THCV236 D[24]*	THCV236 D[23]*	THCV236 D[22]*	THCV236 D[21]*	THCV236 D[20]*	THCV236 D[19]*	THCV236 D[18]*	THCV236 D[17]*	THCV236 D[16]*
PH 4byte	ECC7	ECC6	ECC5	ECC4	ECC3	ECC2	ECC1	ECC0	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0
PH 3byte	-	-	-	-	-	-	-	-	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0
PH1 4byte	0	0	0	0	0	0	0	0	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
PH1 3byte	-	-	-	-	-	-	-	-	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
PH2 4byte	0	0	0	0	0	0	0	0	WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8
PH2 3byte	-	-	-	-	-	-	-	-	WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8
PH3 4byte	0	0	0	0	0	0	0	0	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0
PH3 3byte	-	-	-	-	-	-	-	-	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
MIPI PH	WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8	ECC7	ECC6	ECC5	ECC4	ECC3	ECC2	ECC1	ECC0
Vx1 PH *CTL packet	V-by-One®HS_D[15]	V-by-One®HS_D[14]	V-by-One®HS_D[13]	V-by-One®HS_D[12]	V-by-One®HS_D[11]	V-by-One®HS_D[10]	V-by-One®HS_D[9]	V-by-One®HS_D[8]	V-by-One®HS_D[7]	V-by-One®HS_D[6]	V-by-One®HS_D[5]	V-by-One®HS_D[4]	V-by-One®HS_D[3]	V-by-One®HS_D[2]	V-by-One®HS_D[1]	V-by-One®HS_D[0]
THCV236 HFSEL=0	THCV236 D[15]	THCV236 D[14]	THCV236 D[13]	THCV236 D[12]	THCV236 D[11]	THCV236 D[10]	THCV236 D[9]	THCV236 D[8]	THCV236 D[7]	THCV236 D[6]	THCV236 D[5]	THCV236 D[4]	THCV236 D[3]	THCV236 D[2]	THCV236 D[1]	THCV236 D[0]
PH 4byte	WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
PH 3byte	WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
PH1 4byte	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
PH1 3byte	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
PH2 4byte	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
PH2 3byte	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
PH3 4byte	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
PH3 3byte	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V

Figure 7. MIPI Packet Header V-by-One® HS output bridge bit mapping

6.13 MIPI Virtual Channel bridge

When MIPI PH(Packet Header) is bridged to V-by-One® HS output with described schemes above, MIPI Virtual Channel information in PH is bridged to V-by-One® HS at the same time. Virtual Channel is supported.

6.14 V-by-One® HS VSYNC generation

Setting of V-by-One® HS VSYNC output is configurable by 2-wire access on internal register.

Internally generated VSYNC (R_VS_MODE=1) follows Figure 8.

Table 25. V-by-One® HS output VSYNC setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1002	[3:2]	R_FS_FE_SYNCEN	2	R/W	V-by-One® HS Vsync generation Enable at MIPI FS/FE (active only when R_VS_MODE=0) 00:Vsync pulse at both FS and FE (THCV242-Q default) 01:Vsync pulse at FS only 10:Vsync pulse at FE only 11:no Vsync pulse at FS nor FE	2'h0
0x1004	[1]	R_VSYNC_POL	1	R/W	V-by-One® HS Vsync polarity 0:High pulse (High active) (THCV242-Q default) 1:Low pulse (Low active)	1'h0
0x1007	[3]	R_VS_MODE	1	R/W	V-by-One® HS VSYNC output timing mode 0:MIPI FS/FE timing direct use mode (THCV242-Q default) 1:internally generated timing mode	1'h0
0x1007	[2:0]	R_VS_OFFSET	3	R/W	V-by-One® HS internally generated VSYNC offset offset from FE = calculatedVS-HTOTAL x R_VS_OFFSET	3'h0
0x1008	[7:0]	R_VS_WIDTH_PIX	8	R/W	V-by-One® HS internally generated Htotal setting Generated Htotal:calculatedVS-HTOTAL = R_VS_WIDTH_PIX x 16	8'h00
0x1009	[4:2]	R_VS_WIDTH_LINE	3	R/W	V-by-One® HS internally generated VSYNC pulse width VSYNC pulse width = calculatedVS-HTOTAL x R_VS_WIDTH_LINE	3'h0

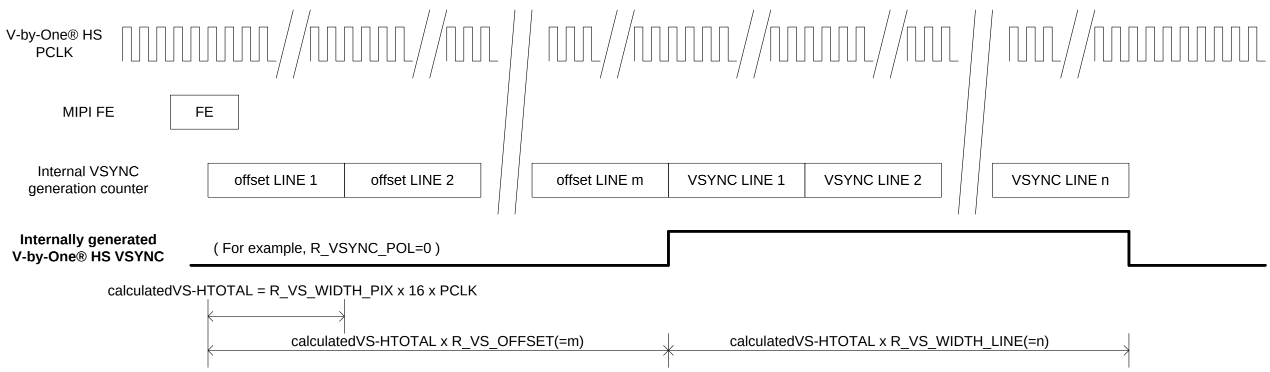


Figure 8. Internally generated VSYNC

6.15 V-by-One® HS HSYNC generation

Setting of V-by-One® HS HSYNC output is configurable by 2-wire access on internal register.

Internally generated HSYNC in Vertical active period (R_HS_MODE=10/11) follows Figure 9.

Internally generated HSYNC in Vertical blanking period (R_HS_VB_EN=10/11) follows Figure 10.

Table 26. V-by-One® HS output HSYNC setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1002	[1:0]	R_LS_LE_SYNCEN	2	R/W	V-by-One® HS Hsync generation Enable at MIPI LS/LE (active only when R_HS_MODE=00, 01) 00:Hsync pulse at both LS and LE (THCV242-Q default) 01:Hsync pulse at LS only 10:Hsync pulse at LE only 11:no Hsync pulse at LS nor LE	2'h0
0x1004	[0]	R_HSYNC_POL	1	R/W	V-by-One® HS Hsync polarity 0:High pulse (High active) (THCV242-Q default) 1:Low pulse (Low active)	1'h0
0x1009	[1:0]	R_HS_MODE	2	R/W	V-by-One® HS HSYNC output timing mode 00, 01:MIPI LS/LE timing direct use mode (THCV242-Q default) 10:internally generated timing mode1 11:internally generated timing mode2	2'h0
0x100A	[4:0]	R_VACT_LINE[12:8]	5	R/W	V-by-One® HS Vactive line skip number MSB	5'h00
0x100B	[7:0]	R_VACT_LINE[7:0]	8	R/W	V-by-One® HS Vactive line skip number LSB	8'h00
0x100C	[1:0]	R_HS_VB_EN	2	R/W	V-by-One® HS HSYNC output in vertical blanking period setting 00, 01:no HSYNC output in Vblank 10:HSYNC output in Vblank, starting from FE 11:HSYNC output in Vblank, starting from FS, skipping Vactive	2'h0
0x100D	[7:0]	R_HS_VB_NUM	8	R/W	V-by-One® HS HSYNC output number in vertical blanking period	8'h00

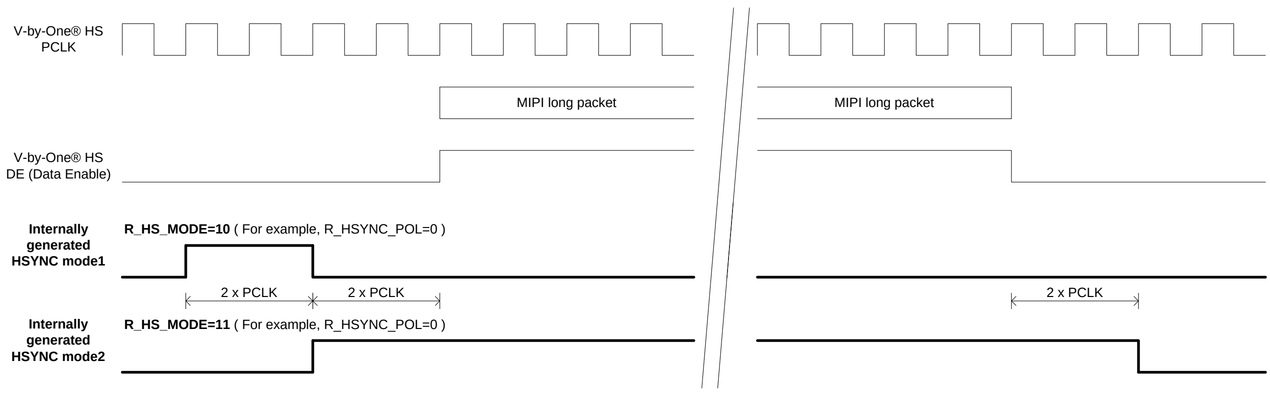


Figure 9. Internally generated HSYNC in Vertical active period

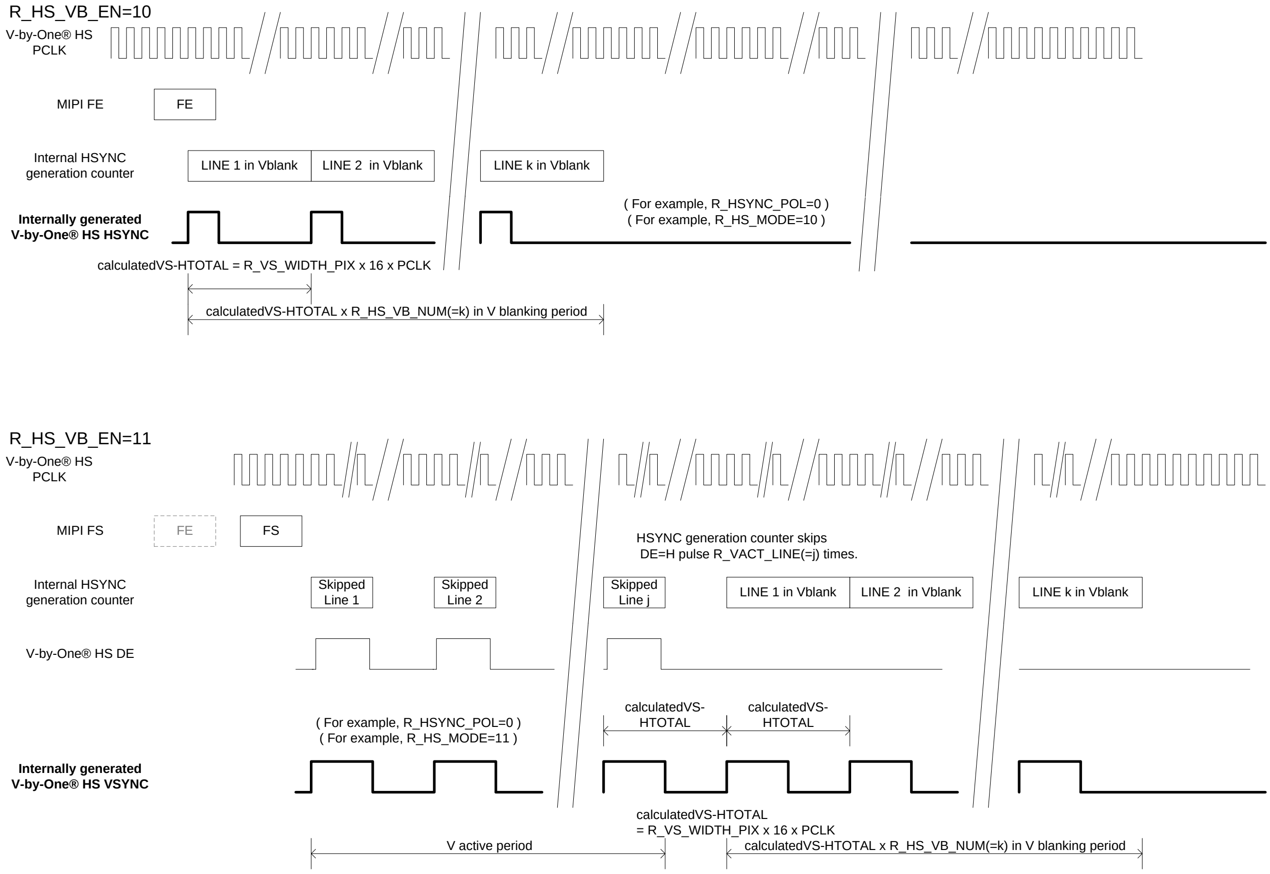


Figure 10. Internally generated HSYNC in Vertical blanking period

6.16 MIPI Short Packet V-by-One® HS output bridge mode

MIPI SP (Short Packet) can be bridge to V-by-One® HS output with the following schemes.

MIPI Short Packet V-by-One® HS output bridge mode is only supported when "R_BITMAP_SEL=2'b00 (MAP1)" or "R_BITMAP_SEL=2'b11 (MAP4)".

"R_VS_MODE=1'b0" and "R_FS_FE_SYNCEN=2'b00" setting is required to bridge both MIPI Frame Start and Frame End Short Packet. "R_VSYNC_POL=1'b0" setting is required to connect THCV242.

THCV236-Q connection is only supported where HFSEL=0 setting is applied on THCV236-Q.

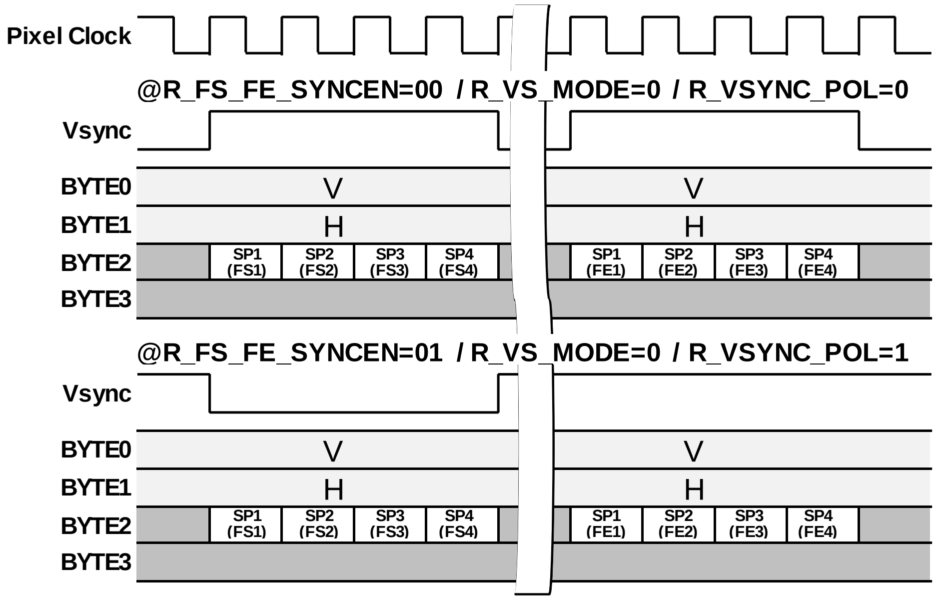


Figure 11. MIPI Short Packet V-by-One® HS bridge timing

Packet		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
mipi Short Packet		DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8	ECC7	ECC6	ECC5	ECC4	ECC3	ECC2	ECC1	ECC0
Vx1 Short Packet *CTL packet		V-by-One®HS_D[31]*	V-by-One®HS_D[30]*	V-by-One®HS_D[29]*	V-by-One®HS_D[28]*	V-by-One®HS_D[27]*	V-by-One®HS_D[26]*	V-by-One®HS_D[25]*	V-by-One®HS_D[24]*	V-by-One®HS_D[23]*	V-by-One®HS_D[22]*	V-by-One®HS_D[21]*	V-by-One®HS_D[20]*	V-by-One®HS_D[19]*	V-by-One®HS_D[18]*	V-by-One®HS_D[17]*	V-by-One®HS_D[16]*	V-by-One®HS_D[15]	V-by-One®HS_D[14]	V-by-One®HS_D[13]	V-by-One®HS_D[12]	V-by-One®HS_D[11]	V-by-One®HS_D[10]	V-by-One®HS_D[9]	V-by-One®HS_D[8]	V-by-One®HS_D[7]	V-by-One®HS_D[6]	V-by-One®HS_D[5]	V-by-One®HS_D[4]	V-by-One®HS_D[3]	V-by-One®HS_D[2]	V-by-One®HS_D[1]	V-by-One®HS_D[0]
THCV236 HFSEL=0		*THCV236 D[31]**	*THCV236 D[30]**	*THCV236 D[29]**	*THCV236 D[28]**	*THCV236 D[27]**	*THCV236 D[26]**	*THCV236 D[25]**	*THCV236 D[24]**	*THCV236 D[23]**	*THCV236 D[22]**	*THCV236 D[21]**	*THCV236 D[20]**	*THCV236 D[19]**	*THCV236 D[18]**	*THCV236 D[17]**	*THCV236 D[16]**	*THCV236 D[15]*	*THCV236 D[14]*	*THCV236 D[13]*	*THCV236 D[12]*	*THCV236 D[11]*	*THCV236 D[10]*	*THCV236 D[9]*	*THCV236 D[8]*	*THCV236 D[7]*	*THCV236 D[6]*	*THCV236 D[5]*	*THCV236 D[4]*	*THCV236 D[3]*	*THCV236 D[2]*	*THCV236 D[1]*	*THCV236 D[0]*
SP1	4byte	0	0	0	0	0	0	0	0	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
	3byte	-	-	-	-	-	-	-	-	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
SP2	4byte	0	0	0	0	0	0	0	0	DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
	3byte	-	-	-	-	-	-	-	-	DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
SP3	4byte	0	0	0	0	0	0	0	0	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
	3byte	-	-	-	-	-	-	-	-	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
SP4	4byte	0	0	0	0	0	0	0	0	ECC7	ECC6	ECC5	ECC4	ECC3	ECC2	ECC1	ECC0	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V
	3byte	-	-	-	-	-	-	-	-	ECC7	ECC6	ECC5	ECC4	ECC3	ECC2	ECC1	ECC0	H	H	H	H	H	H	H	H	V	V	V	V	V	V	V	V

Figure 12. MIPI Short Packet V-by-One® HS bridge bit mapping

6.17 2-wire serial interface

6.17.1 2-wire serial I/F slave Device ID

To use GPIO (General Purpose Input/Output), fault/error detection, and interrupt function, 2-wire serial I/F enables to access registers. AIN pin determines 2-wire slave Device ID setting.

Table 27. 2-wire serial I/F Device ID select by AIN pin

Pin Name	Pin #	type*	Description
AIN	27	I	Select Slave Address 0 : 2wire serial Address = 7'b000_1011 1 : 2wire serial Address = 7'b011_0100

As an additional method, 2-wire slave Device ID setting can be changed from default value by register setting.

Table 28. 2-wire serial I/F Device ID select by register setting

Sub-Link Master Addr(h)	Sub-Link Slave Addr(h)	Bits	Register	width	R/W	Description	Default	Master or Slave related
0x0050	0x00D0	[7:0]	R_2WIRE_SADR	8	RW	2WIRE slave device address setting [7]2WIRE slave device address control 0: 2WIRE slv device addr. is set by AIN pin 1: 2WIRE slv device addr. is set by following register [6:0] [6:0]2WIRE slave device address value for register control	8'd0	MS

6.17.2 2-wire serial Read/Write access to local Register

HOST MPU can directly access THCV241A local register by 2-wire serial I/F.

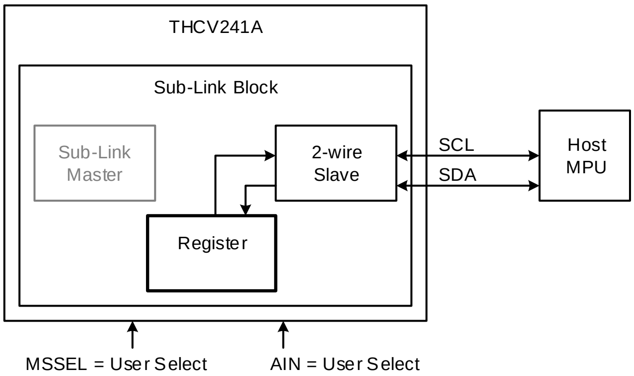


Figure 13. Host to THCV241A local register access configuration

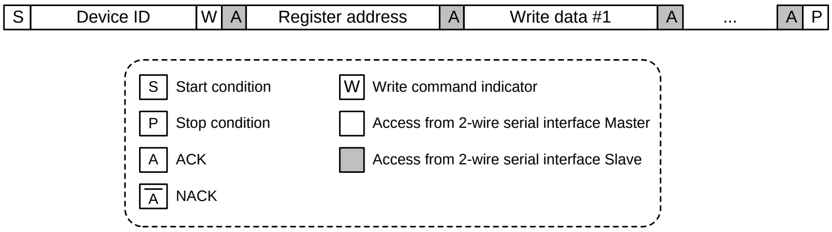


Figure 14. 2-wire serial I/F write to THCV241A local register protocol

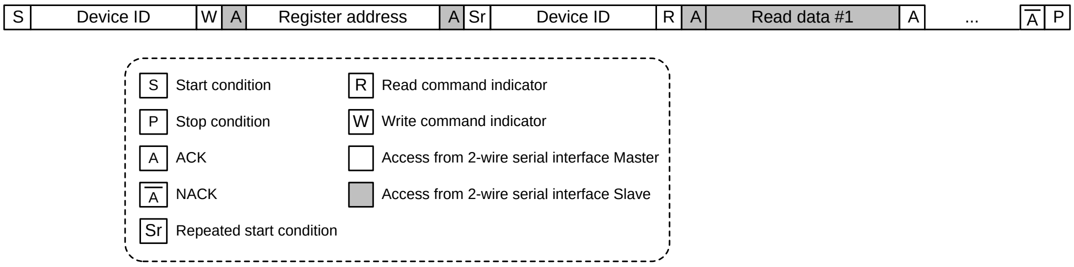


Figure 15. 2-wire serial I/F read to THCV241A local register protocol

6.18 2-wire serial I/F Watch Dog Timer

2-wire Watch Dog Timer (WDT) is installed to monitor status.

Table 29. 2-wire WDT setting

Sub-Link Master Addr(h)	Sub-Link Slave Addr(h)	Bits	Register	width	R/W	Description	Default	Master or Slave related
0x004B	0x00CB	[4]	R_2WIRE_WD_EN	1	RW	2-wire WDT Enable 0:Disable 1:Enable	1'b1	MS
0x004B	0x00CB	[0]	R_2WIRE_WD_OFFSET	1	RW	2-wire WDT offset time 1:11'd2047 0:11'd1023	1'd1	MS
0x004C	0x00CC	[7:0]	R_2WIRE_WD_TIM	8	RW	2-wire WDT time = 64×{R_2WIRE_WD_TIM<7:0>+1}×{"2WIRE WDT offset time"} × tOSC	8'd255	MS

6.19 Register Auto Checksum diagnosis

Register values checksum is continuously calculated as R_CKSUM_RVAL and checked compared to user-defined target, R_CKSUM_VAL. If any change occurs, it can be reported as interrupt.

Table 30. Register Auto Checksum diagnosis control and monitoring

Sub-Link Master Addr(h)	Sub-Link Slave Addr(h)	Bits	Register	width	R/W	Description	Default	Master or Slave related
0x0008	0x0088	[0]	R_CKSUM_EN	1	RW	Internal Register AutoCheckSum Enable 0:Disable 1:Enable	1'b0	MS
0x0009	0x0089	[7:0]	R_CKSUM_TIM	8	RW	Internal Register AutoCheckSum check interval =1024×64×(R_CKSUM_TIM<7:0>+1) × tOSC	8'd19	MS
0x000A	0x008A	[7:0]	R_CKSUM_VAL	8	RW	Internal Register AutoCheckSum expected target value	8'd0	MS
0x000B	0x008B	[7:0]	R_CKSUM_RVAL	8	R	Internal Register AutoCheckSum read value	-	MS
0x0060	0x00E0	[4]	R_INT_CKSUM_ERR	1	R	Interrupt factor: Internal register Checksum error 1: Interrupt (error is detected)	-	MS
0x0061	0x00E1	[4]	R_INTM_CKSUM_ERR	1	RW	Interrupt mask: Internal register CheckSum error 0: Interrupt mask	1'b0	MS
0x0062	0x00E2	[4]	R_INTC_CKSUM_ERR	1	W	Interrupt clear: Internal register CheckSum error 1: Interrupt clear	-	MS

6.20 Sub-Link setting

Sub-Link Master or Sub-Link Slave operation is selectable by MSSEL pin control.

Sub-Link Master control register address and Sub-Link Slave control register address are different even for the same Sub-Link function register.

Sub-Link Master control register is from 0x0000 to 0x007F.

Sub-Link Slave control register is from 0x0080 to 0x00FF.

As a note, registers other than Sub-Link control register from 0x1000 have only one address for one function, which is independent of Sub-Link operation as Master or Slave.

Sub-Link Master “2-wire Set&Trigger mode1” (R_SLINK_MODE setting) is compatible with THCV236-Q.

Sub-Link Polling interval is controllable from 1us to 800us, that may have relationships on fault/error detection, interrupt, or other UART / GPIO transfer time designed on application. SSR (Sub-Link Status Read) interval determines recovery quickness from 2-wire serial remote communication completion. SSR interval effects only on Sub-Link Master “2-wire Set&Trigger mode1” (R_SLINK_MODE setting).

Table 31. Sub-Link Master protocol basic setting

Sub-Link Master Addr(h)	Sub-Link Slave Addr(h)	Bits	Register	width	R/W	Description	Default	Master or Slave related
0x0004	-	[1:0]	R_SLINK_MODE	2	RW	Sub-Link basic protocol setting as Sub-Link Master 0: Reserved 1: 2-wire Set&Trigger (Normal) mode1 (compatible with THCV236) 2: Reserved 3: Reserved Note: When THCV241A is used as Sub-Link Slave, this register setting has no meaning. Counterpart Sub-Link Master setting controls Sub-Link protocol including THCV241A as slave device.	2'd1	M
0x0010	-	[0]	R_SLINK_EN	1	RW	Sub-link Enable 0:Sublink Disable 1:Sublink Enable	1'b0	M
0x0014	-	[4]	R_SLINK_POL_EN	1	RW	Sublink Polling Enable 0:Disable 1:Enable	1'b1	M
0x0014	-	[1:0]	R_SLINK_POL_TIM_UP	2	RW	Sublink Polling interval setting	2'd0	M
0x0015	-	[7:0]	R_SLINK_POL_TIM_DN	8	RW	Sublink Polling interval time=64×(256×R_SLINK_POL_TIM_UP<1:0>+R_SLINK_POL_TIM_DN<7:0>+1)×tOSC *No Polling when R_SLINK_POL_TIM_UP=0 and R_SLINK_POL_TIM_DN=0	8'd124	M
0x0016	-	[4]	R_SLINK_SSR_EN	1	RW	Sublink SSR Enable 0:Disable 1:Enable	1'b1	M
0x0016	-	[1:0]	R_SLINK_SSR_TIM_UP	2	RW	Sublink SSR interval setting	2'd0	M
0x0017	-	[7:0]	R_SLINK_SSR_TIM_DN	8	RW	Sublink SSR interval time=64×(256×R_SLINK_SSR_TIM_UP<1:0>+R_SLINK_SSR_TIM_DN<7:0>+1)×tOSC *No SSR when R_SLINK_SSR_TIM_UP=0 and R_SLINK_SSR_TIM_DN=0	8'd249	M

To use GPIO (General Purpose Input/Output) pin, fault/error detection and interrupt function, “2-wire Set&Trigger mode1” enables remote register access. Sub-Link Master device has 2-wire serial slave block and can connect to HOST MPU, Sub-Link Slave device has 2-wire serial master block and can connect to remote side 2-wire serial slave devices.

HOST MPU can access register of Sub-Link Master device, Sub-Link Slave device and remote side 2-wire serial slave devices.

For “from remote THCV236-Q Sub-Link Master or from remote THCV242 Sub-Link mode1 or remote THCV244 Sub-Link mode1 to THCV241A Sub-Link Slave” access, “0x00FE” /”R_WB_MSB” and “R_WA_MODE” Word Address and Bank setting is required at the beginning before any read access. “0x00FE” Word Address write access from THCV236-Q, THCV242 or THCV244 is supposed to be divided into “0x00” and “0xFE” commands by 8bit Sub-Address restriction.

Table 32. Sub-Link Word Address control setting

Sub-Link								Master
Master	Slave							or Slave
Addr(h)	Addr(h)	Bits	Register	width	R/W	Description	Default	related
-	0x00FE	[6:4]	R_WB_MSB	3	RW	Word Address Bank MSB setting on 1Byte Word-addr. acess from remote Sub-Link Master (e.g. THCV236-Q) (active only when R_WA_MODE=1) 3'd1=3'b001:"Word Address MSB[15:8]" bank is "8'h00" 3'd2=3'b010:"Word Address MSB[15:8]" bank is "8'h10" 3'd3=3'b011:"Word Address MSB[15:8]" bank is "8'h11" others:Reserved	3'b0	S
-	0x00FE	[0]	R_WA_MODE	1	RW	Word Address Byte number setting from remote Sub-Link Master 0:2Byte Word Address acess from remote Sub-Link Master 1:1Byte Word Address acess from remote Sub-Link Master (THCV236-Q setting is "1")	1'b0	S

Under “1Byte Word Address access” operation (0x00FE bit0=1’b1), 1Byte access to 0xFE has the same meaning as 2Byte access to 0x00FE, being independent of “Word Address Bank MSB setting” (0x00FE bit[6:4]). This procedure enables users to reset Word Address Bank MSB setting on 1Byte Word Address access and Word Address Byte number setting itself.

6.20.1 Sub-Link 2-wire Set and Trigger mode (2-wire Normal mode)

Sub-Link Master 2-wire Set&Trigger mode1 (R_SLINK_MODE setting) is compatible with THCV236-Q.

HOST MPU can access to Sub-Link Slave's register via THCV241A as Sub-Link Master only by THCV241A internal local register control and monitoring on 2-wire Set&Trigger mode1.

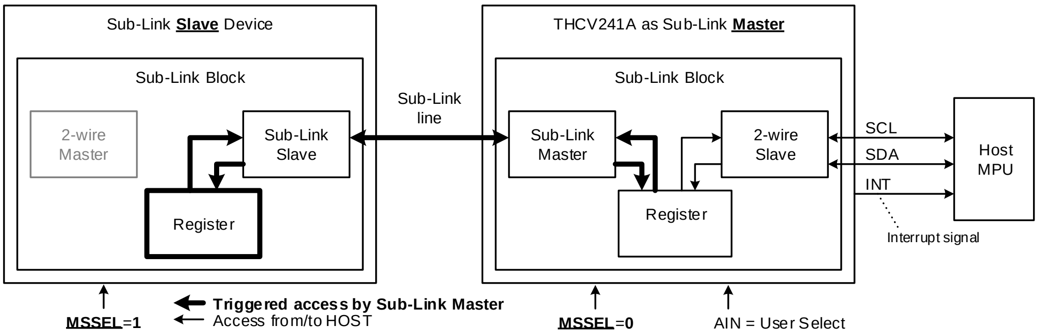


Figure 16. Host MPU to Sub-Link Slave Register via THCV241A access configuration

HOST MPU can access to remote side 2-wire serial slave register via THCV241A as Sub-Link Master only by THCV241A internal local register control and monitoring on 2-wire Set&Trigger mode1.

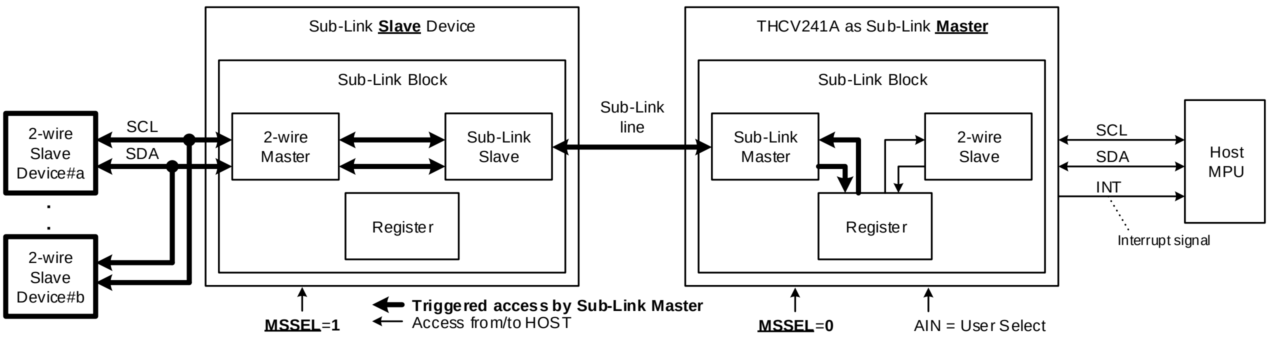


Figure 17. Host MPU to 2-wire slave devices connected to Sub-Link Slave via THCV241A access configuration

In principle, when Sub-Link bridges 2-wire serial interface communication from Sub-Link Master to Sub-Link Slave or remote side 2-wire serial slave devices, time lag occurs between HOST MPU side 2-wire serial access and Sub-Link Slave internal bus access or remote side 2-wire serial access.

R_2WIRE_CLKSEN (Sub-Link Master side register, 0x0042 bit0) selects whether 2-wire serial slave of Sub-Link Master perform clock stretching.

When R_2WIRE_CLKSEN = 1, Sub-Link Master device waits HOST MPU until Sub-Link Slave register access or remote side 2-wire serial slave register access complete by clock stretching.

When R_2WIRE_CLKSEN = 0, Sub-Link Master device informs HOST MPU that Sub-Link Slave register access or remote side 2-wire serial register access has completed by interruption (detectable on INT pin) without clock stretching.

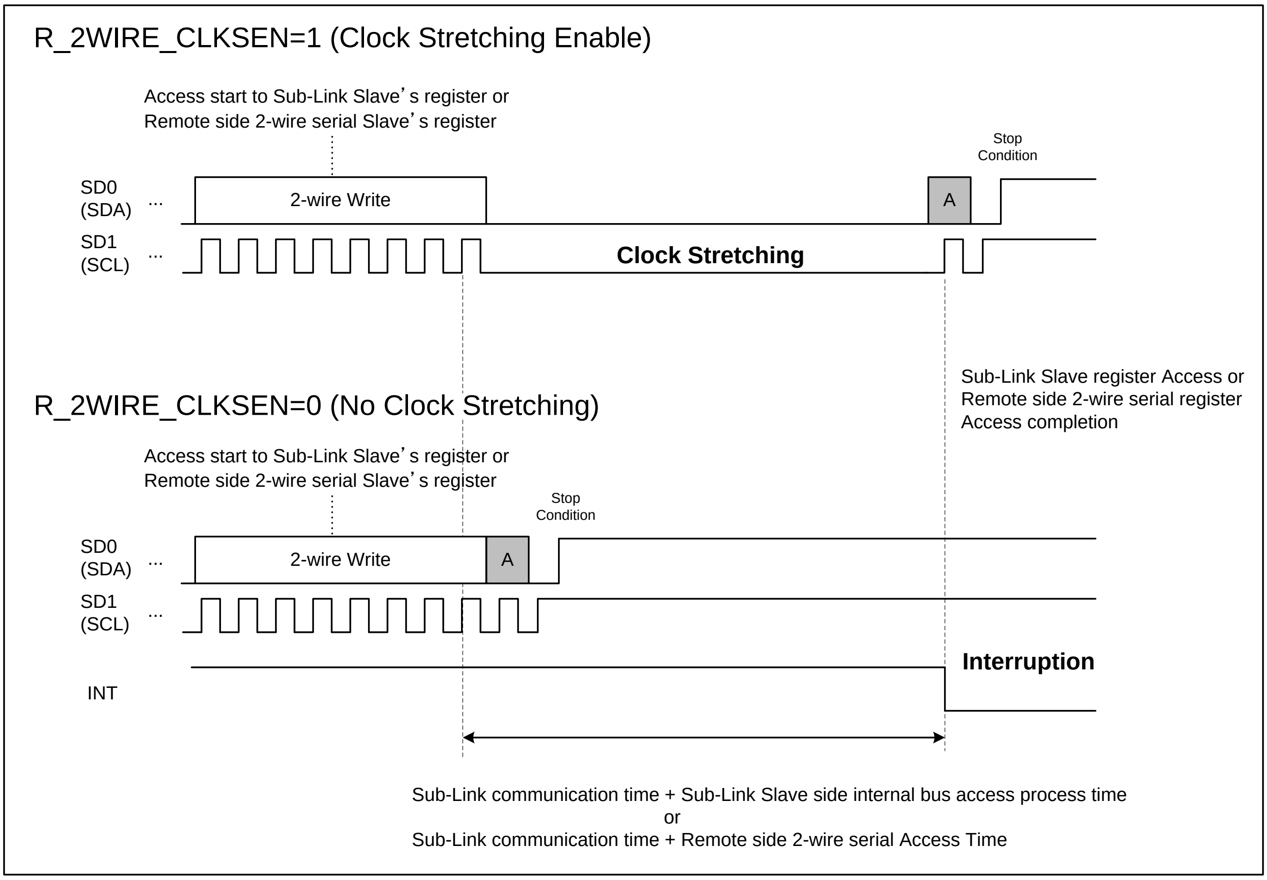


Figure 18. Sub-Link Master 2-wire slave clock stretching operation

Table 33. 2-wire serial I/F Set& Trigger mode remote access control and monitoring local registers

Sub-Link Master Addr(h)	Sub-Link Slave Addr(h)	Bits	Register	width	R/W	Description	Default	Master or Slave related
0x0030	-	[7:0]	R_2WIRE_DATA0	8	RW	2-wire serial I/F remote write/read data #0	8'd0	M
0x0031	-	[7:0]	R_2WIRE_DATA1	8	RW	2-wire serial I/F remote write/read data #1	8'd0	M
0x0032	-	[7:0]	R_2WIRE_DATA2	8	RW	2-wire serial I/F remote write/read data #2	8'd0	M
0x0033	-	[7:0]	R_2WIRE_DATA3	8	RW	2-wire serial I/F remote write/read data #3	8'd0	M
0x0034	-	[7:0]	R_2WIRE_DATA4	8	RW	2-wire serial I/F remote write/read data #4	8'd0	M
0x0035	-	[7:0]	R_2WIRE_DATA5	8	RW	2-wire serial I/F remote write/read data #5	8'd0	M
0x0036	-	[7:0]	R_2WIRE_DATA6	8	RW	2-wire serial I/F remote write/read data #6	8'd0	M
0x0037	-	[7:0]	R_2WIRE_DATA7	8	RW	2-wire serial I/F remote write/read data #7	8'd0	M
0x0038	-	[7:0]	R_2WIRE_DATA8	8	RW	2-wire serial I/F remote write/read data #8	8'd0	M
0x0039	-	[7:0]	R_2WIRE_DATA9	8	RW	2-wire serial I/F remote write/read data #9	8'd0	M
0x003A	-	[7:0]	R_2WIRE_DATA10	8	RW	2-wire serial I/F remote write/read data #10	8'd0	M
0x003B	-	[7:0]	R_2WIRE_DATA11	8	RW	2-wire serial I/F remote write/read data #11	8'd0	M
0x003C	-	[7:0]	R_2WIRE_DATA12	8	RW	2-wire serial I/F remote write/read data #12	8'd0	M
0x003D	-	[7:0]	R_2WIRE_DATA13	8	RW	2-wire serial I/F remote write/read data #13	8'd0	M
0x003E	-	[7:0]	R_2WIRE_DATA14	8	RW	2-wire serial I/F remote write/read data #14	8'd0	M
0x003F	-	[7:0]	R_2WIRE_DATA15	8	RW	2-wire serial I/F remote write/read data #15	8'd0	M
0x0040	-	[7:1]	R_2WIRE_DEVADR	7	RW	2-wire serial I/F remote access target device address. if target=self addr.; access to Sub-Link Slave inside register, else; access to remote side 2-wire serial Slave devices externally connected to Sub-Link slave	7'h00	M
0x0040	-	[0]	R_2WIRE_WR	1	RW	2-wire serial I/F remote access write or read select 0:Write 1:Read	1'b0	M
0x0041	-	[7]	reserved	1	-	-	-	-
0x0041	-	[6:4]	R_2WIRE_WADR_BYTE	3	RW	2-wire serial I/F remote device's Sub Address (Word Address, register address) Byte width select. address Byte width=R_2WIRE_WADR_BYTE<2:0>+1 0 : 1Byte= 8bit Sub addr.(refgister addr.) 1 : 2Byte=16bit Sub addr.(refgister addr.) 4 : 5Byte=40bit Sub addr.(refgister addr.), etc.	3'd0	M
0x0041	-	[3:0]	R_2WIRE_DATA_BYTE	4	RW	2-wire serial I/F remote access data Byte number Byte Number = R_2WIRE_DATA_BYTE + 1 (e.g. 0x2 for 3byte burst) [write rule] R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE =< 'd16 [read rule] R_2WIRE_DATA_BYTE=<'d16	4'd0	M
0x0042	-	[7:1]	reserved	7	-	-	-	-
0x0042	-	[0]	R_2WIRE_CLKSEN	1	RW	2-wire serial I/F local response clock stretching Enable 0: Sub-Link Master (2-wire slave) No clock stretching 1: Sub-Link Master (2-wire slave) clock stretching Enable *2-wire Pass Through mode forces clock stretching Enable	1'b0	M
0x0043	-	[7:1]	reserved	7	-	-	-	-
0x0043	-	[0]	R_2WIRE_START	1	W	2-wire serial I/F remote access start trigger	-	M
-	-	[7:0]	reserved	8	-	-	-	-
-	-	[7:0]	reserved	8	-	-	-	-
-	-	[7:0]	reserved	8	-	-	-	-
-	-	[7:0]	reserved	8	-	-	-	-
-	0x00C8	[7:1]	reserved	7	-	-	-	-
-	0x00C8	[0]	R_2WIRE_BUS_CLR	1	W	2-wire serial I/F remote side bus clear Write 1: 2-wire bus clear action triggered from Sub-Link Slave (2-wire master) to 2-wire slave device connected to Sub-Link Slave. This bit is automatically cleared into 0 after reset action. 0 is always read.	-	S
-	0x00C9	[7:0]	R_2WIRE_SCL_HW	8	RW	SCL High width [tHIGH] setting on Sub-Link Slave side. Output SCL High width is defined as below. 16×{R_2WIRE_SCL_HW<7:0>+1} * tOSC	8'd31	S
-	0x00CA	[7:0]	R_2WIRE_SCL_LW	8	RW	SCL Low width [tLOW] setting on Sub-Link Slave side. Output SCL Low width is defined as below. 16×{R_2WIRE_SCL_LW<7:0>+1} * tOSC	8'd31	S

6.21 Sub-Link Watch Dog Timer

Sub-Link Watch Dog Timer (WDT) is installed to monitor status. When Sub-Link single transaction started but was not normally ended in time, WDT report Interrupt event of "R_INT_SLINK_TMOUT".

Table 34. Sub-Link WDT setting

Sub-Link Master Addr(h)	Sub-Link Slave Addr(h)	Bits	Register	width	R/W	Description	Default	Master or Slave related
0x0018	0x0098	[7:5]	reserved	3	-	-	-	-
0x0018	0x0098	[4]	R_SLINK_WD_EN	1	RW	Sublink WDT Enable 0:Disable 1:Enable	1'b1	MS
0x0018	0x0098	[3:2]	reserved	2	-	-	-	-
0x0018	0x0098	[1:0]	R_SLINK_WD_TIM_UP	2	RW	Sublink WDT time parameter	2'd0	MS
0x0019	0x0099	[7:0]	R_SLINK_WD_TIM_DN	8	RW	Sublink WDT time =64×(256×R_SLINK_WD_TIM_UP<1:0> + R_SLINK_WD_TIM_DN<7:0>+1) ×tOSC	8'd187	MS

6.22 Sub-Link Interrupt detection

For fault/error and significant event detection, Sub-Link prepares mechanism of monitoring for several internal status and interrupt notification. More than one selected factors are logically OR operated for INT pin output. At the same time the OR operated result is informed from Sub-Link Slave to Sub-Link Master.

Detectable interrupts both on Sub-Link Master and Slave are as follows.

- IC Internal event except Sub-Link
- Internal register Checksum error
- 2-wire access time out error
- Sub-Link CRC error
- Sub-Link protocol error
- Sub-Link access time out error

Detectable interrupts as Sub-Link Master are as follows.

- Main-Link LOCKN transition
- Main-Link HTPDN transition
- Sub-Link Slave side factor
- remote 2-wire access on Sub-Link end

Detectable interrupts as Sub-Link Slave are as follows.

- Sub-Link Slave 2-wire master bus clear end
- Sub-Link Slave 2-wire NACK detection

6.23 GPIO setting

Setting of GPIO can be configurable by 2-wire access to internal register.

6.23.1 Sub-Link Polling GPIO input/output

Local GPIO input is continuously reflected to remote GPIO output via Sub-Link polling. Input pins become target of interrupt monitoring.

Table 35. Sub-Link Polling GPIO setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x103D	[3:0]	R_GPIO_TYP	4	R/W	GPIO Mode Select [3]: 0:GPIO3 Register Mode, 1:GPIO3 Sub-Link Polling [2]: 0:GPIO2 Register Mode, 1:GPIO2 Sub-Link Polling [1]: 0:GPIO1 Register Mode, 1:GPIO1 Sub-Link Polling* [0]: 0:GPIO0 Register Mode, 1:GPIO0 Sub-Link Polling* *Sub-Link Polling is compatible with THCV236 GPIO Through mode	4'h0
0x103E	[3:0]	R_GPIO_OEN	4	R/W	GPIO0-3 Input/Output Select [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:GPIO Output Mode 1:GPIO Input Mode	4'hf
0x103F	[3:0]	R_GPIO_CMOSEN	4	R/W	GPIO0-3 CMOS/OpenDrain Select(for GPIO Output Mode) [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:OpenDrain 1:CMOS	4'h0

As default setting with THCV236-Q as Sub-Link Master communication (THCV241A as Sub-Link Slave), GPIO1 Sub-Link Polling bridges output from THCV236-Q-GPIO4 Through Mode and GPIO0 Sub-Link Polling bridges output from THCV236-Q-GPIO3 Through Mode respectively.

As default setting with THCV242 or THCV244 as Sub-Link Master communication (THCV241A as Sub-Link Slave), GPIO1/0 Sub-Link Polling bridges output from THCV242 or THCV244-GPIO Through Mode and GPIO3/2 Sub-Link Polling bridges input to THCV242 or THCV244-GPIO Through Mode respectively.

Polling GPIO Bridging data are sampled every Sub-Link polling, whose basic interval is controlled by register R_SLINK_POL_TIM_UP/_DN. Remote 2-wire access may become long transaction and could lengthen Through GPIO polling reflection interval.

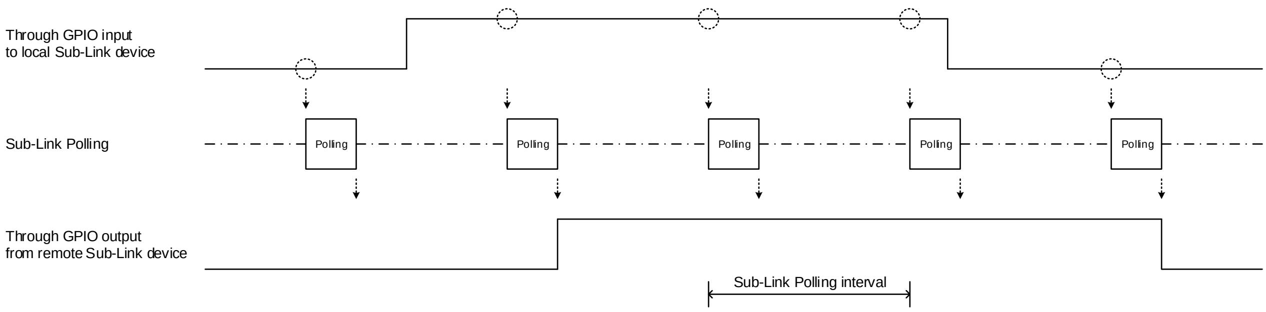


Figure 19. Host MPU to Sub-Link Slave Register via THCV241A access configuration

Remote UART bridge is supported with Sub-Link Polling GPIO input/output. Remote UART Tx and Rx bridge baud rate is supposed to be designed against Sub-Link Polling interval to accommodate deterministic jitter caused by intermittent Sub-Link communication timing.

6.23.2 Register GPIO

GPIO input monitoring and output control are available with register. Input pins become target of interrupt monitoring.

Table 36. Register GPIO setting and status monitoring

Addr(h)	Bits	Register	width	R/W	Description	Default
0x103D	[3:0]	R_GPIO_TYP	4	R/W	GPIO Mode Select [3]: 0:GPIO3 Register Mode, 1:GPIO3 Sub-Link Polling [2]: 0:GPIO2 Register Mode, 1:GPIO2 Sub-Link Polling [1]: 0:GPIO1 Register Mode, 1:GPIO1 Sub-Link Polling* [0]: 0:GPIO0 Register Mode, 1:GPIO0 Sub-Link Polling* *Sub-Link Polling is compatible with THCV236 GPIO Through mode	4'h0
0x103E	[7:4]	R_GPIO_OUT	4	R/W	GPIO0-3 Output Data Register [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0	4'h0
0x103E	[3:0]	R_GPIO_OEN	4	R/W	GPIO0-3 Input/Output Select [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:GPIO Output Mode 1:GPIO Input Mode	4'hf
0x103F	[3:0]	R_GPIO_CMOSEN	4	R/W	GPIO0-3 CMOS/OpenDrain Select(for GPIO Output Mode) [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:OpenDrain 1:CMOS	4'h0
0x1121	[7:4]	R_GPIO_IMON	4	R	GPIO0-3 Input Monitor Register [7]:GPIO3, [6]:GPIO2, [5]:GPIO1, [4]:GPIO0	-
0x1121	[3:0]	R_GPIO_INT_DETECT	4	R	Interrput Signal for GPI [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:No Interrupt 1:Interrupt (detect for asserted or negated of GPI Input)	-
0x1122	[3:0]	R_GPIO_INTC_DETECT	4	W	Interrupt Clear for GPI [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:Interrupt No Clear 1:Interrupt Clear	-

6.24 Internal Error / status signal monitoring GPIO output

Internal error or status signal can be monitored as GPIO output by register setting.

Table 37. Internal Error / status signal monitoring GPIO output setting 1/2

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1038 0x1038 0x1039 0x1039	[6:4] [2:0] [6:4] [2:0]	R_GPIO_SEL0 R_GPIO_SEL1 R_GPIO_SEL2 R_GPIO_SEL3	3	R/W	GPIO0-3 Error / status output select 3b'000:Normal 3b'001:R_ERR_SEL1(Internal Selected Error1) 3b'010:R_ERR_SEL2(Internal Selected Error2) 3b'011:R_EXT_ERR_SEL0(External Selected Error1) 3b'100:R_EXT_ERR_SEL1(External Selected Error2) Others:Normal	3'h0
0x105D	[7:4]	R_ERR_SEL1	4	R/W	Internal Selected Error1 output to GPIO and Sub-Link	4'h0
0x105D	[3:0]	R_ERR_SEL2	4	R/W	Internal Selected Error2 output to GPIO and Sub-Link	4'h0

Table 38. Internal Error / status signal monitoring GPIO output setting 2/2

Sub-Link Master Addr(h)	Sub-Link Slave Addr(h)	Bits	Register	width	R/W	Description	Default	Master or Slave related
0x006E	0x00EE	[7:4]	R_SLINK_ERR_SEL1	4	RW	Sublink Polling to inform error signal select #1	4'd0	MS
0x006D	0x00ED	[3:0]	R_SLINK_ERR_SEL0	4	RW	Sublink Polling to inform error signal select #0	4'd0	MS
0x006F	0x00EF	[7:4]	R_EXT_ERR_SEL1	4	RW	Sub-Link operator Selected Error#1 output to GPIO	4'd0	MS
0x006F	0x00EF	[3:0]	R_EXT_ERR_SEL0	4	RW	Sub-Link operator Selected Error#0 output to GPIO	4'd0	MS

Table 39. IC Internal selectable Error / status signal

R_ERR_SEL1/2[3:0]	Error signal
4'b0000	reserved
4'b0001	MIPI CRC error
4'b0010	MIPI ECC 1bit error
4'b0011	MIPI ECC 2bit error
4'b0100	MIPI ID error (MIPI ID is not equal to Main-Link setting)
4'b0101	MIPI SoT sequence not detected error
4'b0110	MIPI SYNCCODE SoT 1bit error
4'b0111	MIPI FRAMESYNC FS/FE position error
4'b1000	reserved
4'b1001	MIPI Control state error
4'b1010	MIPI FS
4'b1011	MIPI FE
4'b1100	reserved
4'b1101	reserved
4'b1110	Main-Link Data Handle error
4'b1111	PLL auto configuration setting error

Table 40. IC External sub-link operator selectable Error / status signal

R_SLINK_ERR_SELn[3:0] (n=0,1) R_EXT_ERR_SELn[3:0] (n=0,1)	Assignment on Sub-Link Master (MSSEL=0)	Assignment on Sub-Link Slave (MSSEL=1)
'h00	R_ERR_SEL1	
'h01	R_ERR_SEL2	
'h02	R_SLINK_ERR_SEL0 of Sub-Link Slave	R_SLINK_ERR_SEL0 of Sub-Link Master
'h03	R_SLINK_ERR_SEL1 of Sub-Link Slave	R_SLINK_ERR_SEL1 of Sub-Link Master
'h04	R_INT_EXTERNAL	
'h05	R_INT_CKSUM_ERR	
'h06	R_INT_I2C_TMOUT	
'h07	1'b0	
'h08	R_INT_SLINK_PROTERR	
'h09	R_INT_SLINK_TMOUT	
'h0A	R_INT_LOCKN	1'b0
'h0B	R_INT_HTPDN	1'b0
'h0C	R_INT_SLAVESIDE	1'b0
'h0D	R_INT_EXTI2C_ACSEND	1'b0
'h0E	1'b0	R_INT_EXTI2CS_BUSCLR
'h0F	1'b0	R_INT_EXTI2CS_NACK

6.25 Internal Error / status signal monitoring register

Internal error or status signal can be monitored as register read value.

Error count register can be cleared by particular register write "1" access.

Error status register can be masked to "0" fixed by particular register appropriate write access.

Table 41. Internal Error / status signal monitoring register

Module	*ERR* / ERR_CNT	CLEAR	MASK/EN/OFF	Description
Main-Link	*R_DHNDL_ERR*	-	R_DHNDL_INT_MSK	Main-Link Data Handle error
PLL	*PLL_SET_NG*	-	R_PLL_SET_NG_MSK	PLL auto configuration setting error
MIPI	R_RX_CRC_ERR_CNT[15:0]	R_CRC_ERR_CNT_CLR	-	CRC error count by every Line
MIPI	R_RX_ECC_ERR_CRCT_CNT[15:0]	R_ECC_ERR_CRCT_CNT_CLR	-	ECC1bit error count by every Line
MIPI	R_RX_ECC_ERR_DBLE_CNT[15:0]	R_ECC_ERR_DBLE_CNT_CLR	-	ECC2bit error count by every Line
Sub-Link	R_SLINK_FBETERR_NUM_*[15:0]	R_SLINK_FBETERR_CLR	-	Sub-link Feald BET error count

*H:Enable L:Disable, which is defferent polarity from other mask registers

6.26 Interrupt monitoring

Interrupt (INT) detects occurrence of internal error or status signal and then, latch the detected state.

Interrupt factor can be cleared by particular register write “1” access.

Interrupt factor can be masked to “0” fixed by particular register appropriate write access.

Table 42. Interrupt monitoring

Module	INT	CLEAR	MASK/EN/OFF	Description
MIPI	R_ERR_CRC	R_CRC_ERR_CLR	R_CRC_CMP_MSK	MIPI CRC error
MIPI	R_ERR_ECCCOR	R_ECC_CRCT_ERR_CLR	R_ECC1_CMP_MSK	MIPI ECC 1bit error
MIPI	R_ERR_ECCDBL	R_ECC_DOUBLE_ERR_CLR	R_ECC2_CMP_MSK	MIPI ECC 2bit error
MIPI	R_ERR_ID	R_ERR_ID_CLR	R_ERR_ID_MSK	MIPI ID error (MIPI ID is not equal to Main-Link setting)
MIPI	R_ERR_SOTSYNC[3:0]	R_SOT_SYNC_HS_CLR[3:0]	R_ERR_SOT_HS_MSK_R[3:0]	MIPI SoT sequence not detected error
MIPI	R_ERR_SYNCCODE[3:0]	R_SOT_SYNCCODE_CLR[3:0]	R_RX_IGNORE_DERR[3:0]	MIPI SYNCCODE SoT 1bit error
MIPI	R_ERR_FRAMESYNC[3:0]	R_ERR_FR_SYNC_ON_CLR[3:0]	R_ERR_FR_SYNC_MSK_R[3:0]	MIPI FRAMESYNC FS/FE position error
MIPI	R_ERR_CONTROL[4:0]	R_ERR_CTL_CLR[4:0]	R_ERR_CTL_MSK[4:0]	MIPI Control state error
MIPI	R_INT_FS[3:0]	R_INT_FS_ON_CLR[3:0]	R_INT_FS_MSK_R[3:0]	MIPI FS
MIPI	R_INT_FE[3:0]	R_INT_FE_ON_CLR[3:0]	R_INT_FE_MSK_R[3:0]	MIPI FE
Main-Link	R_DHNDL_INT	R_DHNDL_INT_CLR	R_DHNDL_INT_MSK	Main-Link Data Handle error
GPIO	R_GPIO_INT_DETECT[3:0]	R_GPIO_INTC_DETECT[3:0]	R_GPIO_INTM_DETECT[3:0]	GPIO input transition detect
Sub-Link	R_INT_EXTERNAL	R_INTC_EXTERNAL	R_INTM_EXTERNAL	IC Internal event except Sub-Link
Sub-Link	R_INT_CKSUM_ERR	R_INTC_CKSUM_ERR	R_INTM_CKSUM_ERR	Internal register Checksum error
Sub-Link	R_INT_I2C_TMOUT	R_INTC_I2C_TMOUT	R_INTM_I2C_TMOUT	2-wire access time out error
Sub-Link	R_INT_SLINK_PROTERR	R_INTC_SLINK_PROTERR	R_INTM_SLINK_PROTERR	Sub-Link protocol error
Sub-Link	R_INT_SLINK_TMOUT	R_INTC_SLINK_TMOUT	R_INTM_SLINK_TMOUT	Sub-Link access time out error
Sub-Link	R_INT_LOCKN	R_INTC_LOCKN	R_INTM_LOCKN	Main-Link LOCKN transition
Sub-Link	R_INT_HTPDN	R_INTC_HTPDN	R_INTM_HTPDN	Main-Link HTPDN transition
Sub-Link	R_INT_SLAVESIDE	R_INTC_SLAVESIDE	R_INTM_SLAVESIDE	Sub-Link Slave side factor
Sub-Link	R_INT_EXTI2C_ACSEND	R_INTC_EXTI2C_ACSEND	R_INTM_EXTI2C_ACSEND	remote 2-wire access on Sub-Link end
Sub-Link	R_INT_EXTI2CS_BUSCLR	R_INTC_EXTI2CS_BUSCLR	R_INTM_EXTI2CS_BUSCLR	Sub-Link Slave 2-wire master bus clear end
Sub-Link	R_INT_EXTI2CS_NACK	R_INTC_EXTI2CS_NACK	R_INTM_EXTI2CS_NACK	Sub-Link Slave 2-wire NACK detection

As a register, interrupt detected state is “1” and cleared state is “0”. When multiple interrupt sources are activated, the OR operated result is indicated as IC external INT pin output, which at the same time can be sent to Sub-Link counterpart device.

As an external INT pin output, open drain output interrupt detected state is “Low” and cleared state is “Hi-Z”, while INT pin CMOS push-pull output interrupt detected state is “High” and cleared state is “Low”.

Table 43. INT pin output control

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1041	[0]	R_INT_CMOSEN	1	R/W	[IO] INT CMOS/OpenDrain Select 0:OpenDrain 1:CMOS	1'h0

INT interrupt function is supposed to be cleared before start monitoring any desired status because INT status may have been changed before monitoring activation.

For Sub-Link remote interrupt bridge, Sub-Link Master prepares “SLAVESIDE” interrupt factor monitoring element. This Sub-Link SLAVESIDE interrupt monitoring element connected to THCV241A Sub-Link block of THCV241A as Sub-Link Slave.

MIPI, Main-Link, GPIO and other modules of THCV241A are designed as separated module and not included in Sub-Link Module so that R_INT_EXTERNAL factor must be set as “No mask” in order to report those MIPI, Main-Link, GPIO and other Interrupt factor to remote Sub-Link Master.

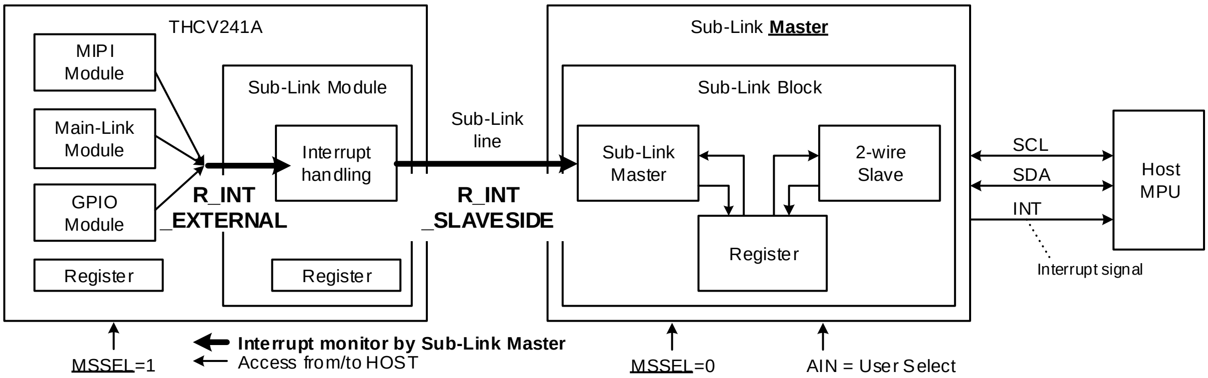


Figure 20. Interrupt configuration external of Sub-Link module.

6.27 Build-In Self-Test pattern generator (BIST)

RGB888 3Byte mode pattern generator is available. Hsync width is 1 pixel fixed. Vsync width is 1 line fixed. Generated pattern is transmitted on Main-Link. As of V-by-One® HS output format, R_OUTPUT_FMT register value is ignored and format is fixed to RGB888 when R_BISTEN = 1, Enabled.

Table 44. V-by-One® HS Build-In Self-Test pattern generator (BIST) setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1004	[1]	R_VSYNC_POL	1	R/W	V-by-One® HS Vsync polarity 0:High pulse (High active) (THCV242-Q default) 1:Low pulse (Low active)	1'h0
0x1004	[0]	R_HSYNC_POL	1	R/W	V-by-One® HS Hsync polarity 0:High pulse (High active) (THCV242-Q default) 1:Low pulse (Low active)	1'h0
0x105F	[0]	R_BISTEN	1	R/W	BIST Enable 0:Disable 1:Enable	1'h0
0x1060	[4:0]	R_BIST_PTN	5	R/W	BIST pattern select 00: Automatic pattern switching repetition from 01 to 0E 01~05: raster patterns 06~07: color bar patterns 08~0B: ramp patterns 0C: 16x16 pixel checker 0D: Frame 0E: Sub checker 0F: reserved 10: Frame2 11~16: checkers 17: Cursor 18~1F: reserved	5'h00
0x1061	[7:0]	R_GS_SEL_R	8	R/W	BIST Gradient Setting Red 00:Black <=> FF:Red	8'hff
0x1062	[7:0]	R_GS_SEL_G	8	R/W	BIST Gradient Setting Green 00:Black <=> FF:Green	8'hff
0x1063	[7:0]	R_GS_SEL_B	8	R/W	BIST Gradient Setting Blue 00:Black <=> FF:Blue	8'hff
0x1064	[3:0]	R_CURSOH[11:8]	4	R/W	BIST Cursor position on horizontal direction	4'h0
0x1065	[7:0]	R_CURSOH[7:0]	8	R/W	BIST Cursor position on horizontal direction	8'h00
0x1066	[3:0]	R_CURSOV[11:8]	4	R/W	BIST Cursor position on vertical direction	4'h0
0x1067	[7:0]	R_CURSOV[7:0]	8	R/W	BIST Cursor position on vertical direction	8'h00
0x1068	[1:0]	R_HACTIVE_V[9:8]	2	R/W	BIST Hactive pixel number setting Hactive pixel number = "R_HACTIVE_V" x4	2'h1
0x1069	[7:0]	R_HACTIVE_V[7:0]	8	R/W	BIST Hactive pixel number Hactive pixel number = "R_HACTIVE_V" x4	8'hE0
0x106A	[2:0]	R_VACTIVE_V[10:8]	3	R/W	BIST Vactive line number (must be even number)	3'h4
0x106B	[7:0]	R_VACTIVE_V[7:0]	8	R/W	BIST Vactive line number (must be even number)	8'h38
0x106C	[1:0]	R_HBLANK_V[9:8]	2	R/W	BIST Hblank pixel number setting Hblank pixel number = "R_HBLANK_V" x4	2'h0
0x106D	[7:0]	R_HBLANK_V[7:0]	8	R/W	BIST Hblank pixel number Hblank pixel number = "R_HBLANK_V" x4	8'h46
0x106E	[1:0]	R_VBLANK_V[9:8]	2	R/W	BIST Vblank line number	2'h0
0x106F	[7:0]	R_VBLANK_V[7:0]	8	R/W	BIST Vblank line number	8'h27
0x1070	[0]	R_HBP_V[8]	1	R/W	BIST Hbackporch pixel number setting Hbackporch pixel number = "R_HBP_V" x4	1'h0
0x1071	[7:0]	R_HBP_V[7:0]	8	R/W	BIST Hbackporch pixel number setting Hbackporch pixel number = "R_HBP_V" x4	8'h28
0x1072	[6:0]	R_VBP_V	7	R/W	BIST Vbackporch line number	7'h10

Automatic pattern switching BIST repetition is available.

Gradient setting only effects on particular patterns.

Cursor position can be set by “R_CURSOR_H”, “R_CURSOR_V” resistor.

Table 45. V-by-One® HS Build-In Self-Test (BIST) selectable patterns

BIST_PTN[4:0]	Pattern	Gradient setting effect	Automatic switch order
00	Automatic switch BIST	○	-
01	White raster	○	1
02	Black raster	×	2
03	Red raster	○	3
04	Green raster	○	4
05	Blue raster	○	5
06	Horizontal color bars	○	6
07	Vertical color bars	○	7
08	Horizontal gray ramp	×	8
09	Vertical gray ramp	×	9
0A	Horizontal RGBW ramp	×	10
0B	Vertical RGBW ramp	×	11
0C	16×16 pixel checker	○	12
0D	Frame	○	13
0E	Sub pixel checker	○	14
0F	reserved	×	-

BIST_PTN[4:0]	Pattern	Gradient setting effect	Automatic switch order
10	Frame2	×	-
11	4×1 checker 1	○	-
12	4×1 checker 2	×	-
13	2×1 checker 1	○	-
14	2×1 checker 2	×	-
15	1×1 checker 1	○	-
16	1×1 checker 2	×	-
17	Cursor	○	-
18	reserved	×	-
19	reserved	×	-
1A	reserved	×	-
1B	reserved	×	-
1C	reserved	×	-
1D	reserved	×	-
1E	reserved	×	-
1F	reserved	×	-

6.28 Main-Link Field BET

In order to help users to check validity of CML serial line (Main-Link and Sub-Link), THCV241A and particular V-by-One® HS receiver have an operation mode in which they act as a bit error tester (BET). In Main-Link Field BET mode, THCV241A internally generates test pattern which is then serialized onto the Main-Link CML line. The counterpart particular receiver, that also has BET function mode, receives the data stream and checks bit errors. The generated data pattern is then 8b/10b encoded, scrambled, and serialized onto the CML channel. As for the receiver, the internal test pattern check circuit gets enabled and reports result on a certain pin or register.

Table 46. V-by-One® HS Field BET pattern generator setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1052	[1]	R_ML_BETEN	1	R/W	V-by-One® HS Main Filed-BET Enable 0 : Normal Mode 1 : Filed-BET Mode	1'h0

6.29 Sub-Link Field BET operation and output from GPIO

In Sub-Link Field BET mode, Sub-Link Master device internally generates test pattern which is then serialized onto the Sub-Link line. Sub-Link Slave device also has BET function mode. Sub-Link Slave device receives the data stream and checks bit errors. Note that Sub-Link Slave device must be set this mode prior to Sub-Link Master device. Pattern check result is output from BETOUT pin of the Sub-Link Slave device. The BETOUT pin goes LOW whenever bit errors occur, or it stays HIGH when there is no bit error.

LATEN enables latched result of once-error-detected. BETOUT/LATEN output pin is assigned according to priority GPIO0 > GPIO1 > GPIO2 > GPIO3 when the same Sub-Link Field BET MODE Signal overlap several pins as register setting.

Table 47. Sub-Link Field BET result GPIO output setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1056	[0]	R_SUB_BETEN	1	R/W	Sub-Link Filed-BET Enable 0 : Normal Mode 1 : Filed-BET Mode	1'h0
0x1057	[7:0]	R_SUB_BETSEL	8	R/W	Sub-Link Field-BET MODE Signal Select [7:6] 10 : GPIO3 BETOUT 01 : GPIO3 LATEN 11,00 : Don't Care [5:4] 10 : GPIO2 BETOUT 01 : GPIO2 LATEN 11,00 : Don't Care [3:2] 10 : GPIO1 BETOUT 01 : GPIO1 LATEN 11,00 : Don't Care [1:0] 10 : GPIO0 BETOUT 01 : GPIO0 LATEN 11,00 : Don't Care	8'h06

6.30 CMOS IO Input noise Filter

IO Filter is available and applied default.

Table 48. CMOS IO input noise filter

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1048	[3:0]	R_IOFLT_RANGE1	4	R/W	CMOS IO Input Signal Noise Fillter Setting for PDN1, MSSEL, AIN 0:No Filter n:Filtering Glitch Signal when Pulse Width is Less than tOSC*n*16 (ns)	4'h4
0x1049	[3:0]	R_IOFLT_RANGE2	4	R/W	CMOS IO Input Signal Noise Fillter Setting for SCL, SDA 0:No Fillter n:Filtering Glitch Signal when Pulse Width is Less than tOSC*n*2 (ns)	4'h2
0x104A	[3:0]	R_IOFLT_RANGE3	4	R/W	CMOS IO Input Signal Noise Fillter Setting for GPIO0 0:No Fillter n:Filtering Glitch Signal when Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104B	[3:0]	R_IOFLT_RANGE4	4	R/W	CMOS IO Input Signal Noise Fillter Setting for GPIO1 0:No Fillter n:Filtering Glitch Signal when Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104C	[3:0]	R_IOFLT_RANGE5	4	R/W	CMOS IO Input Signal Noise Fillter Setting for GPIO2 0:No Fillter n:Filtering Glitch Signal when Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104D	[3:0]	R_IOFLT_RANGE6	4	R/W	CMOS IO Input Signal Noise Fillter Setting for GPIO3 0:No Fillter n:Filtering Glitch Signal when Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104E	[3:0]	R_IOFLT_RANGE7	4	R/W	CMOS IO Input Signal Noise Fillter Setting for LOCKN 0:No Fillter n:Filtering Glitch Signal when Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104F	[3:0]	R_IOFLT_RANGE8	4	R/W	CMOS IO Input Signal Noise Fillter Setting for PDN0 0:No Fillter n:Filtering Glitch Signal when Pulse Width is Less than tOSC*n*16 (ns)	4'hF

6.31 CMOS output drive strength

CMOS output drive strength can be configurable.

Table 49. CMOS output drive strength setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1040	[3:0]	R_GPIO_TDRV	4	R/W	GPIO0-3 CMOS IO Drive Strength Select [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0: Normal Drive(4mA) 1: Strong Drive(8mA)	4'h0
0x1047	[6:0]	R_IO_DRV[7:0]	8	R/W	CMOS IO Drive Strength Select [6]:INT, [3]:CKO, [1]:SDA, [0]:SCL [5], [4], [2]:ReservedL 0: Normal Drive(4mA) 1: Strong Drive(8mA)	7'h00

6.32 CKO reference clock buffer output

CKO reference clock buffer output can be configurable by 2-wire access to internal register.

Table 50. CKO setting

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1076	[6]	R_CKOSTOP	1	R/W	CKO output source select 0:CKI, 1: Low fix	1'h1

6.33 Soft Reset

Soft Reset is available by 2-wire access to internal register.

PLL and V-by-One® HS initial statuses are reset state; therefore Soft Reset is supposed to be released in accordance with appropriate sequence: PLL Soft Reset release => V-by-One® HS TX Soft Reset release.

Table 51. Soft Reset register

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1005	[0]	R_PLL_SNRST	1	R/W	Software Reset for PLL 0:Software Reset Active 1:Software Reset Release (PLL Normal Operation)	1'h0
0x1006	[0]	R_TX_SNRST	1	R/W	Software Reset for V-by-One® HS TX 0:Software Reset Active 1:Software Reset Release (Vx1HS TX Normal Operation)	1'h0
0x1021	[0]	R_C_SNRST	1	R/W	MIPI CSI-2 Soft Reset 0:Reset 1:Reset Release (MIPI CSI-2 Normal Operation)	1'h1
0x1022	[0]	R_DCLKSNRST	1	R/W	Digital logic Clock Soft Reset 0:Reset 1:Reset Release (Digital logic Clock Normal Operation)	1'h1
0x1023	[0]	R_MCLKSNRST	1	R/W	MIPI Clock Soft Reset 0:Reset 1:Reset Release (MIPI Clock Normal Operation)	1'h1
0x10FF	[7:0]	R_REGSNRST	8	R/W	Register Soft Reset AA:Reset others:Reserved	8'h00

Also, change of PLL and V-by-One® HS parameters automatically cause Soft Reset without any touch on R_PLL_SNRST nor R_TX_SNRST, whose temporary reset time length can be defined by R_PLL_CTERM and R_TX_CTERM respectively.

Table 52. Automatic Soft Reset of PLL and V-by-One® HS recovery time control

Addr(h)	Bits	Register	width	R/W	Description	Default
0x105B	[7:0]	R_PLL_CTERM	8	R/W	PLL parameter change automatic reset recovery time length 00 Disable(Disable Auto Soft Reset) 01 1*256*tOSC (typ.3.2us) 02 2*256*tOSC (typ.6.4us) 03 3*256*tOSC (typ.9.6us) : : FE 254*256*tOSC (typ.812.8us) FF 255*256*tOSC (typ.816us)	8'h55
0x105C	[7:0]	R_TX_CTERM	8	R/W	V-by-One® HS parameter change automatic reset recovery time length 00 Disable(Disable Auto Soft Reset) 01 1*256*tOSC (typ.3.2us) 02 2*256*tOSC (typ.6.4us) 03 3*256*tOSC (typ.9.6us) : : FE 254*256*tOSC (typ.812.8us) FF 255*256*tOSC (typ.816us)	8'h55

The registers that may trigger PLL automatic Soft Reset are as follows.

If R_PLL_SET_MODE=0,
R_CKI_FREQ
R_MIPI_MULT
R_VX1_LANE
R_OUTPUT_FMT
R_HFSEL
R_RX_LANE_SEL_EN

else if R_PLL_SET_MODE=1,
R_PLL_SETTING[47:0]
R_DIVVAL

on both R_PLL_SET_MODE=0 and R_PLL_SET_MODE=1,
R_SPREAD
R_DISABLE_SSCG

The registers that may trigger V-by-One® HS automatic Soft Reset are as follows.

R_NHSEL
R_LFQEN
R_ML0_PRE
R_ML1_PRE
R_ML0_DRV
R_ML1_DRV
R_COL_SEL
R_COL_MAN[1:0]
R_OUTPUT_FMT
R_HFSEL
R_BITMAP_SEL

6.34 Power On Sequence

Power On Sequence must be controlled appropriate.

MIPI, PLL and V-by-One® HS block are reset state at power on default and require Reset Release.
. MIPI Soft Reset / PLL Soft Reset => V-by-One® HS Soft Reset is proper. See below detail.

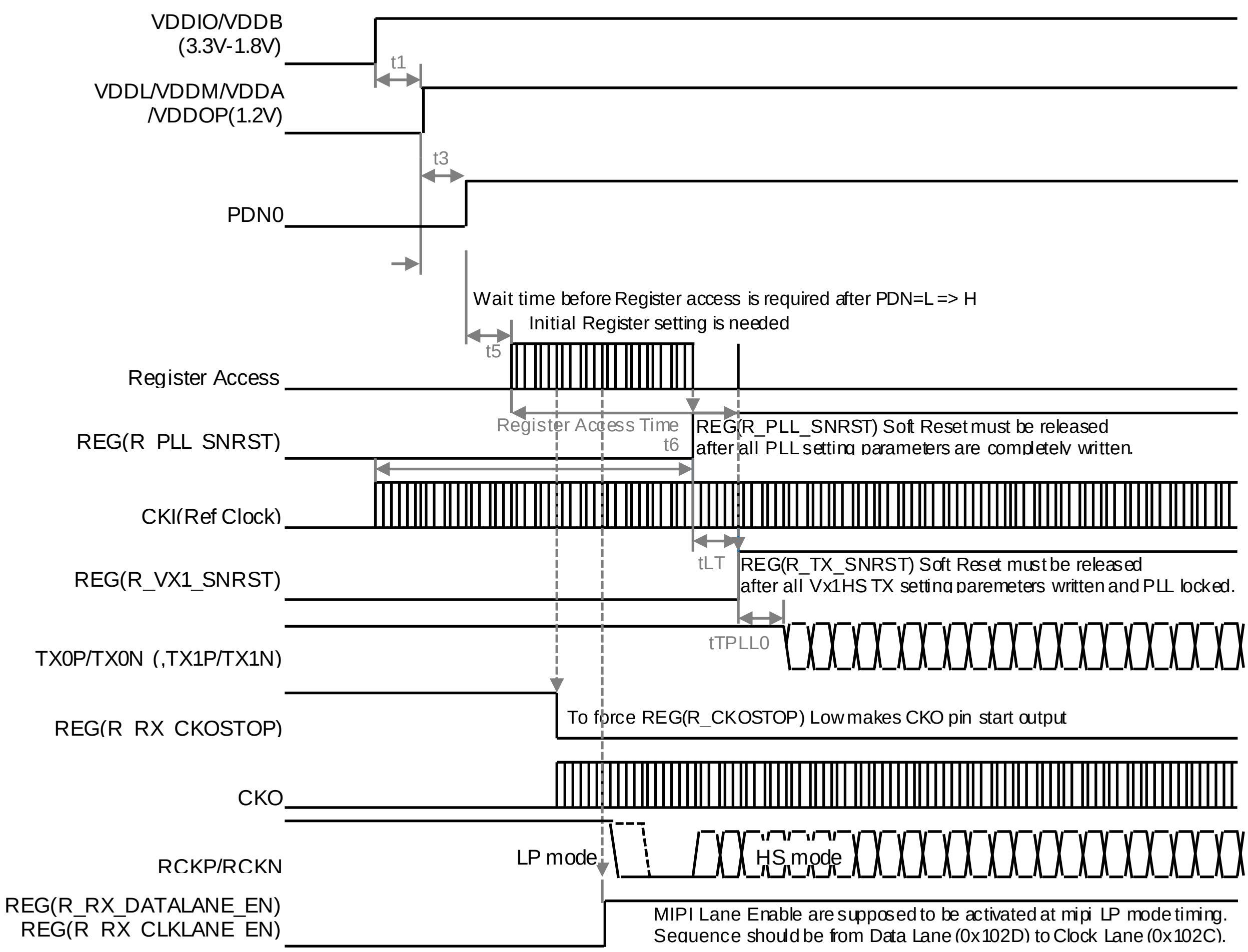


Figure 21. Power On Sequence procedure

Table 53. Power On Sequence specification

Symbol	Parameter	Min	Typ	Max	Unit
t1	3.3V to 1.2V	0	-	-	us
t3	PDN0 Reset Rerease Time	0	-	-	us
t5	Required wait from PDN0=H to Register Access	300	-	-	us
t6	Required wait from CKI input to PLL Enable	200	-	-	us
tLT	Required wait from PLL Lock Time to CML output	$\frac{1000}{F(CKI)}$	-	-	us
tTPLL0	V-by-One® HS Reset Release to CML Out Delay	-	-	250	us

6.35 Lock / Re-Lock Sequence

Lock and re-lock sequence are as follows. V-by-One® HS automatically shifts into lock status from initial status or unlock status caused by external noise under appropriate parameter set condition.

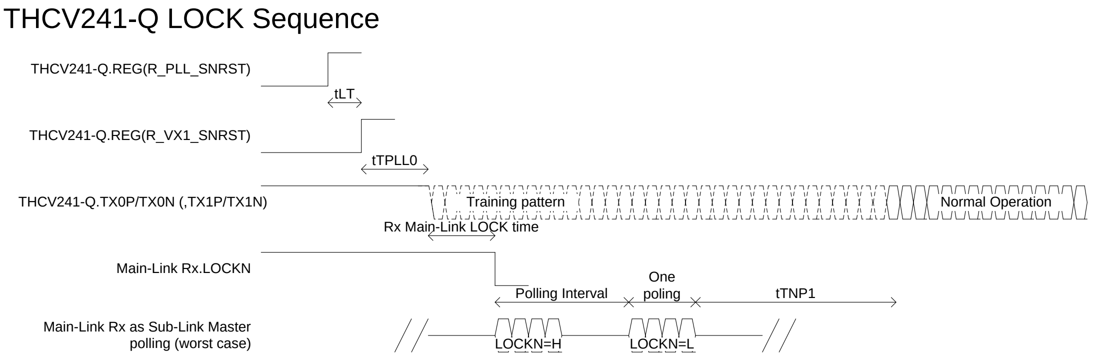


Figure 22. Lock Sequence

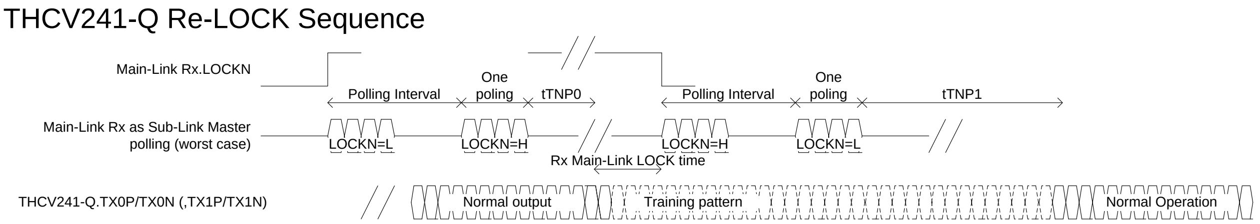


Figure 23. Re-Lock Sequence

Table 54. Lock / Re-Lock Sequence specification

Symbol	Parameter	Min	Typ	Max	Unit
tTNP0	LOCKN=H to Training pattern output delay	-	-	2	us
tTNP1	LOCKN=L to Data pattern output delay	-	-	$\frac{1200}{F(OUT)}$	us

7 Absolute Maximum Ratings

Table 55. Absolute Maximum Ratings*

Parameter	Min	Typ	Max	Unit
Supply Voltage VDDH (VDDIO, VDDB)	-0.3	-	4	V
Supply Voltage VDD12 (VDDM, VDDOP, VDDL, VDDA)	-0.3	-	1.6	V
LVCMOS Input Voltage	-0.3	-	VDDIO+0.3 *1	V
MIPI Input Voltage	-0.3	-	VDDM+0.3 *2	V
CML Transmitter Output Voltage	-0.3	-	VDDA+0.3 *2	V
CML Bi-directional buffer Input / Output Voltage	-0.3	-	VDDB+0.3 *1	V
Storage Temperature Range	-55	-	125	degC
Junction temperature	-	-	125	degC
Reflow Peak Temperature/Time	-	-	260/10	degC /sec

*1 Max. must be below 4V at the same time
*2 Max. must be below 1.6V at the same time

* "Absolute Maximum Ratings" are values of safety limit for a device beyond which a device safety cannot be guaranteed.

They do not imply that a device should be operated at these limits. The tables of "Recommended Operating Conditions" specify conditions for device operation.

8 Recommended Operating Conditions

Table 56. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDDH	Supply Voltage (VDDIO, VDDB)	3.3V Drive	3.0	3.3	3.6	V
		2.5V Drive	2.0	2.5	3.0	V
		1.8V Drive	1.7	1.8	2.0	V
VDD12	Supply Voltage 1.2V (VDDM, VDDOP, VDDL, VDDA)	-	1.1	-	1.3	V
Ta	Operating Ambient Temperature	-	-40	-	105	degC

9 Consumption Current

Table 57. Consumption Current 1/2

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCS33	Power Down Supply Current	PDN1=0, PDN0=0, VDDB=3.6V	-	0.04	-	mA
ICCS12		PDN1=0, PDN0=0, VDDM=1.3V	-	8	-	mA
ICCW33_1	Main-link : FHD 60Hz+HDR MPRF (RAW10) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 860Mbps x4Lane V-by-One® HS = 2.16Gbps x2Lane	-	29.1	45	mA
ICCW12_1			-	120.5	208	mA
ICCW33_2	Main-link : FHD 60Hz+HDR MPRF (RAW10) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 1.2Gbps x4Lane V-by-One® HS = 3.0Gbps x2Lane	-	28.9	45	mA
ICCW12_2			-	139	226	mA
ICCW33_3	Main-link : FHD 60Hz+HDR MPRF (RAW10)+Distribution Sub-Link : active	PDN0=1, PDN1=1 MIPI = 1.2Gbps x4Lane V-by-One® HS = 4.0Gbps x2Lane	-	27.6	45	mA
ICCW12_3			-	143.8	228	mA

Table 58. Consumption Current 2/2

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCW33_11	Main-link :720p 30fps MPRF(RAW) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 594Mbps x1Lane V-by-One® HS = 742.5Mbps x1Lane	-	27.9	45	mA
ICCW12_11			-	67.5	145	mA
ICCW33_12	Main-link :720p 30fps MPRF(YUV422) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 600Mbps x1Lane V-by-One® HS = 750Mbps x1Lane	-	30	45	mA
ICCW12_12			-	66.5	145	mA
ICCW33_13	Main-link :720p60fps MPRF(RAW) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 445.5Mbps x2Lane V-by-One® HS = 1113.75Mbps x1Lane	-	30.5	45	mA
ICCW12_13			-	71.1	150	mA
ICCW33_14	Main-link :1080p30fps MPRF(RAW) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 445.5Mbps x2Lane V-by-One® HS = 1113.75Mbps x1Lane	-	30	45	mA
ICCW12_14			-	71.7	150	mA
ICCW33_15	Main-link :720p60fps MPRF(YUV422) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 594Mbps x2Lane V-by-One® HS = 1485Mbps x1Lane	-	28.8	45	mA
ICCW12_15			-	77.1	155	mA
ICCW33_16	Main-link :1080p30fps MPRF(YUV422) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 594Mbps x2Lane V-by-One® HS = 1485Mbps x1Lane	-	28.5	45	mA
ICCW12_16			-	80.9	160	mA
ICCW33_17	Main-link :720p120fps MPRF(RAW) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 891Mbps x2Lane V-by-One® HS = 2227.5Mbps x1Lane	-	30.1	45	mA
ICCW12_17			-	91.4	175	mA
ICCW33_18	Main-link :1080p60fps MPRF(RAW) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 891Mbps x2Lane V-by-One® HS = 2227.5Mbps x1Lane	-	30.7	45	mA
ICCW12_18			-	88.9	170	mA
ICCW33_19	Main-link :720p120fps MPRF(YUV422) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 594Mbps x4Lane V-by-One® HS = 2970Mbps x1Lane	-	28.2	45	mA
ICCW12_19			-	101	180	mA
ICCW33_20	Main-link :1080p60fps MPRF(YUV422) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 594Mbps x4Lane V-by-One® HS = 2970Mbps x1Lane	-	29.5	45	mA
ICCW12_20			-	95.3	180	mA
ICCW33_21	Main-link :1080p120fps MPRF(RAW) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 891Mbps x4Lane V-by-One® HS = 2227.5Mbps x2Lane	-	28.6	45	mA
ICCW12_21			-	121.5	205	mA
ICCW33_22	Main-link :1080p120fps MPRF(YUV422) Sub-Link : active	PDN0=1, PDN1=1 MIPI = 1200Mbps x4Lane V-by-One® HS = 3000Mbps x2Lane	-	29.6	45	mA
ICCW12_22			-	133.2	222	mA

10 DC Specifications

10.1 CMOS DC Specifications

Table 59. CMOS DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIH	LVCMOS Input Leak Current High	-	-	-	10	uA
IIL	LVCMOS Input Leak Current Low	-	-	-	10	uA
VIHIO	LVCMOS High Level Input Voltage	3.3V Drive	2	-	VDDIO	V
		2.5V Drive	0.70*VDDIO	-	VDDIO	V
		1.8V Drive	0.65*VDDIO	-	VDDIO	V
VILIO	LVCMOS Low Level Input Voltage	3.3V Drive	0	-	0.8	V
		2.5V Drive	0	-	0.30*VDDIO	V
		1.8V Drive	0	-	0.35*VDDIO	V
VOH	LVCMOS High Level Output Voltage	-	VDDIO-0.45	-	VDDIO	V
VOL	LVCMOS Low Level Output Voltage	-	0	-	0.45	V

10.2 MIPI Receiver DC Specifications

Table 60. MIPI Receiver DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ILEAK	mipi D-PHY pin Leak Current	PowerDown	-10	-	10	uA
Vcmrx(DC)	mipi D-PHY Voltage input common Rx	HS mode	70	200	330	mV
Vidth	mipi D-PHY Voltage diff. input high thres.	HS mode	-	-	70	mV
Vidtl	mipi D-PHY Voltage diff. input low thres.	HS mode	-70	-	-	mV
Vihhs	mipi D-PHY Single-end. input high limit at HS mode	HS mode	-	-	460	mV
Vilhs	mipi D-PHY Single-end. input low limit at HS mode	HS mode	-40	-	-	mV
Vterm-en	mipi D-PHY Single-ended threshold for HS termination enable	HS mode	-	-	450	mV
Zid	mipi D-PHY differential input impedance	HS mode	80	100	125	ohm
Vih	mipi D-PHY Single-end input high thres.	LP mode	-	-	880	mV
Vil	mipi D-PHY Single-end input low thres.	LP mode	550	-	-	mV

10.3 CML Transmitter DC Specifications

Table 61. CML Transmitter DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VTOD	CML Differential Mode Output Voltage	R_ML*_DRV [1:0]=00	133	200	267	mV
		R_ML*_DRV [1:0]=01	200	300	400	mV
		R_ML*_DRV [1:0]=10	300	400	500	mV
PRE	CML Pre-emphasis level	R_ML*_PRE[1:0]=00	-	0	-	%
		R_ML*_PRE[1:0]=01 R_ML*_DRV [1:0]=00/01	40	50	60	%
		R_ML*_PRE[1:0]=10 R_ML*_DRV[1:0]=00	80	100	120	%
VTOC	CML Common Mode Output Voltage	R_ML*_PRE[1:0]=00	-	VDDA- VTOD	-	V
		R_ML*_PRE[1:0]=01	-	VDDA- 1.5*VTOD	-	V
		R_ML*_PRE[1:0]=10	-	VDDA- 2*VTOD	-	V
ITOZH	CML Output Leak Current High	R_TX_SNRST=1	-10	-	10	uA
ITOZL	CML Output Leak Current Low	R_TX_SNRST=1	-30	-	10	uA
ITOS	CML Output Short Circuit Current	R_TX_SNRST=0 or PDN0=0 VDDA=1.20v	-60	-	-20	mA

10.4 CML Bi-directional Buffer DC Specifications

Table 62. CML Bi-directional Buffer DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBTH	CML Bi-Directional Buffer Differential Input High Threshold	R_BDCZ_HYS=0	-	-	50	mV
		R_BDCZ_HYS=1	-	-	150	mV
VBTL	CML Bi-Directional Buffer Differential Input Low Threshold	R_BDCZ_HYS=0	-50	-	-	mV
		R_BDCZ_HYS=1	-150	-	-	mV
VBIC	CML Bi-Directional Buffer Input Terminated Common Voltage	R_BDCZ_TERM_** [1:0]= 2'b00 R_BDCZ_DRIVE_** DRIVE[1:0]= 2'b00	-	VDDB-300	-	mV
IBIH	CML Bi-Directional Buffer Output Leak Current High	TCMP/N=VDD	-10	-	10	uA
IBIL	CML Bi-Directional Buffer Output Leak Current Low	TCMP/N=0V	-10	-	10	uA
VBOD	CML Bi-Directional Buffer Differential Output Voltage	R_BDCZ_TERM_** [1:0]=2'b10 R_BDCZ_DRIVE_** [1:0]=2'b10 Diff. 100ohm terminated	200	300	400	mV
VBOC	CML Bi-Directional Buffer Common Output Voltage	R_BDCZ_TERM_** [1:0]=2'b00 R_BDCZ_DRIVE_** [1:0]=2'b00	-	VDDB-300	-	mV
IBOZ	CML Bi-Directional Buffer TRI-STATE Current	PDN1=0	-10	-	10	uA
IBOS	CML Bi-Directional Buffer Output Short Circuit Current	R_BDCZ_TERM_** [1:0]=2'b10 R_BDCZ_DRIVE_** [1:0]=2'b11	-	-30	-	mA
RTERM	CML Bi-Directional Buffer Termination Registance	R_BDCZ_TERM_TX/ RX [1:0]=2'b10	-	50	-	ohm
		R_BDCZ_TERM_TX/ RX [1:0]=2'b01	-	100	-	ohm
		R_BDCZ_TERM_TX/ RX [1:0]=2'b00	-	200	-	ohm
IDRIVE	CML Bi-Directional Buffer Drive Current	R_BDCZ_DRIVE_TX/ RX [1:0]=2'b10	-	12	-	mA
		R_BDCZ_DRIVE_TX/ RX [1:0]=2'b01	-	6	-	mA
		R_BDCZ_DRIVE_TX/ RX [1:0]=2'b00	-	3	-	mA

11 AC Specifications

11.1 MIPI Receiver AC Specifications

Table 63. MIPI Receiver AC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
UI	Unit Interval	-	0.833	-	12.5	ns
tSETUP	Data to Clock Setup Time	-	0.15*UI	-	-	ps
tHOLD	Clock to Data Hold Time	-	0.15*UI	-	-	ps

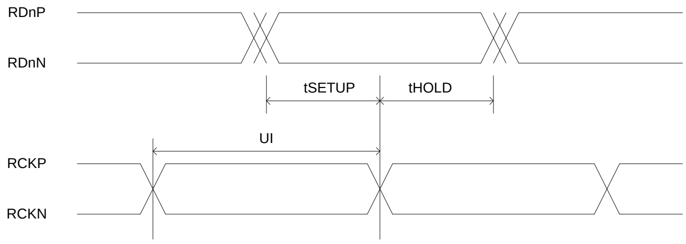


Figure 24. MIPI Receiver setup and hold time at HS mode

11.2 CML Transmitter AC Specifications

Table 64. CML Transmitter AC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tTRF	CML Tx Output Rise and Fall Time	-	50	-	150	ps

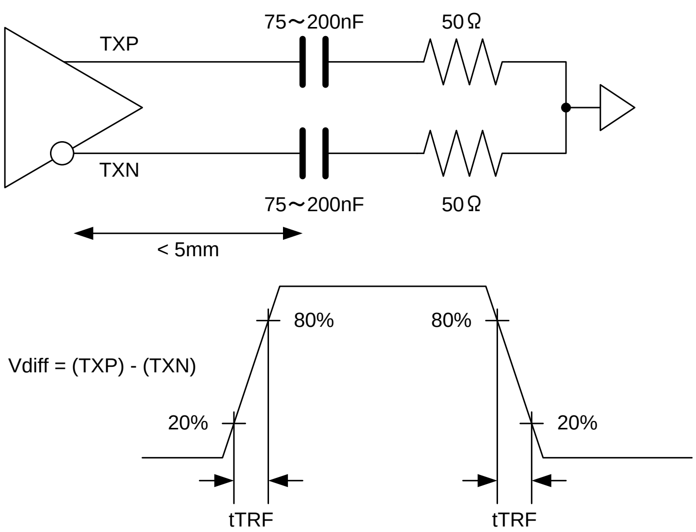


Figure 25. CML Transmitter tTRF

11.3 CML B-directional Buffer AC Specifications

Table 65. CML B-directional Buffer AC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tBUI	Bi-Directional CML Buffer Unit Interval	REG0x0076/F6 = 0x15	128.7	137.5	172.7	ns

11.4 2-wire serial Master/Slave AC Specifications

Table 66. 2-wire serial Slave AC Specifications (Sub-Link Master)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
fSCL	SCL clock frequency	-	-	-	1000	kHz
tHD;STA	Hold time (repeated) START condition	-	0.26	-	-	us
tLOW	LOW period of the SCL clock	-	0.5	-	-	us
tHIGH	HIGH period of the SCL clock	-	0.26	-	-	us
tSU;STA	Set-up time for a repeated START condition	-	0.26	-	-	us
tHD;DAT	Data hold time: output	-	0	2*tOSC	-	us
	Data hold time: input	-	0	-	-	ns
tSU;DAT	Data setup time: output	-	50	-	-	ns
	Data setup time: input	-	50	-	-	ns
tr	Rise time of both SDA and SCL signals	-	-	-	120(*1)	ns
tf	Fall time of both SDA and SCL signals	pull-up:2.5kΩ, bus capacitance : 400pF	-	-	120	ns
tSU;STO	Setup time for STOP condition	-	0.26	-	-	ns
tBUF	Bus free time between a STOP and START condition	-	0.5	-	-	us
tSP	Pulse width of spikes which must be suppressed by the input filter (at R_IOFLT_RANGE 2:5)	-	-	-	50	ns
tPDS	Required wait time from PDN0 high to START condition	-	300	-	-	us

*1 Please adjust Pull-up resistor and bus capacitance to meet the spec value.

Table 67. 2-wire serial Master AC Specifications (Sub-Link Slave)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tOSC	Cycle of internal oscillator clock	-	11.7	12.5	15.7	ns
tHD;STA	Hold time (repeated) START condition	-	-	(16× R_I2C_SCL_HW + 16) * tOSC	-	us
tLOW	LOW period of the SCL clock	-	-	(16× R_I2C_SCL_HW + 16) * tOSC	-	us
tHIGH	HIGH period of the SCL clock	-	-	(16× R_I2C_SCL_HW + 5) * tOSC	-	us
tHD;DAT	Data hold time: output			9*tOSC		us
	Data hold time: input		0			ns
tSU;DAT	Data setup time: output			tLOW – 9 * tOSC		ns
	Data setup time: input		0			ns
tr	Rise time of both SDA and SCL signals	-	-	-	120(*1)	ns
tf	Fall time of both SDA and SCL signals	pull-up:2.5kΩ, bus capacitance : 400pF	-	-	120	ns
tSU;STO	Setup time for STOP condition	-	0.26	-	-	ns

*1 Please adjust Pull-up resistor and bus capacitance to meet the spec value.

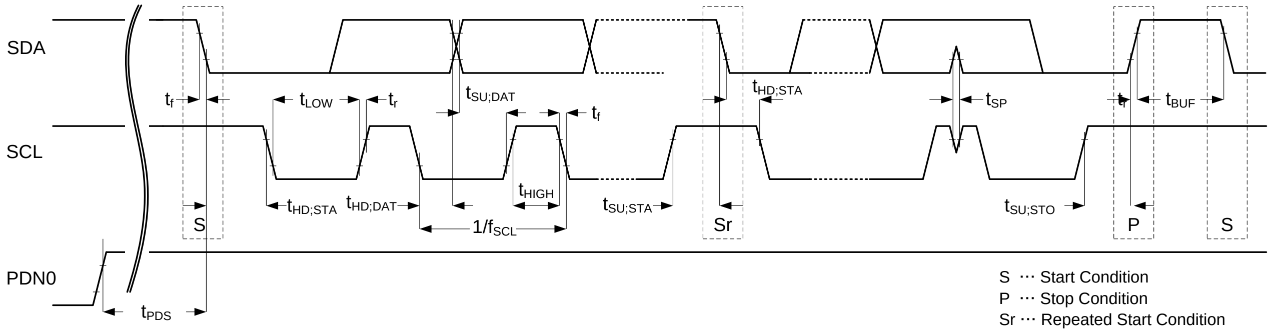
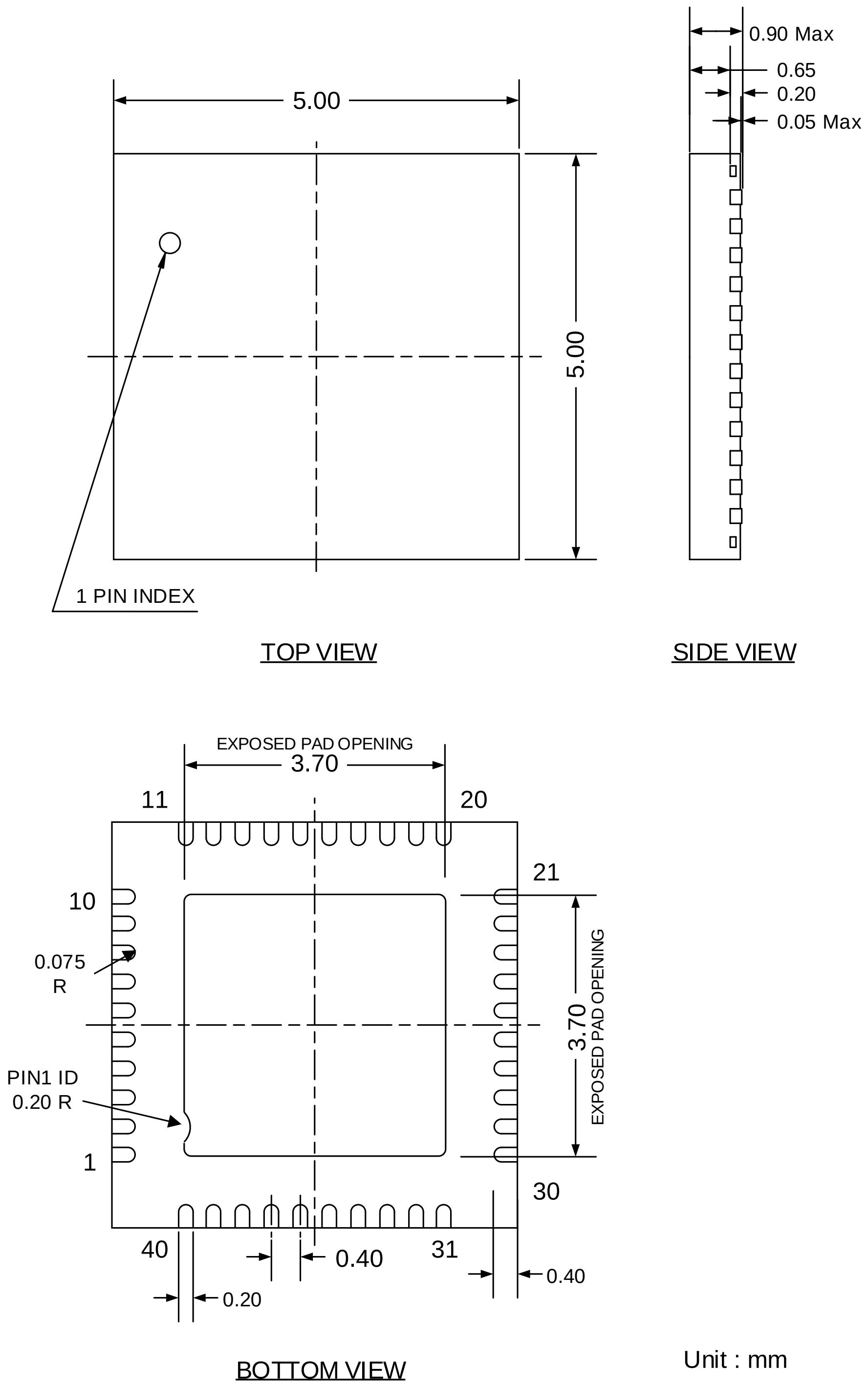


Figure 26. 2-wire serial interface timing diagram

12 Package


5.00
5.00
1 PIN INDEX
0.90 Max
0.65
0.20
0.05 Max
TOP VIEW
SIDE VIEW
EXPOSED PAD OPENING
3.70
11
20
21
10
0.075
R
PIN1 ID
0.20 R
1
30
3.70
EXPOSED PAD OPENING
40
0.40
31
0.40
0.20
BOTTOM VIEW
Unit : mm

13 Notices and Requests

1.The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. (“THine”) is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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4. Note that even if infringement of any third party's industrial ownership should occur by using this product, THine will be exempted from the responsibility unless it directly relates to the production process or functions of the product.

5. Product Application
5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of IATF16949 ("the Specified Product") in this data sheet. THine accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user’s request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

Contact:

THine@cel.com

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения **«JONHON»**, а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов **«FORSTAR»**.

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

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