

General Description

PSoC® is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with Arm® Cortex™ CPUs (single and multi-core). The PSoC 63 product family, based on an ultra low-power 40-nm platform, is a combination of a dual-core microcontroller with low-power Flash technology and digital programmable logic, high-performance analog-to-digital and digital-to-analog conversion, low-power comparators, and standard communication and timing peripherals. The PSoC 63 family provides wireless connectivity with BLE 5.0 compliance.

Features

32-bit Dual Core CPU Subsystem

- 150-MHz Arm Cortex-M4F CPU with single-cycle multiply (Floating Point and Memory Protection Unit)
- 100-MHz Cortex M0+ CPU with single-cycle multiply and MPU.
- User-selectable core logic operation at either 1.1 V or 0.9 V
- Inter-processor communication supported in hardware
- 8 KB 4-way set-associative Instruction Caches for the M4 and M0+ CPUs respectively
- Active CPU power consumption slope with 1.1-V core operation for the Cortex M4 is 40 μ A/MHz and 20 μ A/MHz for the Cortex M0+, both at 3.3-V chip supply voltage with the internal buck regulator
- Active CPU power consumption slope with 0.9-V core operation for the Cortex M4 is 22 μ A/MHz and 15 μ A/MHz for the Cortex M0+, both at 3.3-V chip supply voltage with the internal buck regulator
- Two DMA controllers with 16 channels each

Flash Memory Sub-system

- 1 MB Application Flash with 32-KB EEPROM area and 32-KB Secure Flash
- 128-bit wide Flash accesses reduce power
- SRAM with Selectable Retention Granularity
- 288-KB integrated SRAM
- 32-KB retention boundaries (can retain 32 KB to 288 KB in 32-KB increments)
- One-Time-Programmable (OTP) E-Fuse memory for validation and security

Bluetooth Low Energy (Bluetooth Smart) BT 5.0 Subsystem

- 2.4-GHz RF transceiver with 50- Ω antenna drive
- Digital PHY
- Link Layer engine supporting master and slave modes
- Programmable output power: up to 4 dBm
- RX sensitivity: -95 dBm
- RSSI: 4-dB resolution
- 5.7 mA TX (0 dBm) and 6.7 mA RX (2 Mbps) current with 3.3-V battery and internal SIMO Buck converter
- Link Layer engine supports four connections simultaneously
- Supports 2 Mbps LE data rate

Low-Power 1.7-V to 3.6-V Operation

- Active, Low-power Active, Sleep, Low-power Sleep, Deep Sleep, and Hibernate modes for fine-grained power management
- Deep Sleep mode current with 64-KB SRAM retention is 7 μ A with 3.3-V external supply and internal buck
- On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, <1 μ A quiescent current
- Backup domain with 64 bytes of memory and Real-Time-Clock

Flexible Clocking Options

- On-chip crystal oscillators (High-speed, 4 to 33 MHz, and Watch crystal, 32 kHz)
- Phase Locked Loop (PLL) for multiplying clock frequencies
- 8 MHz Internal Main Oscillator (IMO) with $\pm 2\%$ accuracy
- Ultra low-power 32 kHz Internal Low-speed Oscillator (ILO) with $\pm 10\%$ accuracy
- Frequency Locked Loop (FLL) for multiplying IMO frequency

Serial Communication

- Nine independent run-time reconfigurable serial communication blocks (SCBs), each is software configurable as I²C, SPI, or UART

Timing and Pulse-Width Modulation

- Thirty-two Timer/Counter Pulse-Width Modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals

Up to 78 Programmable GPIOs

- Drive modes, strengths, and slew rates are programmable
- Six overvoltage tolerant (OVT) pins

Packages

- 116-BGA and 104-MCSP packages with PSoC 6 and BLE Radio

Audio Subsystem

- I2S Interface; up to 192 kilosamples (ksps) Word Clock
- Two PDM channels for stereo digital microphones

QSPI Interface

- Execute-In-Place (XIP) from external Quad SPI Flash
- On-the-fly encryption and decryption
- 4-KB QSPI cache for greater XIP performance with lower power
- Supports 1, 2, 4, and Dual-Quad interfaces

Programmable Analog

- 12-bit 1 Msps SAR ADC with differential and single-ended modes and Sequencer with signal averaging
- One 12-bit voltage mode DAC with < 5- μ s settling time
- Two opamps with low-power operation modes
- Two low-power comparators that operate in Deep Sleep and Hibernate modes.
- Built-in temp sensor connected to ADC

Programmable Digital

- 12 programmable logic blocks, each with 8 Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
- Usable as drag-and-drop Boolean primitives (gates, registers), or as Verilog programmable blocks
- Cypress-provided peripheral component library using UDBs to implement functions such as Communication peripherals (for example, LIN, UART, SPI, I²C, S/PDIF and other protocols), Waveform Generators, Pseudo-Random Sequence (PRS) generation, and many other functions.
- Smart I/O (Programmable I/O) blocks enable Boolean operations on signals coming from, and going to, GPIO pins
- Two ports with Smart_IO blocks, capability are provided; these are available during Deep Sleep

Capacitive Sensing

- Cypress Capacitive Sigma-Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing
- Mutual Capacitance sensing (Cypress CSX) with dynamic usage of both Self and Mutual sensing
- Wake on Touch with very low current
- Cypress-supplied software component makes capacitive sensing design fast and easy
- Automatic hardware tuning (SmartSense™)

Energy Profiler

- Block that provides history of time spent in different power modes
- Allows software energy profiling to observe and optimize energy consumption

PSoC Creator Design Environment

- Integrated Development Environment provides schematic design entry and build (with analog and digital automatic routing) and code development and debugging
- Applications Programming Interface (API Component) for all fixed-function and programmable peripherals
- Bluetooth Smart Component (BLE4.2 compliant protocol stack) with Application level function calls and Profiles

Industry-Standard Tool Compatibility

- After schematic entry, development can be done with Arm-based industry-standard development tools
- Configure in PSoC Creator and export to Arm/Keil or IAR IDEs for code development and debugging
- Supports industry standard Arm Trace Emulation Trace Module

Security Built into Platform Architecture

- Multi-faceted secure architecture based on ROM-based root of trust
- Secure Boot uninterruptible until system protection attributes are established
- Authentication during boot using hardware hashing
- Step-wise authentication of execution images
- Secure execution of code in execute-only mode for protected routines
- All Debug and Test ingress paths can be disabled

Cryptography Accelerators

- Hardware acceleration for Symmetric and Asymmetric cryptographic methods (AES, 3DES, RSA, and ECC) and Hash functions (SHA-512, SHA-256)
- True Random Number Generator (TRNG) function

More Information

Cypress provides a wealth of data at www.cypress.com to help you select the right PSoC device and quickly and effectively integrate it into your design. The following is an abbreviated list of resources for PSoC 6 MCU:

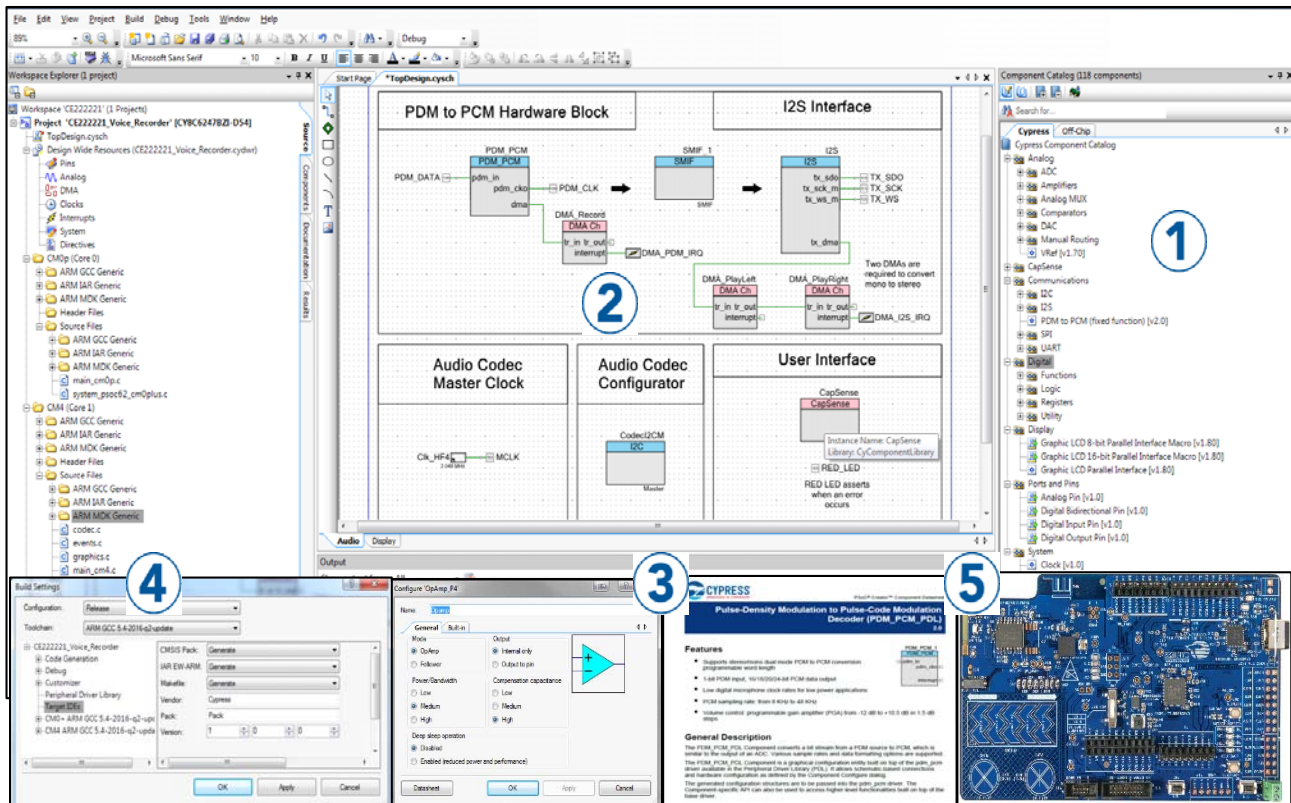
- **Overview:** [PSoC Portfolio](#), [PSoC Roadmap](#)
- **Product Selectors:** [PSoC 6 MCU Page](#)
- **Application Notes** cover a broad range of topics, from basic to advanced level, and include the following:
 - [AN210781](#): Getting Started with PSoC 6 MCU BLE
 - [AN218241](#): PSoC 6 MCU Hardware Design Considerations
 - [AN213924](#): PSoC 6 MCU Bootloader Guide
 - [AN215656](#): PSoC 6 MCU Dual-Core CPU System Design
 - [AN219434](#): Importing PSoC Creator Code into an IDE
 - [AN219528](#): PSoC 6 MCU Power Reduction Techniques
 - [AN221111](#): PSoC 6 MCU: Creating a Secure System
- **Code Examples** provides [PSoC Creator](#) example projects for different product features and usage.
- **Technical Reference Manuals (TRMs)** provide detailed descriptions of PSoC 6 MCU architecture and registers.
- **Development Tools**
 - [CY8CKIT-062-Wi-Fi/BT](#) supports the PSoC 62 series MCU with WiFi and Bluetooth connectivity.
 - [CY8CKIT-062-BLE](#) supports the PSoC 63 series MCU with Bluetooth Low-Energy (BLE) connectivity.
- **Training Videos:** Visit www.cypress.com/training for a wide variety of video training resources on PSoC Creator

PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables you to design hardware and firmware systems concurrently, based on PSoC 6 MCU. As shown below, with PSoC Creator, you can:

1. Explore the library of 200+ Components in PSoC Creator
2. Drag and drop Component icons to complete your hardware system design in the main design workspace
3. Configure Components using the Component Configuration Tools and the Component datasheets
4. Co-design your application firmware and hardware in the PSoC Creator IDE or build project for 3rd party IDE
5. Prototype your solution with the PSoC 6 Pioneer Kits. If a design change is needed, PSoC Creator and Components enable you to make changes on the fly without the need for hardware revisions.

Figure 1. PSoC Creator Schematic Entry and Components



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Blocks and Functionality

The PSoC 63 block diagram is shown in Figure 2. There are five major subsystems: CPU subsystem, BLE subsystem, system resources, peripheral blocks, and I/O subsystem.

Figure 2. Block Diagram

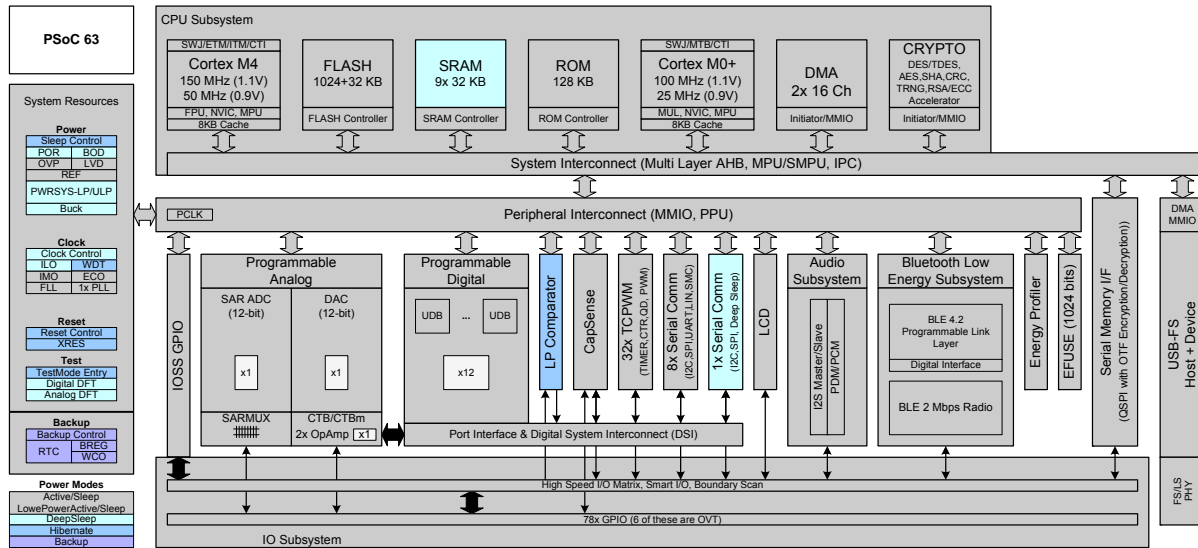


Figure 2 shows the subsystems of the chip and gives a very simplified view of their inter-connections (Multi-layer AHB is used in practice). The color-coding shows the lowest power mode where the particular block is still functional (for example, LP Comparator is functional in Deep Sleep mode).

PSoC 63 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 63 devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 63 family provides a very high level of security.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is a trade-off the customer can make.

Functional Definition

CPU and Memory Subsystem

CPU

The CPU subsystem in the PSoC 63 consists of two Arm Cortex cores and their associated busses and memories: M4 with Floating-point unit and Memory Protection Units (FPU and MPU) and an M0+ with an MPU. The Cortex M4 and M0+ have 8 KB Instruction Caches (I-Cache) with 4-way set associativity. This subsystem also includes independent DMA controllers with 32 channels each, a Cryptographic accelerator block, 1 MB of on-chip Flash, 288 KB of SRAM, and 128 KB of ROM.

The Cortex M0+ provides a secure, un-interruptible Boot function. This guarantees that post-Boot, system integrity is checked and privileges enforced. Shared resources can be accessed through the normal Arm multi-layer bus arbitration and exclusive accesses are supported by an Inter-Processor Communication (IPC) scheme, which implements hardware semaphores and protection. Active power consumption for the Cortex M4 is 22 μ A/MHz and 15 μ A/MHz for the Cortex M0+, both at 3.3 V chip supply voltage with the internal buck enabled and at 0.9 V internal supply. Note that at Cortex M4 speeds above 100 MHz, the M0+ and Peripheral subsystem are limited to half the M4 speed. If the M4 is running at 150 Mhz, the M0+ and peripheral subsystem is limited to 75 MHz.

DMA Controllers

There are two DMA controllers with 16 channels each. They support independent accesses to peripherals using the AHB Multi-layer bus.

Flash

PSoC 63 has a 1 MB flash module with additional 32 KB of Flash that can be used for EEPROM emulation for longer retention and a separate 32 KB block of Flash that can be securely locked and is only accessible via a key lock that cannot be changed (one Time Programmable).

SRAM with 32 KB Retention Granularity

There is 288 KB of SRAM memory, which can be fully retained or retained in increments of user-designated 32 KB blocks.

SROM

There is a supervisory 128 KB ROM that contains boot and configuration routines. This ROM will guarantee Secure Boot if authentication of User Flash is required.

One-Time-Programmable (OTP) eFuse

The 1024-bit OTP memory can provide a unique and unalterable Identifier on a per-chip basis. This unalterable key can be used to access Secured Flash.

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) when the power supply drops below specified levels. The design will guaranteed safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the Reset occurring. There are no voltage sequencing requirements. The VDD core logic supply (1.7 to 3.6 V) will feed an on-chip buck, which will produce the core logic supply of either 1.1 V or 0.9 V selectable. Depending on the frequency of operation, the buck converter will have a quiescent current of <1 μ A. A separate power domain called Backup is provided; note this is not a power mode. This domain is powered from the VBACKUP domain and includes the 32-kHz WCO, RTC, and backup registers. It is connected to VDD when not used as a backup domain. Port 0 is powered from this supply. Pin 5 of Port 0 (P0.5) can be assigned as a PMIC wakeup output (timed by the RTC); P0.5 is driven to the resistive pull-up mode by default.

Clock System

The PSoC 63 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 63 consists of the Internal Main Oscillator (IMO) and the Internal Low-speed Oscillator (ILO), crystal oscillators (ECO and WCO), PLL, FLL, and provision for an external clock. An FLL will provide fast wake-up at high clock speeds without waiting for a PLL lock event (which can take up to 50 μ s). Clocks may be buffered and brought out to a pin on a Smart I/O port.

The 32-kHz oscillator is trimmable to within 2 ppm using a higher accuracy clock. The ECO will deliver ± 20 ppm accuracy and will use an external crystal.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 63. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz. IMO tolerance is $\pm 2\%$ and its current consumption is less than 10 μ A.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which may be used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO or from the WCO; this allows watchdog operation during Deep Sleep and Hibernate modes, and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Clock Dividers

Integer and Fractional clock dividers are provided for peripheral use and timing purposes. There are eight 8-bit integer and sixteen 16-bit integer clock dividers. There is also one 24.5-bit fractional and four 16.5-bit fractional clock dividers.

Reset

The PSoC 63 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

BLE Radio and Subsystem

PSoC 63 incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 2 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 5.0. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel (Bluetooth 4.1 feature)
- GAP features
 - Broadcaster, Observer, Peripheral, and Central roles
 - Security mode 1: Level 1, 2, and 3
 - User-defined advertising data
 - Multiple bond support

■ GATT features

- GATT client and server
- Supports GATT sub-procedures
- 32-bit universally unique identifier (UUID) (Bluetooth 4.1 feature)

■ Security Manager (SM)

- Pairing methods: Just works, Passkey Entry, and Out of Band
- LE Secure Connection Pairing model
- Authenticated man-in-the-middle (MITM) protection and data signing

■ Link Layer (LL)

- Master and Slave roles
- 128-bit AES engine
- Low-duty cycle advertising
- LE Ping

■ Supports all SIG-adopted BLE profiles

- Power levels for Adv (1.28s, 31 bytes, 0 dBm) and Con (300 ms, 0 byte, 0 dBm) are 42 μW and 70 μW respectively

Analog Blocks

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD} , $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. There are 16 channels of which any 13 can be sampled in a single scan.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 3.6 V.

Temperature Sensor

PSoC 63 has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

12-bit Digital-Analog Converter

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 5 μ s. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output.

Continuous Time Block (CTBm) with Two Opamps

This block consists of two opamps, which have their inputs and outputs connected to fixed pins and have three power modes and a comparator mode. The outputs of these opamps can be used as buffers for the SAR inputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware. The opamps can be set to one of the four power levels; the lowest level allowing operation in Deep Sleep mode in order to preserve lower performance Continuous-Time functionality in Deep Sleep mode. The DAC output can be buffered through an opamp.

Low-Power Comparators

PSoC 63 has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Programmable Digital

Smart I/O

There are two Smart I/O blocks, which allow Boolean operations on signals going to the GPIO pins from the subsystems of the chip or on signals coming into the chip. Operation can be synchronous or asynchronous and the blocks operate in low-power modes, such as Deep Sleep and Hibernate. This allows, for example, detection of logic conditions that can indicate that the CPU should wake up instead of waking up on general I/O interrupts, which consume more power and can generate spurious wake-ups.

Universal Digital Blocks (UDBs) and Port Interfaces

PSoC 63 has 12 UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

Fixed-Function Digital

Timer/Counter/PWM Block

The timer/counter/PWM block consists of 32 counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. There are eight 32-bit counters and 24 16-bit counters.

Serial Communication Blocks (SCB)

PSoC 63 has nine SCBs, which can each implement an I²C, UART, or SPI interface. One SCB will operate in Deep Sleep with an external clock, this SCB will only operate in Slave mode (requires external clock).

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI²C that creates a mailbox address range in the memory of PSoC 63 and effectively reduces the I²C communication to reading from and writing to an array in the memory. In addition, the block supports a 256 byte FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I²C peripheral is compatible with I²C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256 byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codex), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with up to a 25-MHz SPI clock.

USB Full-Speed Dual Role Host and Device Interface

PSoC 63 incorporates a dual-role USB Host and Device interface. The device can have up to eight endpoints. A 512byte SRAM buffer is provided and DMA is supported.

QSPI Interface

A Quad SPI (QSPI) interface is provided running at 80 MHz. This block also supports on-the-fly encryption and decryption to support Execute-In-Place operation at reasonable speeds. It supports Single/dual/quad/octal SPI and dual-quad SPI modes.

GPIO

PSoC 63 has up to 78 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Hold mode for latching previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it. Six GPIO pins are capable of overvoltage tolerant (OVT) operation where the input voltage may be higher than VDD (these may be used for I²C functionality to allow powering the chip off while maintaining physical connection to an operating I²C bus without affecting its functionality).

GPIO pins can be ganged to sink 16 mA or higher values of sink current. GPIO pins, including OVT pins, may not be pulled up higher than 3.6 V.

Special-Function Peripherals

CapSense

CapSense is supported on all pins in the PSoC 63 through a CapSense Sigma-Delta (CSD) block that can be connected to an analog multiplexed bus. Any GPIO pin can be connected to this AMUX bus through an analog switch. CapSense function can thus be provided on any pin or a group of pins in a system under software control. Cypress provides a software component for the CapSense block for ease-of-use.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

The CapSense block has two 7-bit IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). A (slow) 10-bit Slope ADC may be realized by using one of the IDACs.

The block can implement Swipe, Tap, Wake-up on Touch (< 3 μ A at 1.8 V), mutual capacitance, and other types of sensing functions.

Audio Subsystem

This subsystem consists of an I2S block and two PDM channels. The PDM channels interface to a PDM microphone's bit-stream output. The PDM processing channel provides droop correction and can operate with clock speeds ranging from 384 kHz to 3.072 MHz and produce word lengths of 16 to 24 bits at audio sample rates of up to 48 ksps.

The I2S interface supports both Master and Slave modes with Word Clock rates of up to 192 ksps (8-bit to 32-bit words).

Pinouts

Table 1. Pinouts for 116-BGA and 104-MCSP Packages

| 104-MCSP-BLE | | 116-BGA-BLE | |
|--------------|---------|--------------------------------------------|---------|
| Pin | Name | Pin | Name |
| C7 | VCCD | A2 | VCCD |
| C6 | VDDD | B1 | VDDD |
| C9 | VBACKUP | C1 | VBACKUP |
| D8 | P0.0 | C2 | P0.0 |
| E6 | P0.1 | D3 | P0.1 |
| D9 | P0.2 | E4 | P0.2 |
| E7 | P0.3 | E3 | P0.3 |
| E8 | P0.4 | F3 | P0.4 |
| E9 | P0.5 | D2 | P0.5 |
| E5 | XRES | E2 | XRES |
| F5 | P1.0 | G3 | P1.0 |
| F6 | P1.1 | F2 | P1.1 |
| | | J5 | P1.2 |
| F9 | P1.3 | J4 | P1.3 |
| F8 | P1.4 | J3 | P1.4 |
| F7 | P1.5 | J2 | P1.5 |
| G9 | VDD_NS | H3 | VDD_NS |
| G8 | VIND1 | F1 | VIND1 |
| H8 | VIND2 | G1 | VIND2 |
| J8 | VBUCK1 | G2 | VBUCK1 |
| H9 | VRF | H1 | VRF |
| L9 | VDDR1 | L2 | VDDR1 |
| N9 | VSSR | J1, K2, K3, K4, K5, L1, L3, L4, L5, M3, M8 | VSSR |
| M9 | ANT | K1 | ANT |
| M9 | ANT | K1 | ANT |
| K2 | P6.1 | J8 | P6.1 |
| M2 | P6.2 | L9 | P6.2 |
| L1 | P6.3 | K9 | P6.3 |
| J2 | P6.4 | J9 | P6.4 |
| K1 | P6.5 | M10 | P6.5 |
| N2 | P6.6 | L10 | P6.6 |
| M1 | P6.7 | K10 | P6.7 |

| 104-MCSP-BLE | | 116-BGA-BLE | |
|--------------|----------|--------------------------------------------|----------|
| Pin | Name | Pin | Name |
| N9 | VSSR | J1, K2, K3, K4, K5, L1, L3, L4, L5, M3, M8 | VSSR |
| P9 | VDDR2 | M1 | VDDR2 |
| P6,P7 | VSSR | J1, K2, K3, K4, K5, L1, L3, L4, L5, M3, M8 | VSSR |
| P8 | VDDR3 | M2 | VDDR3 |
| P1 | VSS | J1, K2, K3, K4, K5, L1, L3, L4, L5, M3, M8 | VSSR |
| M5 | XI | M4 | XI |
| P5 | XO | M5 | XO |
| M3 | VSSR | J1, K2, K3, K4, K5, L1, L3, L4, L5, M3, M8 | VSSR |
| M4 | DVDD | M6 | DVDD |
| P1 | VSS | J1, K2, K3, K4, K5, L1, L3, L4, L5, M3, M8 | VSSR |
| P4 | VD CDC | M7 | VD CDC |
| P2 | NC | | |
| P3 | VSSR | J1, K2, K3, K4, K5, L1, L3, L4, L5, M3, M8 | VSSR |
| L2 | VDDR_HVL | L7 | VDDR_HVL |
| J7 | P5.0 | L6 | P5.0 |
| J5 | P5.1 | K6 | P5.1 |
| J6 | P5.2 | J6 | P5.2 |
| H7 | P5.3 | K7 | P5.3 |
| H6 | P5.4 | J7 | P5.4 |
| J4 | P5.5 | L8 | P5.5 |
| K3 | P5.6 | M9 | P5.6 |
| K4 | P5.7 | | |
| L2 | VDDR_HVL | L7 | VDDR_HVL |
| L2 | VDDR_HVL | L7 | VDDR_HVL |
| J3 | P6.0 | K8 | P6.0 |
| B2 | P10.1 | A8 | P10.1 |
| C3 | P10.2 | F6 | P10.2 |
| E4 | P10.3 | E6 | P10.3 |
| A2 | P10.4 | D6 | P10.4 |
| A3 | P10.5 | B7 | P10.5 |
| D5 | P10.6 | A7 | P10.6 |
| B3 | P10.7 | | |

Table 1. Pinouts for 116-BGA and 104-MCSP Packages (continued)

| 104-MCSP-BLE | | 116-BGA-BLE | | 104-MCSP-BLE | | 116-BGA-BLE | |
|--------------|--------|-------------|--------|----------------|--------|--------------------|--------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| N1 | P7.0 | J10 | P7.0 | C4 | P11.0 | F5 | P11.0 |
| G6 | P7.1 | H10 | P7.1 | C5 | P11.1 | E5 | P11.1 |
| H4 | P7.2 | H8 | P7.2 | D6 | P11.2 | D5 | P11.2 |
| G5 | P7.3 | H7 | P7.3 | | | B10 | VREF |
| H3 | P7.4 | H6 | P7.4 | A1 | VDDA | A9 | VDDA |
| H2 | P7.5 | G9 | P7.5 | A1 | VDDA | A9 | VDDA |
| G3 | P7.6 | G8 | P7.6 | C2 | P10.0 | B8 | P10.0 |
| G2 | P7.7 | G7 | P7.7 | B4 | P11.3 | C6 | P11.3 |
| D1 | VDDIO1 | G10 | VDDIO1 | A4 | P11.4 | B6 | P11.4 |
| G4 | P8.0 | F10 | P8.0 | B5 | P11.5 | A6 | P11.5 |
| G1 | P8.1 | F9 | P8.1 | A5 | P11.6 | B5 | P11.6 |
| F3 | P8.2 | F8 | P8.2 | A6 | P11.7 | A5 | P11.7 |
| F2 | P8.3 | F7 | P8.3 | B6 | VDDIO0 | B3 | VDDIO0 |
| F1 | P8.4 | G6 | P8.4 | D7, D4, F4, G7 | VSS | B2, B9, H2, H9, D1 | VSS |
| E3 | P8.5 | E9 | P8.5 | B7 | P12.0 | A4 | P12.0 |
| E1 | P8.6 | E8 | P8.6 | A7 | P12.1 | B4 | P12.1 |
| E2 | P8.7 | E7 | P8.7 | B8 | P12.2 | C4 | P12.2 |
| A1 | VDDA | A9 | VDDA | A8 | P12.3 | A3 | P12.3 |
| D2 | P9.0 | D10 | P9.0 | C8 | P12.4 | C5 | P12.4 |
| C1 | P9.1 | D9 | P9.1 | | | D4 | P12.5 |
| D3 | P9.2 | D8 | P9.2 | | | G5 | P12.6 |
| B1 | P9.3 | D7 | P9.3 | | | H5 | P12.7 |
| | | C10 | P9.4 | A9 | P13.0 | H4 | P13.0 |
| | | C9 | P9.5 | B9 | P13.1 | G4 | P13.1 |
| | | C8 | P9.6 | | | F4 | P13.6 |
| | | C7 | P9.7 | | | C3 | P13.7 |

Note: Balls H5 and J9 are No-Connects (NC) in the 104-MCSP package.

The correspondence of power supplies to ports by package type is as follows:

- P0: VBACKUP
- P1: VDDD. Port 1 Pins are Over-Voltage Tolerant (OVT).
- P5, P6, P7, P8: VDDIO1
- P9, P10: VDDA
- P11, P12, P13: VDDIO0

Each Port Pin has multiple alternate functions. These are defined in [Table 2](#).

Table 2. Multiple Alternate Functions

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|-------------------------|--------------------------|-------|----------------|--------|-------------------|------------------|----------------------|--------------------|---------|------------------------|------------------------|---------|---------|-------|-----------------|-------|
| P0.0 | tcpwm[0].line[0]:0 | tcpwm[1].line[0]:0 | | srss.ext_clk:0 | | | | scb[0].spi_select1:0 | | | peri.tr_io_input[0]:0 | | | | | | |
| P0.1 | tcpwm[0].line_comp[0]:0 | tcpwm[1].line_comp[0]:0 | | | | | | scb[0].spi_select2:0 | | | peri.tr_io_input[1]:0 | | | | | cpuss.swj_trstn | |
| P0.2 | tcpwm[0].line[1]:0 | tcpwm[1].line[1]:0 | | | | scb[0].uart_rx:0 | scb[0].i2c_scl:0 | scb[0].spi_mosi:0 | | | | | | | | | |
| P0.3 | tcpwm[0].line_comp[1]:0 | tcpwm[1].line_comp[1]:0 | | | | scb[0].uart_tx:0 | scb[0].i2c_sda:0 | scb[0].spi_miso:0 | | | | | | | | | |
| P0.4 | tcpwm[0].line[2]:0 | tcpwm[1].line[2]:0 | | | | scb[0].uart_rts:0 | | scb[0].spi_clk:0 | | | | peri.tr_io_output[0]:2 | | | | | |
| P0.5 | tcpwm[0].line_comp[2]:0 | tcpwm[1].line_comp[2]:0 | | srss.ext_clk:1 | | scb[0].uart_cts:0 | | scb[0].spi_select0:0 | | | | peri.tr_io_output[1]:2 | | | | | |
| P1.0 | tcpwm[0].line[3]:0 | tcpwm[1].line[3]:0 | | | | scb[7].uart_rx:0 | scb[7].i2c_scl:0 | scb[7].spi_mosi:0 | | | peri.tr_io_input[2]:0 | | | | | | |
| P1.1 | tcpwm[0].line_comp[3]:0 | tcpwm[1].line_comp[3]:0 | | | | scb[7].uart_tx:0 | scb[7].i2c_sda:0 | scb[7].spi_miso:0 | | | peri.tr_io_input[3]:0 | | | | | | |
| P1.2 | tcpwm[0].line[4]:4 | tcpwm[1].line[12]:1 | | | | scb[7].uart_rts:0 | | scb[7].spi_clk:0 | | | | | | | | | |
| P1.3 | tcpwm[0].line_comp[4]:4 | tcpwm[1].line_comp[12]:1 | | | | scb[7].uart_cts:0 | | scb[7].spi_select0:0 | | | | | | | | | |
| P1.4 | tcpwm[0].line[5]:4 | tcpwm[1].line[13]:1 | | | | | | scb[7].spi_select1:0 | | | | | | | | | |
| P1.5 | tcpwm[0].line_comp[5]:4 | tcpwm[1].line_comp[14]:1 | | | | | | scb[7].spi_select2:0 | | | | | | | | | |
| P5.0 | tcpwm[0].line[4]:0 | tcpwm[1].line[4]:0 | | | | scb[5].uart_rx:0 | scb[5].i2c_scl:0 | scb[5].spi_mosi:0 | audioss.clk_i2s_if | | peri.tr_io_input[10]:0 | | | | | | |
| P5.1 | tcpwm[0].line_comp[4]:0 | tcpwm[1].line_comp[4]:0 | | | | scb[5].uart_tx:0 | scb[5].i2c_sda:0 | scb[5].spi_miso:0 | audioss.tx_sck | | peri.tr_io_input[11]:0 | | | | | | |
| P5.2 | tcpwm[0].line[5]:0 | tcpwm[1].line[5]:0 | | | | scb[5].uart_rts:0 | | scb[5].spi_clk:0 | audioss.tx_ws | | | | | | | | |
| P5.3 | tcpwm[0].line_comp[5]:0 | tcpwm[1].line_comp[5]:0 | | | | scb[5].uart_cts:0 | | scb[5].spi_select0:0 | audioss.tx_sdo | | | | | | | | |
| P5.4 | tcpwm[0].line[6]:0 | tcpwm[1].line[6]:0 | | | | | | scb[5].spi_select1:0 | audioss.rx_sck | | | | | | | | |
| P5.5 | tcpwm[0].line_comp[6]:0 | tcpwm[1].line_comp[6]:0 | | | | | | scb[5].spi_select2:0 | audioss.rx_ws | | | | | | | | |

Table 2. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|-------------------------|--------------------------|------------------|--------|--------|-------------------|------------------|----------------------|-------------------|----------------|------------------------|------------------------|----------------------------|-----------------------|-------|----------------------|----------------------|
| P5.6 | tcpwm[0].line[7]:0 | tcpwm[1].line[7]:0 | | | | | | scb[5].spi_select3:0 | | audioss.rx_sdi | | | | | | | |
| P5.7 | tcpwm[0].line_comp[7]:0 | tcpwm[1].line_comp[7]:0 | | | | | | scb[3].spi_select3:0 | | | | | | | | | |
| P6.0 | tcpwm[0].line[0]:1 | tcpwm[1].line[8]:0 | scb[8].i2c_scl:0 | | | scb[3].uart_rx:0 | scb[3].i2c_scl:0 | scb[3].spi_mosi:0 | | | | | cpuss.fault_out[0] | | | | scb[8].spi_mosi:0 |
| P6.1 | tcpwm[0].line_comp[0]:1 | tcpwm[1].line_comp[8]:0 | scb[8].i2c_sda:0 | | | scb[3].uart_tx:0 | scb[3].i2c_sda:0 | scb[3].spi_miso:0 | | | | | cpuss.fault_out[1] | | | | scb[8].spi_miso:0 |
| P6.2 | tcpwm[0].line[1]:1 | tcpwm[1].line[9]:0 | | | | scb[3].uart_rts:0 | | scb[3].spi_clk:0 | | | | | | | | | scb[8].spi_clk:0 |
| P6.3 | tcpwm[0].line_comp[1]:1 | tcpwm[1].line_comp[9]:0 | | | | scb[3].uart_cts:0 | | scb[3].spi_select0:0 | | | | | | | | | scb[8].spi_select0:0 |
| P6.4 | tcpwm[0].line[2]:1 | tcpwm[1].line[10]:0 | scb[8].i2c_scl:1 | | | scb[6].uart_rx:2 | scb[6].i2c_scl:2 | scb[6].spi_mosi:2 | | | peri.tr_io_input[12]:0 | peri.tr_io_output[0]:1 | | | | cpuss.swj_swo_tdo | scb[8].spi_mosi:1 |
| P6.5 | tcpwm[0].line_comp[2]:1 | tcpwm[1].line_comp[10]:0 | scb[8].i2c_sda:1 | | | scb[6].uart_tx:2 | scb[6].i2c_sda:2 | scb[6].spi_miso:2 | | | peri.tr_io_input[13]:0 | peri.tr_io_output[1]:1 | | | | cpuss.swj_swdoe_tdi | scb[8].spi_miso:1 |
| P6.6 | tcpwm[0].line[3]:1 | tcpwm[1].line[11]:0 | | | | scb[6].uart_rts:2 | | scb[6].spi_clk:2 | | | | | | | | cpuss.swj_swdio_tms | scb[8].spi_clk:1 |
| P6.7 | tcpwm[0].line_comp[3]:1 | tcpwm[1].line_comp[11]:0 | | | | scb[6].uart_cts:2 | | scb[6].spi_select0:2 | | | | | | | | cpuss.swj_swclk_tclk | scb[8].spi_select0:1 |
| P7.0 | tcpwm[0].line[4]:1 | tcpwm[1].line[12]:0 | | | | scb[4].uart_rx:1 | scb[4].i2c_scl:1 | scb[4].spi_mosi:1 | | | peri.tr_io_input[14]:0 | | cpuss.trace_clock | | | | |
| P7.1 | tcpwm[0].line_comp[4]:1 | tcpwm[1].line_comp[12]:0 | | | | scb[4].uart_tx:1 | scb[4].i2c_sda:1 | scb[4].spi_miso:1 | | | peri.tr_io_input[15]:0 | | | | | | |
| P7.2 | tcpwm[0].line[5]:1 | tcpwm[1].line[13]:0 | | | | scb[4].uart_rts:1 | | scb[4].spi_clk:1 | | | | | | | | | |
| P7.3 | tcpwm[0].line_comp[5]:1 | tcpwm[1].line_comp[13]:0 | | | | scb[4].uart_cts:1 | | scb[4].spi_select0:1 | | | | | | | | | |
| P7.4 | tcpwm[0].line[6]:1 | tcpwm[1].line[14]:0 | | | | | | scb[4].spi_select1:1 | | | | | bless.ext_nrx_ctl_out | cpuss.trace_data[3]:2 | | | |
| P7.5 | tcpwm[0].line_comp[6]:1 | tcpwm[1].line_comp[14]:0 | | | | | | scb[4].spi_select2:1 | | | | | bless.ext_pax_ctl_out | cpuss.trace_data[2]:2 | | | |
| P7.6 | tcpwm[0].line[7]:1 | tcpwm[1].line[15]:0 | | | | | | scb[4].spi_select3:1 | | | | | bless.ext_pana_chip_en_out | cpuss.trace_data[1]:2 | | | |
| P7.7 | tcpwm[0].line_comp[7]:1 | tcpwm[1].line_comp[15]:0 | | | | | | scb[3].spi_select1:0 | cpuss.clk_fm_pump | | | | | cpuss.trace_data[0]:2 | | | |

Table 2. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|-------------------------|--------------------------|-------|--------|--------|-------------------|------------------|----------------------|--------|---------------------|------------------------|---------|---------|-----------------------|-------|-------|-------|
| P8.0 | tcpwm[0].line[0]:2 | tcpwm[1].line[16]:0 | | | | scb[4].uart_rx:0 | scb[4].i2c_scl:0 | scb[4].spi_mosi:0 | | | peri.tr_io_input[16]:0 | | | | | | |
| P8.1 | tcpwm[0].line_comp[0]:2 | tcpwm[1].line_comp[16]:0 | | | | scb[4].uart_tx:0 | scb[4].i2c_sda:0 | scb[4].spi_miso:0 | | | peri.tr_io_input[17]:0 | | | | | | |
| P8.2 | tcpwm[0].line[1]:2 | tcpwm[1].line[17]:0 | | | | scb[4].uart_rts:0 | | scb[4].spi_clk:0 | | | | | | | | | |
| P8.3 | tcpwm[0].line_comp[1]:2 | tcpwm[1].line_comp[17]:0 | | | | scb[4].uart_cts:0 | | scb[4].spi_select0:0 | | | | | | | | | |
| P8.4 | tcpwm[0].line[2]:2 | tcpwm[1].line[18]:0 | | | | | | scb[4].spi_select1:0 | | | | | | | | | |
| P8.5 | tcpwm[0].line_comp[2]:2 | tcpwm[1].line_comp[18]:0 | | | | | | scb[4].spi_select2:0 | | | | | | | | | |
| P8.6 | tcpwm[0].line[3]:2 | tcpwm[1].line[19]:0 | | | | | | scb[4].spi_select3:0 | | | | | | | | | |
| P8.7 | tcpwm[0].line_comp[3]:2 | tcpwm[1].line_comp[19]:0 | | | | | | scb[3].spi_select2:0 | | | | | | | | | |
| P9.0 | tcpwm[0].line[4]:2 | tcpwm[1].line[20]:0 | | | | scb[2].uart_rx:0 | scb[2].i2c_scl:0 | scb[2].spi_mosi:0 | | | peri.tr_io_input[18]:0 | | | cpuss.trace_data[3]:0 | | | |
| P9.1 | tcpwm[0].line_comp[4]:2 | tcpwm[1].line_comp[20]:0 | | | | scb[2].uart_tx:0 | scb[2].i2c_sda:0 | scb[2].spi_miso:0 | | | peri.tr_io_input[19]:0 | | | cpuss.trace_data[2]:0 | | | |
| P9.2 | tcpwm[0].line[5]:2 | tcpwm[1].line[21]:0 | | | | scb[2].uart_rts:0 | | scb[2].spi_clk:0 | | pass.dsi_ctb_cmp0:1 | | | | cpuss.trace_data[1]:0 | | | |
| P9.3 | tcpwm[0].line_comp[5]:2 | tcpwm[1].line_comp[21]:0 | | | | scb[2].uart_cts:0 | | scb[2].spi_select0:0 | | pass.dsi_ctb_cmp1:1 | | | | cpuss.trace_data[0]:0 | | | |
| P9.4 | tcpwm[0].line[7]:5 | tcpwm[1].line[0]:2 | | | | | | scb[2].spi_select1:0 | | | | | | | | | |
| P9.5 | tcpwm[0].line_comp[7]:5 | tcpwm[1].line_comp[0]:2 | | | | | | scb[2].spi_select2:0 | | | | | | | | | |
| P9.6 | tcpwm[0].line[0]:6 | tcpwm[1].line[1]:2 | | | | | | scb[2].spi_select3:0 | | | | | | | | | |
| P9.7 | tcpwm[0].line_comp[0]:6 | tcpwm[1].line_comp[1]:2 | | | | | | | | | | | | | | | |
| P10.0 | tcpwm[0].line[6]:2 | tcpwm[1].line[22]:0 | | | | scb[1].uart_rx:1 | scb[1].i2c_scl:1 | scb[1].spi_mosi:1 | | | peri.tr_io_input[20]:0 | | | cpuss.trace_data[3]:1 | | | |
| P10.1 | tcpwm[0].line_comp[6]:2 | tcpwm[1].line_comp[22]:0 | | | | scb[1].uart_tx:1 | scb[1].i2c_sda:1 | scb[1].spi_miso:1 | | | peri.tr_io_input[21]:0 | | | cpuss.trace_data[2]:1 | | | |

Table 2. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|-------------------------|---------------------------|-------|--------|------------------|-------------------|------------------|----------------------|------------------|---------|---------|---------|---------|-----------------------|------------------------|-------|-------|
| P10.2 | tcpwm[0].line[7]:2 | tcpwm[1].line[23]:0 | | | | scb[1].uart_rts:1 | | scb[1].spi_clk:1 | | | | | | cpuss.trace_data[1]:1 | | | |
| P10.3 | tcpwm[0].line_comp[7]:2 | tcpwm[1].line_compl[23]:0 | | | | scb[1].uart_cts:1 | | scb[1].spi_select0:1 | | | | | | cpuss.trace_data[0]:1 | | | |
| P10.4 | tcpwm[0].line[0]:3 | tcpwm[1].line[0]:1 | | | | | | scb[1].spi_select1:1 | audioss.pdm_clk | | | | | | | | |
| P10.5 | tcpwm[0].line_comp[0]:3 | tcpwm[1].line_compl[0]:1 | | | | | | scb[1].spi_select2:1 | audioss.pdm_data | | | | | | | | |
| P10.6 | tcpwm[0].line[1]:6 | tcpwm[1].line[2]:2 | | | | | | scb[1].spi_select3:1 | | | | | | | | | |
| P10.7 | tcpwm[0].line_comp[1]:6 | tcpwm[1].line_compl[2]:2 | | | | | | | | | | | | | | | |
| P11.0 | tcpwm[0].line[1]:3 | tcpwm[1].line[1]:1 | | | smif.spi_select2 | scb[5].uart_rx:1 | scb[5].i2c_scl:1 | scb[5].spi_mosi:1 | | | | | | | peri.tr_io_input[22]:0 | | |
| P11.1 | tcpwm[0].line_comp[1]:3 | tcpwm[1].line_compl[1]:1 | | | smif.spi_select1 | scb[5].uart_tx:1 | scb[5].i2c_sda:1 | scb[5].spi_miso:1 | | | | | | | peri.tr_io_input[23]:0 | | |
| P11.2 | tcpwm[0].line[2]:3 | tcpwm[1].line[2]:1 | | | smif.spi_select0 | scb[5].uart_rts:1 | | scb[5].spi_clk:1 | | | | | | | | | |
| P11.3 | tcpwm[0].line_comp[2]:3 | tcpwm[1].line_compl[2]:1 | | | smif.spi_data3 | scb[5].uart_cts:1 | | scb[5].spi_select0:1 | | | | | | | peri.tr_io_output[0]:0 | | |
| P11.4 | tcpwm[0].line[3]:3 | tcpwm[1].line[3]:1 | | | smif.spi_data2 | | | scb[5].spi_select1:1 | | | | | | | peri.tr_io_output[1]:0 | | |
| P11.5 | tcpwm[0].line_comp[3]:3 | tcpwm[1].line_compl[3]:1 | | | smif.spi_data1 | | | scb[5].spi_select2:1 | | | | | | | | | |
| P11.6 | | | | | smif.spi_data0 | | | scb[5].spi_select3:1 | | | | | | | | | |
| P11.7 | | | | | smif.spi_clk | | | | | | | | | | | | |
| P12.0 | tcpwm[0].line[4]:3 | tcpwm[1].line[4]:1 | | | smif.spi_data4 | scb[6].uart_rx:0 | scb[6].i2c_scl:0 | scb[6].spi_mosi:0 | | | | | | | peri.tr_io_input[24]:0 | | |
| P12.1 | tcpwm[0].line_comp[4]:3 | tcpwm[1].line_compl[4]:1 | | | smif.spi_data5 | scb[6].uart_tx:0 | scb[6].i2c_sda:0 | scb[6].spi_miso:0 | | | | | | | peri.tr_io_input[25]:0 | | |
| P12.2 | tcpwm[0].line[5]:3 | tcpwm[1].line[5]:1 | | | smif.spi_data6 | scb[6].uart_rts:0 | | scb[6].spi_clk:0 | | | | | | | | | |
| P12.3 | tcpwm[0].line_comp[5]:3 | tcpwm[1].line_compl[5]:1 | | | smif.spi_data7 | scb[6].uart_cts:0 | | scb[6].spi_select0:0 | | | | | | | | | |
| P12.4 | tcpwm[0].line[6]:3 | tcpwm[1].line[6]:1 | | | smif.spi_select3 | | | scb[6].spi_select1:0 | audioss.pdm_clk | | | | | | | | |

Table 2. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|-------------------------|--------------------------|-------|--------|--------|-------------------|------------------|----------------------|------------------|---------|---------|---------|------------------------|---------|-------|-------|-------|
| P12.5 | tcpwm[0].line_comp[6]:3 | tcpwm[1].line_comp[6]:1 | | | | | | scb[6].spi_select2:0 | audioss.pdm_data | | | | | | | | |
| P12.6 | tcpwm[0].line[7]:3 | tcpwm[1].line[7]:1 | | | | | | scb[6].spi_select3:0 | | | | | | | | | |
| P12.7 | tcpwm[0].line_comp[7]:3 | tcpwm[1].line_comp[7]:1 | | | | | | | | | | | | | | | |
| P13.0 | tcpwm[0].line[0]:4 | tcpwm[1].line[8]:1 | | | | scb[6].uart_rx:1 | scb[6].i2c_scl:1 | scb[6].spi_mosi:1 | | | | | peri.tr_io_input[26]:0 | | | | |
| P13.1 | tcpwm[0].line_comp[0]:4 | tcpwm[1].line_comp[8]:1 | | | | scb[6].uart_tx:1 | scb[6].i2c_sda:1 | scb[6].spi_miso:1 | | | | | peri.tr_io_input[27]:0 | | | | |
| P13.2 | tcpwm[0].line[1]:4 | tcpwm[1].line[9]:1 | | | | scb[6].uart_rts:1 | | scb[6].spi_clk:1 | | | | | | | | | |
| P13.3 | tcpwm[0].line_comp[1]:4 | tcpwm[1].line_comp[9]:1 | | | | scb[6].uart_cts:1 | | scb[6].spi_select0:1 | | | | | | | | | |
| P13.4 | tcpwm[0].line[2]:4 | tcpwm[1].line[10]:1 | | | | | | scb[6].spi_select1:1 | | | | | | | | | |
| P13.5 | tcpwm[0].line_comp[2]:4 | tcpwm[1].line_comp[10]:1 | | | | | | scb[6].spi_select2:1 | | | | | | | | | |
| P13.6 | tcpwm[0].line[3]:4 | tcpwm[1].line[11]:1 | | | | | | scb[6].spi_select3:1 | | | | | | | | | |
| P13.7 | tcpwm[0].line_comp[3]:4 | tcpwm[1].line_comp[11]:1 | | | | | | | | | | | | | | | |

Analog, Smart I/O, and DSI alternate Port Pin functionality is provided in [Table 3](#).

Table 3. Port Pin Analog, Smart I/O, and DSI Functions

| Port/Pin | Name | Analog | Digital HV | DSI | SMARTIO |
|----------|------|------------------|---------------------------------------|-------------------|---------|
| P0.0 | P0.0 | wco_in | | dsi[0].port_if[0] | |
| P0.1 | P0.1 | wco_out | | dsi[0].port_if[1] | |
| P0.2 | P0.2 | | | dsi[0].port_if[2] | |
| P0.3 | P0.3 | | | dsi[0].port_if[3] | |
| P0.4 | P0.4 | | pmic_wakeup_in hibernate_wakeup[1] | dsi[0].port_if[4] | |
| P0.5 | P0.5 | | pmic_wakeup_out | dsi[0].port_if[5] | |
| P1.0 | P1.0 | | | dsi[1].port_if[0] | |
| P1.1 | P1.1 | | | dsi[1].port_if[1] | |
| P1.2 | P1.2 | | | dsi[1].port_if[2] | |
| P1.3 | P1.3 | | | dsi[1].port_if[3] | |
| P1.4 | P1.4 | | hibernate_wakeup[0] | dsi[1].port_if[4] | |
| P1.5 | P1.5 | | | dsi[1].port_if[5] | |
| P2.0 | P2.0 | | | dsi[2].port_if[0] | |
| P2.1 | P2.1 | | | dsi[2].port_if[1] | |
| P2.2 | P2.2 | | | dsi[2].port_if[2] | |
| P2.3 | P2.3 | | | dsi[2].port_if[3] | |
| P2.4 | P2.4 | | | dsi[2].port_if[4] | |
| P2.5 | P2.5 | | | dsi[2].port_if[5] | |
| P2.6 | P2.6 | | | dsi[2].port_if[6] | |
| P2.7 | P2.7 | | | dsi[2].port_if[7] | |
| P3.0 | P3.0 | | | | |
| P3.1 | P3.1 | | | | |
| P3.2 | P3.2 | | | | |
| P3.3 | P3.3 | | | | |
| P3.4 | P3.4 | | | | |
| P3.5 | P3.5 | | | | |
| P4.0 | P4.0 | | | dsi[0].port_if[6] | |
| P4.1 | P4.1 | | | dsi[0].port_if[7] | |
| P4.2 | P4.2 | | | dsi[1].port_if[6] | |
| P4.3 | P4.3 | | | dsi[1].port_if[7] | |
| P5.0 | P5.0 | | | dsi[3].port_if[0] | |
| P5.1 | P5.1 | | | dsi[3].port_if[1] | |
| P5.2 | P5.2 | | | dsi[3].port_if[2] | |
| P5.3 | P5.3 | | | dsi[3].port_if[3] | |
| P5.4 | P5.4 | | | dsi[3].port_if[4] | |
| P5.5 | P5.5 | | | dsi[3].port_if[5] | |
| P5.6 | P5.6 | lpcomp.inp_comp0 | | dsi[3].port_if[6] | |
| P5.7 | P5.7 | lpcomp.inn_comp0 | | dsi[3].port_if[7] | |
| P6.0 | P6.0 | | | dsi[4].port_if[0] | |
| P6.1 | P6.1 | | | dsi[4].port_if[1] | |
| P6.2 | P6.2 | lpcomp.inp_comp1 | | dsi[4].port_if[2] | |

Table 3. Port Pin Analog, Smart I/O, and DSI Functions *(continued)*

| Port/Pin | Name | Analog | Digital HV | DSI | SMARTIO |
|----------|-------|--------------------------------------|------------|--------------------|------------------|
| P6.3 | P6.3 | lpcomp.inn_comp1 | | dsi[4].port_if[3] | |
| P6.4 | P6.4 | | | dsi[4].port_if[4] | |
| P6.5 | P6.5 | | | dsi[4].port_if[5] | |
| P6.6 | P6.6 | | swd_data | dsi[4].port_if[6] | |
| P6.7 | P6.7 | | swd_clk | dsi[4].port_if[7] | |
| P7.0 | P7.0 | | | dsi[5].port_if[0] | |
| P7.1 | P7.1 | csd.cmodpadd csd.cmodpads | | dsi[5].port_if[1] | |
| P7.2 | P7.2 | csd.csh_tankpadd csd.csh_tankpads | | dsi[5].port_if[2] | |
| P7.3 | P7.3 | csd.vref_ext | | dsi[5].port_if[3] | |
| P7.4 | P7.4 | | | dsi[5].port_if[4] | |
| P7.5 | P7.5 | | | dsi[5].port_if[5] | |
| P7.6 | P7.6 | | | dsi[5].port_if[6] | |
| P7.7 | P7.7 | csd.cshieldpads | | dsi[5].port_if[7] | |
| P8.0 | P8.0 | | | dsi[11].port_if[0] | smartio[8].io[0] |
| P8.1 | P8.1 | | | dsi[11].port_if[1] | smartio[8].io[1] |
| P8.2 | P8.2 | | | dsi[11].port_if[2] | smartio[8].io[2] |
| P8.3 | P8.3 | | | dsi[11].port_if[3] | smartio[8].io[3] |
| P8.4 | P8.4 | | | dsi[11].port_if[4] | smartio[8].io[4] |
| P8.5 | P8.5 | | | dsi[11].port_if[5] | smartio[8].io[5] |
| P8.6 | P8.6 | | | dsi[11].port_if[6] | smartio[8].io[6] |
| P8.7 | P8.7 | | | dsi[11].port_if[7] | smartio[8].io[7] |
| P9.0 | P9.0 | ctb_oa0+ | | dsi[10].port_if[0] | smartio[9].io[0] |
| P9.1 | P9.1 | ctb_oa0- | | dsi[10].port_if[1] | smartio[9].io[1] |
| P9.2 | P9.2 | ctb_oa0_out | | dsi[10].port_if[2] | smartio[9].io[2] |
| P9.3 | P9.3 | ctb_oa1_out | | dsi[10].port_if[3] | smartio[9].io[3] |
| P9.4 | P9.4 | ctb_oa1- | | dsi[10].port_if[4] | smartio[9].io[4] |
| P9.5 | P9.5 | ctb_oa1+ | | dsi[10].port_if[5] | smartio[9].io[5] |
| P9.6 | P9.6 | ctb_oa0+ | | dsi[10].port_if[6] | smartio[9].io[6] |
| P9.7 | P9.7 | ctb_oa1+ or ext_vref | | dsi[10].port_if[7] | smartio[9].io[7] |
| P10.0 | P10.0 | sarmux[0] | | dsi[9].port_if[0] | |
| P10.1 | P10.1 | sarmux[1] | | dsi[9].port_if[1] | |
| P10.2 | P10.2 | sarmux[2] | | dsi[9].port_if[2] | |
| P10.3 | P10.3 | sarmux[3] | | dsi[9].port_if[3] | |
| P10.4 | P10.4 | sarmux[4] | | dsi[9].port_if[4] | |
| P10.5 | P10.5 | sarmux[5] | | dsi[9].port_if[5] | |
| P10.6 | P10.6 | sarmux[6] | | dsi[9].port_if[6] | |
| P10.7 | P10.7 | sarmux[7] | | dsi[9].port_if[7] | |
| P11.0 | P11.0 | | | dsi[8].port_if[0] | |
| P11.1 | P11.1 | | | dsi[8].port_if[1] | |

Table 3. Port Pin Analog, Smart I/O, and DSI Functions *(continued)*

| Port/Pin | Name | Analog | Digital HV | DSI | SMARTIO |
|----------|-------|--------------|------------|-------------------|---------|
| P11.2 | P11.2 | | | dsi[8].port_if[2] | |
| P11.3 | P11.3 | | | dsi[8].port_if[3] | |
| P11.4 | P11.4 | | | dsi[8].port_if[4] | |
| P11.5 | P11.5 | | | dsi[8].port_if[5] | |
| P11.6 | P11.6 | | | dsi[8].port_if[6] | |
| P11.7 | P11.7 | | | dsi[8].port_if[7] | |
| P12.0 | P12.0 | | | dsi[7].port_if[0] | |
| P12.1 | P12.1 | | | dsi[7].port_if[1] | |
| P12.2 | P12.2 | | | dsi[7].port_if[2] | |
| P12.3 | P12.3 | | | dsi[7].port_if[3] | |
| P12.4 | P12.4 | | | dsi[7].port_if[4] | |
| P12.5 | P12.5 | | | dsi[7].port_if[5] | |
| P12.6 | P12.6 | srss.eco_in | | dsi[7].port_if[6] | |
| P12.7 | P12.7 | srss.eco_out | | dsi[7].port_if[7] | |
| P13.0 | P13.0 | | | dsi[6].port_if[0] | |
| P13.1 | P13.1 | | | dsi[6].port_if[1] | |
| P13.2 | P13.2 | | | dsi[6].port_if[2] | |
| P13.3 | P13.3 | | | dsi[6].port_if[3] | |
| P13.4 | P13.4 | | | dsi[6].port_if[4] | |
| P13.5 | P13.5 | | | dsi[6].port_if[5] | |
| P13.6 | P13.6 | | | dsi[6].port_if[6] | |
| P13.7 | P13.7 | | | dsi[6].port_if[7] | |

Power

The power system diagram (see [Figure 3](#)) shows the general requirements for power pins on the PSoC 63. The diagram also shows the radio pins that need to be decoupled. The PSoC 63 power scheme allows different VDDIO and VDDA connections. Since no sequencing requirements need to be analyzed and specified, customers may bring up the power supplies in any order and the power system is responsible for ensuring power is good in all domains before allowing operation. VDDD, VDDA, and VDDIO may be separate nets, which are not ohmically connected on chip. Depending on different package requirements, these may be required to be connected off chip.

The power system will have a buck regulator in addition to an LDO. A Single Input Multiple Output (SIMO) Buck regulator with multiple outputs allows saving an inductor and also providing a high-efficiency supply to the radio.

The preliminary diagram is shown in [Figure 3](#).

Figure 3. SOC Power Connections with Radio (For 104-CSP and 116-BGA Packages)

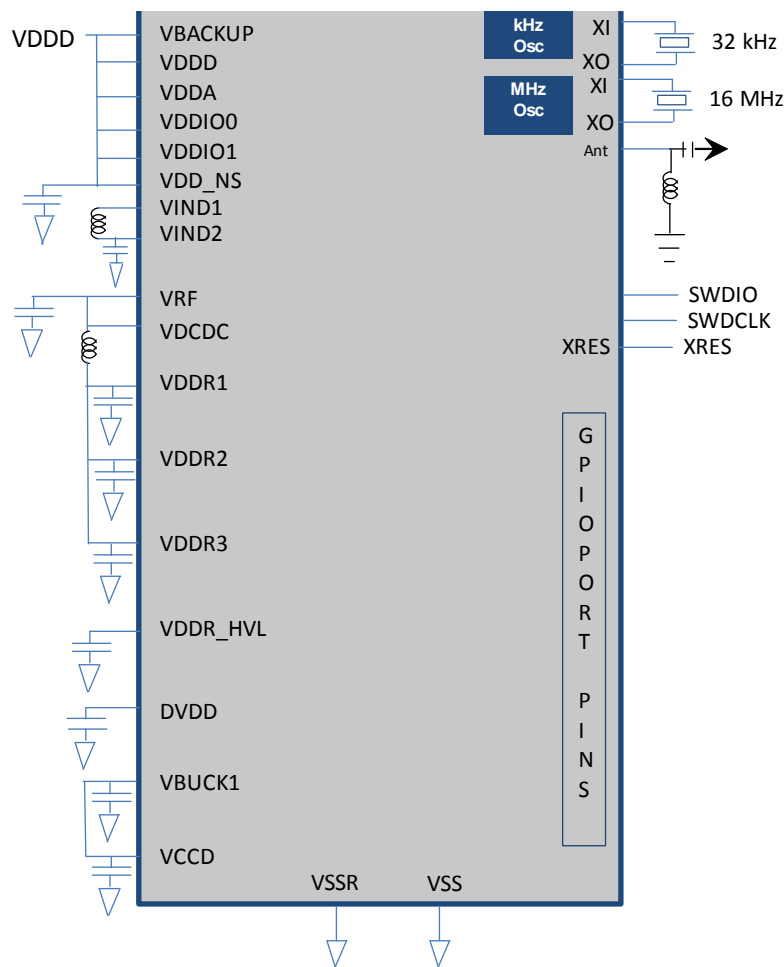


Figure 3 shows the power supply pins to the PSoC and the connections between the PSoC and the radio. It also shows which pins need bypass capacitors.

Description of power pins is as follows:

1. VBACKUP is the supply to the backup domain. The backup domain includes the 32-kHz WCO, RTC, and backup registers. It can generate a wake-up interrupt to the chip via the RTC timers or an external input. It can also generate an output to wakeup external circuitry. It is connected to VDDD when not used as a separate battery backup domain. VBACKUP provides the supply for Port 0.
2. VDDD is the main digital supply input (1.7 to 3.6 V). It provides the inputs for the internal Regulators and for Port 1.
3. VDDA is the supply for analog peripherals (1.7 to 3.6 V). It must be connected to VDDIOA on the PCB.
4. VDDIOA is the supply to for Ports 9 and 10. It must be connected to VDDA on the PCB when present. Ports 9 and 10 are supplied by VDDA when VDDIOA is not present.
5. VDD_NS is the supply input to the Buck and should be at the same potential as VDDD. The bypass capacitor between VDD_NS and ground should be 10 μ F.
6. VDDIO0 is the Supply for Ports 11 to 13 when present. When not present, these ports are supplied by VDDD.
7. VDDIO1 is the Supply for Ports 5 to 8 when present. When not present, these ports are supplied by VDDA.
8. VDDIOR is the Supply for Ports 2 to 4 on the 124 BGA only.

All the pins above may be shorted to VDDD as shown in Figure 3.

9. VRF is the output of the SIMO buck going to the Radio and should be connected to VDCDC and decoupled.
10. VDCDC is the digital supply input to the Radio and should be connected to VRF.
11. The VDDR1, VDDR2, and VDDR3 pins are for the radio sub-systems and need to be decoupled individually and connected to VDCDC through a bead for filtering high frequency power supply noise.
12. VDDR_HVL is the regulated output to the Radio from the PSoC 63 subsystem and needs to be decoupled.
13. DVDD is a Digital LDO output from the Radio and needs to be decoupled.
14. VBUCK1 is the SIMO buck output to the internal core logic and is to be connected to VCCD.
15. VCCD is the internal core logic and needs to be connected to VBUCK1 and decoupled.

The supply voltage range is 1.71 to 3.6 V with all functions and circuits operating over that range. All grounds must be shorted together on the PCB. Bypass capacitors must be used from VDDD and VDDA to ground and wherever indicated in the diagram. Typical practice for systems in this frequency range is to use a capacitor in the 10- μ F range in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing. Recommended Buck output capacitor values are 10 μ F for Vrf and 4.7 μ F for VBUCK1. The capacitor connected to Vind2 should be 100 nF. All capacitors should be \pm 20% or better; the recommended inductor value is 2.2 μ H \pm 20% (for example, TDK MLP2012H2R2MT0S1).

Development Support

The PSoC 63 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit <http://www.cypress.com/products/32-bit-arm-cortex-m4-psoc-6> to find out more.

Documentation

A suite of documentation supports the PSoC 63 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at <http://www.cypress.com/products/32-bit-arm-cortex-m4-psoc-6>.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 63 family is part of a development tool ecosystem. Visit us at www.cypress.com/products/psoc-creator-integrated-design-environment-ide for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Note: These are preliminary and subject to change.

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings^[1]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------------------------|---------------------------------------------------------------------------------------------|------|-----|-----------------------|-------|--------------------------|
| SID1 | V _{DD_ABS} | Analog or digital supply relative to V _{SS} (V _{SSD} = V _{SSA}) | -0.5 | - | 4 | V | Absolute Maximum |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SSD} | -0.5 | - | 1.2 | V | Absolute Maximum |
| SID3 | V _{GPIO_ABS} | GPIO voltage; V _{DDD} or V _{DDA} | -0.5 | - | V _{DD} + 0.5 | V | Absolute Maximum |
| SID4 | I _{GPIO_ABS} | Current per GPIO | -25 | - | 25 | mA | Absolute Maximum |
| SID5 | I _{GPIO_injection} | GPIO injection current per pin | -0.5 | - | 0.5 | mA | Absolute Maximum |
| SID3A | ESD_HBM | Electrostatic discharge Human Body Model | 2200 | - | - | V | Absolute Maximum |
| SID3B | ESD_HBM_ANT | Electrostatic discharge Human Body Model; Antenna Pin | 500 | - | - | V | Absolute Maximum; RF pin |
| SID4A | ESD_CDM | Electrostatic discharge Charged Device Model | 500 | - | - | V | Absolute Maximum |
| SID4B | ESD_CDM_ANT | Electrostatic discharge Charged Device Model; Antenna Pin | 200 | - | - | V | Absolute Maximum; RF pin |
| SID5A | LU | Pin current for latchup-free operation | -100 | - | 100 | mA | Absolute Maximum |

Device-Level Specifications

All specifications are valid for -40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------------------|--------------------|--------------------------------------------------------------------|------|-----|------|-------|-----------------------------------------------------|
| DC Specifications | | | | | | | |
| SID6 | V _{DDD} | Internal regulator and Port 1 GPIO supply | 1.7 | - | 3.6 | V | Also supplies Port 0 in 56 QFN |
| SID7 | V _{DDA} | Analog power supply voltage. Shorted to V _{DDIOA} on PCB. | 1.7 | - | 3.6 | V | Internally unregulated Supply |
| SID7A | V _{DDIO1} | GPIO Supply for Ports 5 to 8 when present | 1.7 | - | 3.6 | V | V _{DDIO_1} must be ≥ to V _{DDA} . |
| SID7B | V _{DDIO0} | GPIO Supply for Ports 11 to 13 when present | 1.7 | - | 3.6 | V | |
| SID7E | V _{DDIO0} | Supply for E-Fuse Programming | 2.38 | 2.5 | 2.62 | V | E-Fuse Programming Voltage |
| SID7C | V _{DDIOR} | GPIO supply for Ports 2 to 4 on BGA 124 only | 1.7 | - | 3.6 | V | |
| SID7D | V _{DDIOA} | GPIO Supply for Ports 9 to 10. Shorted to V _{DDA} on PCB. | 1.7 | - | 3.6 | V | Also supplies Ports 5 to 7 in 56 QFN |

Note

- Usage above the absolute maximum conditions listed in Table 4 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------------------------------------------------------------------------------|---------------------|-------------------------------------------------------------------------------------|-----|------|------|-------|----------------------------------------------------|
| SID7F | V _{DDUSB} | Supply for Port 14 (USB or GPIO) when present | 1.7 | – | 3.6 | V | Min supply is 2.85 V for USB |
| SID6B | V _{BACKUP} | Backup Power and GPIO Port 0 supply when present | 1.7 | – | 3.6 | V | Min is 1.4 V in Backup mode |
| SID8 | V _{CCD1} | Output voltage (for core logic bypass) | – | 1.1 | – | V | High-speed mode |
| SID9 | V _{CCD2} | Output voltage (for core logic bypass) | – | 0.9 | – | | ULP mode. Valid for –20 to 85 °C |
| SID10 | C _{EFC} | External regulator voltage (V _{CCD}) bypass | 3.8 | 4.7 | 5.6 | µF | X5R ceramic or better |
| SID11 | C _{EXC} | Power supply decoupling capacitor | – | 10 | – | µF | X5R ceramic or better |
| LP RANGE POWER SPECIFICATIONS (for V_{CCD} = 1.1 V with Buck and LDO) | | | | | | | |
| Cortex M4. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF1 | I _{DD1} | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1). | – | 2.3 | 3.2 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 3.1 | 3.6 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 4.2 | 5.1 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDF2 | I _{DD2} | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1) | – | 0.9 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.2 | 1.6 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.6 | 2.4 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC1 | I _{DD3} | Execute from Cache; CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO & FLL. Dhrystone. | – | 6.3 | 7 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 9.7 | 11.2 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 13.2 | 13.7 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDC2 | I _{DD4} | Execute from Cache; CM4 Active 100 MHz, CM0+ Sleep 100MHz. IMO & FLL. Dhrystone. | – | 4.8 | 5.8 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 7.4 | 8.4 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 10.1 | 10.7 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDC3 | I _{DD5} | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25MHz. IMO & FLL. Dhrystone | – | 2.4 | 3.4 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 3.7 | 4.1 | | V _{DDD} = 1.8V, Buck ON, max at 60 °C |
| | | | – | 5.1 | 5.8 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDC4 | I _{DD6} | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone | – | 0.90 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.27 | 1.75 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.8 | 2.6 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------------------------------------|-------------------|-----------------------------------------------------------------------------|-----|------|-----|-------|----------------------------------------------------|
| Cortex M0+. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF3 | I _{DD7} | Execute from Flash;CM4 Off, CM0+ Active 50 MHz. With IMO & FLL. While (1). | – | 2.4 | 3.3 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 3.2 | 3.7 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 4.1 | 4.8 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDF4 | I _{DD8} | Execute from Flash;CM4 Off, CM0+ Active 8 MHz. With IMO. While (1) | – | 0.8 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.1 | 1.6 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.45 | 1.9 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC5 | I _{DD9} | Execute from Cache;CM4 Off, CM0+ Active 100 MHz. With IMO & FLL. Dhrystone. | – | 3.8 | 4.5 | mA | V _{DDD} = 3.3V, Buck ON, max at 60 °C |
| | | | – | 5.9 | 6.5 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 7.7 | 8.2 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDC6 | I _{DD10} | Execute from Cache;CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone | – | 0.80 | 1.3 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.2 | 1.7 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.41 | 2 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Cortex M4. Sleep Mode | | | | | | | |
| SIDS1 | I _{DD11} | CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. | – | 1.5 | 2.2 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 2.2 | 2.7 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 2.9 | 3.5 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDS2 | I _{DD12} | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL | – | 1.20 | 1.9 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.70 | 2.2 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 2.20 | 2.8 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDS3 | I _{DD13} | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | – | 0.7 | 1.3 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.96 | 1.5 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.22 | 2 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|------------------------------------------------|-------------------|---------------------------------------------------------------------------|-----|------|------|-------|----------------------------------------------------|
| Cortex M0+. Sleep Mode | | | | | | | |
| SIDS4 | I _{DD14} | CM4 Off, CM0+ Sleep 50 MHz. With IMO & FLL. | – | 1.3 | 2 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.94 | 2.4 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 2.57 | 3.2 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDS5 | I _{DD15} | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | – | 0.7 | 1.3 | mA | V _{DDD} = 3.3V, Buck ON, max at 60 °C |
| | | | – | 0.95 | 1.5 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.25 | 2 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Cortex M4. Low Power Active (LPA) Mode | | | | | | | |
| SIDLPA1 | I _{DD16} | Execute from Flash; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1). | – | 0.85 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.18 | 1.65 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.63 | 2.4 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDLPA2 | I _{DD17} | Execute from Cache; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | – | 0.90 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.27 | 1.75 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.77 | 2.5 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Cortex M0+. Low Power Active (LPA) Mode | | | | | | | |
| SIDLPA3 | I _{DD18} | Execute from Flash; CM4 Off, CM0+ LPA 8 MHz. With IMO. While (1) | – | 0.8 | 1.4 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.14 | 1.6 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.6 | 2.4 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDLPA4 | I _{DD19} | Execute from Cache; CM4 Off, CM0+ LPA 8 MHz. With IMO. Dhrystone. | – | 0.8 | 1.4 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.15 | 1.65 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.62 | 2.4 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Cortex M4. Low Power Sleep (LPS) Mode | | | | | | | |
| SIDLPS1 | I _{DD20} | CM4 LPS 8 MHz, CM0+ LPS 8 MHz. With IMO. | – | 0.65 | 1.1 | mA | V _{DDD} =3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.95 | 1.5 | | V _{DDD} =1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.31 | 2.1 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---------------------------------------------------------------------------------------------------------------------------|-------------------|--------------------------------------------------------------------------------------|-----|------|------|-------|----------------------------------------------------|
| Cortex M0+. Low Power Sleep (LPS) Mode | | | | | | | |
| SIDLPS3 | I _{DD22} | CM4 Off, CM0+ LPS 8 MHz. With IMO. | – | 0.64 | 1.1 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.93 | 1.45 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| | | | – | 1.29 | 2 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| ULP RANGE POWER SPECIFICATIONS (for V_{CCD} = 0.9 V using the Buck). ULP mode is valid from –20 to +85 °C. | | | | | | | |
| Cortex M4. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF5 | I _{DD3} | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1). | – | 1.7 | 2.2 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 2.1 | 2.4 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| SIDF6 | I _{DD4} | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1) | – | 0.56 | 0.8 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.75 | 1 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC8 | I _{DD10} | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. Dhrystone. | – | 1.6 | 2.2 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 2.4 | 2.7 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| SIDC9 | I _{DD11} | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | – | 0.65 | 0.8 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.8 | 1.1 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Cortex M0+. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF7 | I _{DD16} | Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Write(1). | – | 1.00 | 1.4 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.34 | 1.6 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| SIDF8 | I _{DD17} | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1) | – | 0.54 | 0.75 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.73 | 1 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC10 | I _{DD18} | Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Dhrystone. | – | 0.91 | 1.25 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.34 | 1.6 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| SIDC11 | I _{DD19} | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | – | 0.51 | 0.72 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.73 | 0.95 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-------------------------------------------------------|--------------------|---------------------------------------------------------------------------|-----|------|------|-------|-------------------------------------------------|
| Cortex M4. Sleep Mode | | | | | | | |
| SIDS7 | I _{DD21} | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL | – | 0.76 | 1.1 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 1.1 | 1.4 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| SIDS8 | I _{DD22} | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO | – | 0.42 | 0.65 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.59 | 0.8 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Cortex M0+. Sleep Mode | | | | | | | |
| SIDS9 | I _{DD23} | CM4 Off, CM0+ Sleep 25 MHz. With IMO & FLL. | – | 0.62 | 0.9 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.88 | 1.1 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| SIDS10 | I _{DD24} | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | – | 0.41 | 0.6 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.58 | 0.8 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Cortex M4. Ultra Low Power Active (ULPA) Mode | | | | | | | |
| SIDLPA5 | I _{DD25} | Execute from Flash. CM4 ULPA 8 MHz, CM0+ ULPS 8 MHz. With IMO. While(1). | – | 0.52 | 0.75 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.76 | 1 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| SIDLPA6 | I _{DD26} | Execute from Cache. CM4 ULPA 8 MHz, CM0+ ULPS 8 MHz. With IMO. Dhrystone. | – | 0.54 | 0.76 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.78 | 1 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Cortex M0+. Ultra Low Power Active (ULPA) Mode | | | | | | | |
| SIDLPA7 | I _{DD27} | Execute from Flash. CM4 Off, CM0+ ULPA 8 MHz. With IMO. While (1). | – | 0.51 | 0.75 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.75 | 1 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| SIDLPA8 | I _{DD28} | Execute from Cache. CM4 Off, CM0+ ULPA 8 MHz. With IMO. Dhrystone. | – | 0.48 | 0.7 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.7 | 0.95 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Cortex M4. Ultra Low Power Sleep (ULPS) Mode | | | | | | | |
| SIDLPS5 | I _{DD29} | CM4 ULPS 8 MHz, CM0 ULPS 8 MHz. With IMO. | – | 0.4 | 0.6 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.57 | 0.8 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Cortex M0+. Ultra Low Power Sleep (ULPS) Mode | | | | | | | |
| SIDLPS7 | I _{DD31} | CM4 Off, CM0+ ULPS 8 MHz. With IMO. | – | 0.39 | 0.6 | mA | V _{DDD} = 3.3 V, Buck ON, max at 60 °C |
| | | | – | 0.56 | 0.8 | | V _{DDD} = 1.8 V, Buck ON, max at 60 °C |
| Deep Sleep Mode | | | | | | | |
| SIDDS1 | I _{DD33A} | With internal Buck enabled and 64 KB SRAM retention | – | 7 | – | µA | Max value is at 85 °C |

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|------------------------------------|------------------------|------------------------------------------------------|-----|-----|-----|-------|-------------------------|
| SIDDS1_B | I _{DD33A_B} | With internal Buck enabled and 64 KB SRAM retention | – | 7 | – | μA | Max value is at 60 °C |
| SIDDS2 | I _{DD33B} | With internal Buck enabled and 256 KB SRAM retention | – | 9 | – | μA | Max value is at 85 °C |
| SIDDS2_B | I _{DD33B_B} | With internal Buck enabled and 256 KB SRAM retention | – | 9 | – | μA | Max value is at 60 °C |
| Hibernate Mode | | | | | | | |
| SIDHIB1 | I _{DD34} | V _{DDD} = 1.8 V | – | 300 | – | nA | No clocks running |
| SIDHIB2 | I _{DD34A} | V _{DDD} = 3.3 V | – | 800 | – | nA | No clocks running |
| Power Mode Transition Times | | | | | | | |
| SID12 | T _{LPACT_ACT} | Low Power Active to Active transition time | – | – | 35 | μs | Including PLL lock time |
| SID13 ^[2] | T _{DS_LPACT} | Deep Sleep to LP Active transition time | – | – | 25 | μs | Guaranteed by design |
| SID13A ^[3] | T _{DS_ACT} | Deep Sleep to Active transition time | – | – | 25 | μs | Guaranteed by design |
| SID14 | T _{HIB_ACT} | Hibernate to Active transition time | – | 500 | – | μs | Including PLL lock time |

XRES

Table 6. XRES

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-----------------------------------------|-------------------------|----------------------------------------------------------------------|--------------------------|-----|--------------------------|-------|--------------------------|
| XRES (Active Low) Specifications | | | | | | | |
| XRES AC Specifications | | | | | | | |
| SID15 | T _{XRES_ACT} | POR or XRES release to Active transition time | – | 750 | – | μs | Normal mode, 50 MHz M0+. |
| SID16 | T _{XRES_PW} | XRES Pulse width | 5 | – | – | μs | |
| XRES DC Specifications | | | | | | | |
| SID17 | T _{XRES_IDD} | IDD when XRES asserted | – | 300 | – | nA | V _{DDD} = 1.8 V |
| SID17A | T _{XRES_IDD_1} | IDD when XRES asserted | – | 800 | – | nA | V _{DDD} = 3.3 V |
| SID77 | V _{IH} | Input Voltage high threshold | 0.7 * V _{DD} | – | – | V | CMOS Input |
| SID78 | V _{IL} | Input Voltage low threshold | – | – | 0.3 * V _{DD} | V | CMOS Input |
| SID80 | C _{IN} | Input Capacitance | – | 3 | – | pF | |
| SID81 | V _{HYSXRES} | Input voltage hysteresis | – | 100 | – | mV | |
| SID82 | I _{DIODE} | Current through protection diode to V _{DD} /V _{SS} | – | – | 100 | μA | |

Notes

- Cypress-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25 μs) before transition to Application code. With an 8-MHz CPU clock (LP Active), the time before user code executes is 25 + 12.5 = 37.5 μs.
- Cypress-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25 μs) before transition to Application code. With a 25-MHz CPU clock (FLL), the time before user code executes is 25 + 4 = 29 μs. With a 100-MHz CPU clock, the time is 25 + 1 = 26 μs.

GPIO

Table 7. GPIO Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-------------------------------|-----------------------|----------------------------------------------------------------------|------------------------------|-----|-----------------------|-------|--------------------------------------------------------------------|
| GPIO DC Specifications | | | | | | | |
| SID57 | V _{IH} | Input voltage high threshold | 0.7 * V _{DD} | – | – | V | CMOS Input |
| SID57A | I _{IHS} | Input current when Pad > VDDIO for OVT inputs | – | – | 10 | μA | Per I ² C Spec |
| SID58 | V _{IL} | Input voltage low threshold | – | – | 0.3 * V _{DD} | V | CMOS Input |
| SID241 | V _{IH} | LVTTL input, V _{DD} < 2.7 V | 0.7 * V _{DD} | – | – | V | |
| SID242 | V _{IL} | LVTTL input, V _{DD} < 2.7 V | – | – | 0.3*V _{DD} | V | |
| SID243 | V _{IH} | LVTTL input, V _{DD} ≥ 2.7 V | 2.0 | – | – | V | |
| SID244 | V _{IL} | LVTTL input, V _{DD} ≥ 2.7 V | – | – | 0.8 | V | |
| SID59 | V _{OH} | Output voltage high level | V _{DD} – 0.5 | – | – | V | I _{OH} = 8 mA |
| SID62A | V _{OL} | Output voltage low level | – | – | 0.4 | V | I _{OL} = 8 mA |
| SID63 | R _{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID64 | R _{PULLDOWN} | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID65 | I _{IL} | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, V _{DD} = 3.0 V |
| SID65A | I _{IL_CTBM} | Input leakage on CTBm input pins | – | – | 4 | nA | |
| SID66 | C _{IN} | Input Capacitance | – | – | 5 | pF | |
| SID67 | V _{HYSTTL} | Input hysteresis LVTTL V _{DD} > 2.7 V | 100 | 0 | – | mV | |
| SID68 | V _{HYSCMOS} | Input hysteresis CMOS | 0.05 * V _{DD} | – | – | mV | |
| SID69 | I _{DIODE} | Current through protection diode to V _{DD} /V _{SS} | – | – | 100 | μA | |
| SID69A | I _{TOT_GPIO} | Maximum Total Source or Sink Chip Current | – | – | 200 | mA | |
| GPIO AC Specifications | | | | | | | |
| SID70 | T _{RISEF} | Rise time in Fast Strong Mode. 10% to 90% of V _{DD} | – | – | 2.5 | ns | Load = 15 pF, 8 mA drive strength |
| SID71 | T _{FALLF} | Fall time in Fast Strong Mode. 10% to 90% of V _{DD} | – | – | 2.5 | ns | Load = 15 pF, 8 mA drive strength |
| SID72 | T _{RISES_1} | Rise time in Slow Strong Mode. 10% to 90% of V _{DD} | 52 | – | 142 | ns | Load = 15 pF, 8 mA drive strength, V _{DD} ≤ 2.7 V |
| SID72A | T _{RISES_2} | Rise time in Slow Strong Mode. 10% to 90% of V _{DD} | 48 | – | 102 | ns | Load = 15 pF, 8 mA drive strength, 2.7 V < V _{DD} ≤ 3.6 V |
| SID73 | T _{FALLS_1} | Fall time in Slow Strong Mode. 10% to 90% of V _{DD} | 44 | – | 211 | ns | Load = 15 pF, 8 mA drive strength, V _{DD} ≤ 2.7 V |
| SID73A | T _{FALLS_2} | Fall time in Slow Strong Mode. 10% to 90% of V _{DD} | 42 | – | 93 | ns | Load = 15 pF, 8 mA drive strength, 2.7 V < V _{DD} ≤ 3.6 V |
| SID73G | T _{FALL_I2C} | Fall time (30% to 70% of V _{DD}) in Slow Strong mode | 20 * V _{DDIO} / 5.5 | – | 250 | ns | Load = 10 pF to 400 pF, 8-mA drive strength |
| SID74 | F _{GPIOUT1} | GPIO Fout. Fast Strong mode. | – | – | 100 | MHz | 90/10%, 15-pF load, 60/40 duty cycle |

Table 7. GPIO Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------------------|-------------------------------------------------------------------------------|-----|-----|------|-------|--------------------------------------|
| SID75 | F _{GPIOOUT2} | GPIO Fout; Slow Strong mode. | – | – | 16.7 | MHz | 90/10%, 15-pF load, 60/40 duty cycle |
| SID76 | F _{GPIOOUT3} | GPIO Fout; Fast Strong mode. | – | – | 7 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID245 | F _{GPIOOUT4} | GPIO Fout; Slow Strong mode. | – | – | 3.5 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID246 | F _{GPIOIN} | GPIO input operating frequency; $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | – | – | 100 | MHz | 90/10% V _{IO} |

Analog Peripherals

Opamp

Table 8. Opamp Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------------|---------------------------------------------------|-----|------|------------------------|-------|------------------------------------------|
| | I _{DD} | Opamp Block current. No load. | – | – | – | | – |
| SID269 | I _{DD_HI} | Power = Hi | – | 1300 | 1500 | μA | – |
| SID270 | I _{DD_MED} | Power = Med | – | 450 | 600 | μA | – |
| SID271 | I _{DD_LOW} | Power = Lo | – | 250 | 350 | μA | – |
| | GBW | Load = 20 pF, 0.1 mA. V _{DDA} = 2.7 V | – | – | – | | – |
| SID272 | G _{BW_HI} | Power = Hi | 6 | – | – | MHz | – |
| SID273 | G _{BW_MED} | Power = Med | 4 | – | – | MHz | – |
| SID274 | G _{BW_LO} | Power = Lo | – | 1 | – | MHz | – |
| | I _{OUT_MAX} | V _{DDA} ≥ 2.7 V, 500 mV from rail | – | – | – | | – |
| SID275 | I _{OUT_MAX_HI} | Power = Hi | 10 | – | – | mA | – |
| SID276 | I _{OUT_MAX_MID} | Power = Mid | 10 | – | – | mA | – |
| SID277 | I _{OUT_MAX_LO} | Power = Lo | – | 5 | – | mA | – |
| | I _{OUT} | V _{DDA} = 1.71 V, 500 mV from rail | – | – | – | | – |
| SID278 | I _{OUT_MAX_HI} | Power = Hi | 4 | – | – | mA | – |
| SID279 | I _{OUT_MAX_MID} | Power = Mid | 4 | – | – | mA | – |
| SID280 | I _{OUT_MAX_LO} | Power = Lo | – | 2 | – | mA | – |
| SID281 | V _{IN} | Input voltage range | 0 | – | V _{DDA} – 0.2 | V | – |
| SID282 | V _{CM} | Input common mode voltage | 0 | – | V _{DDA} – 0.2 | V | – |
| | V _{OUT} | V _{DDA} ≥ 2.7 V | – | – | – | | – |
| SID283 | V _{OUT_1} | Power = hi, Iload = 10 mA | 0.5 | – | V _{DDA} – 0.5 | V | – |
| SID284 | V _{OUT_2} | Power = hi, Iload = 1 mA | 0.2 | – | V _{DDA} – 0.2 | V | – |
| SID285 | V _{OUT_3} | Power = med, Iload = 1 mA | 0.2 | – | V _{DDA} – 0.2 | V | – |
| SID286 | V _{OUT_4} | Power = lo, Iload = 0.1 mA | 0.2 | – | V _{DDA} – 0.2 | V | – |
| SID287 | V _{OS_UNTR} | Offset voltage, untrimmed | – | – | – | mV | – |
| SID288 | V _{OS_TR} | Offset voltage, trimmed | –1 | ±0.5 | 1 | mV | High mode, 0.2 to V _{DDA} – 0.2 |
| SID288A | V _{OS_TR} | Offset voltage, trimmed | – | ±1 | – | mV | Medium mode |
| SID288B | V _{OS_TR} | Offset voltage, trimmed | – | ±2 | – | mV | Low mode |
| SID289 | V _{OS_DR_UNTR} | Offset voltage drift, untrimmed | – | – | – | μV/°C | – |

Table 8. Opamp Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|-----------------------------------------------------------|-----|------|------|---------|---------------------------------------------------------------------------------------------------------|
| SID290 | V _{OS_DR_TR} | Offset voltage drift, trimmed | -10 | ±3 | 10 | μV/°C | High mode, 0.2 to V _{DDA} - 0.2 |
| SID290A | V _{OS_DR_TR} | Offset voltage drift, trimmed | - | ±10 | - | μV/°C | Medium mode |
| SID290B | V _{OS_DR_TR} | Offset voltage drift, trimmed | - | ±10 | - | μV/°C | Low mode |
| SID291 | CMRR | DC Common mode rejection ratio | 67 | 80 | - | dB | V _{DDDD} = 3.3 V |
| SID292 | PSRR | Power supply rejection ratio at 1 kHz, 10-mV ripple | 70 | 85 | - | dB | V _{DDDD} = 3.3 V |
| Noise | | | - | - | - | - | - |
| SID293 | VN1 | Input-referred, 1 Hz–1 GHz, power = Hi | - | 100 | - | μVrms | - |
| SID294 | VN2 | Input-referred, 1 kHz, power = Hi | - | 180 | - | nV/rtHz | - |
| SID295 | VN3 | Input-referred, 10 kHz, power = Hi | - | 70 | - | nV/rtHz | - |
| SID296 | VN4 | Input-referred, 100 kHz, power = Hi | - | 38 | - | nV/rtHz | - |
| SID297 | CLOAD | Stable up to max. load. Performance specs at 50 pF. | - | - | 125 | pF | - |
| SID298 | SLEW_RATE | Output slew rate | 6 | - | - | V/μs | Clod = 50 pF, Power = High, V _{DDA} ≥ 2.7 V |
| SID299 | T _{OP_WAKE} | From disable to enable, no external RC dominating | - | 25 | - | μs | - |
| | COMP_MODE | Comparator mode; 50-mV overdrive, Trise = Tfall (approx.) | - | - | - | - | - |
| SID300 | T _{PD1} | Response time; power = hi | - | 150 | - | ns | - |
| SID301 | T _{PD2} | Response time; power = med | - | 400 | - | ns | - |
| SID302 | T _{PD3} | Response time; power = lo | - | 2000 | - | ns | - |
| SID303 | V _{HYST_OP} | Hysteresis | - | 10 | - | mV | - |
| Deep Sleep Mode | | Mode 2 is lowest current range. Mode 1 has higher GBW. | | | | | Deep Sleep mode operation: V _{DDA} ≥ 2.7 V. V _{IN} is 0.2 to V _{DDA} - 1.5 V |
| SID_DS_1 | I _{DD_HI_M1} | Mode 1, High current | - | 1300 | 1500 | μA | Typ at 25 °C |
| SID_DS_2 | I _{DD_MED_M1} | Mode 1, Medium current | - | 460 | 600 | μA | Typ at 25 °C |
| SID_DS_3 | I _{DD_LOW_M1} | Mode 1, Low current | - | 230 | 350 | μA | Typ at 25 °C |
| SID_DS_4 | I _{DD_HI_M2} | Mode 2, High current | - | 120 | - | μA | 25 °C |
| SID_DS_5 | I _{DD_MED_M2} | Mode 2, Medium current | - | 60 | - | μA | 25 °C |
| SID_DS_6 | I _{DD_LOW_M2} | Mode 2, Low current | - | 15 | - | μA | 25 °C |
| SID_DS_7 | GBW_HI_M1 | Mode 1, High current | - | 4 | - | MHz | 25 °C |
| SID_DS_8 | GBW_MED_M1 | Mode 1, Medium current | - | 2 | - | MHz | 25 °C |
| SID_DS_9 | GBW_LOW_M1 | Mode 1, Low current | - | 0.5 | - | MHz | 25 °C |
| SID_DS_10 | GBW_HI_M2 | Mode 2, High current | - | 0.5 | - | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} - 1.5 V |
| SID_DS_11 | GBW_MED_M2 | Mode 2, Medium current | - | 0.2 | - | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} - 1.5 V |

Table 8. Opamp Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|--------------------|------------------------|-----|-----|-----|-------|------------------------------------------------------|
| SID_DS_12 | GBW_LOW_M2 | Mode 2, Low current | – | 0.1 | – | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_13 | $V_{OS_HI_M1}$ | Mode 1, High current | – | 5 | – | mV | With trim 25 °C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_14 | $V_{OS_MED_M1}$ | Mode 1, Medium current | – | 5 | – | mV | With trim 25 °C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_15 | $V_{OS_LOW_M1}$ | Mode 1, Low current | – | 5 | – | mV | With trim 25 °C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_16 | $V_{OS_HI_M2}$ | Mode 2, High current | – | 5 | – | mV | With trim 25 °C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_17 | $V_{OS_MED_M2}$ | Mode 2, Medium current | – | 5 | – | mV | With trim 25 °C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_18 | $V_{OS_LOW_M2}$ | Mode 2, Low current | – | 5 | – | mV | With trim 25 °C, 0.2 V to $V_{DDA} - 1.5$ V |
| SID_DS_19 | $I_{OUT_HI_M1}$ | Mode 1, High current | – | 10 | – | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_20 | $I_{OUT_MED_M1}$ | Mode 1, Medium current | – | 10 | – | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_21 | $I_{OUT_LOW_M1}$ | Mode 1, Low current | – | 4 | – | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_22 | $I_{OUT_HI_M2}$ | Mode 2, High current | – | 1 | – | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_23 | $I_{OUT_MED_M2}$ | Mode 2, Medium current | – | 1 | – | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |
| SID_DS_24 | $I_{OUT_LOW_M2}$ | Mode 2, Low current | – | 0.5 | – | mA | Output is 0.5 V to $V_{DDA} - 0.5$ V |

Table 9. Low-Power (LP) Comparator Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------------------------------------|---------------|-------------------------------------------------------|-----|----------|-------------------|-------|-----------------------------|
| LP Comparator DC Specifications | | | | | | | |
| SID84 | $V_{OFFSET1}$ | Input offset voltage for COMP1. Normal power mode. | –10 | – | 10 | mV | COMP0 offset is ± 25 mV |
| SID85A | $V_{OFFSET2}$ | Input offset voltage. Low-power mode. | –25 | ± 12 | 25 | mV | – |
| SID85B | $V_{OFFSET3}$ | Input offset voltage. Ultra low-power mode. | –25 | ± 12 | 25 | mV | – |
| SID86 | V_{HYST1} | Hysteresis when enabled in Normal mode | – | – | 60 | mV | – |
| SID86A | V_{HYST2} | Hysteresis when enabled in Low-power mode | – | – | 80 | mV | – |
| SID87 | V_{ICM1} | Input common mode voltage in Normal mode | 0 | – | $V_{DDIO1} - 0.1$ | V | – |
| SID247 | V_{ICM2} | Input common mode voltage in Low power mode | 0 | – | $V_{DDIO1} - 0.1$ | V | – |
| SID247A | V_{ICM3} | Input common mode voltage in Ultra low power mode | 0 | – | $V_{DDIO1} - 0.1$ | V | – |

Table 9. Low-Power (LP) Comparator Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------------------------------------|----------------------|-------------------------------------------------------|-----|-----|------|-------|----------------------------|
| SID88 | CMRR | Common mode rejection ratio in Normal power mode | 50 | – | – | dB | – |
| SID89 | I _{CMP1} | Block Current, Normal mode | – | – | 150 | μA | – |
| SID248 | I _{CMP2} | Block Current, Low power mode | – | – | 10 | μA | – |
| SID259 | I _{CMP3} | Block Current in Ultra low-power mode | – | 0.3 | 0.85 | μA | – |
| SID90 | ZCMP | DC Input impedance of comparator | 35 | – | – | MΩ | – |
| LP Comparator AC Specifications | | | | | | | |
| SID91 | T _{RESP1} | Response time, Normal mode, 100 mV overdrive | – | – | 100 | ns | – |
| SID258 | T _{RESP2} | Response time, Low power mode, 100 mV overdrive | – | – | 1000 | ns | – |
| SID92 | T _{RESP3} | Response time, Ultra-low power mode, 100 mV overdrive | – | – | 20 | μs | – |
| SID92E | T _{CMP_EN1} | Time from Enabling to operation | – | – | 10 | μs | Normal and Low-power modes |
| SID92F | T _{CMP_EN2} | Time from Enabling to operation | – | – | 50 | μs | Ultra low-power mode |

Table 10. Temperature Sensor Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|-----------------------------|-----|-----|-----|-------|--------------------|
| SID93 | T _{SENSACC} | Temperature sensor accuracy | –5 | ±1 | 5 | °C | –40 to +85 °C |

Table 11. Internal Reference Specification

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|-------------|-------|-----|-------|-------|--------------------|
| SID93R | V _{REFBG} | – | 1.188 | 1.2 | 1.212 | V | – |

SAR ADC
Table 12. 12-bit SAR ADC DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|------------------------------------------------------------|-----------------|-----|------------------|-------|---------------------------------|
| SID94 | A_RES | SAR ADC Resolution | – | – | 12 | bits | – |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | – | 8 full speed. |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 8 | – | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | – | – | – | – | Yes |
| SID98 | A_GAINERR | Gain error | – | – | ±0.2 | % | With external reference. |
| SID99 | A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V reference |
| SID100 | A_ISAR_1 | Current consumption at 1 Msps | – | – | 1 | mA | At 1 Msps. External Bypass Cap. |
| SID100A | A_ISAR_2 | Current consumption at 1 Msps. Reference = V _{DD} | – | – | 1.25 | mA | At 1 Msps. External Bypass Cap. |
| SID101 | A_VINS | Input voltage range - single-ended | V _{SS} | – | V _{DDA} | V | – |
| SID102 | A_VIND | Input voltage range - differential | V _{SS} | – | V _{DDA} | V | – |

Table 12. 12-bit SAR ADC DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|-------------------|-----|-----|-----|-------|--------------------|
| SID103 | A_INRES | Input resistance | – | – | 2.2 | kΩ | – |
| SID104 | A_INCAP | Input capacitance | – | – | 10 | pF | – |

Table 13. 12-bit SAR ADC AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-----------------------------------------|-----------|---------------------------------------------------------------------------------------|-----|-----|-----|-------|----------------------------------------------------------------------------------------|
| 12-bit SAR ADC AC Specifications | | | | | | | |
| SID106 | A_PSR | Power supply rejection ratio | 70 | – | – | dB | |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | – | – | dB | Measured at 1 V |
| One Megasample per second mode: | | | | | | | |
| SID108 | A_SAMP_1 | Sample rate with external reference bypass cap. | – | – | 1 | Msp | |
| SID108A | A_SAMP_2 | Sample rate with no bypass cap; Reference = V _{DD} | – | – | 250 | ksps | |
| SID108B | A_SAMP_3 | Sample rate with no bypass cap. Internal reference. | – | – | 100 | ksps | |
| SID109 | A_SINAD | Signal-to-noise and Distortion ratio (SINAD). V _{DDA} = 2.7 to 3.6 V, 1 Msp. | 64 | – | – | dB | Fin = 10 kHz |
| SID111A | A_INL | Integral Non Linearity. V _{DDA} = 2.7 to 3.6 V, 1 Msp | –2 | – | 2 | LSB | Measured with internal V _{REF} = 1.2 V and bypass cap. |
| SID111B | A_INL | Integral Non Linearity. V _{DDA} = 2.7 to 3.6 V, 1 Msp | –4 | – | 4 | LSB | Measured with external V _{REF} ≥ 1 V and V _{IN} common mode < 2*Vref |
| SID112A | A_DNL | Differential Non Linearity. V _{DDA} = 2.7 to 3.6 V, 1 Msp | –1 | – | 1.4 | LSB | Measured with internal V _{REF} = 1.2 V and bypass cap. |
| SID112B | A_DNL | Differential Non Linearity. V _{DDA} = 2.7 to 3.6 V, 1 Msp | –1 | – | 1.7 | LSB | Measured with external V _{REF} ≥ 1 V and V _{IN} common mode < 2*Vref |
| SID113 | A_THD | Total harmonic distortion. V _{DDA} = 2.7 to 3.6 V, 1 Msp. | – | – | –65 | dB | Fin = 10 kHz |

Table 14. 12-bit DAC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-------------------------------------|-------------|--------------------------------------------|-----|-----|-----|-------|-----------------------------------------|
| 12-bit DAC DC Specifications | | | | | | | |
| SID108D | DAC_RES | DAC resolution | – | – | 12 | bits | |
| SID111D | DAC_INL | Integral Non-Linearity | –4 | – | 4 | LSB | |
| SID112D | DAC_DNL | Differential Non Linearity | –2 | – | 2 | LSB | Monotonic to 11 bits. |
| SID99D | DAC_OFFSET | Output Voltage zero offset error | –10 | – | 10 | mV | For 000 (hex) |
| SID103D | DAC_OUT_RES | DAC Output Resistance | – | 15 | – | kΩ | |
| SID100D | DAC_IDD | DAC Current | – | – | 125 | μA | |
| SID101D | DAC_QIDD | DAC Current when DAC stopped | – | – | 1 | μA | |
| 12-bit DAC AC Specifications | | | | | | | |
| SID109D | DAC_CONV | DAC Settling time | – | – | 2 | μs | Driving through CTBm buffer; 25-pF load |
| SID110D | DAC_Wakeup | Time from Enabling to ready for conversion | – | – | 10 | μs | |

CSD

Table 15. CapSense Sigma-Delta (CSD) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------------------------------------------------------------------------------------------------|----------------------------|------------------------------------------------------------|-----|-----|------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| CSD V2 Specifications | | | | | | | |
| SYS.PER#3 | V _{DD_RIPPLE} | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | V _{DDA} > 2 V (with ripple), 25 °C T _A , Sensitivity = 0.1 pF |
| SYS.PER#16 | V _{DD_RIPPLE_1.8} | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | V _{DDA} > 1.75 V (with ripple), 25 °C T _A , Parasitic Capacitance (C _p) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | I _{CSD} | Maximum block current | | | 4500 | µA | |
| SID.CSD#15 | V _{REF} | Voltage reference for CSD and Comparator | 0.6 | 1.2 | V _{DDA} – 0.6 | V | V _{DDA} – V _{REF} ≥ 0.6 V |
| SID.CSD#15A | V _{REF_EXT} | External Voltage reference for CSD and Comparator | 0.6 | | V _{DDA} – 0.6 | V | V _{DDA} – V _{REF} ≥ 0.6 V |
| SID.CSD#16 | I _{DAC1IDD} | IDAC1 (7-bits) block current | – | – | 1900 | µA | |
| SID.CSD#17 | I _{DAC2IDD} | IDAC2 (7-bits) block current | – | – | 1900 | µA | |
| SID308 | V _{CSD} | Voltage range of operation | 1.7 | – | 3.6 | V | 1.71 to 3.6 V |
| SID308A | V _{COMPIDAC} | Voltage compliance range of IDAC | 0.6 | – | V _{DDA} – 0.6 | V | V _{DDA} – V _{REF} ≥ 0.6 V |
| SID309 | I _{DAC1DNL} | DNL | –1 | – | 1 | LSB | |
| SID310 | I _{DAC1INL} | INL | –3 | – | 3 | LSB | If V _{DDA} < 2 V then for LSB of 2.4 µA or less |
| SID311 | I _{DAC2DNL} | DNL | –1 | – | 1 | LSB | |
| SID312 | I _{DAC2INL} | INL | –3 | – | 3 | LSB | If V _{DDA} < 2 V then for LSB of 2.4 µA or less |
| SNRC of the following is Ratio of counts of finger to noise. Guaranteed by characterization | | | | | | | |
| SID313_1A | SNRC_1 | SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 9.5-pF max. capacitance |
| SID313_1B | SNRC_2 | SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 31-pF max. capacitance |
| SID313_1C | SNRC_3 | SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 61-pF max. capacitance |
| SID313_2A | SNRC_4 | PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 12-pF max. capacitance |
| SID313_2B | SNRC_5 | PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 47-pF max. capacitance |
| SID313_2C | SNRC_6 | PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 86-pF max. capacitance |
| SID313_3A | SNRC_7 | PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 27-pF max. capacitance |
| SID313_3B | SNRC_8 | PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 86-pF max. capacitance |
| SID313_3C | SNRC_9 | PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 168-pF max. capacitance |
| SID314 | I _{DAC1CRT1} | Output current of IDAC1 (7 bits) in low range | 4.2 | | 5.7 | µA | LSB = 37.5-nA typ |

Table 15. CapSense Sigma-Delta (CSD) Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|---------------------------|--------------------------------------------------------------------------------|------|-----|------|-------|------------------------------------------|
| SID314A | I _{DAC1CRT2} | Output current of IDAC1(7 bits) in medium range | 33.7 | | 45.6 | µA | LSB = 300-nA typ. |
| SID314B | I _{DAC1CRT3} | Output current of IDAC1(7 bits) in high range | 270 | | 365 | µA | LSB = 2.4-µA typ. |
| SID314C | I _{DAC1CRT12} | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | | 11.4 | µA | LSB = 37.5-nA typ. 2X output stage |
| SID314D | I _{DAC1CRT22} | Output current of IDAC1(7 bits) in medium range, 2X mode | 67 | | 91 | µA | LSB = 300-nA typ. 2X output stage |
| SID314E | I _{DAC1CRT32} | Output current of IDAC1(7 bits) in high range, 2X mode. V _{DDA} > 2 V | 540 | | 730 | µA | LSB = 2.4-µA typ.2X output stage |
| SID315 | I _{DAC2CRT1} | Output current of IDAC2 (7 bits) in low range | 4.2 | | 5.7 | µA | LSB = 37.5-nA typ. |
| SID315A | I _{DAC2CRT2} | Output current of IDAC2 (7 bits) in medium range | 33.7 | | 45.6 | µA | LSB = 300-nA typ. |
| SID315B | I _{DAC2CRT3} | Output current of IDAC2 (7 bits) in high range | 270 | | 365 | µA | LSB = 2.4-µA typ. |
| SID315C | I _{DAC2CRT12} | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | | 11.4 | µA | LSB = 37.5-nA typ. 2X output stage |
| SID315D | I _{DAC2CRT22} | Output current of IDAC2(7 bits) in medium range, 2X mode | 67 | | 91 | µA | LSB = 300-nA typ. 2X output stage |
| SID315E | I _{DAC2CRT32} | Output current of IDAC2(7 bits) in high range, 2X mode. V _{DDA} > 2V | 540 | | 730 | µA | LSB = 2.4-µA typ.2X output stage |
| SID315F | I _{DAC3CRT13} | Output current of IDAC in 8-bit mode in low range | 8 | | 11.4 | µA | LSB = 37.5-nA typ. |
| SID315G | I _{DAC3CRT23} | Output current of IDAC in 8-bit mode in medium range | 67 | | 91 | µA | LSB = 300-nA typ. |
| SID315H | I _{DAC3CRT33} | Output current of IDAC in 8-bit mode in high range. V _{DDA} > 2V | 540 | | 730 | µA | LSB = 2.4-µA typ. |
| SID320 | I _{DACOFFSET} | All zeroes input | – | – | 1 | LSB | Polarity set by Source or Sink |
| SID321 | I _{DACGAIN} | Full-scale error less offset | – | – | ±15 | % | LSB = 2.4-µA typ. |
| SID322 | I _{DACMISMATCH1} | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5-nA typ. |
| SID322A | I _{DACMISMATCH2} | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 6 | LSB | LSB = 300-nA typ. |
| SID322B | I _{DACMISMATCH3} | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 5.8 | LSB | LSB = 2.4-µA typ. |
| SID323 | I _{DACSET8} | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID324 | I _{DACSET7} | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID325 | C _{MOD} | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap. |

Table 16. CSD ADC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---------------------------------|----------------|--------------------------------------------------------------------------------------------------------------------------------|------------------|-----|------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CSDv2 ADC Specifications | | | | | | | |
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every milli-second |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | – | 16 | |
| SIDA97 | A-MONO | Monotonicity | – | – | Yes | – | V _{REF} mode |
| SIDA98 | A_GAINERR_VREF | Gain error | – | 0.6 | – | % | Reference Source: SRSS (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA98A | A_GAINERR_VDDA | Gain error | – | 0.2 | – | % | Reference Source: SRSS (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA99 | A_OFFSET_VREF | Input offset voltage | – | 0.5 | – | LSb | After ADC calibration, Ref. Src = SRSS, (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA99A | A_OFFSET_VDDA | Input offset voltage | – | 0.5 | – | LSb | After ADC calibration, Ref. Src = SRSS, (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA100 | A_ISAR_VREF | Current consumption | – | 0.3 | – | mA | CSD ADC Block current |
| SIDA100A | A_ISAR_VDDA | Current consumption | – | 0.3 | – | mA | CSD ADC Block current |
| SIDA101 | A_VINS_VREF | Input voltage range - single ended | V _{SSA} | – | V _{REF} | V | (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA101A | A_VINS_VDDA | Input voltage range - single ended | V _{SSA} | – | V _{DDA} | V | (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA103 | A_INRES | Input charging resistance | – | 15 | – | kΩ | |
| SIDA104 | A_INCAP | Input capacitance | – | 41 | – | pF | |
| SIDA106 | A_PSRR | Power supply rejection ratio (DC) | – | 60 | – | dB | |
| SIDA107 | A_TACQ | Sample acquisition time | – | 10 | – | μs | Measured with 50-Ω source impedance. 10 μs is default software driver acquisition time setting. Settling to within 0.05%. |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = F _{clk} /(2 ^N (N+2)). Clock frequency = 50 MHz. | – | 25 | – | μs | Does not include acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = F _{clk} /(2 ^N (N+2)). Clock frequency = 50 MHz. | – | 60 | – | μs | Does not include acquisition time. |
| SIDA109 | A_SND_VRE | Signal-to-noise and Distortion ratio (SINAD) | – | 57 | – | dB | Measured with 50-Ω source impedance |

Table 16. CSD ADC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|------------|----------------------------------------------|-----|-----|-----|-------|-------------------------------------|
| SIDA109A | A_SND_VDDA | Signal-to-noise and Distortion ratio (SINAD) | – | 52 | – | dB | Measured with 50-Ω source impedance |
| SIDA111 | A_INL_VREF | Integral Non Linearity. 11.6 ksp | – | – | 2 | LSB | Measured with 50-Ω source impedance |
| SIDA111A | A_INL_VDDA | Integral Non Linearity. 11.6 ksp | – | – | 2 | LSB | Measured with 50-Ω source impedance |
| SIDA112 | A_DNL_VREF | Differential Non Linearity. 11.6 ksp | – | – | 1 | LSB | Measured with 50-Ω source impedance |
| SIDA112A | A_DNL_VDDA | Differential Non Linearity. 11.6 ksp | – | – | 1 | LSB | Measured with 50-Ω source impedance |

Digital Peripherals

Table 17. Timer/Counter/PWM (TCPWM) Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------|-----------------------|--------------------------------------------------|----------------------|-----|-----|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID.TCPWM.1 | I _{TCPWM1} | Block current consumption at 8 MHz | – | – | 70 | μA | All modes (TCPWM) |
| SID.TCPWM.2 | I _{TCPWM2} | Block current consumption at 24 MHz | – | – | 180 | μA | All modes (TCPWM) |
| SID.TCPWM.2A | I _{TCPWM3} | Block current consumption at 50 MHz | – | – | 270 | μA | All modes (TCPWM) |
| SID.TCPWM.2B | I _{TCPWM4} | Block current consumption at 100 MHz | – | – | 540 | μA | All modes (TCPWM) |
| SID.TCPWM.3 | TCPWM _{FREQ} | Operating frequency | – | – | 100 | MHz | F _c max = F _{cpu} Maximum = 100 MHz |
| SID.TCPWM.4 | TPWM _{ENEXT} | Input Trigger Pulse Width for all Trigger Events | 2 / F _c | – | – | ns | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. F _c is counter operating frequency. |
| SID.TCPWM.5 | TPWM _{EXT} | Output Trigger Pulse widths | 1.5 / F _c | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs |
| SID.TCPWM.5A | TC _{RES} | Resolution of Counter | 1 / F _c | – | – | ns | Minimum time between successive counts |
| SID.TCPWM.5B | PWM _{RES} | PWM Resolution | 1 / F _c | – | – | ns | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | Q _{RES} | Quadrature inputs resolution | 2 / F _c | – | – | ns | Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar. |

Table 18. Serial Communication Block (SCB) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-------------------------------------------------------------------------------------------|---------------------------------|------------------------------------------------------------------------------------------|-----|-----|---------------------------------------------------------------------------------|-------|-----------------------------------------------------|
| Fixed I²C DC Specifications | | | | | | | |
| SID149 | I _{I2C1} | Block current consumption at 100 kHz | – | – | 30 | μA | |
| SID150 | I _{I2C2} | Block current consumption at 400 kHz | – | – | 80 | μA | |
| SID151 | I _{I2C3} | Block current consumption at 1 Mbps | – | – | 180 | μA | |
| SID152 | I _{I2C4} | I2C enabled in Deep Sleep mode | – | – | 1.7 | μA | At 60 °C |
| Fixed I²C AC Specifications | | | | | | | |
| SID153 | F _{I2C1} | Bit Rate | – | – | 1 | Mbps | |
| Fixed UART DC Specifications | | | | | | | |
| SID160 | I _{UART1} | Block current consumption at 100 kbps | – | – | 30 | μA | |
| SID161 | I _{UART2} | Block current consumption at 1000 kbps | – | – | 180 | μA | |
| Fixed UART AC Specifications | | | | | | | |
| SID162A | F _{UART1} | Bit Rate | – | – | 3 | Mbps | ULP Mode |
| SID162B | F _{UART2} | | – | – | 8 | | LP Mode |
| Fixed SPI DC Specifications | | | | | | | |
| SID163 | I _{SPI1} | Block current consumption at 1Mbps | – | – | 220 | μA | |
| SID164 | I _{SPI2} | Block current consumption at 4 Mbps | – | – | 340 | μA | |
| SID165 | I _{SPI3} | Block current consumption at 8 Mbps | – | – | 360 | μA | |
| SID165A | I _{SPI4} | Block current consumption at 25 Mbps | – | – | 800 | μA | |
| Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise | | | | | | | |
| SID166 | F _{SPI} | SPI Operating frequency Master and Externally Clocked Slave | – | – | 25 | MHz | 14-MHz max for ULP (0.9 V) mode |
| SID166A | F _{SPI_IC} | SPI Slave Internally Clocked | – | – | 15 | MHz | 5-MHz max for ULP (0.9 V) mode |
| Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise | | | | | | | |
| SID167 | T _{DMO} | MOSI Valid after SClock driving edge | – | – | 12 | ns | 20-ns max for ULP (0.9 V) mode |
| SID168 | T _{DSI} | MISO Valid before SClock capturing edge | 5 | – | – | ns | Full clock, late MISO sampling |
| SID169 | T _{HMO} | MOSI data hold time | 0 | – | – | ns | Referred to Slave capturing edge |
| Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise | | | | | | | |
| SID170 | T _{DMI} | MOSI Valid before Sclock Capturing edge | 5 | – | – | ns | |
| SID171A | T _{D_{SO}_EXT} | MISO Valid after Sclock driving edge in Ext. Clk. mode | – | – | 20 | ns | 35-ns max. for ULP (0.9 V) mode |
| SID171 | T _{D_{SO}} | MISO Valid after Sclock driving edge in Internally Clk. Mode | – | – | T _{D_{SO}_EX_T} ⁺ 3 * T _{scb} | ns | T _{scb} is Serial Comm Block clock period. |
| SID171B | T _{D_{SO}} | MISO Valid after Sclock driving edge in Internally Clk. Mode with Median filter enabled. | – | – | T _{D_{SO}_EX_T} ⁺ 4 * T _{scb} | ns | T _{scb} is Serial Comm Block clock period. |
| SID172 | T _{H_{SO}} | Previous MISO data hold time | 5 | – | – | ns | |
| SID172A | TSSEL _{SCK1} | SSEL Valid to first SCK Valid edge | 65 | – | – | ns | |
| SID172B | TSSEL _{SCK2} | SSEL Hold after Last SCK Valid edge | 65 | – | – | ns | |

LCD Specifications

Table 19. LCD Direct Drive DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|----------------------------------------------------|-----|-----|------|-------|---------------------------------------|
| SID154 | I _{LCDLOW} | Operating current in low-power mode | – | 5 | – | μA | 16 × 4 small segment display at 50 Hz |
| SID155 | C _{LCDCAP} | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID156 | LCD _{OFFSET} | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | I _{LCDOP1} | PWM Mode current. 3.3-V bias. 8-MHz IMO. 25 °C. | – | 0.6 | – | mA | 32 × 4 segments 50 Hz |
| SID158 | I _{LCDOP2} | PWM Mode current. 3.3-V bias. 8-MHz IMO. 25 °C. | – | 0.5 | – | mA | 32 × 4 segments 50 Hz |

Table 20. LCD Direct Drive AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|----------------|-----|-----|-----|-------|--------------------|
| SID159 | F _{LCD} | LCD frame rate | 10 | 50 | 150 | Hz | – |

Memory

Table 21. Flash Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------------------------|--------------------------|-----------------------------------------------------|-------|-----|-----|---------|-------------------------|
| Flash DC Specifications | | | | | | | |
| SID173 | VPE | Erase and program voltage | 1.71 | – | 3.6 | V | |
| Flash AC Specifications | | | | | | | |
| SID174 | T _{ROWWRITE} | Row (Block) write time (erase & program) | – | – | 16 | ms | Row (Block) = 512 bytes |
| SID175 | T _{ROWERASE} | Row erase time | – | – | 11 | ms | |
| SID176 | T _{ROWPROGRAM} | Row program time after erase | – | – | 5 | ms | |
| SID178 | T _{BULKERASE} | Bulk erase time (1024 KB) | – | – | 11 | ms | |
| SID179 | T _{SECTORERASE} | Sector erase time (256 KB) | – | – | 11 | ms | 512 rows per sector |
| SID178S | T _{SSERIAE} | Sub-sector erase time | – | – | 11 | ms | 8 rows per sub-sector |
| SID179S | T _{SSWRITE} | Sub-sector write time; 1 erase plus 8 program times | – | – | 51 | ms | |
| SID180S | T _{SWRITE} | Sector write time; 1 erase plus 512 program times | – | – | 2.6 | seconds | |
| SID180 | T _{DEVPROG} | Total device program time | – | – | 15 | seconds | |
| SID181 | F _{END} | Flash Endurance | 100 k | – | – | cycles | |
| SID182 | F _{RET1} | Flash Retention. Ta ≤ 25 °C, 100 k P/E cycles | 10 | – | – | years | |
| SID182A | F _{RET2} | Flash Retention. Ta ≤ 85 °C, 10 k P/E cycles | 10 | – | – | years | |
| SID182B | F _{RET3} | Flash Retention. Ta ≤ 55 °C, 20 k P/E cycles | 20 | – | – | years | |
| SID256 | T _{WS100} | Number of Wait states at 100 MHz | 3 | – | – | | |
| SID257 | T _{WS50} | Number of Wait states at 50 MHz | 2 | – | – | | |

Note

- It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources
Table 22. PSoC 6 System Resources

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------------------------------------------------|------------------------|----------------------------------------------------------------|------|------|------|-------|----------------------------------------------|
| Power-On-Reset with Brown-out DC Specifications | | | | | | | |
| Precise POR(PPOR) | | | | | | | |
| SID190 | V _{FALLPPOR} | BOD trip voltage in Active and Sleep modes. V _{DDD} . | 1.54 | – | – | V | BOD Reset guaranteed for levels below 1.54 V |
| SID192 | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep. V _{DDD} | 1.54 | – | – | V | – |
| SID192A | V _{DDRAMP} | Maximum power supply ramp rate (any supply) | – | – | 100 | mV/μs | Active Mode |
| POR with Brown-out AC Specification | | | | | | | |
| SID194A | V _{DDRAMP_DS} | Maximum power supply ramp rate (any supply) in Deep Sleep | – | – | 10 | mV/μs | BOD operation guaranteed |
| Voltage Monitors DC Specifications | | | | | | | |
| SID195R | V _{HVD0} | | 1.18 | 1.23 | 1.27 | V | – |
| SID195 | V _{HVD1} | | 1.38 | 1.43 | 1.47 | V | – |
| SID196 | V _{HVD2} | | 1.57 | 1.63 | 1.68 | V | – |
| SID197 | V _{HVD3} | | 1.76 | 1.83 | 1.89 | V | – |
| SID198 | V _{HVD4} | | 1.95 | 2.03 | 2.1 | V | – |
| SID199 | V _{HVD5} | | 2.05 | 2.13 | 2.2 | V | – |
| SID200 | V _{HVD6} | | 2.15 | 2.23 | 2.3 | V | – |
| SID201 | V _{HVD7} | | 2.24 | 2.33 | 2.41 | V | – |
| SID202 | V _{HVD8} | | 2.34 | 2.43 | 2.51 | V | – |
| SID203 | V _{HVD9} | | 2.44 | 2.53 | 2.61 | V | – |
| SID204 | V _{HVD10} | | 2.53 | 2.63 | 2.72 | V | – |
| SID205 | V _{HVD11} | | 2.63 | 2.73 | 2.82 | V | – |
| SID206 | V _{HVD12} | | 2.73 | 2.83 | 2.92 | V | – |
| SID207 | V _{HVD13} | | 2.82 | 2.93 | 3.03 | V | – |
| SID208 | V _{HVD14} | | 2.92 | 3.03 | 3.13 | V | – |
| SID209 | V _{HVD15} | | 3.02 | 3.13 | 3.23 | V | – |
| SID211 | LVI_IDD | Block current | – | 5 | 15 | μA | – |
| Voltage Monitors AC Specification | | | | | | | |
| SID212 | T _{MONTRIP} | Voltage monitor trip time | – | – | 170 | ns | – |

SWD Interface
Table 23. SWD and Trace Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------------------------|--------------|---------------------------------------------------------|------------|-----|-----------|-------|--------------------------------------|
| SWD and Trace Interface | | | | | | | |
| SID214 | F_SWCLK2 | $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | – | – | 25 | MHz | LP Mode; $V_{CCD} = 1.1\text{ V}$ |
| SID214L | F_SWCLK2L | $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | – | – | 12 | MHz | ULP Mode. $V_{CCD} = 0.9\text{ V}$. |
| SID215 | T_SWDI_SETUP | $T = 1/f\text{ SWCLK}$ | $0.25 * T$ | – | – | ns | |
| SID216 | T_SWDI_HOLD | $T = 1/f\text{ SWCLK}$ | $0.25 * T$ | – | – | ns | |
| SID217 | T_SWDO_VALID | $T = 1/f\text{ SWCLK}$ | – | – | $0.5 * T$ | ns | |
| SID217A | T_SWDO_HOLD | $T = 1/f\text{ SWCLK}$ | 1 | – | – | ns | |
| SID214T | F_TRCLK_LP1 | With Trace Data setup/hold times of 2/1 ns respectively | – | – | 75 | MHz | LP Mode. $V_{DD} = 1.1\text{ V}$ |
| SID215T | F_TRCLK_LP2 | With Trace Data setup/hold times of 3/2 ns respectively | – | – | 70 | MHz | LP Mode. $V_{DD} = 1.1\text{ V}$ |
| SID216T | F_TRCLK_ULP | With Trace Data setup/hold times of 3/2 ns respectively | – | – | 25 | MHz | ULP Mode. $V_{DD} = 0.9\text{ V}$ |

Internal Main Oscillator
Table 24. IMO DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|--------------------------------|-----|-----|-----|-------|--------------------|
| SID218 | I _{IMO1} | IMO operating current at 8 MHz | – | 9 | 15 | μA | – |

Table 25. IMO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|---------------------------------------|-----|------|-----|-------|--------------------|
| SID223 | F _{IMOTOL1} | Frequency variation centered on 8 MHz | – | – | ±2 | % | – |
| SID227 | T _{JITR} | Cycle-to-Cycle and Period jitter | – | ±250 | – | ps | – |

Internal Low-Speed Oscillator
Table 26. ILO DC Specification

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|-----|-------|--------------------|
| SID231 | I _{ILO2} | ILO operating current at 32 kHz | – | 0.3 | 0.7 | μA | – |

Table 27. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|--------------------------|------|-----|------|-------|----------------------------------------|
| SID234 | T _{STARTILO1} | ILO startup time | – | – | 7 | μs | Startup time to 95% of final frequency |
| SID236 | T _{LIODUTY} | ILO Duty cycle | 45 | 50 | 55 | % | – |
| SID237 | F _{ILOTRIM1} | 32-kHz trimmed frequency | 28.8 | 32 | 35.2 | kHz | ±10% variation |

Crystal Oscillator Specifications
Table 28. ECO Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------------------------------|---------------------|------------------------------------------------|-----|--------|------|-------|-----------------------------|
| MHz ECO DC Specifications | | | | | | | |
| SID316 | I _{DD_MHz} | Block operating current with Cload up to 18 pF | – | 800 | 1600 | μA | Max = 33 MHz, Type = 16 MHz |
| MHz ECO AC Specifications | | | | | | | |
| SID317 | F_MHz | Crystal frequency range | 4 | – | 33 | MHz | – |
| kHz ECO DC Specification | | | | | | | |
| SID318 | I _{DD_kHz} | Block operating current with 32-kHz crystal | – | 0.38 | 1 | μA | – |
| SID321E | ESR32K | Equivalent Series Resistance | – | 80 | – | kΩ | – |
| SID322E | PD32K | Drive level | – | – | 1 | μW | – |
| kHz ECO AC Specification | | | | | | | |
| SID319 | F_kHz | 32-kHz trimmed frequency | – | 32.768 | – | kHz | – |
| SID320 | Ton_kHz | Startup time | – | – | 500 | ms | – |
| SID320E | F _{TOL32K} | Frequency tolerance | – | 50 | 250 | ppm | – |

External Clock Specifications
Table 29. External Clock Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|-------------------------------------------|-----|-----|-----|-------|--------------------|
| SID305 | EXTCLK _{FREQ} | External Clock input Frequency | 0 | – | 100 | MHz | – |
| SID306 | EXTCLK _{DUTY} | Duty cycle; Measured at V _{DD/2} | 45 | – | 55 | % | – |

Table 30. PLL Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|---------------------------------|-----|------|-----|-------|--------------------------|
| SID305P | PLL_LOCK | Time to achieve PLL Lock | – | 16 | 35 | μs | – |
| SID306P | PLL_OUT | Output frequency from PLL Block | – | – | 150 | MHz | – |
| SID307P | PLL_IDD | PLL Current | – | 0.55 | 1.1 | mA | Typ at 100 MHz out. |
| SID308P | PLL_JTR | Period Jitter | – | – | 150 | ps | 100-MHz output frequency |

Table 31. Clock Source Switching Time

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|----------------------------------------------------|-----|-----|-----------------|---------|--------------------|
| SID262 | TCLK _{SWITCH} | Clock switching from clk1 to clk2 in clock periods | – | – | 4 clk1 + 3 clk2 | periods | – |

Table 32. Frequency Locked Loop (FLL) Specifications

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---------------------------------------------------|---------------|------------------------------------------------------------------------|-------|-----|--------|--------|-----------------------------------------------------------------------------------------------|
| Frequency Locked Loop (FLL) Specifications | | | | | | | |
| SID450 | FLL_RANGE | Input frequency range. | 0.001 | – | 100 | MHz | Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input. |
| SID451 | FLL_OUT_DIV2 | Output frequency range. $V_{CCD} = 1.1\text{ V}$ | 24.00 | – | 100.00 | MHz | Output range of FLL divided-by-2 output |
| SID451A | FLL_OUT_DIV2 | Output frequency range. $V_{CCD} = 0.9\text{ V}$ | 24.00 | – | 50.00 | MHz | Output range of FLL divided-by-2 output |
| SID452 | FLL_DUTY_DIV2 | Divided-by-2 output; High or Low | 47.00 | – | 53.00 | % | |
| SID454 | FLL_WAKEUP | Time from stable input clock to 1% of final value on deep sleep wakeup | – | – | 7.50 | µs | With IMO input, less than 10 °C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz. |
| SID455 | FLL_JITTER | Period jitter (1 sigma at 100 MHz) | – | – | 35.00 | ps | 50 ps at 48 MHz, 35 ps at 100 MHz |
| SID456 | FLL_CURRENT | CCO + Logic current | – | – | 5.50 | µA/MHz | |

Table 33. UDB AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------------------------------------------------------------------|---------------------------|----------------------------------------------------|-----|-----|-----|-------|--------------------|
| Data Path Performance | | | | | | | |
| SID249 | F _{MAX-TIMER} | Max frequency of 16-bit timer in a UDB pair | – | – | 100 | MHz | – |
| SID250 | F _{MAX-ADDER} | Max frequency of 16-bit adder in a UDB pair | – | – | 100 | MHz | – |
| SID251 | F _{MAX_CRC} | Max frequency of 16-bit CRC/PRS in a UDB pair | – | – | 100 | MHz | – |
| PLD Performance in UDB | | | | | | | |
| SID252 | F _{MAX_PLD} | Max frequency of 2-pass PLD function in a UDB pair | – | – | 100 | MHz | – |
| Clock to Output Performance | | | | | | | |
| SID253 | T _{CLK_OUT_UBD1} | Prop. delay for clock in to data out | – | 5 | – | ns | – |
| UDB Port Adaptor Specifications | | | | | | | |
| <i>Conditions: 10-pF load, 3-V V_{DDIO} and V_{DDD}</i> | | | | | | | |
| SID263 | T _{LCLKDO} | LCLK to Output delay | – | – | 11 | ns | – |
| SID264 | T _{DINLCLK} | Input setup time to LCLK rising edge | – | – | 7 | ns | – |
| SID265 | T _{DINLCLKHLD} | Input hold time from LCLK rising edge | 5 | – | – | ns | – |
| SID266 | T _{LCLKHIZ} | LCLK to Output tristated | – | – | 28 | ns | – |
| SID267 | T _{FLCLK} | LCLK frequency | – | – | 33 | MHz | – |
| SID268 | T _{LCLKDUTY} | LCLK duty cycle (percentage high) | 40% | – | 60% | % | – |

Note

5. The undivided output of the FLL must be a minimum of 2.5X the input frequency.

Table 34. USB Specifications (USB requires LP Mode 1.1-V Internal Supply)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------------------------|-----------------|-------------------------------------------------------------|-------|-----|------|-------|-----------------------------------------------|
| USB Block Specifications | | | | | | | |
| SID322U | Vusb_3.3 | Device supply for USB operation | 3.15 | – | 3.6 | V | USB Configured, USB Reg. bypassed |
| SID323U | Vusb_3.3 | Device supply for USB operation (functional operation only) | 2.85 | – | 3.6 | V | USB Configured, USB Reg. bypassed |
| SID325U | Iusb_config | Device supply current in Active mode | – | 8 | – | mA | V _{DDD} = 3.3 V |
| SID328 | Isub_suspend | Device supply current in Sleep mode | – | 0.5 | – | mA | V _{DDD} = 3.3 V, PICU wakeup |
| SID329 | Isub_suspend | Device supply current in Sleep mode | – | 0.3 | – | mA | V _{DDD} = 3.3 V, Device disconnected |
| SID330U | USB_Drive_Res | USB driver impedance | 28 | – | 44 | Ω | Series resistors are on chip |
| SID331U | USB_Pulldown | USB pull-down resistors in Host mode | 14.25 | – | 24.8 | kΩ | – |
| SID332U | USB_Pullup_Idle | Idle mode range | 900 | – | 1575 | Ω | Bus idle |
| SID333U | USB_Pullup | Active mode | 1425 | – | 3090 | Ω | Upstream device transmitting |

Table 35. QSPI Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-------------------------------------------------------------|---------------|-------------------------------------------------------------|-------|-----|------|-------|---------------------------------------|
| SMIF QSPI Specifications. All specs with 15-pF load. | | | | | | | |
| SID390Q | Fsmifclock | SMIF QSPI output clock frequency | – | – | 80 | MHz | LP mode (1.1 V) |
| SID390QU | Fsmifclocku | SMIF QSPI output clock frequency | – | – | 50 | MHz | ULP mode (0.9 V). Guaranteed by Char. |
| SID397Q | Idd_qspi | Block current in LP mode (1.1 V) | – | – | 1900 | μA | LP mode (1.1 V) |
| SID398Q | Idd_qspi_u | Block current in ULP mode (0.9 V) | – | – | 590 | μA | ULP mode (0.9 V) |
| SID391Q | Tsetup | Input data set-up time with respect to clock capturing edge | 4.5 | – | – | ns | |
| SID392Q | Tdatahold | Input data hold time with respect to clock capturing edge | 0 | – | – | ns | |
| SID393Q | Tdataoutvalid | Output data valid time with respect to clock falling edge | – | – | 3.7 | ns | |
| SID394Q | Tholdtime | Output data hold time with respect to clock rising edge | 3 | – | – | ns | |
| SID395Q | Tseloutvalid | Output Select valid time with respect to clock rising edge | – | – | 7.5 | ns | |
| SID396Q | Tselouthold | Output Select hold time with respect to clock rising edge | Tsclk | – | – | ns | Tsclk = Fsmifclk cycle time |

Table 36. Audio Subsystem Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-----------------------------------------------------------------------------------|--------------|----------------------------------------------------------------|-------------------|-------|--------|-------|---------------------------------------|
| Audio Subsystem specifications | | | | | | | |
| PDM Specifications | | | | | | | |
| SID400P | PDM_IDD1 | PDM Active current, Stereo operation, 1-MHz clock | – | 175 | – | µA | 16-bit audio at 16 ksps |
| SID401 | PDM_IDD2 | PDM Active current, Stereo operation, 3-MHz clock | – | 600 | – | µA | 24-bit audio at 48 ksps |
| SID402 | PDM_JITTER | RMS Jitter in PDM clock | –200 | – | 200 | ps | |
| SID403 | PDM_CLK | PDM Clock speed | 0.384 | – | 3.072 | MHz | |
| SID403A | PDM_BLK_CLK | PDM Block input clock | 1.024 | – | 49.152 | MHz | |
| SID403B | PDM_SETUP | Data input set-up time to PDM_CLK edge | 10 | – | – | ns | |
| SID403C | PDM_HOLD | Data input hold time to PDM_CLK edge | 10 | – | – | ns | |
| SID404 | PDM_OUT | Audio sample rate | 8 | – | 48 | ksps | |
| SID405 | PDM_WL | Word Length | 16 | – | 24 | bits | |
| SID406 | PDM_SNR | Signal-to-Noise Ratio (A-weighted) | – | 100 | – | dB | PDM input, 20 Hz to 20 kHz BW |
| SID407 | PDM_DR | Dynamic Range (A-weighted) | – | 100 | – | dB | 20 Hz to 20 kHz BW, –60 dB FS |
| SID408 | PDM_FR | Frequency Response | –0.2 | – | 0.2 | dB | DC to 0.45. DC Blocking filter off. |
| SID409 | PDM_SB | Stop Band | – | 0.566 | – | f | |
| SID410 | PDM_SBA | Stop Band Attenuation | – | 60 | – | dB | |
| SID411 | PDM_GAIN | Adjustable Gain | –12 | – | 10.5 | dB | PDM to PCM, 1.5 dB/step |
| SID412 | PDM_ST | Startup time | – | 48 | – | | WS (Word Select) cycles |
| I2S Specifications. The same for LP and ULP modes unless stated otherwise. | | | | | | | |
| SID413 | I2S_WORD | Length of I2S Word | 8 | – | 32 | bits | |
| SID414 | I2S_WS | Word Clock frequency in LP mode | – | – | 192 | kHz | 12.288-MHz bit clock with 32-bit word |
| SID414M | I2S_WS_U | Word Clock frequency in ULP mode | – | – | 48 | kHz | 3.072-MHz bit clock with 32-bit word |
| SID414A | I2S_WS_TDM | Word Clock frequency in TDM mode for LP | – | – | 48 | kHz | 8 32-bit channels |
| SID414X | I2S_WS_TDM_U | Word Clock frequency in TDM mode for ULP | – | – | 12 | kHz | 8 32-bit channels |
| I2S Slave Mode | | | | | | | |
| SID430 | TS_WS | WS Setup Time to the Following Rising Edge of SCK for LP Mode | 5 | – | – | ns | |
| SID430U | TS_WS | WS Setup Time to the Following Rising Edge of SCK for ULP Mode | 11 | – | – | ns | |
| SID430A | TH_WS | WS Hold Time to the Following Edge of SCK | TMCLK_S OC + 5 | – | – | ns | |

Table 36. Audio Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|------------------------|-------------|------------------------------------------------------------------|-------------------|-----|----------------|-------|--------------------------------------------------------------------------------------|
| SID432 | TD_SDO | Delay Time of TX_SDO Transition from Edge of TX_SCK for LP mode | -(TMCLK_SOC + 25) | - | TMCLK_SOC + 25 | ns | Associated clock edge depends on selected polarity |
| SID432U | TD_SDO | Delay Time of TX_SDO Transition from Edge of TX_SCK for ULP mode | -(TMCLK_SOC + 70) | - | TMCLK_SOC + 70 | ns | Associated clock edge depends on selected polarity |
| SID433 | TS_SDI | RX_SDI Setup Time to the Following Edge of RX_SCK in Lp Mode | 5 | - | - | ns | |
| SID433U | TS_SDI | RX_SDI Setup Time to the Following Edge of RX_SCK in ULP mode | 11 | - | - | ns | |
| SID434 | TH_SDI | RX_SDI Hold Time to the Rising Edge of RX_SCK | TMCLK_SOC + 5 | - | - | ns | |
| SID435 | TSCCKCY | TX/RX_SCK Bit Clock Duty Cycle | 45 | - | 55 | % | |
| I2S Master Mode | | | | | | | |
| SID437 | TD_WS | WS Transition Delay from Falling Edge of SCK in LP mode | -10 | - | 20 | ns | |
| SID437U | TD_WS_U | WS Transition Delay from Falling Edge of SCK in ULP mode | -10 | - | 40 | ns | |
| SID438 | TD_SDO | SDO Transition Delay from Falling Edge of SCK in LP mode | -10 | - | 20 | ns | |
| SID438U | TD_SDO | SDO Transition Delay from Falling Edge of SCK in ULP mode | -10 | - | 40 | ns | |
| SID439 | TS_SDI | SDI Setup Time to the Associated Edge of SCK | 5 | - | - | ns | Associated clock edge depends on selected polarity |
| SID440 | TH_SDI | SDI Hold Time to the Associated Edge of SCK | TMCLK_SOC + 5 | - | - | ns | T is TX/RX_SCK Bit Clock period. Associated clock edge depends on selected polarity. |
| SID443 | TSCCKCY | SCK Bit Clock Duty Cycle | 45 | - | 55 | % | |
| SID445 | FMCLK_SOC | MCLK_SOC Frequency in LP mode | 1.024 | - | 98.304 | MHz | FMCLK_SOC = 8 * Bit-clock |
| SID445U | FMCLK_SOC_U | MCLK_SOC Frequency in ULP mode | 1.024 | - | 24.576 | MHz | FMCLK_SOC_U = 8 * Bit-clock |
| SID446 | TMCLKCY | MCLK_SOC Duty Cycle | 45 | - | 55 | % | |
| SID447 | TJITTER | MCLK_SOC Input Jitter | -100 | - | 100 | ps | |

Table 37. Smart I/O Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|--------------------------|-----|-----|-----|-------|--------------------|
| SID420 | SMIO_BYP | Smart I/O Bypass delay | - | - | 2 | ns | - |
| SID421 | SMIO_LUT | Smart I/O LUT prop delay | - | TBD | - | ns | - |

Table 38. BLE Subsystem Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------|-----|-----|-----|-------|------------------------------------------------|
| BLE Subsystem specifications | | | | | | | |
| RF Receiver Specifications (1 Mbps) | | | | | | | |
| SID317R | RXS,IDLE | RX Sensitivity with Ideal Transmitter | – | –95 | – | dBm | Across RF Operating Frequency Range |
| SID317RR | RXS,IDLE | RX Sensitivity with Ideal Transmitter | – | –93 | – | dBm | 255-byte packet length, across Frequency Range |
| SID318R | RXS,DIRTY | RX Sensitivity with Dirty Transmitter | – | –92 | – | dBm | RF-PHY Specification (RCV-LE/CA/01/C) |
| SID319R | PRXMAX | Maximum received signal strength at < 0.1% PER | – | 0 | – | dBm | RF-PHY Specification (RCV-LE/CA/06/C) |
| SID320R | CI1 | Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX | – | 9 | 21 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID321R | CI2 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 1 MHz | – | 3 | 15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID322R | CI3 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz | – | –26 | –17 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID323R | CI4 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ≥ FRX ± 3 MHz | – | –33 | –27 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID324R | CI5 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE) | – | –20 | –9 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID325R | CI6 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE ± 1 MHz) | – | –28 | –15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| RF Receiver Specifications (2 Mbps) | | | | | | | |
| SID326 | RXS,IDLE | RX Sensitivity with Ideal Transmitter | – | –92 | – | dBm | Across RF Operating Frequency Range |
| SID326R | RXS,IDLE | RX Sensitivity with Ideal Transmitter | – | –90 | – | dBm | 255-byte packet length, across Frequency Range |
| SID327 | RXS,DIRTY | RX Sensitivity with Dirty Transmitter | – | –89 | – | dBm | RF-PHY Specification (RCV-LE/CA/01/C) |
| SID328R | PRXMAX | Maximum received signal strength at < 0.1% PER | – | 0 | – | dBm | RF-PHY Specification (RCV-LE/CA/06/C) |
| SID329R | CI1 | Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX | – | 9 | 21 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID330 | CI2 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz | – | 3 | 15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID331 | CI3 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 4 MHz | – | –26 | –17 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |

Table 38. BLE Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---------------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-------|-----------------------------------------------------------|
| SID332 | CI4 | Adjacent channel interference Wanted Signal at -67 dBm and Interferer at $\geq FRX \pm 6$ MHz | - | -33 | -27 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID333 | CI5 | Adjacent channel interference Wanted Signal at -67 dBm and Interferer at Image frequency (FIMAGE) | - | -20 | -9 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID334 | CI6 | Adjacent channel interference Wanted Signal at -67 dBm and Interferer at Image frequency (FIMAGE \pm 2MHz) | - | -28 | -15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| RF Receiver Specification (1 & 2 Mbps) | | | | | | | |
| SID338 | OBB1 | Out of Band Blocking Wanted Signal at -67 dBm and Interferer at $F = 30-2000$ MHz | -30 | -27 | - | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| SID339 | OBB2 | Out of Band Blocking Wanted Signal at -67 dBm and Interferer at $F = 2003-2399$ MHz | -35 | -27 | - | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| SID340 | OBB3 | Out of Band Blocking, Wanted Signal at -67 dBm and Interferer at $F = 2484-2997$ MHz | -35 | -27 | - | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| SID341 | OBB4 | Out of Band Blocking Wanted Signal at -67 dBm and Interferer at $F = 3000-12750$ MHz | -30 | -27 | - | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| SID342 | IMD | Intermodulation Performance Wanted Signal at -64 dBm and 1 Mbps BLE, 3rd, 4th and 5th offset channel | -50 | - | - | dBm | RF-PHY Specification (RCV-LE/CA/05/C) |
| SID343 | RXSE1 | Receiver Spurious emission 30 MHz to 1.0 GHz | - | - | -57 | dBm | 100-kHz measurement bandwidth ETSI EN300 328 V2.1.1 |
| SID344 | RXSE2 | Receiver Spurious emission 1.0 GHz to 12.75 GHz | - | - | -53 | dBm | 1-MHz measurement bandwidth ETSI EN300 328 V2.1.1 |
| RF Transmitter Specifications | | | | | | | |
| SID345 | TXP,ACC | RF Power Accuracy | -1 | - | 1 | dB | |
| SID346 | TXP,RANGE | Frequency Accuracy | - | 24 | - | dB | -20 dBm to +4 dBm |
| SID347 | TXP,0dBm | Output Power, 0 dB Gain setting | - | 0 | - | dBm | |
| SID348 | TXP,MAX | Output Power, Maximum Power Setting | - | 4 | - | dBm | |
| SID349 | TXP,MIN | Output Power, Minimum Power Setting | - | -20 | - | dBm | |
| SID350 | F2AVG | Average Frequency deviation for 10101010 pattern | 185 | - | - | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID350R | F2AVG_2M | Average Frequency deviation for 10101010 pattern for 2 Mbps | 370 | - | - | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID351 | F1AVG | Average Frequency deviation for 11110000 pattern | 225 | 250 | 275 | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |

Table 38. BLE Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---------------------------------|---------------|------------------------------------------------------------------------------------------------------------------------|------|------|-------|--------------------|-------------------------------------------|
| SID351R | F1AVG_2M | Average Frequency deviation for 11110000 pattern for 2 Mbps | 450 | 500 | 550 | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID352 | EO | Eye opening = $\Delta F2AVG/\Delta F1AVG$ | 0.8 | – | – | – | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID353 | FTX,ACC | Frequency Accuracy | –150 | – | 150 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| SID354 | FTX,MAXDR | Maximum Frequency Drift | –50 | – | 50 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| SID355 | FTX,INITDR | Initial Frequency drift | –20 | – | 20 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| SID356 | FTX,DR | Maximum Drift Rate | –20 | – | 20 | kHz/ 50 μ s | RF-PHY Specification (TRM-LE/CA/06/C) |
| SID357 | IBSE1 | In Band Spurious Emission at 2 MHz offset (1 Mbps) In Band Spurious Emission at 4 MHz offset (2 Mbps) | – | – | –20 | dBm | RF-PHY Specification (TRM-LE/CA/03/C) |
| SID358 | IBSE2 | In Band Spurious Emission at \geq 3 MHz offset (1 Mbps) In Band Spurious Emission at \geq 6 MHz offset (2 Mbps) | – | – | –30 | dBm | RF-PHY Specification (TRM-LE/CA/03/C) |
| SID359 | TXSE1 | Transmitter Spurious Emissions (Averaging), < 1.0 GHz | – | – | –55.5 | dBm | FCC-15.247 |
| SID360 | TXSE2 | Transmitter Spurious Emissions (Averaging), > 1.0 GHz | – | – | –41.5 | dBm | FCC-15.247 |
| RF Current Specification | | | | | | | |
| SID361 | IRX1_wb | Receive Current (1 Mbps) | – | 6.7 | – | mA | VDD_NS = VDD = 3.3 V current with buck |
| SID362 | ITX1_wb_0dBm | TX Current at 0 dBm setting (1 Mbps) | – | 5.7 | – | mA | VDD_NS = VDD = 3.3 V current with buck |
| SID363 | IRX1_nb | Receive Current (1 Mbps) | – | 11 | – | mA | VDD current without buck |
| SID364 | ITX1_nb_0dBm | TX Current at 0-dBm setting (1 Mbps) | – | 10 | – | mA | VDD current without buck |
| SID365 | ITX1_nb_4dBm | TX Current at 4-dBm setting (1 Mbps) | – | 13 | – | mA | VDD current without buck |
| SID365R | ITX1_wb_4dBm | TX Current at 4-dBm setting (1 Mbps) | – | 8.5 | – | mA | VDD_NS = VDD = 3.3 V current with buck |
| SID366 | ITX1_nb_20dBm | TX Current at –20-dBm setting (1 Mbps) | – | 7 | – | mA | VDD current without buck |
| SID367 | IRX2_wb | Receive Current (2 Mbps) | – | 7 | – | mA | VDD_NS = VDD = 3.3 V current with buck |
| SID368 | ITX2_wb_0dBm | TX Current at 0-dBm setting (2 Mbps) | – | 5.7 | – | mA | VDD_NS = VDD = 3.3 V current with buck |
| SID369 | IRX2_nb | Receive Current (2 Mbps) | – | 11.3 | – | mA | VDD current without buck |
| SID370 | ITX2_nb_0dBm | TX Current at 0-dBm setting (2 Mbps) | – | 10 | – | mA | VDD current without buck |
| SID371 | ITX2_nb_4dBm | TX Current at 4-dBm setting (2 Mbps) | – | 13 | – | mA | VDD current without buck |
| SID371R | ITX2_wb_4dBm | TX Current at 4-dBm setting (2 Mbps) | – | 8.5 | – | mA | VDD_NS = VDD = 3.3 V current with buck |

Table 38. BLE Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------------------------------------|---------------|----------------------------------------|------|------|------|-------|--------------------------------------|
| SID372 | ITX2_nb_20dBm | TX Current at -20-dBm setting (2 Mbps) | - | 7 | - | mA | V _{DD} current without buck |
| General RF Specification | | | | | | | |
| SID373 | FREQ | RF operating frequency | 2400 | - | 2482 | MHz | |
| SID374 | CHBW | Channel spacing | - | 2 | - | MHz | |
| SID375 | DR1 | On-air Data Rate (1 Mbps) | - | 1000 | - | kbps | |
| SID376 | DR2 | On-air Data Rate (2 Mbps) | - | 2000 | - | kbps | |
| SID377 | TXSUP | Transmitter Startup time | - | 80 | 82 | μs | |
| SID378 | RXSUP | Receiver Startup time | - | 80 | 82 | μs | |
| RSSI Specification | | | | | | | |
| SID379 | RSSI,ACC | RSSI Accuracy | -4 | - | 4 | dB | -95 dBm to -20 dBm measurement range |
| SID380 | RSSI,RES | RSSI Resolution | - | 1 | - | dB | |
| SID381 | RSSI,PER | RSSI Sample Period | - | 6 | - | μs | |
| System-Level BLE Specifications | | | | | | | |
| SID433R | Adv_Pwr | 1.28s, 32 bytes, 0 dBm | - | 42 | - | μW | 3.3 V, Buck, w/o Deep Sleep current |
| SID434R | Conn_Pwr_300 | 300 ms, 0 byte, 0 dBm | - | 70 | - | μW | 3.3 V, Buck, w/o Deep Sleep current |
| SID435R | Conn_Pwr_1S | 1000 ms, 0 byte, 0 dBm | - | 30 | - | μW | 3.3 V, Buck, w/o Deep Sleep current |
| SID436R | Conn_Pwr_4S | 4000 ms, 0 byte, 0 dBm | - | 4 | - | μW | 3.3 V, Buck, w/o Deep Sleep current |

Table 39. ECO Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------------------------------------|-----------|------------------------------|-----|-----|-----|-------|------------------------------------------------|
| 16-MHz Crystal Oscillator | | | | | | | |
| SID382 | FXO1 | Crystal frequency | - | 16 | - | MHz | - |
| SID383 | ESR1 | Equivalent series resistance | - | 100 | 250 | Ω | - |
| SID384 | Txostart1 | Startup time | - | 400 | - | μs | Frequency Stable (16 MHz ±50 ppm) |
| SID385 | IXO1 | Operating current | - | 300 | - | μA | Includes crystal current, LDO and BG |
| 32-MHz Crystal Oscillator | | | | | | | |
| SID386 | FXO2 | Crystal frequency | - | 32 | - | MHz | - |
| SID387 | ESR2 | Equivalent series resistance | - | 50 | 100 | Ω | - |
| SID388 | Txostart2 | Startup time | - | 400 | - | μs | Frequency Stable (32 MHz ±50 ppm) |
| SID389 | IXO2 | Operating current | - | 350 | - | μA | Includes crystal current, LDO and BG |
| 16-MHz and 32-MHz Crystal Oscillator | | | | | | | |
| SID390 | FTOL | Frequency tolerance | -20 | - | 20 | ppm | After trimming, including aging and temp drift |
| SID391 | PD | Drive level | - | - | 100 | μW | - |

Table 40. Precision ILO (PILO) Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|---------------------|-----------------------------------------|------|-------|-----|-------|-------------------------------|
| SID 430R | I _{PILO} | Operating current | – | 1.2 | 4 | μA | – |
| SID431 | F _{PILO} | PILO nominal frequency | – | 32768 | – | Hz | T = 25 °C with 20-ppm crystal |
| SID432R | ACC _{PILO} | PILO accuracy with periodic calibration | –500 | – | 500 | ppm | – |

Ordering Information

Table 41 lists the PSoC 63 part numbers and features. The following table shows Marketing Part Numbers (MPNs) for products including the BLE Radio. The packages are 104 M CSP and 116 BGA.

Table 41. BLE Series Part Numbers

| Family | MPN | CPU Speed (M4) | CPU Speed (M0+) | Single core/Dual core | ULP/LP | Flash | SRAM | No. of CTBMs | No. of UDBs | CapSense | GPIOs | CRYPTO | Package |
|--------|-------------------|----------------|-----------------|-----------------------|--------|-------|------|--------------|-------------|----------|-------|--------|----------|
| 63 | CY8C6336BZI-BLF03 | 150 | – | Single | LP | 512 | 128 | 0 | 0 | No | 78 | No | 116-BGA |
| | CY8C6316BZI-BLF03 | 50 | – | Single | ULP | 512 | 128 | 0 | 0 | No | 78 | No | 116-BGA |
| | CY8C6316BZI-BLF53 | 50 | – | Single | ULP | 512 | 128 | 1 | 12 | Yes | 78 | Yes | 116-BGA |
| | CY8C6337BZI-BLF13 | 150 | – | Single | LP | 1024 | 288 | 0 | 0 | Yes | 78 | No | 116-BGA |
| | CY8C6336BZI-BLD13 | 150 | 100 | Double | LP | 512 | 128 | 0 | 0 | Yes | 78 | No | 116-BGA |
| | CY8C6347BZI-BLD43 | 150/50 | 100/25 | Double | FLEX | 1024 | 288 | 0 | 0 | Yes | 78 | Yes | 116-BGA |
| | CY8C6347BZI-BLD33 | 150/50 | 100/25 | Double | FLEX | 1024 | 288 | 1 | 12 | Yes | 78 | No | 116-BGA |
| | CY8C6347BZI-BLD53 | 150/50 | 100/25 | Double | FLEX | 1024 | 288 | 1 | 12 | Yes | 78 | Yes | 116-BGA |
| | CY8C6347FMI-BLD13 | 150/50 | 100/25 | Double | FLEX | 1024 | 288 | 0 | 0 | Yes | 70 | No | 104-MCSP |
| | CY8C6347FMI-BLD43 | 150/50 | 100/25 | Double | FLEX | 1024 | 288 | 0 | 0 | Yes | 70 | Yes | 104-MCSP |
| | CY8C6347FMI-BLD33 | 150/50 | 100/25 | Double | FLEX | 1024 | 288 | 1 | 12 | Yes | 70 | No | 104-MCSP |
| | CY8C6347FMI-BLD53 | 150/50 | 100/25 | Double | FLEX | 1024 | 288 | 1 | 12 | Yes | 70 | Yes | 104-MCSP |

Table 42 lists the field values.

Table 42. MPN Nomenclature

| Field | Description | Values | Meaning |
|-------|----------------|--------|--------------|
| CY8C | Cypress Prefix | | |
| 6 | Architecture | 6 | PSoC 6 |
| A | Family | 0 | Value |
| | | 1 | Programmable |
| | | 2 | Performance |
| | | 3 | Connectivity |
| B | Speed | 1 | 50 MHz |
| | | 2 | 100 MHz |
| | | 3 | 150 MHz |
| | | 4 | 150/50 MHz |
| C | Flash Capacity | 4 | 128 KB |
| | | 5 | 256 KB |
| | | 6 | 512 KB |
| | | 7 | 1024 KB |

Table 42. MPN Nomenclature

| Field | Description | Values | Meaning |
|-------|--------------------|--------|--------------------------------------------|
| D | Package Code | AX | TQFP I (0.8 mm pitch) |
| | | AZ | TQFP II (0.5 mm pitch) |
| | | LQ | QFN |
| | | BZ | BGA |
| | | FM | M-CSP |
| E | Temperature Range | C | Consumer |
| | | I | Industrial |
| | | Q | Extended Industrial (105 °C) |
| F | Silicon Family | N/A | PSoC 6A |
| | | S | PSoC 6A-S (Example) |
| | | M | PSoC 6A-M (Example) |
| | | L | PSoC 6A-L (Example) |
| | | BL | PSoC 6A-BLE |
| G | Core | Z | M0+ |
| | | F | M4 |
| | | D | Dual-Core M4/M0+ |
| XY | Attributes Code | 00–99 | Code of feature set in the specific family |
| ES | Engineering sample | ES | Engineering samples or not |
| T | Tape/Reel Shipment | T | Tape and Reel shipment or not |

Packaging

PSoC 63 will be offered in two packages: 116-BGA and 104-MCSP.

Table 43. Package Dimensions

| Spec ID | Package | Description | Package Drawing Number |
|---------|----------|-------------------------------------------------------|------------------------|
| PKG_2 | 104-MCSP | 104-MCSP, 3.8 × 5 × 0.65 mm height with 0.35-mm pitch | 002-16508 |
| PKG_4 | 116-BGA | 116-BGA, 5.2 × 6.4 × 0.70 mm height with 0.5-mm pitch | 002-16574 |

Table 44. Package Characteristics

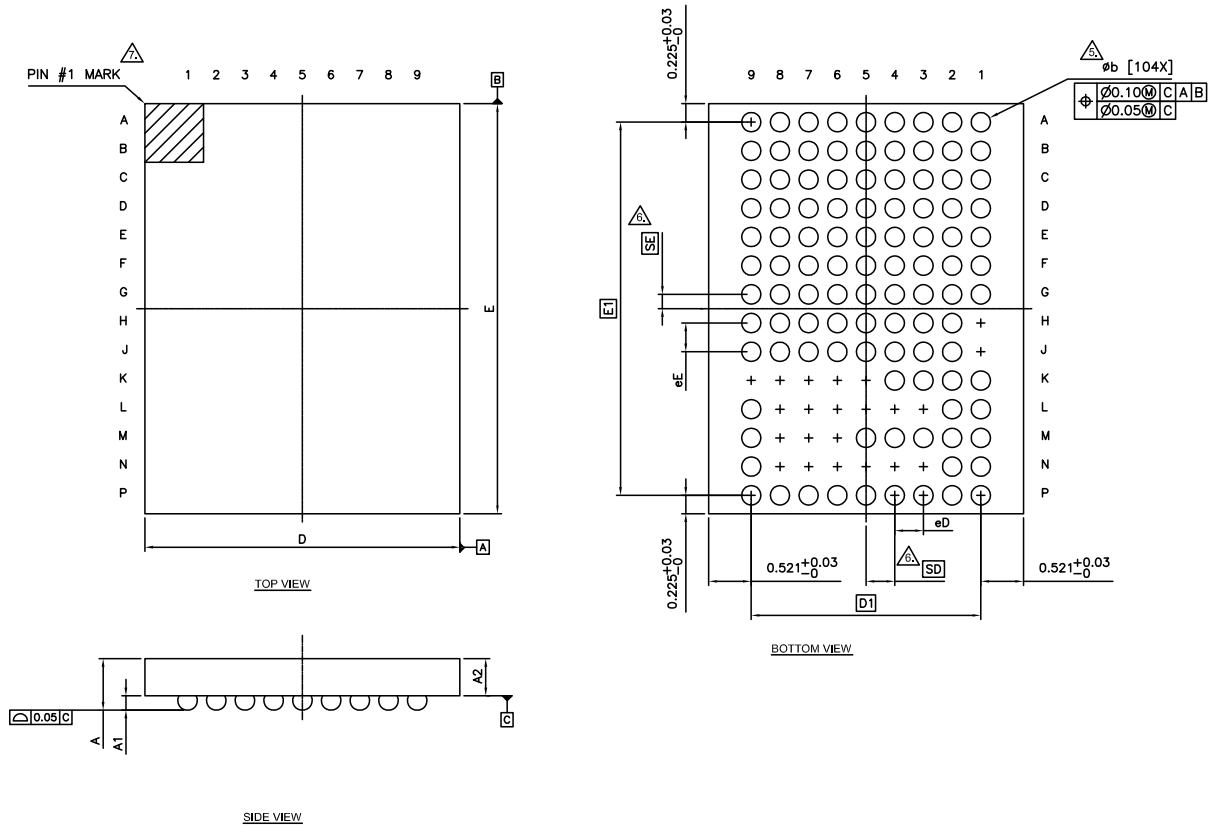
| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------------|-----------------------------------|------------|-----|-------|-----|---------|
| T _A | Operating ambient temperature | – | –40 | 25.00 | 85 | °C |
| T _J | Operating junction temperature | – | –40 | – | 100 | °C |
| T _{JA} | Package θ _{JA} (116-BGA) | – | – | 36 | – | °C/watt |
| T _{JC} | Package θ _{JC} (116-BGA) | – | – | 12 | – | °C/watt |
| T _{JA} | Package θ _{JA} (104-CSP) | – | – | 34 | – | °C/watt |

Table 45. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|----------|--------------------------|----------------------------------|
| 116-BGA | 260 °C | 30 seconds |
| 104-MCSP | 260 °C | 30 seconds |

Table 46. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|----------|-------|
| 116-BGA | MSL 3 |
| 104-MCSP | MSL 3 |

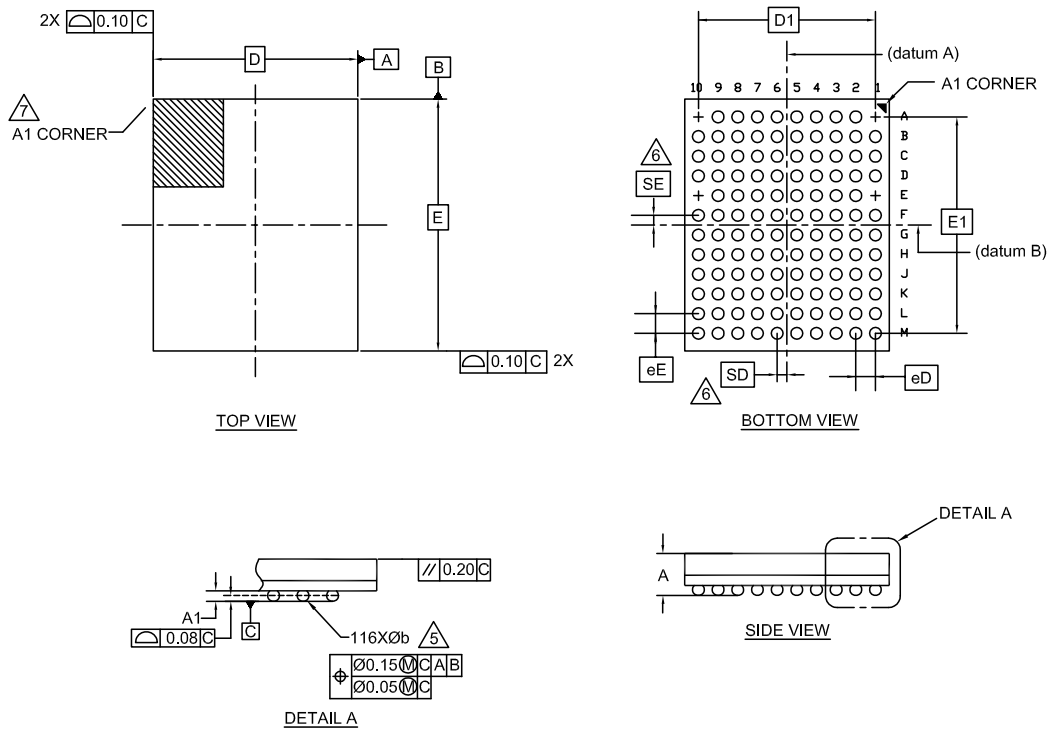
Figure 4. 104-WLCSP 3.8 x 5.0 x 0.65 mm


| SYMBOL | DIMENSIONS | | |
|--------|------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0,560 | 0,605 | 0,650 |
| A1 | 0,165 | 0,185 | 0,205 |
| A2 | 0,395 | 0,420 | 0,445 |
| D | 3,791 | 3,841 | 3,891 |
| E | 4,95 | 5,00 | 5,05 |
| D1 | 2,80 BSC | | |
| E1 | 4,55 BSC | | |
| MD | 9 | | |
| ME | 14 | | |
| N | 104 | | |
| Ø b | 0,205 | 0,235 | 0,265 |
| eD | 0,335 | 0,350 | 0,365 |
| eE | 0,335 | 0,350 | 0,365 |
| SD | 0,35 BSC | | |
| SE | 0,175 BSC | | |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
 - SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
 - "e" REPRESENTS THE SOLDER BALL GRID PITCH.
 - SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- ⚠ DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- ⚠ "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- ⚠ A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
 - JEDEC SPECIFICATION NO, REF.: N/A.

002-16508 *D

Figure 5. 116-BGA 5.2 x 6.4 x 0.70 mm


| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | - | - | 0.70 |
| A1 | 0.16 | 0.21 | 0.26 |
| D | 5.20 BSC | | |
| E | 6.40 BSC | | |
| D1 | 4.50 BSC | | |
| E1 | 5.50 BSC | | |
| MD | 10 | | |
| ME | 12 | | |
| N | 116 | | |
| Ø b | 0.25 | 0.30 | 0.35 |
| eD | 0.50 BSC | | |
| eE | 0.50 BSC | | |
| SD | 0.25 BSC | | |
| SE | 0.25 BSC | | |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
 - SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
 - "e" REPRESENTS THE SOLDER BALL GRID PITCH.
 - SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- ⚠️ DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- ⚠️ "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- ⚠️ A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
 - JEDEC SPECIFICATION NO. REF: N/A

002-16574 *B

Acronyms

Table 47. Acronyms Used in this Document

| Acronym | Description |
|---------|-------------------------------------------------------------------------------------------------|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| Arm® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

Table 47. Acronyms Used in this Document (continued)

| Acronym | Description |
|--------------------------|--------------------------------------------------------|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |

Table 47. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|-------------------|--------------------------------------------------------------|
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC [®] | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |
| SWV | single-wire viewer |

Table 47. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|---------|------------------------------------------------------------------------|
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

Document Conventions

Units of Measure

Table 48. Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| KHR | kilohour |
| KHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |

Table 48. Units of Measure (continued)

| Symbol | Unit of Measure |
|--------|----------------------|
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

Revision History

| Description Title: PSoC [®] 6 MCU: PSoC 63 with BLE Datasheet, Programmable System-on-Chip (PSoC [®]) Document Number: 002-18787 | | | | |
|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|----------------------------------------------------------|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *F | 6164322 | WKA | 05/03/2018 | Release of production datasheet. |
| *G | 6250376 | WKA | 07/17/2018 | Corrected document number in the revision history table. |

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Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А