

## Inverter Grade Thyristors (Hockey PUK Version), 720 A



TO-200AB (E-PUK)

**FEATURES**

- Metal case with ceramic insulator
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- International standard case TO-200AB (E-PUK)
- High surge current capability
- Low thermal impedance
- High speed performance
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS  
COMPLIANT**

PRODUCT SUMMARY	
Package	TO-200AB (E-PUK)
Diode variation	Single SCR
$I_{T(AV)}$	720 A
$V_{DRM}/V_{RRM}$	400 V, 800 V
$V_{TM}$	1.96 V
$I_{TSM}$ at 50 Hz	11 000 A
$I_{TSM}$ at 60 Hz	11 500 A
$I_{GT}$	200 mA
$T_C/T_{hs}$	55 °C

**TYPICAL APPLICATIONS**

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		720	A
	$T_{hs}$	55	°C
$I_{T(RMS)}$		1435	A
	$T_{hs}$	25	°C
$I_{TSM}$	50 Hz	11 000	A
	60 Hz	11 500	
$I^2t$	50 Hz	605	kA <sup>2</sup> s
	60 Hz	553	
$V_{DRM}/V_{RRM}$		400 to 800	V
$t_q$	Range	10 to 30	μs
$T_J$		-40 to 125	°C

**ELECTRICAL SPECIFICATIONS**

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST333C..C	04	400	500	50
	08	800	900	



CURRENT CARRYING CAPABILITY							
FREQUENCY							UNITS
50 Hz	1630	1420	2520	2260	7610	6820	A
400 Hz	1630	1390	2670	2330	4080	3600	
1000 Hz	1350	1090	2440	2120	2420	2100	
2500 Hz	720	550	1450	1220	1230	1027	
Recovery voltage $V_r$	50		50		50		V
Voltage before turn-on $V_d$	$V_{DRM}$		$V_{DRM}$		$V_{DRM}$		
Rise of on-state current $di/dt$	50		-		-		A/ $\mu$ s
Heatsink temperature	40	55	40	55	40	55	$^{\circ}$ C
Equivalent values for RC circuit	10/0.47		10/0.47		10/0.47		$\Omega/\mu$ F

ON-STATE CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave Double side (single side) cooled			720 (350)	A
					55 (75)	$^{\circ}$ C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 $^{\circ}$ C heatsink temperature double side cooled			1435	A
Maximum peak, one half cycle, non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	11 000	
		t = 8.3 ms			11 500	
		t = 10 ms	100 % $V_{RRM}$ reapplied		9250	
		t = 8.3 ms			9700	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	605	$kA^2s$
		t = 8.3 ms			553	
		t = 10 ms	100 % $V_{RRM}$ reapplied		428	
		t = 8.3 ms			391	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			6050	$kA^2\sqrt{s}$
Maximum peak on-state voltage	$V_{TM}$	$I_{TM} = 1810$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine wave pulse			1.96	V
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7 \% \times \pi \times I_{T(AV)}) < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum			0.91	
High level value of threshold voltage	$V_{T(TO)2}$	$I > \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum			0.93	
Low level value of forward slope resistance	$r_{t1}$	$(16.7 \% \times \pi \times I_{T(AV)}) < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum			0.58	$m\Omega$
High level value of forward slope resistance	$r_{t2}$	$I > \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum			0.58	
Maximum holding current	$I_H$	$T_J = 25$ $^{\circ}$ C, $I_T > 30$ A			600	mA
Typical latching current	$I_L$	$T_J = 25$ $^{\circ}$ C, $V_A = 12$ V, $R_a = 6$ $\Omega$ , $I_G = 1$ A			1000	

SWITCHING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS	
			MIN.	MAX.		
Maximum non-repetitive rate of rise of turned on current	$di/dt$	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$ ; $I_{TM} = 2 \times di/dt$	1000		A/ $\mu$ s	
Typical delay time	$t_d$	$T_J = 25$ $^{\circ}$ C, $V_{DM} = \text{Rated } V_{DRM}$ ; $I_{TM} = 50$ A DC, $t_p = 1$ $\mu$ s Resistive load, gate pulse: 10 V, 5 $\Omega$ source	1.1		$\mu$ s	
Maximum turn-off time	$t_q$	$T_J = T_J$ maximum, $I_{TM} = 550$ A, commutating $di/dt = 40$ A/ $\mu$ s $V_R = 50$ V, $t_p = 500$ $\mu$ s, $dV/dt$ : See table in device code	10	30		



<b>BLOCKING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T <sub>J</sub> = T <sub>J</sub> maximum, linear to 80 % V <sub>DRM</sub> , higher value available on request	500	V/μs
Maximum peak reverse and off-state leakage current	I <sub>RRM</sub> , I <sub>DRM</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, rated V <sub>DRM</sub> /V <sub>RRM</sub> applied	50	mA

<b>TRIGGERING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P <sub>GM</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, f = 50 Hz, d% = 50	60	W
Maximum average gate power	P <sub>G(AV)</sub>		10	
Maximum peak positive gate current	I <sub>GM</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, t <sub>p</sub> ≤ 5 ms	10	A
Maximum peak positive gate voltage	+ V <sub>GM</sub>		20	
Maximum peak negative gate voltage	- V <sub>GM</sub>		5	
Maximum DC gate current required to trigger	I <sub>GT</sub>	T <sub>J</sub> = 25 °C, V <sub>A</sub> = 12 V, R <sub>a</sub> = 6 Ω	200	mA
Maximum DC gate voltage required to trigger	V <sub>GT</sub>		3	
Maximum DC gate current not to trigger	I <sub>GD</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, rated V <sub>DRM</sub> applied	20	mA
Maximum DC gate voltage not to trigger	V <sub>GD</sub>		0.25	

<b>THERMAL AND MECHANICAL SPECIFICATIONS</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating temperature range	T <sub>J</sub>		-40 to 125	°C
Maximum storage temperature range	T <sub>Stg</sub>		-40 to 150	
Maximum thermal resistance, junction to heatsink	R <sub>thJ-hs</sub>	DC operation single side cooled	0.09	K/W
		DC operation double side cooled	0.04	
Maximum thermal resistance, case to heatsink	R <sub>thC-hs</sub>	DC operation single side cooled	0.020	
		DC operation double side cooled	0.010	
Mounting force, ± 10 %			9800 (1000)	N (kg)
Approximate weight			83	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (E-PUK)	

<b>ΔR<sub>thJ-hs</sub> CONDUCTION</b>						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.010	0.011	0.007	0.007	T <sub>J</sub> = T <sub>J</sub> maximum	K/W
120°	0.012	0.012	0.012	0.013		
90°	0.015	0.015	0.016	0.017		
60°	0.022	0.022	0.023	0.023		
30°	0.036	0.036	0.036	0.037		

**Note**

- The table above shows the increment of thermal resistance R<sub>thJ-hs</sub> when devices operate at different conduction angles than DC

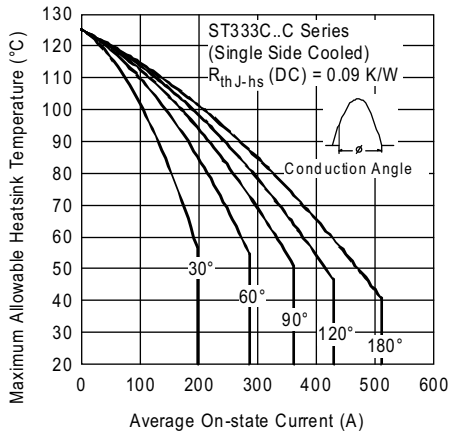


Fig. 1 - Current Ratings Characteristics

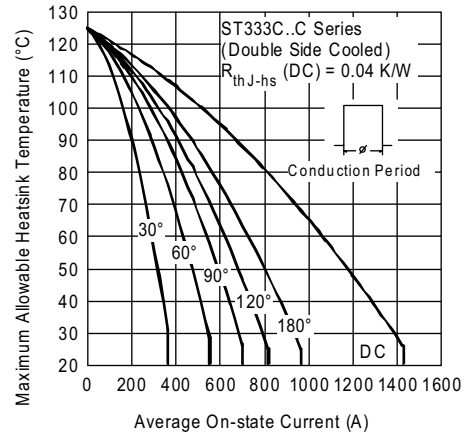


Fig. 4 - Current Ratings Characteristics

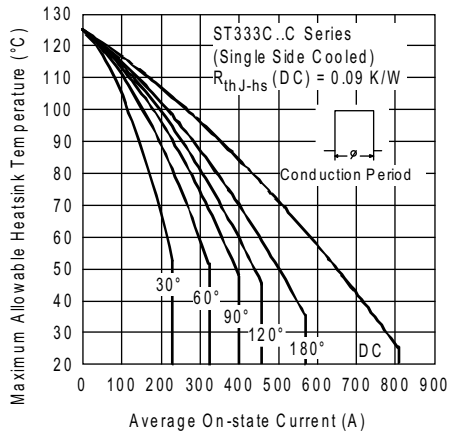


Fig. 2 - Current Ratings Characteristics

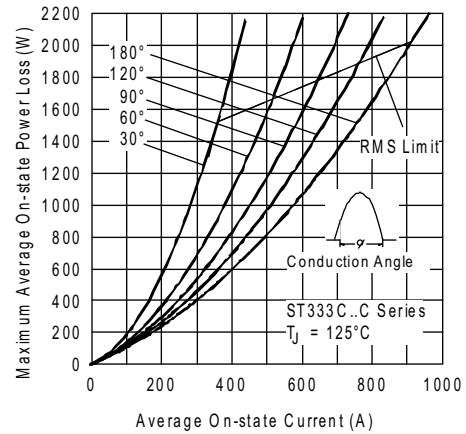


Fig. 5 - On-State Power Loss Characteristics

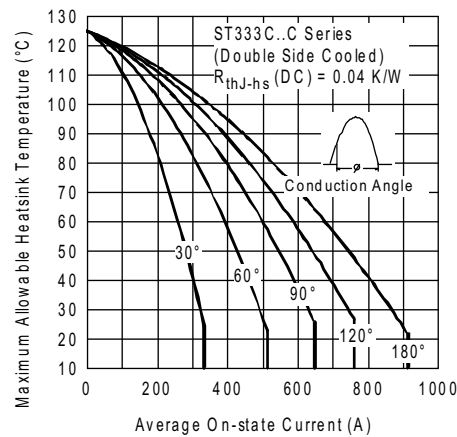


Fig. 3 - Current Ratings Characteristics

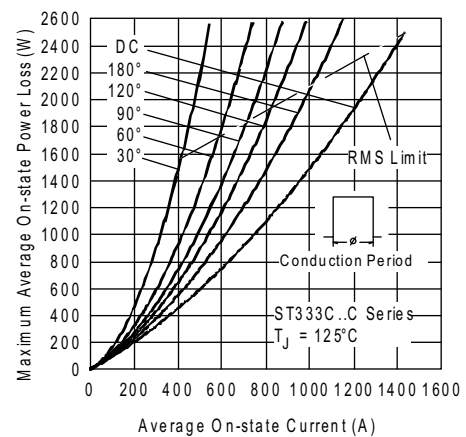


Fig. 6 - On-State Power Loss Characteristics



Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

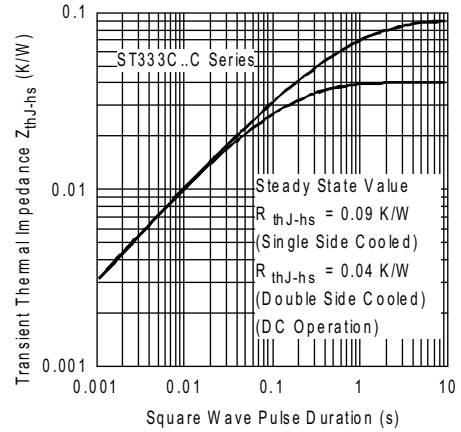


Fig. 10 - Thermal Impedance  $Z_{thJ-hs}$  Characteristics



Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

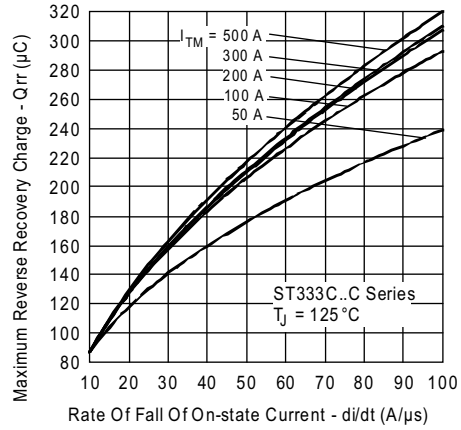


Fig. 11 - Reverse Recovered Charge Characteristics



Fig. 9 - On-State Voltage Drop Characteristics

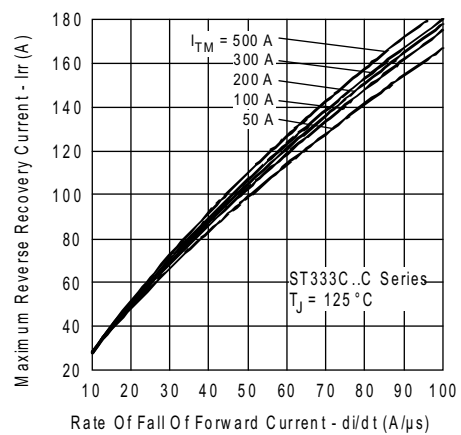


Fig. 12 - Reverse Recovery Current Characteristics

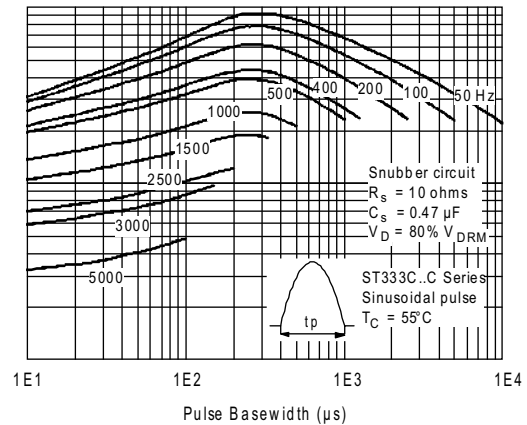
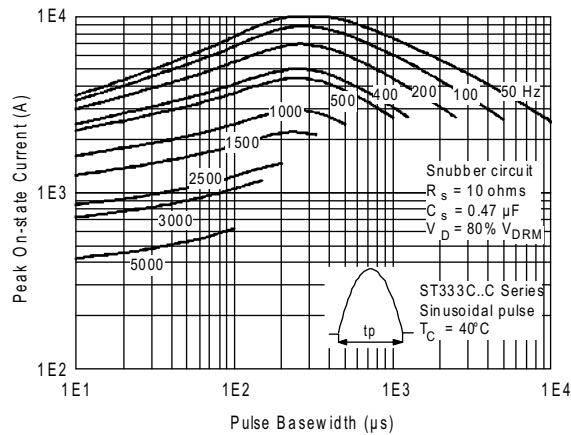


Fig. 13 - Frequency Characteristics

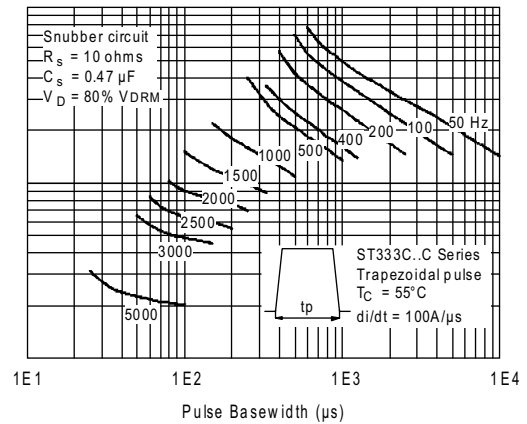
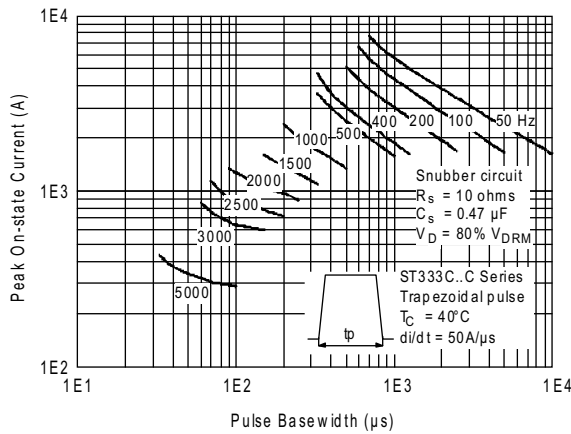


Fig. 14 - Frequency Characteristics

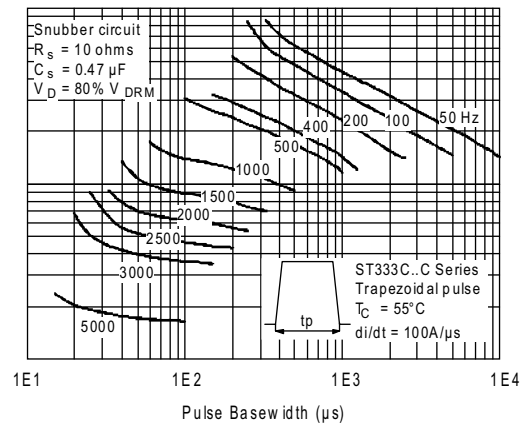
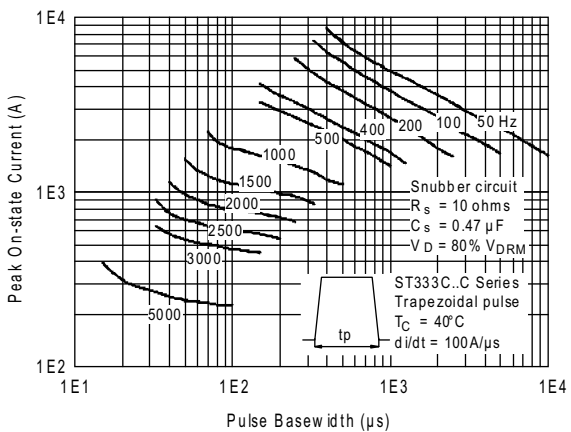


Fig. 15 - Frequency Characteristics



Fig. 16 - Maximum On-State Energy Power Loss Characteristics

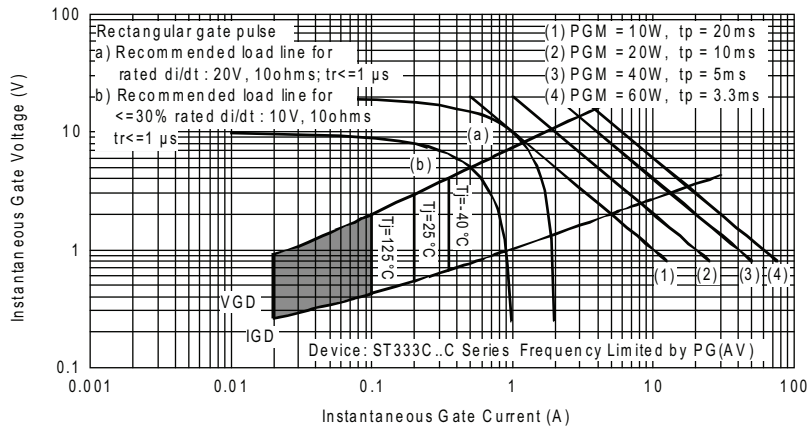


Fig. 17 - Gate Characteristics



ORDERING INFORMATION TABLE

Device code	<b>VS-</b>	<b>ST</b>	<b>33</b>	<b>3</b>	<b>C</b>	<b>08</b>	<b>C</b>	<b>H</b>	<b>K</b>	<b>1</b>	<b>-</b>
	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪

- 1** - Vishay Semiconductors product
- 2** - Thyristor
- 3** - Essential part number
- 4** - 3 = Fast turn off
- 5** - C = Ceramic PUK
- 6** - Voltage code x 100 =  $V_{RRM}$  (see Voltage Ratings table)
- C = PUK case TO-200AB (E-PUK)
- 7** - Reapplied dV/dt code (for  $t_q$  test condition)
- 8** -  $t_q$  code
- 9** - 0 = Eyelet term.
- 10** - (gate and aux. cathode unsoldered leads)  
1 = Fast-on term.  
(gate and aux. cathode unsoldered leads)  
2 = Eyelet term.  
(gate and aux. cathode soldered leads)  
3 = Fast-on term.  
(gate and aux. cathode soldered leads)
- 11** - Critical dV/dt:
  - None = 500 V/ $\mu$ s (standard value)
  - L = 1000 V/ $\mu$ s (special selection)

dV/dt - $t_q$ combinations available					
dV/dt (V/ $\mu$ s)	20	50	100	200	400
10	CN	DN	EN	--	--
12	CM	DM	EM	<b>FM*</b>	--
15	CL	DL	EL	<b>FL*</b>	HL
18	CP	DP	EP	FP	HP
20	CK	DK	EK	FK	HK
25	--	--	--	FJ	HJ
30	--	--	--	--	HH

\* Standard part number.  
All other types available only on request.

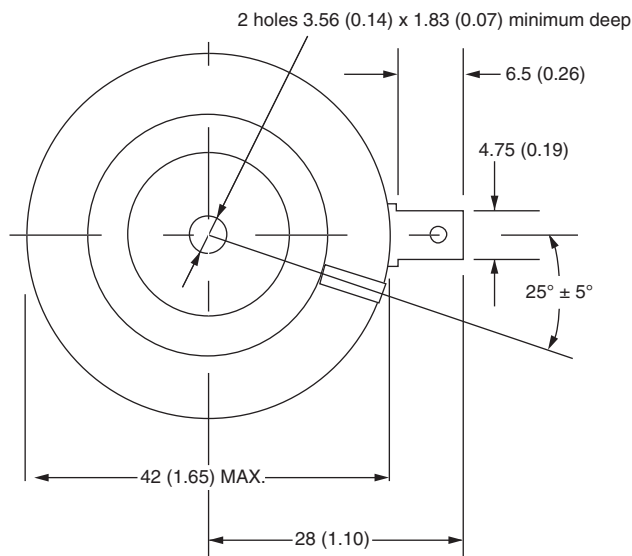
LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95075">http://www.vishay.com/doc?95075</a>



## TO-200AB (E-PUK)

**DIMENSIONS** in millimeters (inches)

Anode to gate  
 Creepage distance: 11.18 (0.44) minimum  
 Strike distance: 7.62 (0.30) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А