

47 μ F AC-Coupling Capacitor 3-Input 1-Output Video Driver with LPF

FEATURES

- Operating Voltage 4.5 to 9.5V
- Small output coupling capacitor 47 μ F
- 3-Input 1-Output Video Switch
- 6dB Amplifier, 75ohm Driver
- Internal LPF 0dBtyp.at 6.75MHz
 -40dBtyp.at 27MHz

- Mute Circuit
- Bipolar Technology
- Package Outline SSOP14

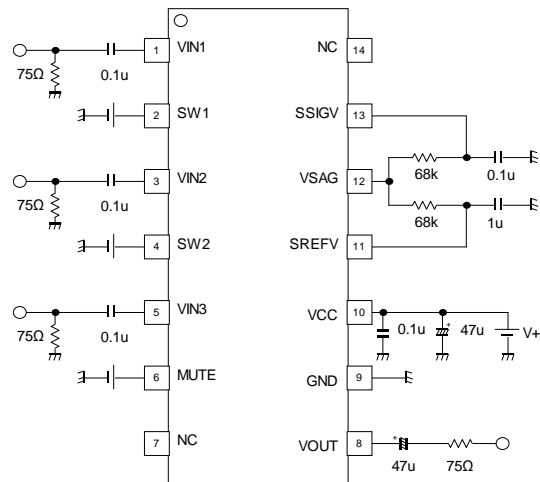
GENERAL DESCRIPTION

NJM41050 is a 3-Input 1-Output general-purpose video switch. It includes 6dB amplifier and 75ohm driver circuit. The NJRC original Technology "ASC(Advanced SAG Correction)" realizes 47 μ F AC-Coupling Capacitor which enables to downsize mounting space.

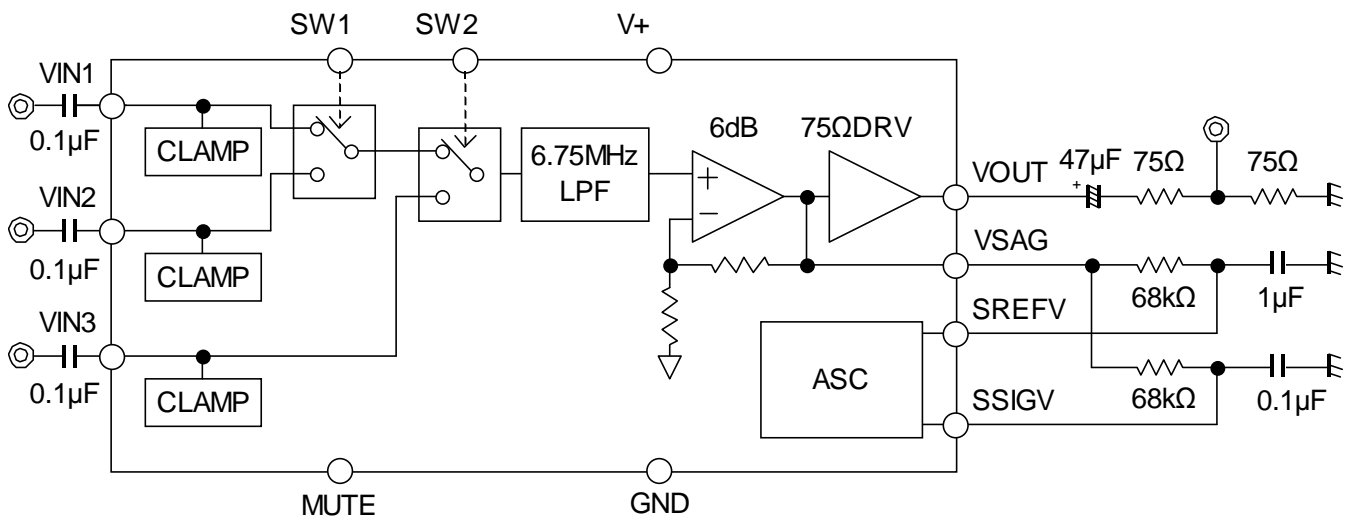
APPLICATION

- Car Navigation
- AV Receiver

APPLICATION CIRCUIT



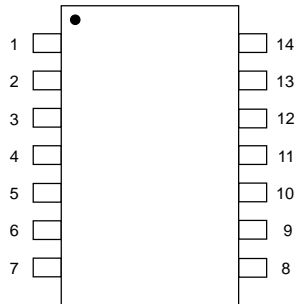
EQUIVALENT CIRCUIT · BLOCK DIAGRAM



■47μF AC-Coupling Capacitor Video Switch Series

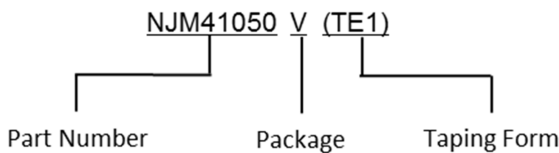
Input-Output	Part No.
8in-2out	NJW1341
4in-2out	NJW1342

■PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	VIN1	Video Signal Input Terminal
2	SW1	Video Signal Switch Terminal
3	VIN2	Video Signal Input Terminal
4	SW2	Video Signal Switch Terminal
5	VIN3	Video Signal Input Terminal
6	MUTE	Mute Terminal
7	N.C.	-
8	VOUT	Video Signal Output Terminal
9	GND	GND Terminal
10	VCC	Power Supply Terminal
11	SREFV	Sag correction Terminal
12	VSAG	Sag correction Terminal
13	SSIGV	Sag correction Terminal
14	N.C.	-

■MARK INFORMATION



■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJM41050V	SSOP14	Yes	Yes	Sn-2Bi	41050	65	2,000

■ABSOLUTE MAXIMUM RATINGS

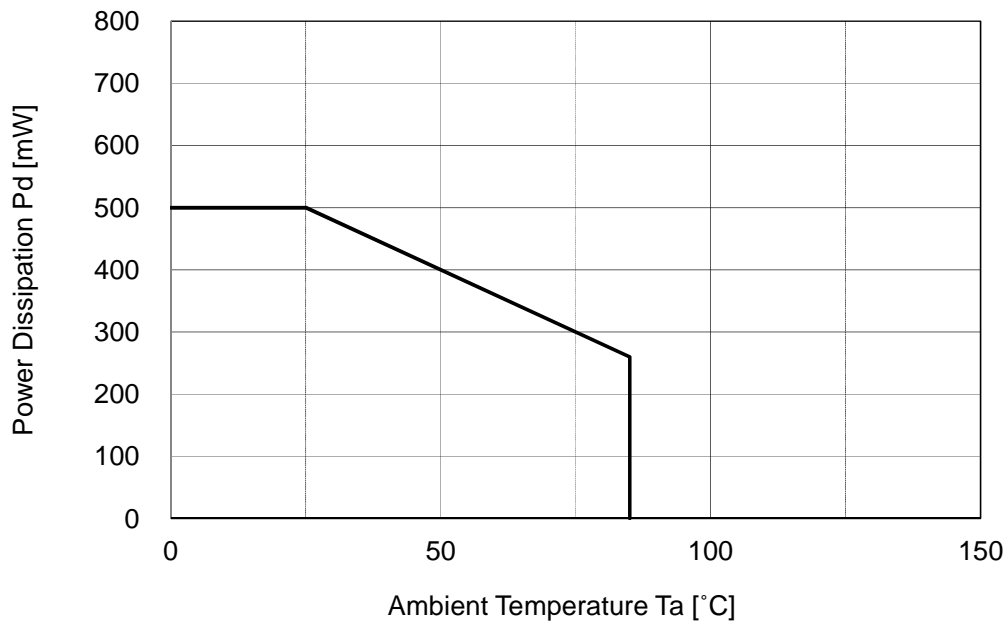
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VCC	13.0	V
Power Dissipation (Ta=25°C) ⁽⁴⁾	P _D	500(1)	mW
Operating Temperature Range	T _{opr}	-40 to +85	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

(1) At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm Two layers, FR-4)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage	Vopr	4.5 to 9.5	V

■POWER DISSIPATION vs. AMBIENT TEMPERATURE



■ ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$, $V^+=5\text{V}$, $R_L=150\Omega$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I_{CC}	No input signal	-	15.0	22.0	mA
Supply Current at Power Save Mode	I_{save}	Mute mode	-	1.5	2.4	mA
Voltage Gain	G_v	$V_{in}=1\text{MHz}$, 1.0Vp-p Sine-signal	5.5	6.0	6.5	dB
Maximum Output Level	V_{om}	$V_{in}=100\text{kHz}$, Sine-signal, THD=1%,	2.2	-	-	Vp-p
LPF Characteristics	$G_{f6.75M}$	$V_{in}=6.75\text{MHz}/1\text{MHz}$, 1.0Vpp Sine-signal	-1.0	0	+1.0	dB
	G_{f27M}	$V_{in}=27\text{MHz}/1\text{MHz}$, 1.0Vpp Sine-signal	-	-40.0	-24.0	
Channel Cross talk	CT	$V_{in}=4.43\text{MHz}$, 1.0Vp-p , Sine-signal	-	-80		dB
Differential Gain	DG	$V_{in}=1.0\text{Vp-p}$ 10step video signal	-	0.5	-	%
Differential Phase	DP	$V_{in}=1.0\text{Vp-p}$ 10step video signal	-	0.5	-	deg
SW Sink Current High Level	I_{SWH}	$V=5\text{V}$	-	-	300	μA
SW Sink Current Low Level	I_{SWL}	$V=0.3\text{V}$	-	-	30	μA
SW Voltage High Level	V_{thH}	SW1,SW2,MUTE	2.0	-	V^+	V
SW Voltage Low Level	V_{thL}	SW1,SW2,MUTE	0	-	1.0	V

■ CONTROL TERMINAL

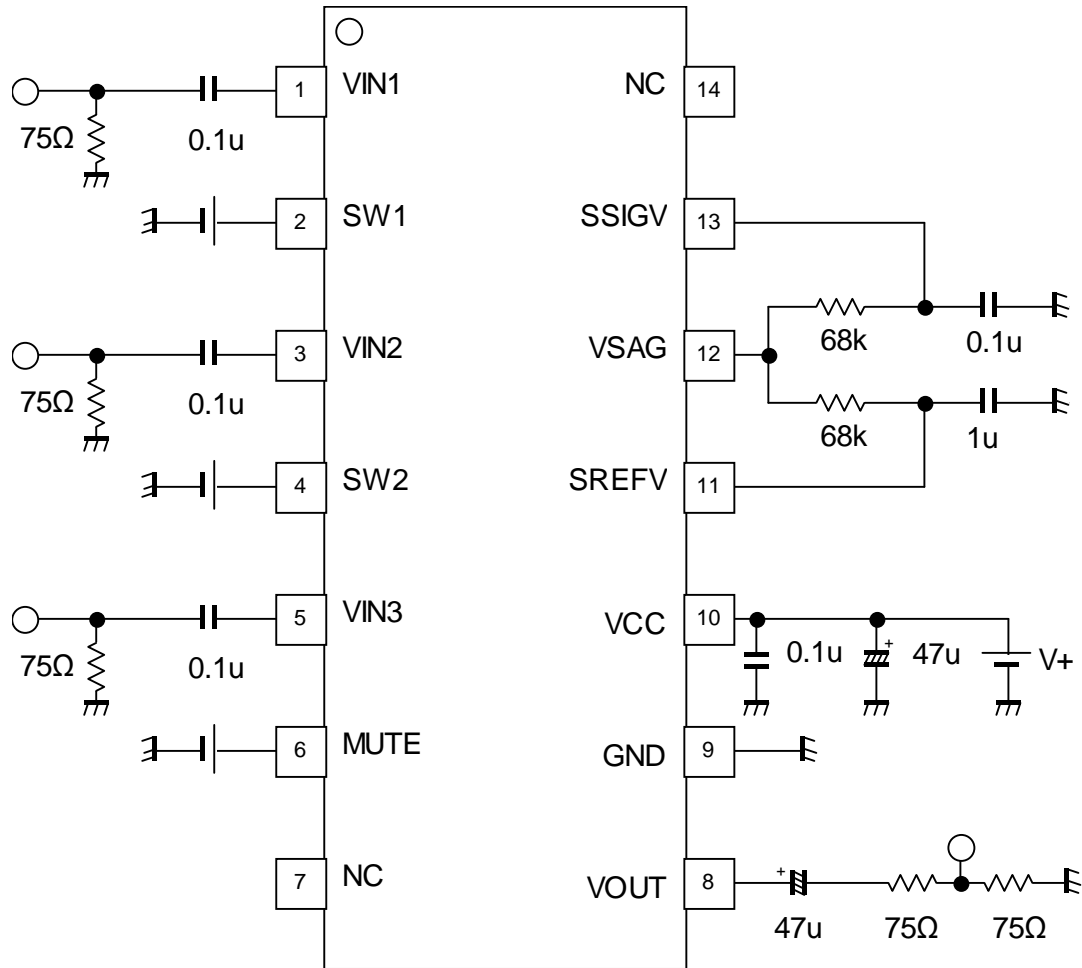
PARAMETER	STATUS	MODE
SW1	H	VIN2 OUTPUT
	L	VIN1 OUTPUT
	OPEN	VIN1 OUTPUT

PARAMETER	STATUS	MODE
SW2	H	VIN3 OUTPUT
	L	VIN1 or VIN2 OUTPUT
	OPEN	VIN1 or VIN2 OUTPUT

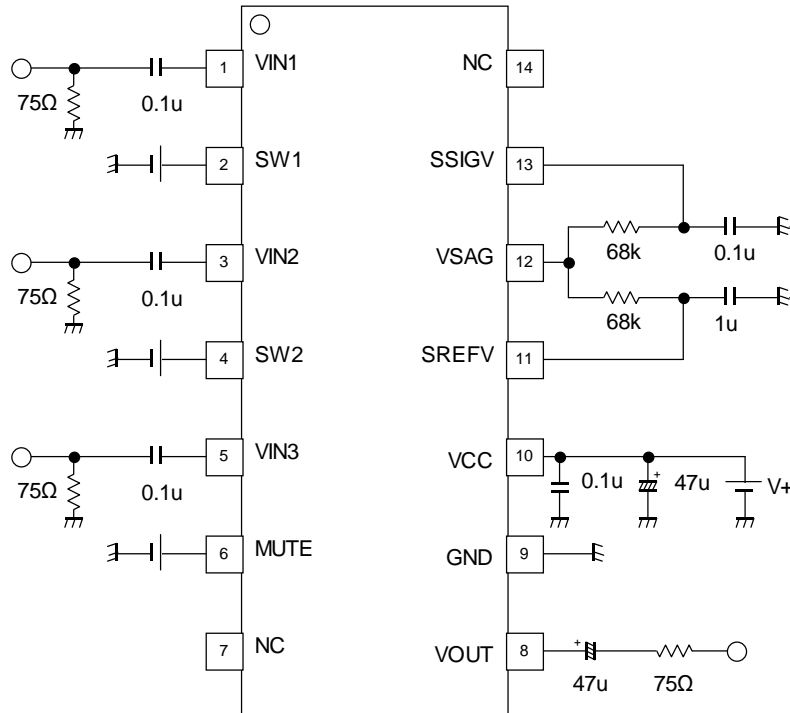
PARAMETER	STATUS	MODE
MUTE	H	ACTIVE
	L	MUTE
	OPEN	MUTE

OUTPUT SIGNAL	SW1	SW2	MUTE
VIN1	L or OPEN	L or OPEN	H
VIN2	H	L or OPEN	H
VIN3	-	H	H
MUTE	-	-	L or OPEN

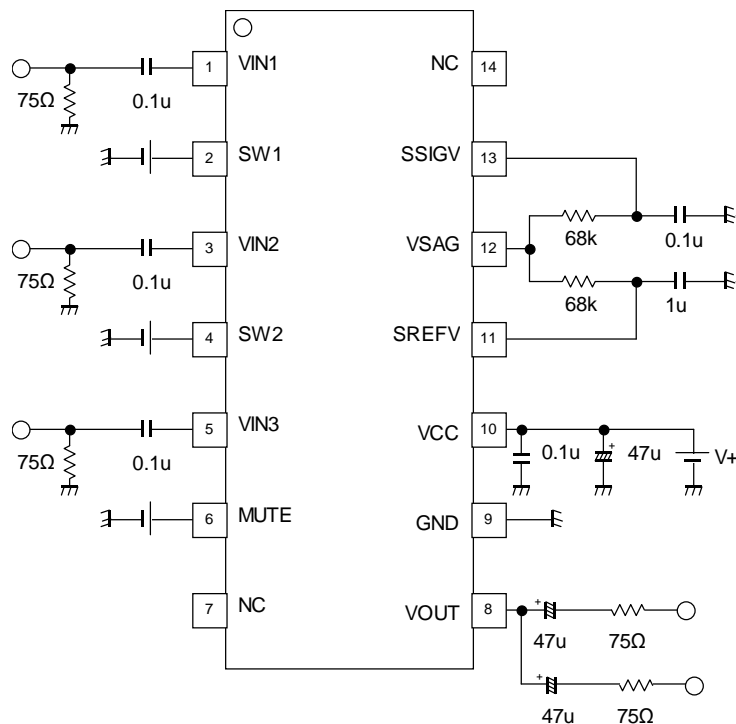
TEST CIRCUIT



APPLICATION CIRCUIT 1



APPLICATION CIRCUIT 2 (Two-system drive)

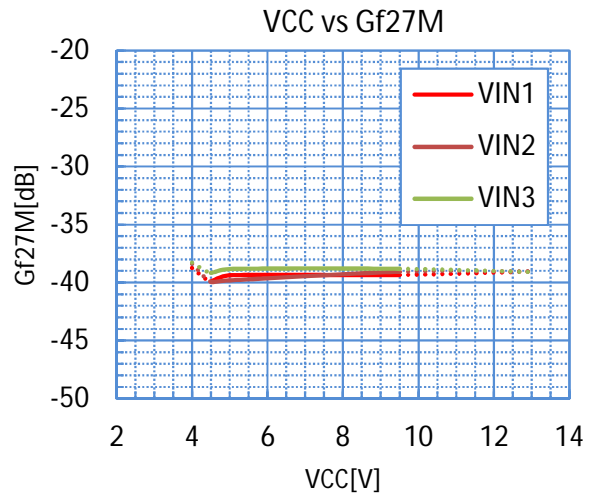
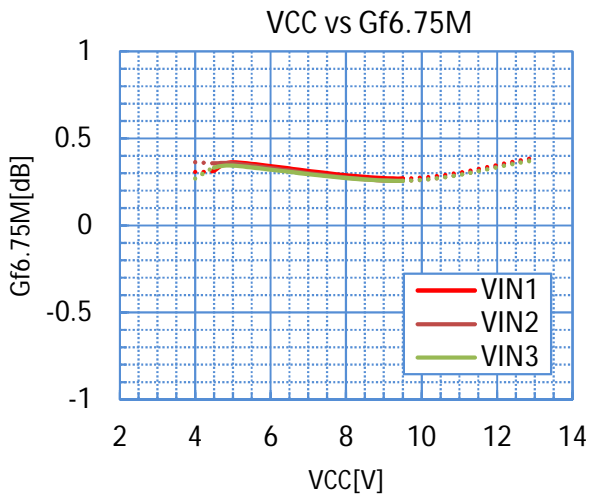
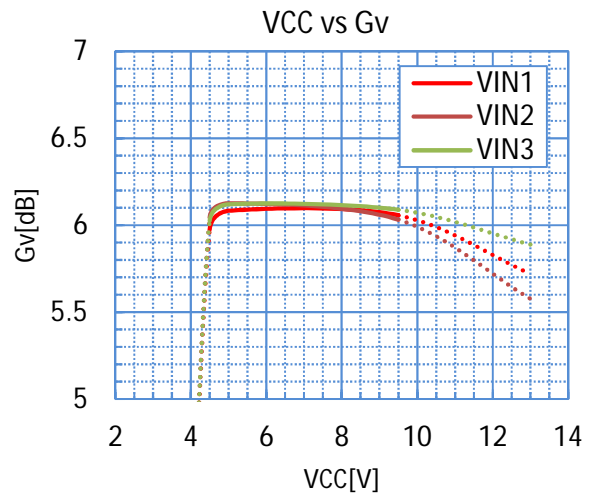
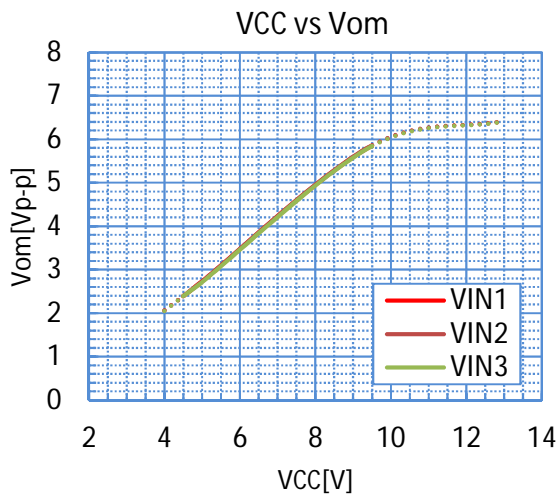
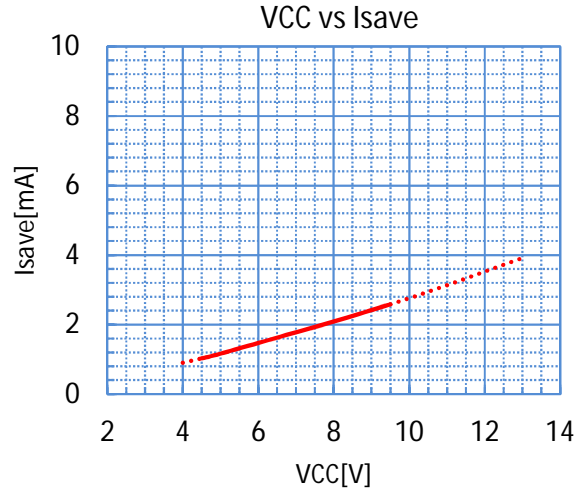
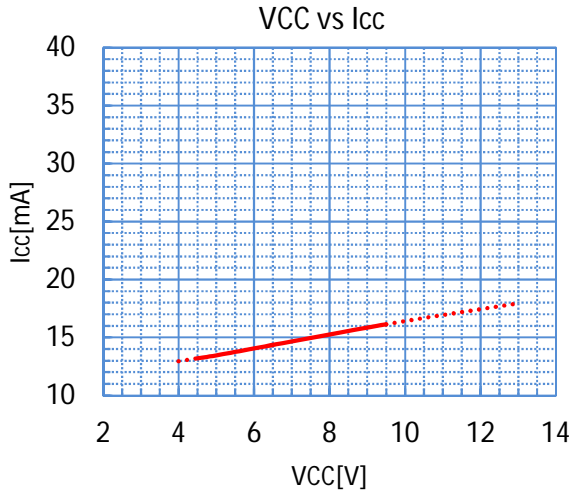


Note) NJM41050 has possibilities that decrease in the capacitance in low-frequency band when the ceramic capacitor is used (pin8). It is a possibility that the sag is generated when the ceramic capacitor decreases capacity. Please verify it in consideration of the capacity drop of the ceramic capacitor.

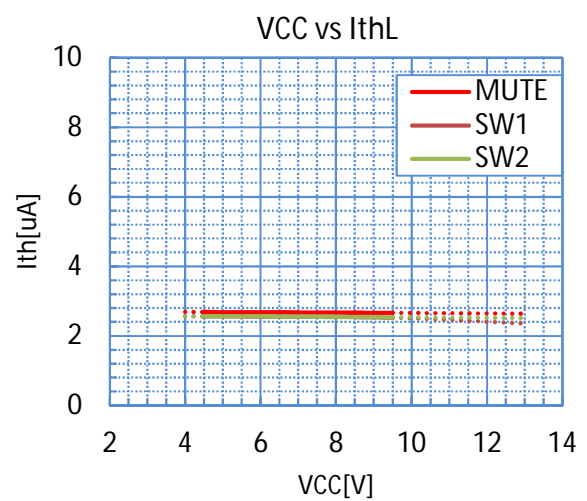
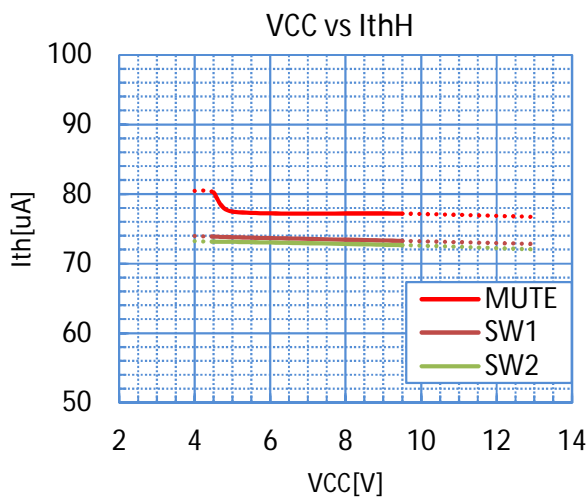
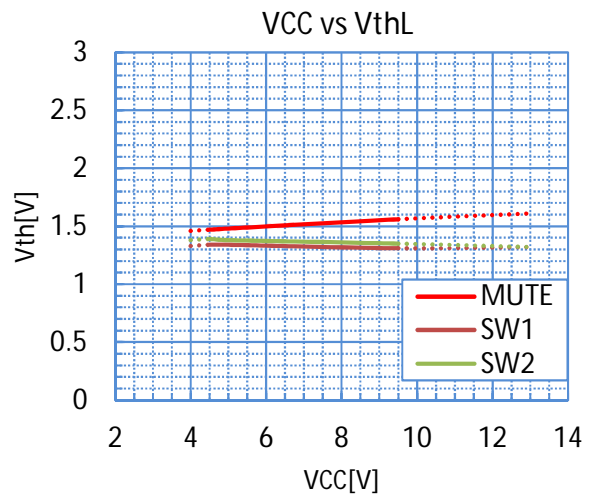
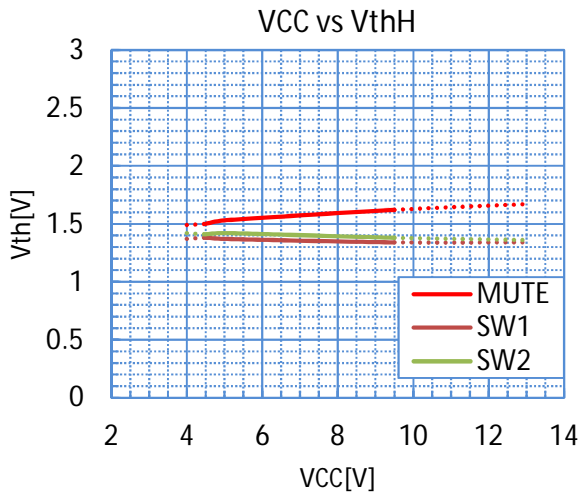
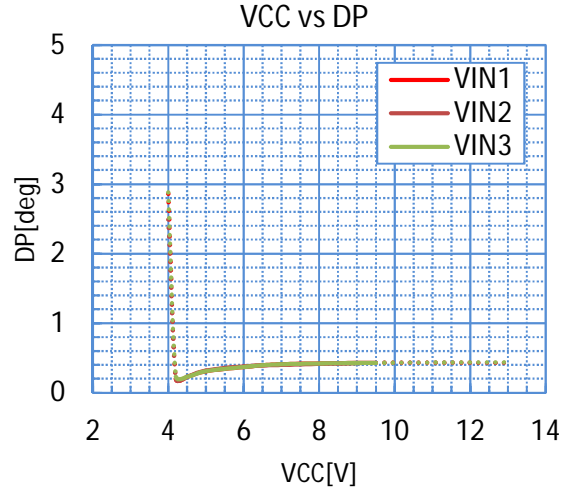
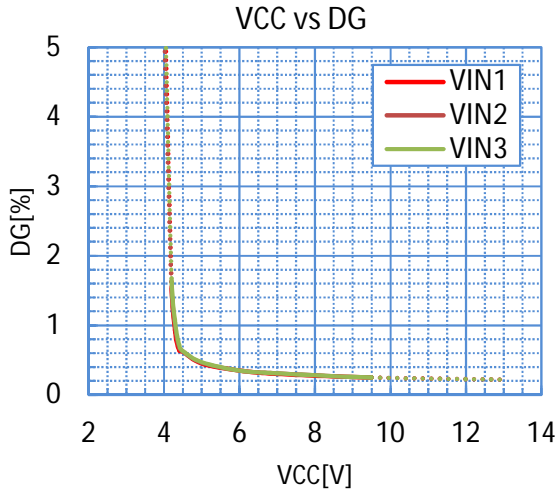
■TERMINAL FUNCTION

PINNo.	PINNAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
1 3 5	VIN1 VIN2 VIN3	Video Signal Input Terminal		1.7V
2 4 6	SW1 SW2 MUTE	Video Signal Switch Terminal Mute Terminal		-
8	VOUT	Video Signal Output Terminal		1.3V
11	SREFV	Sag correction Terminal		1.7V
12	VSAG	Sag correction Terminal		1.7V
13	SSIGV	Sag correction Terminal		1.7V

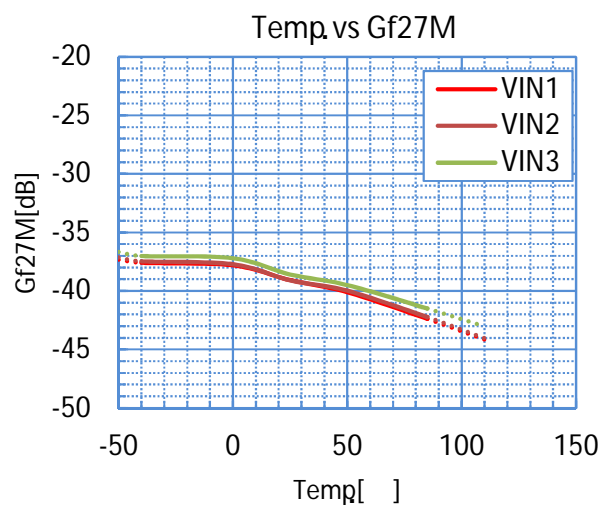
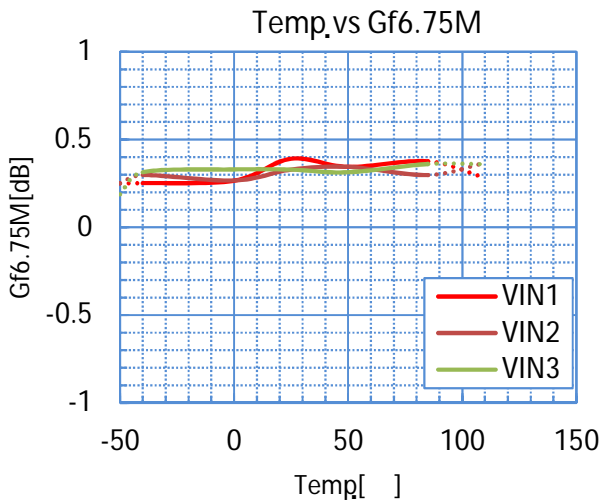
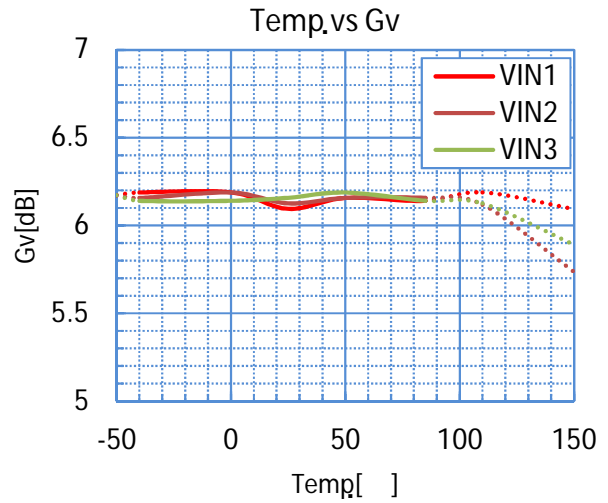
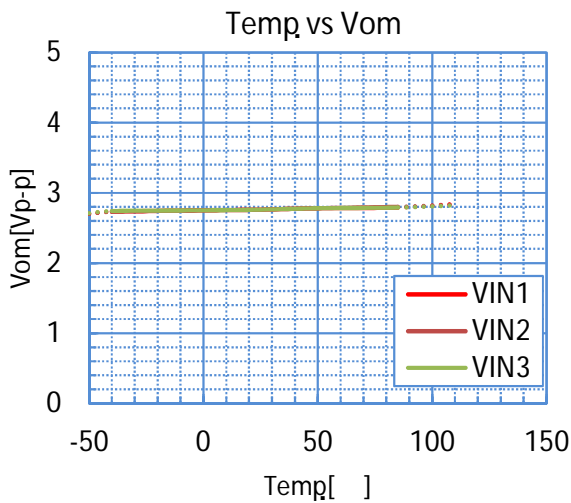
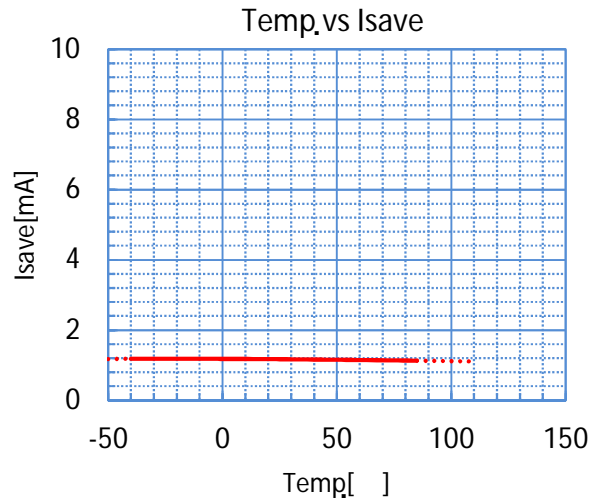
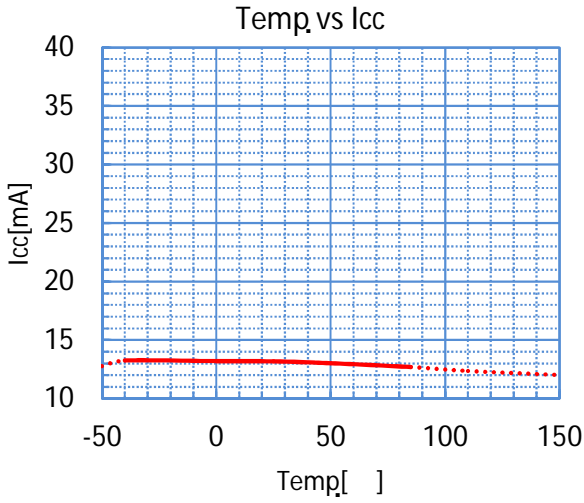
■ TYPICAL CHARACTERISTICS



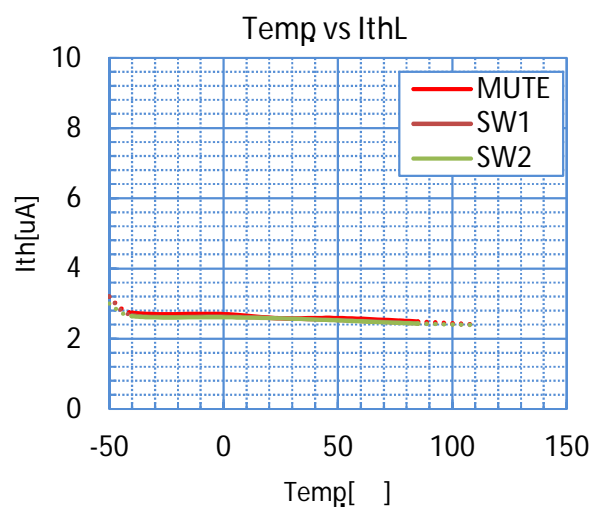
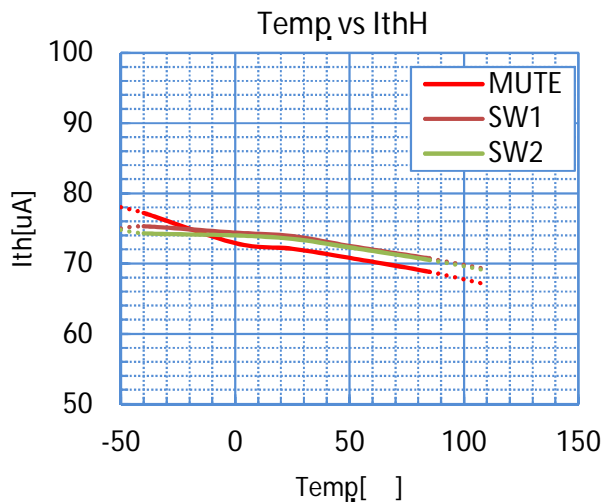
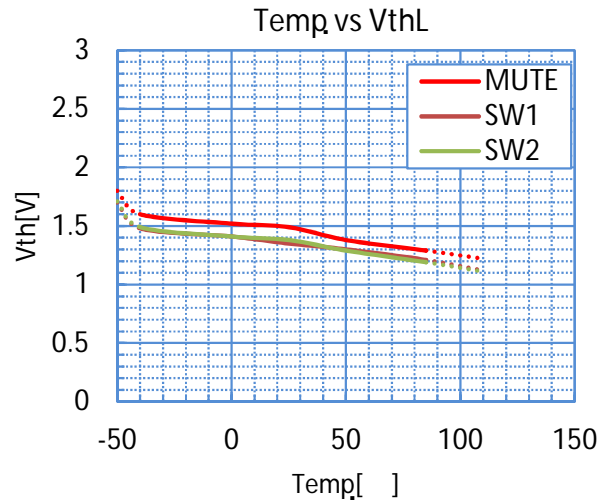
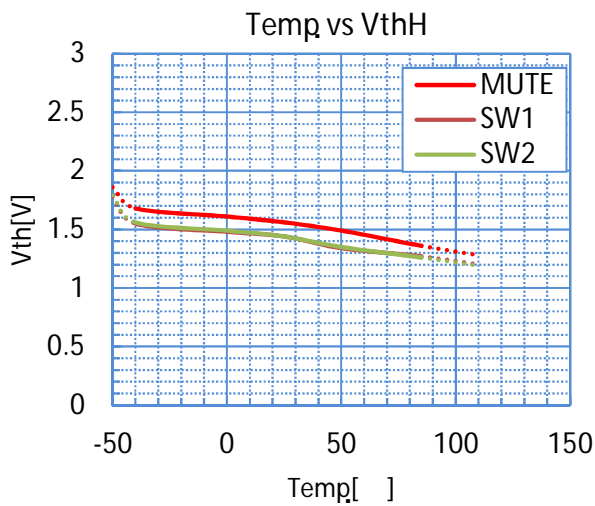
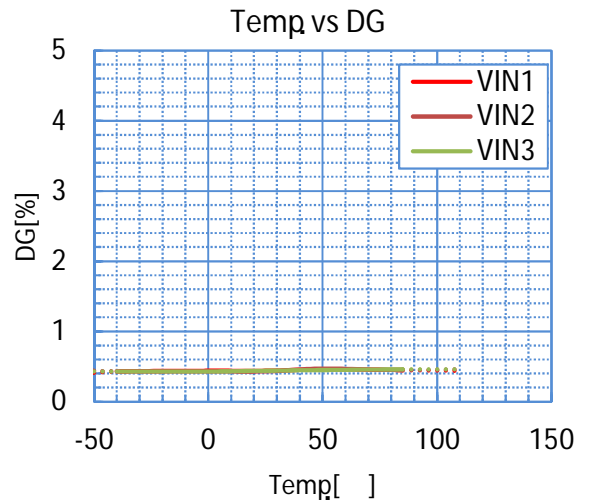
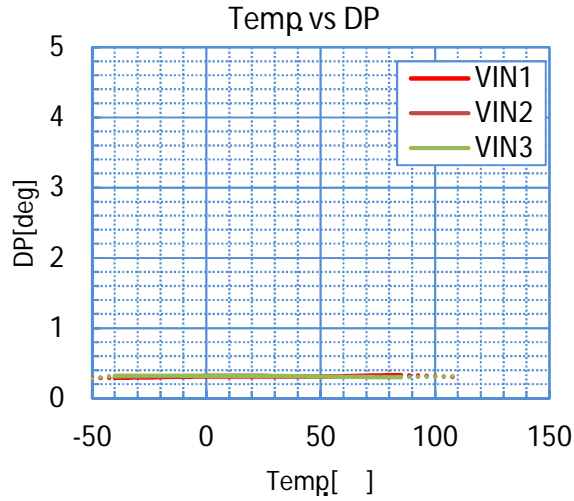
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



■Clamp circuit

1. Operation of Sync-tip-clamp

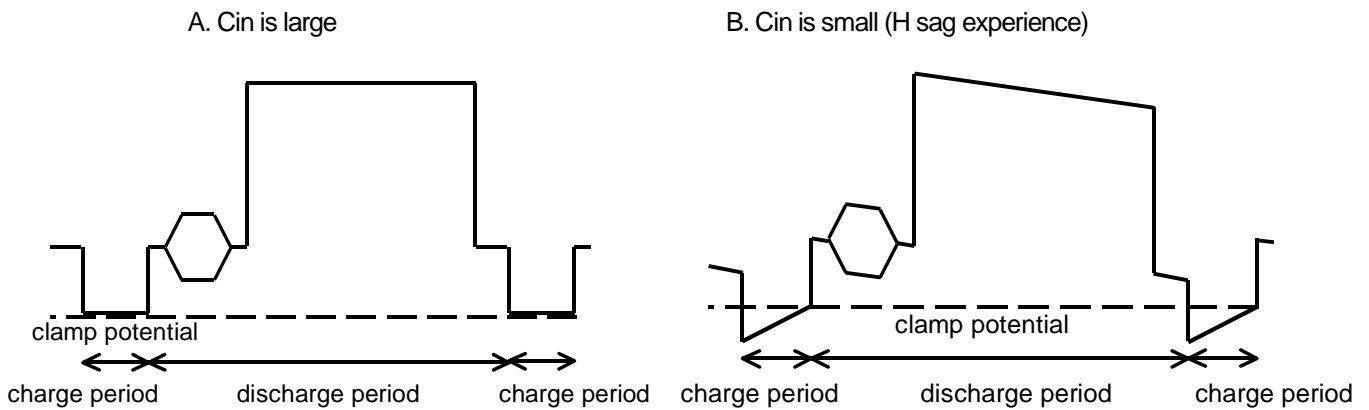
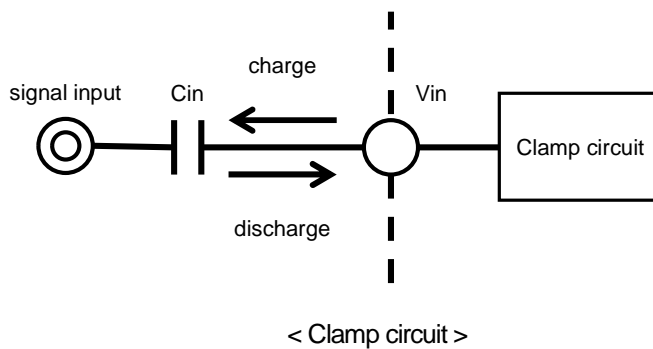
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input C_{in} . It is charged to the capacitor to the external input C_{in} at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor C_{in} at period other than the video signal sync tip. This is due to a small discharge current to the IC.

In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of C_{in} and discharging of C_{in} at every one horizontal period of the video signal.

The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor C_{in} .

If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1 μ F.



< Waveform of input terminal >

2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

The input impedance of the charging period is a few $k\Omega$. On the other hand, the input impedance of the discharge period is several $M\Omega$. Because is a small discharge-current through to the IC.

Thus the input impedance will vary depending on the operating state of the clamp circuit.

3. Impedance of signal source

Source impedance to the input terminal, please lower than 200 Ω . A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

■About the ASC(Advanced SAG Correction) circuit

Advanced SAG Correction circuit is our own sag correction technology (patent). It can reduce the output coupling capacitor than conventional sag correction circuit. You can use the ASC circuit, it will contribute to space saving. Also, because it is not in the output capacitor-less, does not have any anxiety which the output is short-circuited.

This section describes the following four items.

- 1) Overview of the ASC circuit
- 2) How to set up an external circuit
- 3) Circuit example of when the two systems drive
- 4) Notes on Using

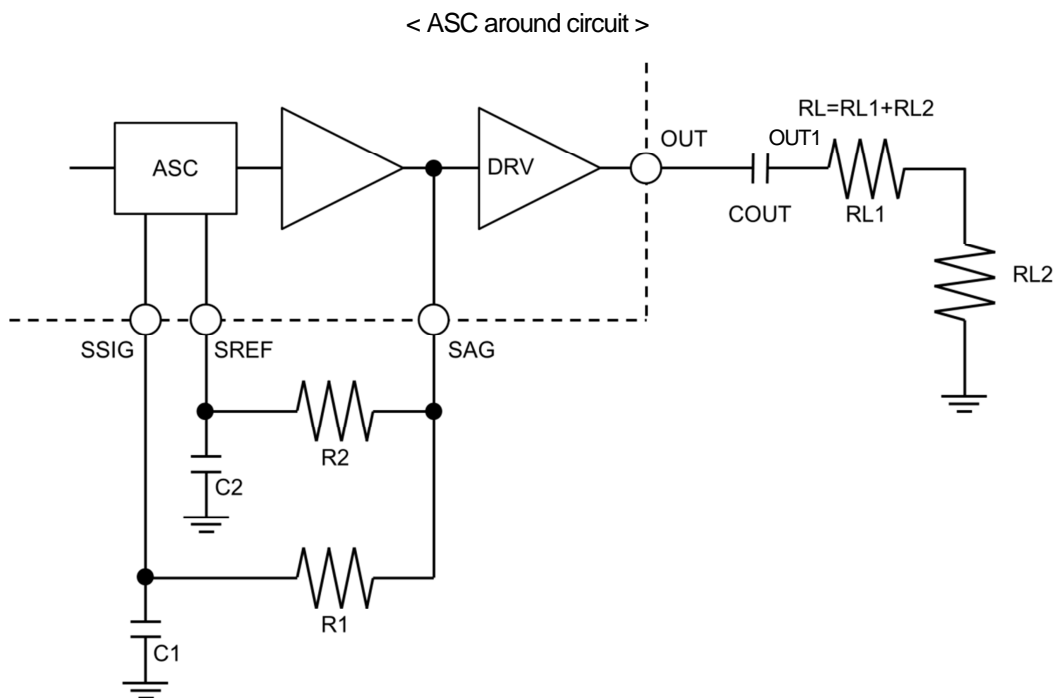
1) Overview of the ASC circuit

A high-pass filter in the load resistance and output coupling capacitor is configured. Sag occurs because the low-frequency component of the signal is attenuated by this high-pass filter. ASC circuit amplifies the low-frequency component of the signal, corrects for attenuation of the low-frequency component.

The figure below shows ASC around circuit.

SAG terminal is a signal output terminal for correcting the sag. Low pass filter of the resistor R1 and the capacitor C1 will cancel the high-pass filter of the load resistor RL and an output coupling capacitor which is connected to the OUT terminal. And, it is connected to the SSIG terminal. The signal input to the SSIG terminal by processing inside the IC, and generates a signal for correcting the sag.

ASC circuit for amplification the low frequency components of the signal, require a wide dynamic range. The low-pass filter of the resistor R2 and the capacitor C2, to generate a signal of APL (Average Picture Level) voltage. And input to the VREF terminal. Use this voltage of SREF terminal it has to optimize the voltage of the internal IC. ASC circuit generates a sag correction waveform by processing the signal of SSIG terminal and SREF terminal. If sag correction component is large, it may exceed the dynamic range of IC. ASC circuit will stop the operation of the sag correction function if it exceeds the dynamic range by sag correction circuit. Therefore, and preventing that the signal is clipped to fit within the dynamic range.



2) How to set up an external circuit

This section describes the constant setting steps of the ASC around circuit.

- 1: First, determine the cut-off frequency: f_{cut} of the high-pass filter to resistance: R_L and the output capacitor: C_{OUT} of the OUT terminal is configured.

The output capacitor: C_{OUT} , please be more than 47 μ F.

$$f_{cut} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_L}$$

- 2: The low-pass filter with a resistor R_1 (> 10k Ω) and capacitor C_1 is configured. Please refer to the cut-off frequency f_{c1} the same as f_{cut} .

$$f_{c1} = \frac{1}{2\pi \cdot C_1 \cdot R_1} = f_{cut}$$

- 3: The low-pass filter with a resistor R_2 (> 10k Ω) and capacitor C_2 is configured. Please do cut-off frequency f_{c2} is less than or equal to 3Hz.

$$f_{c2} = \frac{1}{2\pi \cdot C_2 \cdot R_2} \leq 3$$

- 4: Please make sure that the combined resistance $R_1 // R_2$ of the resistors R_1 and R_2 is equal to or more than 5k Ω .
And please check the sag characteristics.

Parameter Set example

Set the constant in the case where the output capacitor $C_{OUT} = 47\mu$ F, and a resistor $R_L = 150\Omega$.

1. Calculate the cut-off frequency of the high-pass filter formed by capacitor 47 μ F and resistance 150 Ω of OUT terminal.

$$f_{cut} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_L} = \frac{1}{2\pi \cdot 47\mu \cdot 150} = 22.6[\text{Hz}]$$

2. LPF is configured by a resistor R_1 (> 10k Ω) and capacitor C_1 , and so the cut-off frequency f_{c1} is the same as f_{cut} .

$$f_{c1} = \frac{1}{2\pi \cdot C_1 \cdot R_1} = \frac{1}{2\pi \cdot 0.1\mu \cdot R_1} = 22.6$$

$$R_1 = \frac{1}{2\pi \cdot 0.1\mu \cdot 22.6} = 70.4[\text{k}\Omega] \cong 68[\text{k}\Omega]$$

Calculation results of the resistor R_1 is 70.4k Ω . Here are the 68k Ω available at E6 series.

3. LPF is configured by a resistor R_2 (> 10k Ω) and capacitor C_2 , and cut-off frequency f_{c2} is set to be less than 3Hz.

When the capacitor C_2 to 1 μ F, and will be as follows.

$$f_{c2} = \frac{1}{2\pi \cdot C_2 \cdot R_2} = \frac{1}{2\pi \cdot 1\mu \cdot R_2} < 3$$

$$R_2 > \frac{1}{2\pi \cdot 1\mu \cdot 3} = 53[\text{k}\Omega] \Rightarrow 68[\text{k}\Omega]$$

Calculation results of the resistor R_2 must be more than or equal to 53k Ω . Therefore, it is the resistor R_1 and the same 68k Ω .

4. Make sure that the combined resistance of R_1 and R_2 is equal to or more than 5k Ω

$$R_1 // R_2 = 68k // 68k = 34k$$

After constant determination, each characteristic is please makes sure that there is no problem.

This setting example is the same as the test circuit diagram of the data sheet.

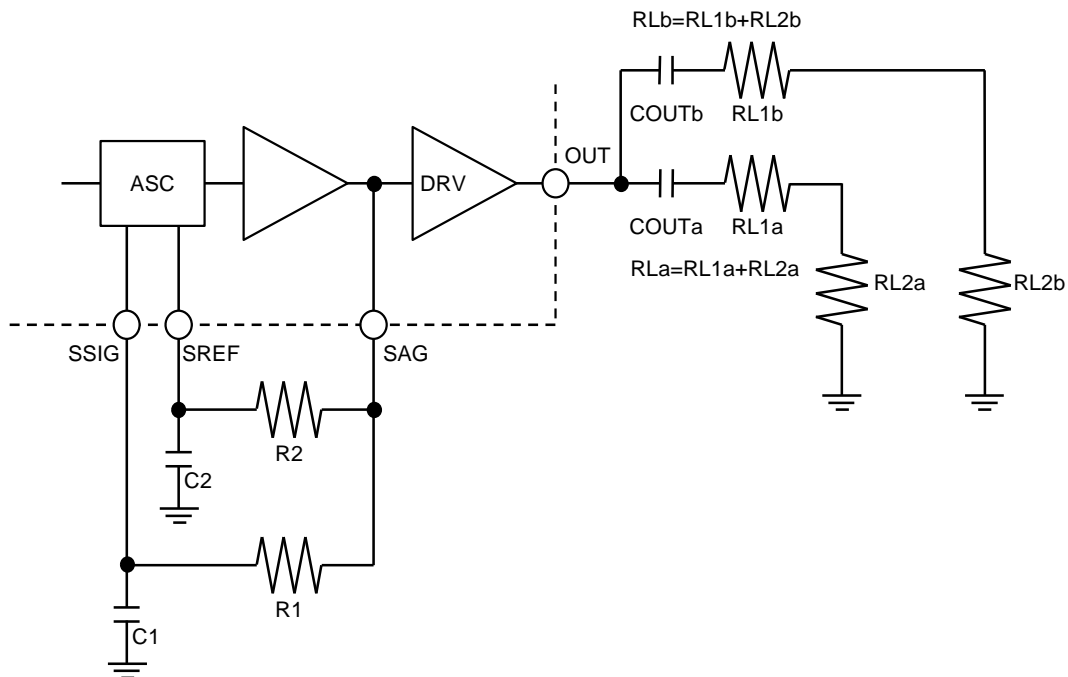
3) Circuit example of two systems drive

An example of a circuit of the two systems drive is shown in the following figure. In the case of a two-system drive, the output capacitor requires $COUTa$ and $COUTb$. As the cut-off frequency of the high-pass filter is the same, the output capacitor ($COUTa$, $COUTb$) and resistance (RLa , RLb) please set.

$$f_{cout} = \frac{1}{2\pi \cdot COUTa \cdot RLa} = \frac{1}{2\pi \cdot COUTb \cdot RLb}$$

Element constant of SAG terminal and SSIG terminal and SREF terminal, please set according to the previous section on how to set up.

< Two system drive circuit >



4) Usage note

Resistance value of SAG terminal $R (= R1 // R2)$, please be more than $5k\Omega$.

If the resistance is small, the signal to output to the OUT terminal may be distorted.

Wiring of SAG terminal and SREF terminal and SSIG terminal please do as much as possible short.

If the noise is mixed to these terminals, the noise is mixed in signals output to the OUT terminal.

If you want to use a ceramic capacitor, please use a capacitor with good DC bias characteristics.

Ceramic capacitors, capacitance value will vary depending on the DC voltage to be applied. This characteristic is referred to as the DC bias characteristics. There is the actual capacitance value and the desired capacitance value is shifted by this DC bias characteristics. Thereby, it may sag correction function does not work well.

You may also set the constants of external elements does not work sag correction function.

If sag correction component is large, it becomes a waveform signal exceeds the dynamic range of the IC.

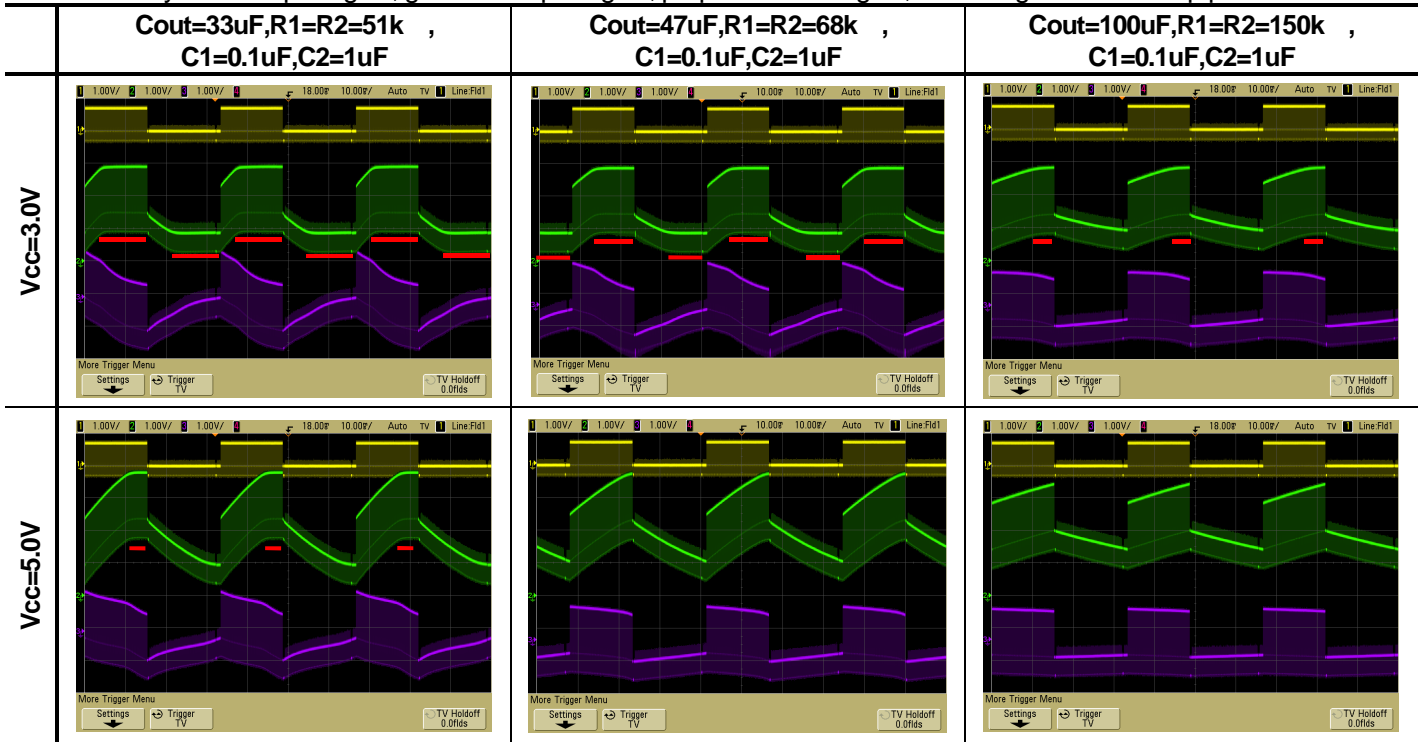
In order to prevent that the signal exceeds the dynamic range is to clip, ASC circuit will stop the sag correction function.

In this case, whether to enhance the power supply voltage, or change each element constant by increasing the output capacitor

Waveform example

Input: Bounce signal (IRE0%, IRE100%, 30Hz), $R_L=150\Omega$

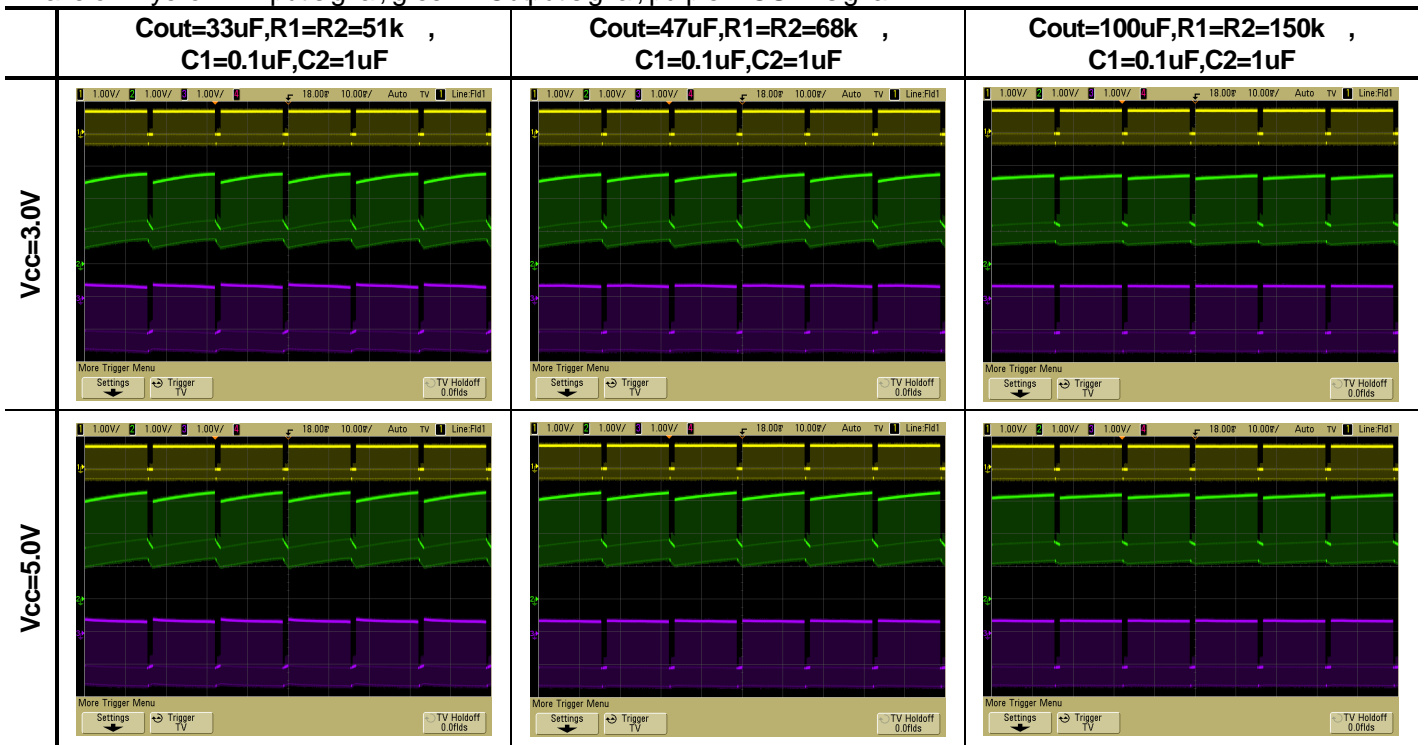
Waveform: yellow = Input signal, green = Output signal, purple = OUT1 signal, red = Sag correction stop period



If the power supply voltage is low, if the output capacitor is small, to prevent signal clipping beyond the dynamic range of the OUT terminal, sag correction function stops.

Input: White 100%, $R_L=150\Omega$

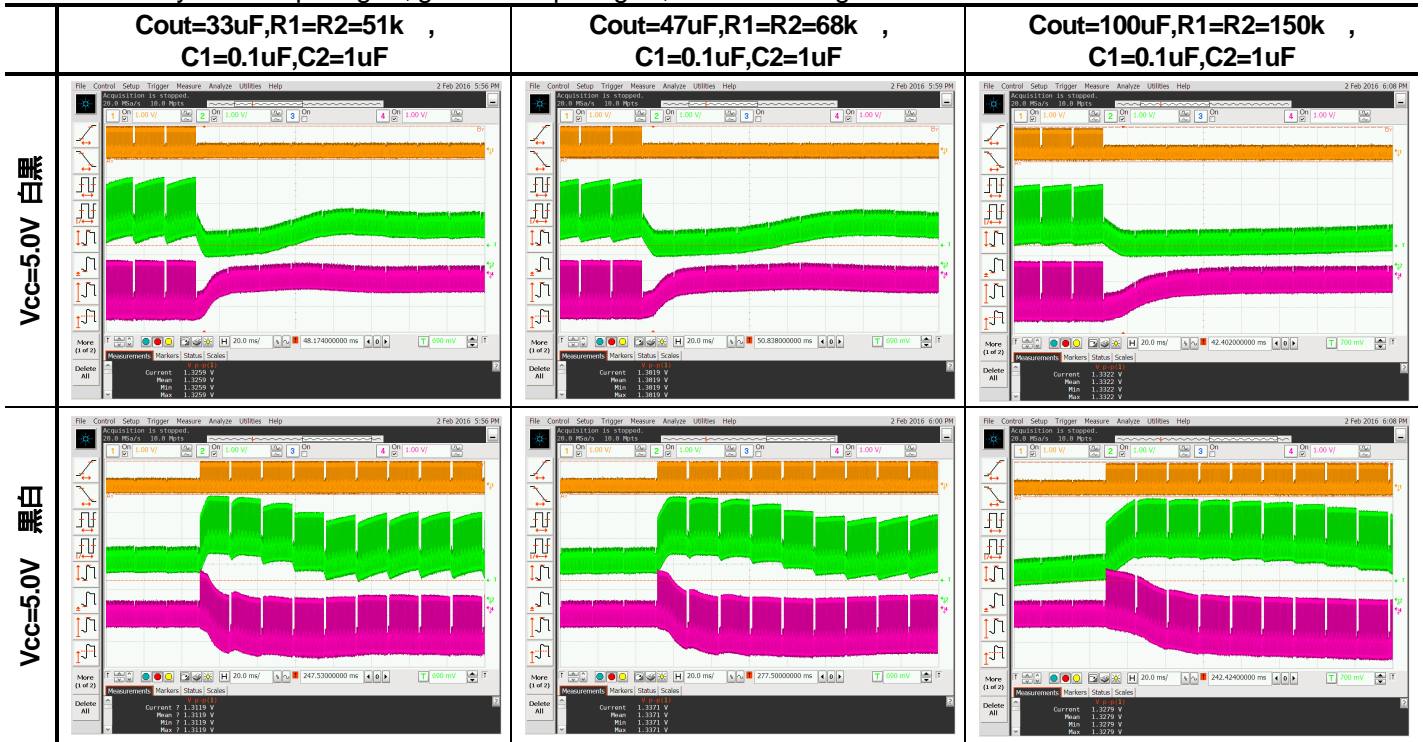
Waveform: yellow = Input signal, green = Output signal, purple = OUT1 signal



■Waveform example at Black-and-White change

Input: Black-and-White change signal, $R_L=150\Omega$

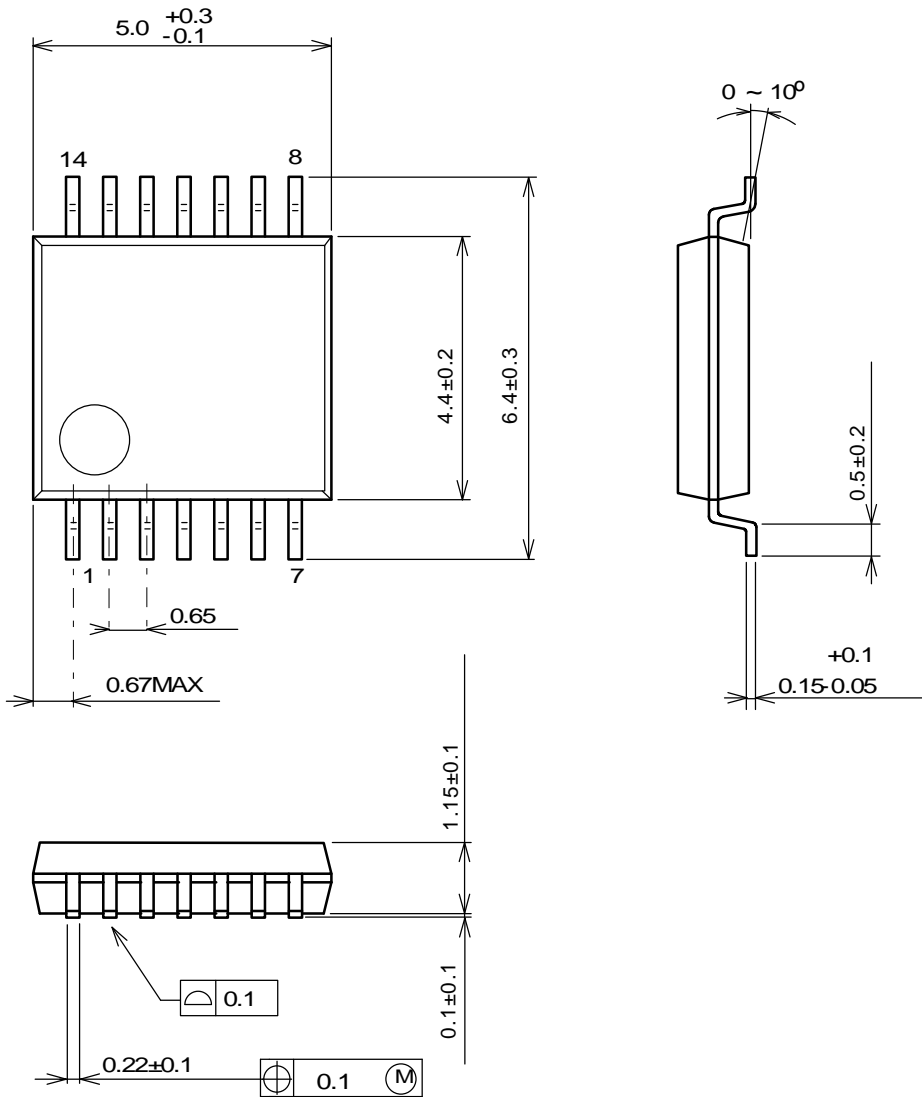
Waveform: yellow = Input signal, green = Output signal, red = OUT1 signal



DC level will change by APL fluctuation at the black-and-white change. The rate of change of the DC level is dependent on the capacitance value of C_{out} .

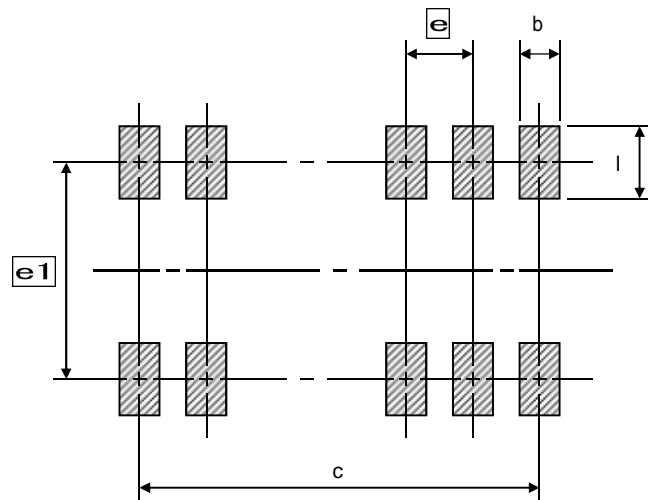
PACKAGE OUTLINE

SSOP14



SOLDER FOOT PRINT

PKG	b	l	c	e1	e
SSOP14	0.35	1.00	3.90	5.90	0.65



Note : These solder foot print dimensions are just examples.
When designing PCB, please estimate the pattern carefully.

Unit : mm

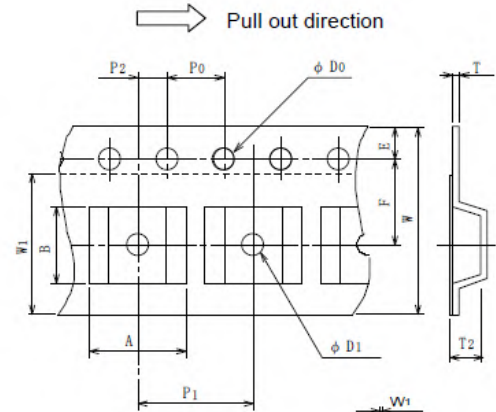
PACKING SPECIFICATION

General Description

NJRC delivers ICs in 4 methods, plastic tube container, two kinds of Taping, tray and vinyl bag packing.
 Except adhesive tape treated anti electrostatic and contain carbon are using as the ESD (Electrostatic Discharge Damage) protection.

SSOP Emboss Taping(TE1)

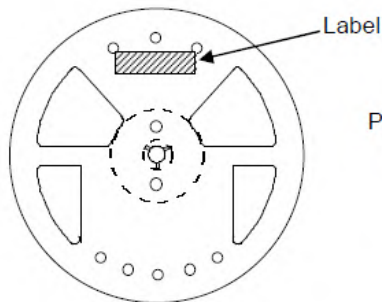
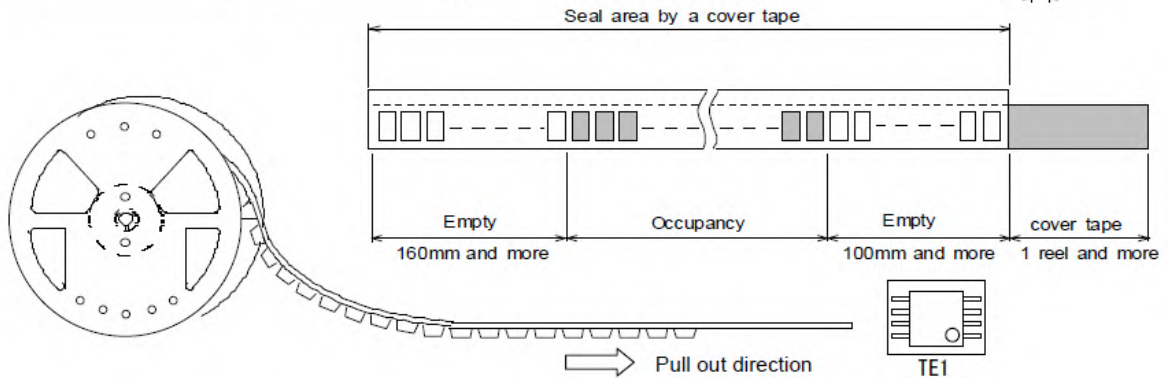
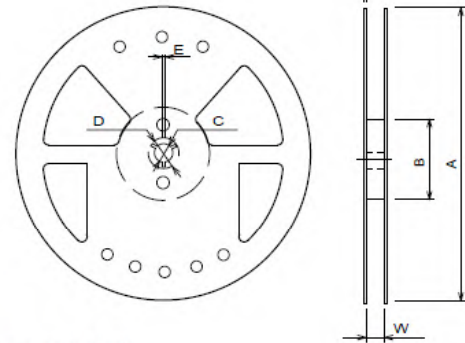
Symbol	SSOP14	Remark
A	6.95	Bottom size
B	5.4	Bottom size
D ₀	1.55±0.05	
D ₁	1.55±0.1	
E	1.75±0.1	
F	5.5±0.05	
P ₀	4.0±0.1	
P ₁	8.0±0.1	
P ₂	2.0±0.05	
T	0.3±0.05	
T ₂	1.9	
W	12.0±0.3	
W ₁	9.5	Thickness 0.1MAX



Unit : mm

Symbol	SSOP14
A	∅254±2
B	∅100±1
C	∅13±0.2
D	∅21±0.8
E	2±0.5
W	13.5±0.5
W ₁	2±0.2
Contents	2,000 pcs

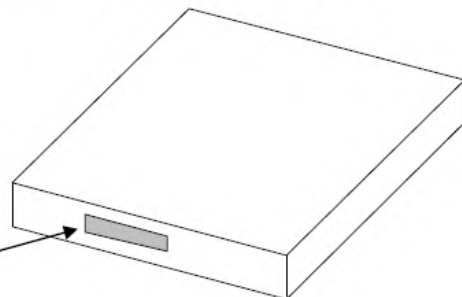
Unit : mm



Put in the outer box

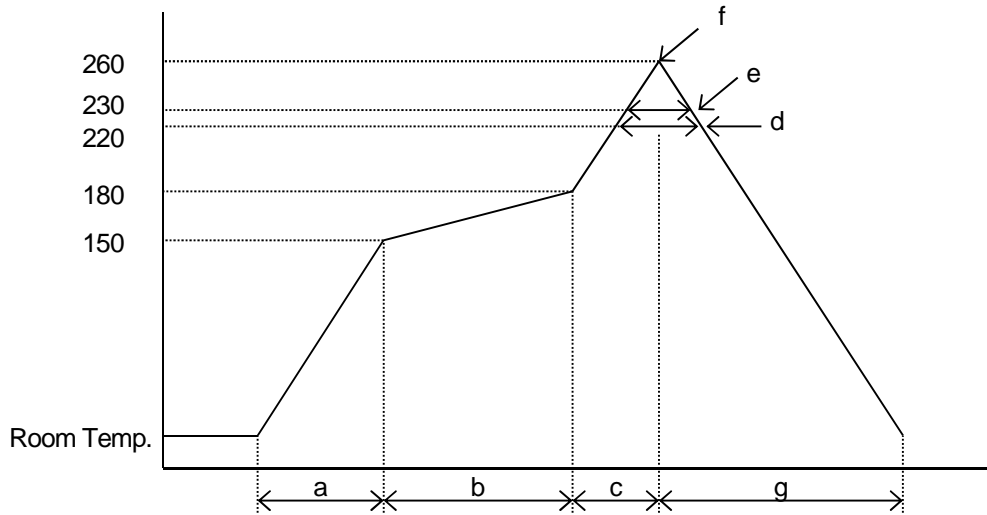


Label



RECOMMENDED MOUNTING METHOD

* Recommended reflow soldering procedure



- a: Temperature ramping rate : 1 to 4 /s
- b: Pre-heating temperature : 150 to 180
- time : 60 to 120s
- c: Temperature ramp rate : 1 to 4 /s
- d: 220 or higher time : Shorter than 60s
- e: 230 or higher time : Shorter than 40s
- f: Peak temperature : Lower than 260
- g: Temperature ramping rate : 1 to 6 /s

The temperature indicates at the surface of mold package.

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