

Description

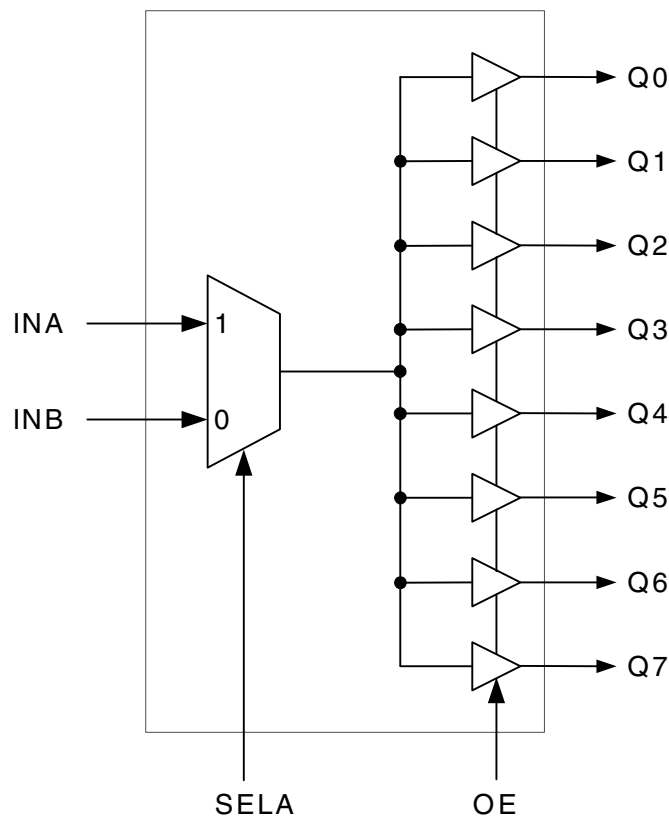
The 552-02S is a low skew, single-input to eight- output clock buffer. The device offers a dual input with pin select for switching between two clock sources. It has best in class Additive Phase Jitter of sub 50fsec

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

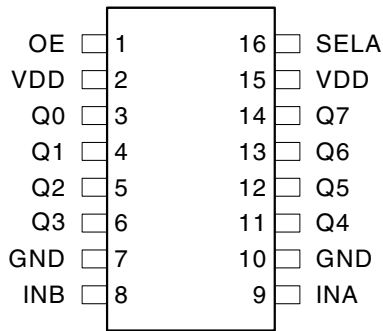
Features

- Low RMS Additive Phase Jitter: 50fs
- Low output skew: 50ps
- Operating Voltages of 1.8V to 3.3V
- Packaged in 16-pin TSSOP and 16-pin VFQFN, Pb-free
- Input clock multiplexer simplifies clock selection
- Output Enable pin tri-states outputs
- Input/Output clock frequency up to 200 MHz
- Low power CMOS technology
- 3.3V tolerant inputs
- Extended temperature (-40°C to +105°C)

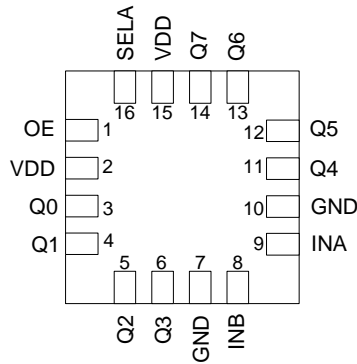
Block Diagram



Pin Assignments



16 Pin TSSOP



16-pin VFQFN

Input Source Select

| SELA | Input |
|------|-------|
| 0 | INB |
| 1 | INA |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | OE | Input | Output Enable. Tri-states outputs when low. Internal pull-up resistor. |
| 2 | VDD | Power | Connect to +1.8V, +2.5V or +3.3V. Must be the same as pin 15. |
| 3 | Q0 | Output | Clock Output 0. |
| 4 | Q1 | Output | Clock Output 1. |
| 5 | Q2 | Output | Clock Output 2. |
| 6 | Q3 | Output | Clock Output 3. |
| 7 | GND | Power | Connect to ground. |
| 8 | INB | Input | Clock Input B. 3.3V tolerant. |
| 9 | INA | Input | Clock Input A. 3.3V tolerant. |
| 10 | GND | Power | Connect to ground. |
| 11 | Q4 | Output | Clock Output 4. |
| 12 | Q5 | Output | Clock Output 5. |
| 13 | Q6 | Output | Clock Output 6. |
| 14 | Q7 | Output | Clock Output 7. |
| 15 | VDD | Power | Connect to +1.8V, +2.5V or +3.3V. Must be the same as pin 2. |
| 16 | SELA | Input | Selects either INA or INB. Internal pull-up resistor. |

External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01 μ F should be connected between VDD on pin 2 and GND on pin 7, and between VDD on pin 15 and GND on pin 10, as close to the device as possible. A 33 Ω series terminating resistor should be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skews that the 552-02S is capable of, careful attention must be paid to board layout. Essentially, all 8 outputs must have identical terminations, identical loads, and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30 Ω series termination on one output (with 33 Ω on the others) will cause at least 15ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 552-02S. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|------------------|
| Supply Voltage, VDD | 3.465V |
| All Inputs and Outputs | -0.5 V to 3.465V |
| Ambient Operating Temperature, Extended | -40 to +105°C |
| Storage Temperature | -65 to +150 °C |
| Junction Temperature | 175 °C |
| Soldering Temperature | 260 °C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|--------|-------|
| Ambient Operating Temperature, Extended | -40 | – | +105 | °C |
| Power Supply Voltage (measured in respect to GND) | +1.71 | | +3.465 | V |

DC Electrical Characteristics

VDD=1.8 V ±5%, Ambient temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------------|-----------------|--------------------------|---------|------|---------|-------|
| Operating Voltage | VDD | | 1.71 | | 1.89 | V |
| Input High Voltage, INA, INB | V _{IH} | Note 1 | 0.7xVDD | | 1.89 | V |
| Input Low Voltage, INA, INB | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Input High Voltage, OE, SELA | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE, SELA | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -10 mA | 1.3 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 10 mA | | | 0.35 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 32 | | mA |

VDD=2.5 V ±5%, Ambient temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------------|-----------------|--------------------------|---------|------|---------|-------|
| Operating Voltage | VDD | | 2.375 | | 2.625 | V |
| Input High Voltage, INA, INB | V _{IH} | Note 1 | 0.7xVDD | | 2.625 | V |
| Input Low Voltage, INA, INB | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Input High Voltage, OE, SELA | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE, SELA | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -16 mA | 1.8 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 16 mA | | | 0.5 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 43 | | mA |

VDD=3.3 V ±5%, Ambient temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------------|-----------------|--------------------------|---------|------|---------|-------|
| Operating Voltage | VDD | | 3.135 | | 3.465 | V |
| Input High Voltage, INA, INB | V _{IH} | Note 1 | 0.7xVDD | | 3.465 | V |
| Input Low Voltage, INA, INB | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Input High Voltage, OE, SELA | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE, SELA | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.2 | | | V |
| Output Low Voltage | V _{OL} | I _{OH} = 25 mA | | | 0.7 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 55 | | mA |

AC Electrical Characteristics

VDD = 1.8V ±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.36 to 1.44 V, C _L =5 pF | | 1 | 1.5 | ns |
| Output Fall Time | t _{OF} | 1.44 to 0.36 V, C _L =5 pF | | 1 | 1.5 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | Note 1 | 135MHz | 2 | 2.5 | 3 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12KHz-20MHz | | 50 | 65 | ps |
| Output to output skew | Note 2 | Rising edges at VDD/2 | | 0 | 65 | ps |
| Input A to Input B skew | Note 3 | | | 0 | 50 | ps |

VDD = 2.5V ±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.5 to 2.0 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 2.0 to 0.5 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | Note 1 | 135MHz | 2 | 2.7 | 3.5 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12KHz-20MHz | | 50 | 65 | ps |
| Output to output skew | Note 2 | Rising edges at VDD/2 | | 0 | 65 | ps |
| Input A to Input B skew | Note 3 | | | 0 | 50 | ps |

VDD = 3.3V ±5%, Ambient Temperature -40°C to +105°C, unless stated otherwise

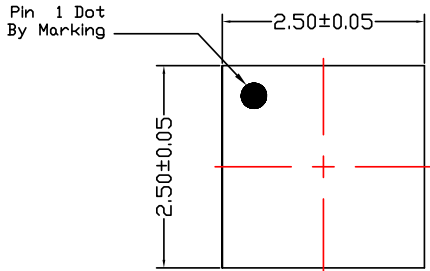
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.66 to 2.64 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 2.64 to 0.66 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | Note 1 | 135MHz | 2 | 2.5 | 3 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12KHz-20MHz | | 50 | 65 | ps |
| Output to output skew | Note 2 | Rising edges at VDD/2 | | 0 | 65 | ps |
| Input A to Input B skew | Note 3 | | | 0 | 50 | ps |

Notes:

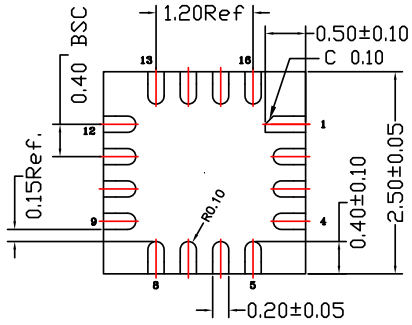
1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.
3. Propagation delay matching through the part.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Package Outline and Dimensions (16-pin VFQFN)

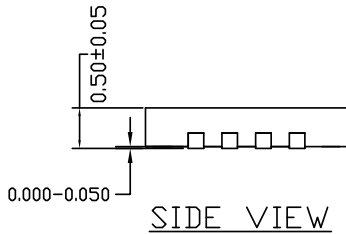
| REVISIONS | | | |
|-----------|------------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/03/14 | JH |
| 01 | ADD PIN1 CHAMFER | 12/11/14 | JH |



TOP VIEW



BOTTOM VIEW



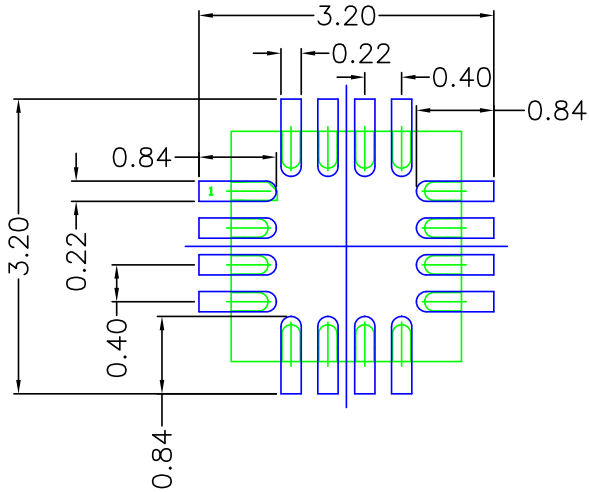
SIDE VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

| | | | | |
|-----------------------------|----------|---|--------------|-----|
| TOLERANCES UNLESS SPECIFIED | | 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com | | |
| DECIMAL | ANGULAR | | | |
| X± | ±1° | | | |
| XX± | | | | |
| XXX± | | | | |
| APPROVALS | DATE | TITLE | | |
| DRAWN <i>[Signature]</i> | 04/03/14 | CMG 16 PACKAGE OUTLINE | | |
| CHECKED | | 2.5 x 2.5 mm BODY | | |
| | | 0.40 mm PITCH VFQFN | | |
| | | SIZE | DRAWING No. | REV |
| | | C | PSC-4478 | 01 |
| DO NOT SCALE DRAWING | | | SHEET 1 OF 2 | |

| REVISIONS | | | |
|-----------|------------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/03/14 | JH |
| 01 | ADD PIN1 CHAMFER | 12/11/14 | JH |



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

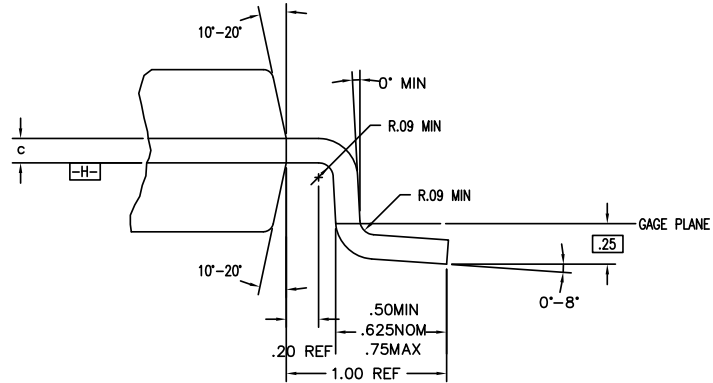
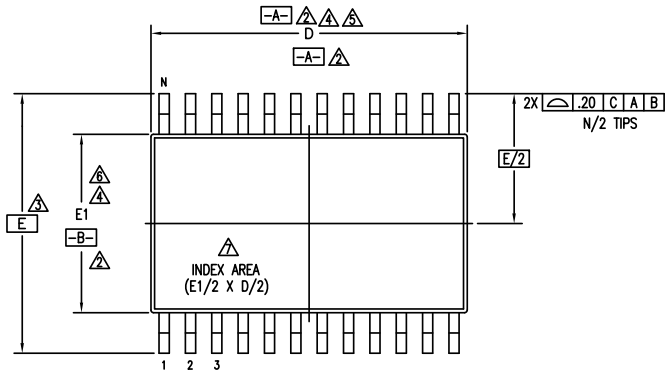
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE IS SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | |
|-----------------------------|----------|---|
| TOLERANCES UNLESS SPECIFIED | | 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com |
| DECIMAL | ANGULAR | |
| X± | ±1° | |
| XX± | | |
| XXX± | | |
| APPROVALS | DATE | TITLE |
| DRAWN <i>psr</i> | 04/03/14 | CMG 16 PACKAGE OUTLINE 2.5 x 2.5 mm BODY 0.40 mm PITCH VFQFN |
| CHECKED | | |
| | SIZE | DRAWING No. |
| | C | PSC-4478 |
| | | REV |
| | | 01 |
| DO NOT SCALE DRAWING | | SHEET 2 OF 2 |

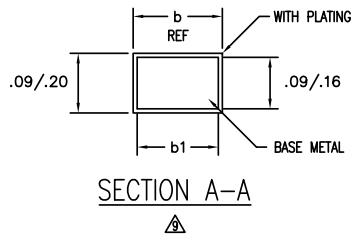
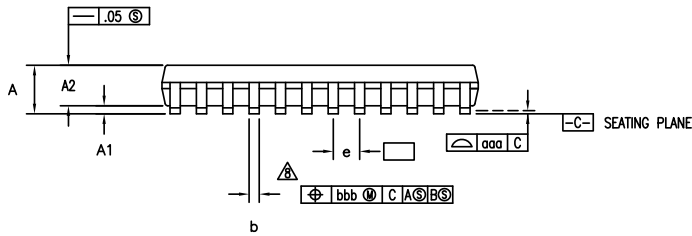
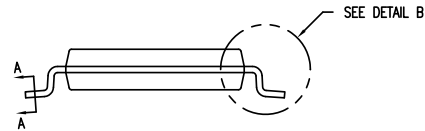
Package Outline and Dimensions (16-pin TSSOP)

| DATE CREATED | REVISIONS | | |
|--------------|-----------|----------------------------------|--------|
| | REV | DESCRIPTION | AUTHOR |
| 08/25/98 | 02 | ADD 14 & 16 LD | T. VU |
| 07/10/99 | 03 | ADD 8 LD | T. VU |
| 5/23/01 | 04 | ADDED TOPMARK TO TITLE | |
| 10/14/04 | 05 | ADD "GREEN" PGG NOMENCLATURE | TU VU |
| 3/8/13 | 06 | ADDED PACKAGE CODE | RAC |
| 9/3/14 | 07 | ADD TOLERANCE FOR A, A1, E AND b | CK LEE |
| 3/10/17 | 08 | ADD OPTION T1 | R.TANH |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE



DETAIL B



SECTION A-A

| | | |
|---|-------------------------|---|
| TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± ± XXXX± ± | | 2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 492-8874 |
| | | www.IDT.com |
| TITLE PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH | | |
| SIZE C | DRAWING No. PSC-4056 | REV 08 |
| DO NOT SCALE DRAWING | | SHEET 1 OF 3 |

Package Outline and Dimensions (16-pin TSSOP), cont.

| DATE CREATED | REVISIONS | | |
|--------------|-----------|----------------------------------|--------|
| | REV | DESCRIPTION | AUTHOR |
| 08/25/98 | 02 | ADD 14 & 16 LD | T. VU |
| 07/10/99 | 03 | ADD 8 LD | T. VU |
| 5/23/01 | 04 | ADDED TOPMARK TO TITLE | |
| 10/14/04 | 05 | ADD "GREEN" PGG NOMENCLATURE | TU VU |
| 3/8/13 | 06 | ADDED PACKAGE CODE | RAC |
| 9/3/14 | 07 | ADD TOLERANCE FOR A, A1, E AND b | CK LEE |
| 3/10/17 | 08 | ADD OPTION T1 | R.TANH |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

| SYMBOL | PG/PGG8 | | | | NOTE | PG/PGG14 | | | | NOTE | PG/PGG16 | | | | NOTE | PG/PGG20 | | | | NOTE | PG/PGG24 | | | | NOTE | PG/PGG28 | | | | NOTE |
|--------|-----------------|------|------|-----|---------|-----------------|------|-----|---------|------|-----------------|-----|---------|------|------|-----------------|---------|------|------|------|-----------------|------|------|-----|---------|-----------------|------|-----|-----|------|
| | JEDEC VARIATION | | | MAX | | JEDEC VARIATION | | | MAX | | JEDEC VARIATION | | | MAX | | JEDEC VARIATION | | | MAX | | JEDEC VARIATION | | | MAX | | JEDEC VARIATION | | | MAX | |
| | MIN | NOM | MAX | | | MIN | NOM | MAX | | | MIN | NOM | MAX | | | MIN | NOM | MAX | | | MIN | NOM | MAX | | | MIN | NOM | MAX | | |
| A | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | | |
| A1 | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | | |
| A2 | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | | |
| D | 2.90 | 3.00 | 3.10 | 4,5 | 4.90 | 5.00 | 5.10 | 4,5 | 4.90 | 5.00 | 5.10 | 4,5 | 6.40 | 6.50 | 6.60 | 4,5 | 7.70 | 7.80 | 7.90 | 4,5 | 9.60 | 9.70 | 9.80 | 4,5 | 9.60 | 9.70 | 9.80 | 4,5 | | |
| E | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | | |
| E1 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | | |
| e | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | | |
| b | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | | |
| b1 | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | | |
| aaa | - | - | .10 | | - | - | .10 | | - | - | .10 | | - | - | .10 | | - | - | .10 | | - | - | .10 | | - | - | .10 | | | |
| bbb | - | - | .10 | | - | - | .10 | | - | - | .10 | | - | - | .10 | | - | - | .10 | | - | - | .10 | | - | - | .10 | | | |
| N | 8 | | | | | 14 | | | | | 16 | | | | | 20 | | | | | 24 | | | | | 28 | | | | |

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- DATUMS \square -A- AND \square -B- TO BE DETERMINED AT DATUM PLANE \square -H-
- DIMENSION E TO BE DETERMINED AT SEATING PLANE \square -C-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE \square -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

| SYMBOL | OPTION T1 PGG14T1 | | | |
|--------|----------------------|------|------|------|
| | JEDEC VARIATION | | | NOTE |
| | MIN | NOM | MAX | |
| A | .90 | 1.10 | 1.20 | |
| A1 | .05 | .10 | .15 | |
| A2 | .80 | 1.00 | 1.05 | |
| D | 4.90 | 5.00 | 5.10 | 4,5 |
| E | 6.20 | 6.40 | 6.60 | 3 |
| E1 | 4.30 | 4.40 | 4.50 | 4,6 |
| e | .65 BSC | | | |
| b | .19 | .25 | .30 | |
| b1 | .19 | .22 | .25 | |
| c | .09 | - | .20 | |
| aaa | - | - | .10 | |
| bbb | - | - | .10 | |
| N | 14 | | | |

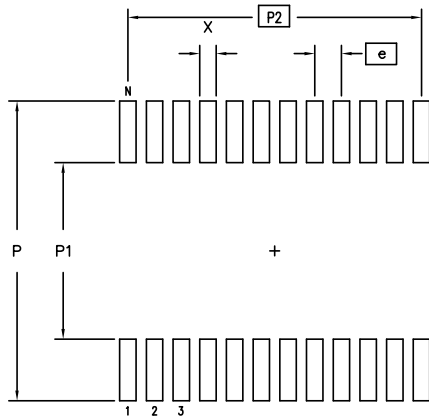
| | |
|--|--|
| TOLERANCES UNLESS SPECIFIED | 2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 www.IDT.com |
| DECIMAL ANGULAR XX± ± XXX± ± XXXX± ± | |
| TITLE PGG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH | |
| SIZE C | DRAWING No. PSC-4056 |
| REV 08 | |
| DO NOT SCALE DRAWING | |
| SHEET 2 OF 3 | |

Package Outline and Dimensions (16-pin TSSOP), cont.

| DATE CREATED | REVISIONS | | |
|--------------|-----------|----------------------------------|--------|
| | REV | DESCRIPTION | AUTHOR |
| 08/25/98 | 02 | ADD 14 & 16 LD | T. VU |
| 07/10/99 | 03 | ADD 8 LD | T. VU |
| 5/23/01 | 04 | ADDED TOPMARK TO TITLE | |
| 10/14/04 | 05 | ADD "GREEN" PGG NOMENCLATURE | TU VU |
| 3/8/13 | 06 | ADDED PACKAGE CODE | RAC |
| 9/3/14 | 07 | ADD TOLERANCE FOR A, A1, E AND b | CK LEE |
| 3/10/17 | 08 | ADD OPTION T1 | R.TANH |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

LAND PATTERN DIMENSIONS



| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
|----|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|
| P | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 |
| P1 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 |
| P2 | 1.95 BSC | | 3.90 BSC | | 4.55 BSC | | 5.85 BSC | | 7.15 BSC | | 8.45 BSC | |
| X | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 |
| e | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | |
| N | 8 | | 14 | | 16 | | 20 | | 24 | | 28 | |

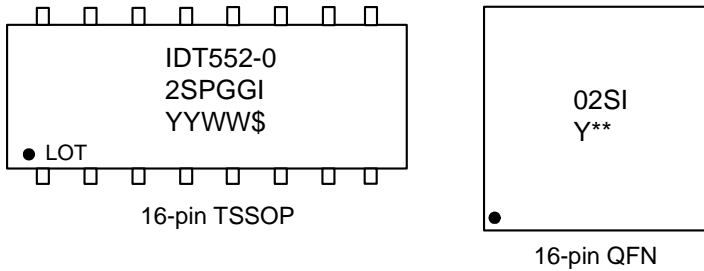
| | | | |
|--|-------------|---|--------------|
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| | | www.IDT.com | |
| TITLE PGG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH | | | |
| SIZE | DRAWING No. | REV | |
| C | PSC-4056 | 08 | |
| DO NOT SCALE DRAWING | | | SHEET 3 OF 3 |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|---------|--------------------|--------------|-----------------|
| 552-02SPGGI | TBD | Tubes | 16-pin TSSOP | -40°C to +105°C |
| 552-02SPGGI8 | | Tape and Reel | 16-pin TSSOP | -40°C to +105°C |
| 552-02SCMGI | | Tubes | 16-pin VFQFN | -40°C to +105°C |
| 552-02SCMGI8 | | Tape and Reel | 16-pin VFQFN | -40°C to +105°C |

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Marking Diagrams



Notes:

1. “**” is the lot sequence.
2. “YYWW” or “Y” is the last digit(s) of the year and week that the part was assembled.
3. “\$” denotes the mark code.
4. “LOT” denotes lot number.
5. “G” after the two-letter package code denotes RoHS compliant package.
6. “I” denotes extended temperature range device.
7. Bottom marking: country of origin (TSSOP only).

Revision History

| Rev. | Date | Originator | Description of Change |
|------|----------|------------|--|
| B | 04/18/17 | C.P. | 1. Replaced package outline drawings with latest CMG16 and PGG16 versions. 2. Updated legal disclaimer. |
| A | 07/11/16 | H.G. | Release to final. |



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