

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

General Description

The MAX5800/MAX5801/MAX5802 2-channel, low-power, 8-/10-/12-bit, voltage-output digital-to-analog converters (DACs) include output buffers and an internal reference that is selectable to be 2.048V, 2.500V, or 4.096V. The MAX5800/MAX5801/MAX5802 accept a wide supply voltage range of 2.7V to 5.5V with extremely low power (1.5mW) consumption to accommodate most low-voltage applications. A precision external reference input allows rail-to-rail operation and presents a $100 \mathrm{k}\Omega$ (typ) load to an external reference.

The MAX5800/MAX5801/MAX5802 have an I²C-compatible, 2-wire interface that operates at clock rates up to 400kHz. The DAC output is buffered and has a low supply current of less than 250µA per channel and a low offset error of ±0.5mV (typ). On power-up, the MAX5800/MAX5801/MAX5802 reset the DAC outputs to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The internal reference is initially powered down to allow use of an external reference. The MAX5800/MAX5801/MAX5802 allow simultaneous output updates using software LOAD commands.

A clear logic input ($\overline{\text{CLR}}$) allows the contents of the CODE and the DAC registers to be cleared asynchronously and sets the DAC outputs to zero. The MAX5800/MAX5801/MAX5802 are available in a small 10-pin µMAX® and an ultra-small, 10-pin TDFN package and are specified over the -40°C to +125°C temperature range.

Applications

Programmable Voltage and Current Sources
Gain and Offset Adjustment
Automatic Tuning and Optical Control
Power Amplifier Control and Biasing
Process Control and Servo Loops
Portable Instrumentation
Data Acquisition

μΜΑΧ is a registered trademark of Maxim Integrated Products, Inc.

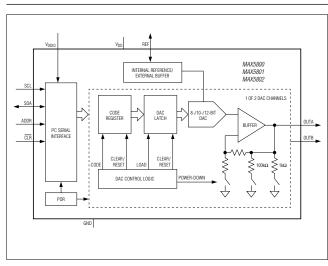
Ordering Information appears at end of data sheet.

Benefits and Features

- **♦ Two High-Accuracy DAC Channels**
 - **♦ 12-Bit Accuracy Without Adjustment**

 - **♦ Monotonic Over All Operating Conditions**
 - ♦ Independent Mode Settings for Each DAC
- ◆ Three Precision Selectable Internal References
 ♦ 2.048V, 2.500V, or 4.096V
- ♦ Internal Output Buffer
 - ♦ Rail-to-Rail Operation with External Reference
 - ♦ 4.5µs Settling Time
 - ♦ Outputs Directly Drive 2kΩ Loads
- ♦ Small 5mm x 3mm 10-Pin µMAX or Ultra-Small 3mm x 3mm 10-Pin TDFN Package
- ♦ Wide 2.7V to 5.5V Supply Range
- ♦ Separate 1.8V to 5.5V V_{DDIO} Power-Supply Input
- ♦ Fast 400kHz I²C-Compatible, 2-Wire Serial Interface
- ♦ Power-On-Reset to Zero-Scale DAC Output
- ♦ CLR For Asynchronous Control
- ♦ Three Software-Selectable Power-Down Output Impedances
 - \diamond 1k Ω , 100k Ω , or High Impedance
- ♦ Low 350µA Supply Current at 3V V_{DD}

Functional Diagram



For related parts and recommended products to use with this part, refer to: www.maximintegrated.com/MAX5800.related

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

ABSOLUTE MAXIMUM RATINGS

V _{DD,} V _{DDIO} to GND0.3V to +6V OUT_, REF to GND0.3V to the lower of	TDFN (derate at 24.4mW/°C above 70°C)1951mW Maximum Continuous Current into Any Pin±50mA
(V _{DD} + 0.3V) and +6V	Operating Temperature Range40°C to +125°C
SCL, SDA, CLR to GND0.3V to +6V	Storage Temperature Range65°C to +150°C
ADDR to GND0.3V to the lower of	Lead Temperature (soldering, 10s)+300°C
$(V_{DDIO} + 0.3V)$ and +6V	Soldering Temperature (reflow)+260°C
Continuous Power Dissipation (T _A = +70°C)	
μMAX (derate at 8.8mW/°C above 70°C)707mW	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

μMAX	TDFN
Junction-to-Ambient Thermal Resistance (θJA)113°C/W	Junction-to-Ambient Thermal Resistance (θ _{JA})41°C/W
Junction-to-Case Thermal Resistance (θ _{JC})42°C/W	Junction-to-Case Thermal Resistance (θ_{JC})9°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

 $(V_{DD}=2.7V\ to\ 5.5V,\ V_{DDIO}=1.8V\ to\ 5.5V,\ V_{GND}=0V,\ C_L=200pF,\ R_L=2k\Omega,\ T_A=-40^{\circ}C\ to\ +125^{\circ}C,\ unless\ otherwise\ noted.$ Typical values are at $T_A=+25^{\circ}C.)$ (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (Note 3)						
		MAX5800	8			
Resolution and Monotonicity	N	MAX5801	10			Bits
		MAX5802	12			
		MAX5800	-0.25	±0.05	+0.25	
Integral Nonlinearity (Note 4)	INL	MAX5801	-0.5	±0.25	+0.5	LSB
		MAX5802	-1	±0.5	+1	
		MAX5800	-0.25	±0.05	+0.25	
Differential Nonlinearity (Note 4)	DNL	MAX5801	-0.5	±0.1	+0.5	LSB
		MAX5802	-1	±0.2	+1	
Offset Error (Note 5)	OE		-5	±0.5	+5	mV
Offset Error Drift				±10		μV/°C
Gain Error (Note 5)	GE		-1.0	±0.1	+1.0	%FS
Gain Temperature Coefficient		With respect to V _{REF}		±3.0		ppm of FS/°C
Zero-Scale Error			0		10	mV
Full-Scale Error		With respect to V _{REF}	-0.5		+0.5	%FS

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD}=2.7V\ to\ 5.5V,\ V_{DDIO}=1.8V\ to\ 5.5V,\ V_{GND}=0V,\ C_L=200pF,\ R_L=2k\Omega,\ T_A=-40^{\circ}C\ to\ +125^{\circ}C,\ unless\ otherwise\ noted.$ Typical values are at $T_A=+25^{\circ}C.)$ (Note 2)

PARAMETER	SYMBOL	СО	NDITIONS	MIN	TYP	MAX	UNITS
DAC OUTPUT CHARACTERIST	cs						
		No load		0		V_{DD}	
Output Voltage Range (Note 6)		$2k\Omega$ load to GND		0		V _{DD} - 0.2	V
		$2k\Omega$ load to V_{DD}		0.2		V_{DD}	
Lord Developing		V /0	$V_{DD} = 3V \pm 10\%,$ $II_{OUT}I \le 5mA$		300		\// ^
Load Regulation		$V_{OUT} = V_{FS}/2$	$V_{DD} = 5V \pm 10\%,$ $II_{OUT}I \le 10mA$		300		μV/mA
DO O to the state of the state of		V /0	$V_{DD} = 3V \pm 10\%,$ $II_{OUT}I \le 5mA$		0.3		
DC Output Impedance		$V_{OUT} = V_{FS}/2$	$V_{DD} = 5V \pm 10\%,$ $II_{OUT}I \le 10mA$			Ω	
Maximum Capacitive Load Handling	CL				500		pF
Resistive Load Handling	RL			2			kΩ
Short-Circuit Output Current		V _{DD} = 5.5V	Sourcing (output shorted to GND)		30		mA
Short-Gircuit Gulput Guirent		VDD = 3.5V	Sinking (output shorted to V _{DD})		50		IIIA
DC Power-Supply Rejection		$V_{DD} = 3V \pm 10\%$ or	5V ±10%		100		μV/V
DYNAMIC PERFORMANCE		1		1			
Voltage-Output Slew Rate	SR	Positive and negat	ive		1.0		V/µs
		1/4 scale to 3/4 scale	e, to ≤ 1 LSB, MAX5800		2.2		
Voltage-Output Settling Time		1/4 scale to 3/4 scale	e, to ≤ 1 LSB, MAX5801		2.6		μs
		1/4 scale to 3/4 scale	e, to ≤ 1 LSB, MAX5802		4.5		
DAC Glitch Impulse		Major code transiti	on		7		nV*s
Channel-to-Channel		External reference			3.5		nV*s
Feedthrough (Note 7)		Internal reference			3.3		117 5
gital Feedthrough		Code = 0, all digita	al inputs from OV to		0.2		nV*s
Dowar I In Timo		Startup calibration	time (Note 8)		200		μs
Power-Up Time		From power-down			50		μs

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD}=2.7V\ to\ 5.5V,\ V_{DDIO}=1.8V\ to\ 5.5V,\ V_{GND}=0V,\ C_L=200pF,\ R_L=2k\Omega,\ T_A=-40^{\circ}C\ to\ +125^{\circ}C,\ unless otherwise noted.$ Typical values are at $T_A=+25^{\circ}C.)$ (Note 2)

PARAMETER	SYMBOL	CON	DITIONS	MIN	TYP	MAX	UNITS
		E la colo (conse	f = 1kHz		90		
		External reference	f = 10kHz		82		
		2.048V internal	f = 1kHz		112		
Output Voltage-Noise Density		reference	f = 10kHz		102		
(DAC Output at Midscale)		2.5V internal	f = 1kHz		125		nV/√Hz
		reference	f = 10kHz		110		
		4.096V internal	f = 1kHz		160		
		reference	f = 10kHz		145		
			f = 0.1Hz to 10Hz		12		
		External reference	f = 0.1Hz to $10kHz$		76		
			f = 0.1Hz to 300kHz		385		
		0.0401/1	f = 0.1Hz to 10Hz		14		
		2.048V internal reference	f = 0.1Hz to $10kHz$		91		
Integrated Output Noise		reference	f = 0.1Hz to 300kHz		450		
(DAC Output at Midscale)		0.5144	f = 0.1Hz to 10Hz		15		μV _{P-P}
		2.5V internal reference	f = 0.1Hz to $10kHz$		99		
		reference	f = 0.1Hz to 300kHz		470		
		4 00 0144	f = 0.1Hz to 10Hz		16		
		4.096V internal reference	f = 0.1Hz to $10kHz$		124		
		reference	f = 0.1Hz to 300kHz		490		
		F	f = 1kHz		114		
		External reference	f = 10kHz		99		
		2.048V internal	f = 1kHz		175		
Output Voltage-Noise Density		reference	f = 10kHz		153		
(DAC Output at Full Scale)		2.5V internal	f = 1kHz		200		nV/√Hz
		reference	f = 10kHz		174		
		4.096V internal	f = 1kHz		295		
		reference	f = 10kHz		255		
			f = 0.1Hz to 10Hz		13		
		External reference	f = 0.1Hz to $10kHz$		94		
			f = 0.1Hz to 300kHz		540		
			f = 0.1Hz to 10Hz		19		
		2.048V internal	f = 0.1Hz to $10kHz$		143		
Integrated Output Noise		reference	f = 0.1Hz to 300kHz		685		
(DAC Output at Full Scale)		0.5)(;;;	f = 0.1Hz to 10Hz		21		μV _{P-P}
		2.5V internal reference	f = 0.1Hz to $10kHz$		159		_
		TEIGIGING	f = 0.1Hz to 300kHz		705		_
		4.0001/1	f = 0.1Hz to 10Hz		26		
		4.096V internal reference	f = 0.1Hz to $10kHz$		213		_
		TEIGIGING	f = 0.1Hz to 300kHz		750		1

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD}=2.7V\ to\ 5.5V,\ V_{DDIO}=1.8V\ to\ 5.5V,\ V_{GND}=0V,\ C_L=200pF,\ R_L=2k\Omega,\ T_A=-40^{\circ}C\ to\ +125^{\circ}C,\ unless\ otherwise\ noted.$ Typical values are at $T_A=+25^{\circ}C.)$ (Note 2)

PARAMETER	SYMBOL	CON	NDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT	,						
Reference Input Range	V _{REF}			1.24		V _{DD}	V
Reference Input Current	I _{REF}	$V_{REF} = V_{DD} = 5.5V$	'		55	74	μΑ
Reference Input Impedance	R _{REF}			75	100		kΩ
REFERENCE OUPUT							
		$V_{REF} = 2.048V, T_{A}$	= +25°C	2.043	2.048	2.053	
Reference Output Voltage	V _{REF}	$V_{REF} = 2.5V, T_{A} = -$	2.494	2.5	2.506	V	
		$V_{REF} = 4.096V, T_{A}$	= +25°C	4.086	4.096	4.106	
		V 2.049V	f = 1kHz		129		
		V _{REF} = 2.048V	f = 10kHz		122		
Reference Output Noise Density		V 0.500V	f = 1kHz		158		nV/√Hz
Therefore Output Noise Density		V _{REF} = 2.500V	f = 10kHz		151		110/ 1112
		V _{REF} = 4.096V	f = 1kHz		254		
		VREF = 4.090V	f = 10kHz		237		
			f = 0.1Hz to $10Hz$		12		
		$V_{REF} = 2.048V$	f = 0.1Hz to $10kHz$		110		
Interveted Deference Output			f = 0.1Hz to 300kHz		390		
			f = 0.1Hz to 10Hz		15		
Integrated Reference Output Noise		$V_{REF} = 2.500V$	f = 0.1Hz to $10kHz$		129		μV _{P-P}
TNOISE			f = 0.1Hz to 300kHz		430		
			f = 0.1Hz to 10Hz		20		
		$V_{REF} = 4.096V$	f = 0.1Hz to $10kHz$		205		
			f = 0.1Hz to 300kHz		525		
Reference Temperature		MAX5802A			±3.7	±10	
Coefficient (Note 9)		MAX5800/MAX580	1/MAX5802B		±10	±25	ppm/°C
Reference Drive Capacity		External load			25		kΩ
Reference Capacitive Load					200		pF
Reference Load Regulation		$I_{\text{SOURCE}} = 0 \text{ to } 500$)μΑ		2		mV/mA
Reference Line Regulation					0.05		mV/V
POWER REQUIREMENTS							
	.,,	V _{REF} = 4.096V	4.5		5.5		
Supply Voltage	V _{DD}	All other options		2.7		5.5	V
I/O Supply Voltage	V _{DDIO}			1.8		5.5	V
Interface Supply Current (Note 10)	I _{DDIO}					1	μΑ

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD}=2.7V\ to\ 5.5V,\ V_{DDIO}=1.8V\ to\ 5.5V,\ V_{GND}=0V,\ C_L=200pF,\ R_L=2k\Omega,\ T_A=-40^{\circ}C\ to\ +125^{\circ}C,\ unless\ otherwise\ noted.$ Typical values are at $T_A=+25^{\circ}C.)$ (Note 2)

PARAMETER	SYMBOL	CON	TYP	MAX	UNITS		
			V _{REF} = 2.048V		0.55	0.75	
		Internal reference	V _{REF} = 2.5V		0.60	0.80	
Supply Current (Note 10)	I _{DD}		V _{REF} = 4.096V		0.65	0.90	mA
		E 1	V _{REF} = 3V		0.40	0.60	
		External reference	V _{REF} = 5V		0.55	0.75	
		Both DACs off, inter	nal reference ON		140		
Power-Down Mode Supply Current	I _{PD}	Both DACs off, inter $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			0.5	1	μΑ
Current		Both DACs off, inter $T_A = +125$ °C	nal reference OFF,		1.2	2.5	
DIGITAL INPUT CHARACTERIS	TICS (SCL, S	DA, ADDR, CLR)		·			
Input High Voltage	V	2.2V < V _{DDIO} < 5.5V	V	0.7 x V _{DDIO}			V
Input High Voltage	V _{IH}	1.8V < V _{DDIO} < 2.2V	V	0.8 x V _{DDIO}			V
Input Low Voltage	V _{IL}	2.2V < V _{DDIO} < 5.5\	/			0.3 x V _{DDIO}	٧
Imput Low Voltage		1.8V < V _{DDIO} < 2.2\	V			0.2 x V _{DDIO}	V
Hysteresis Voltage	V _H				0.15		V
Input Leakage Current	I _{IN}	$V_{IN} = 0V \text{ or } V_{DDIO}$ (I	Note 10)		±0.1	±1	μΑ
Input Capacitance (Note 10)	C _{IN}					10	рF
ADDR Pullup/Pulldown Strength	R _{PU} , R _{PD}	(Note 11)		30	50	90	kΩ
DIGITAL OUTPUT (SDA)							
Output Low Voltage	V _{OL}	I _{SINK} = 3mA				0.2	V
I ² C TIMING CHARACTERISTICS	(SCL, SDA,	CLR)					
SCL Clock Frequency	f _{SCL}					400	kHz
Bus Free Time Between a STOP and a START Condition	t _{BUF}			1.3			μs
Hold Time Repeated for a START Condition	t _{HD;STA}			0.6			μs
SCL Pulse Width Low	t _{LOW}			1.3			μs
SCL Pulse Width High	tHIGH			0.6			μs
Setup Time for Repeated START Condition	t _{SU;STA}			0.6			μs
Data Hold Time	t _{HD;DAT}			0		900	ns
Data Setup Time	t _{SU;DAT}			100			ns

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD}=2.7V\ to\ 5.5V,\ V_{DDIO}=1.8V\ to\ 5.5V,\ V_{GND}=0V,\ C_L=200pF,\ R_L=2k\Omega,\ T_A=-40^{\circ}C\ to\ +125^{\circ}C,\ unless\ otherwise\ noted.$ Typical values are at $T_A=+25^{\circ}C.)$ (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA and SCL Receiving Rise Time	t _r		20 + C _B /10		300	ns
SDA and SCL Receiving Fall Time	t _f		20 + C _B /10		300	ns
SDA Transmitting Fall Time	t _f		20 + C _B /10		250	ns
Setup Time for STOP Condition	tsu;sto		0.6			μs
Bus Capacitance Allowed	C _B	V _{DD} = 2.7V to 5.5V	10		400	рF
Pulse Width of Suppressed Spike	t _{sp}			50		ns
CLR Removal Time Prior to a Recognized START	t _{CLRSTA}		100			ns
CLR Pulse Width Low	t _{CLPW}		20			ns

- **Note 2:** Electrical specifications are production tested at $T_A = +25$ °C. Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at $T_A = +25$ °C and are not guaranteed.
- Note 3: DC Performance is tested without load.
- Note 4: Linearity is tested with unloaded outputs to within 20mV of GND and V_{DD} .
- **Note 5:** Gain and offset calculated from measurements made with $V_{REF} = V_{DD}$ at codes 30 and 4065 for MAX5802, codes 8 and 1016 for MAX5801, and codes 2 and 254 for MAX5800.
- **Note 6:** Subject to zero and full-scale error limits and V_{REF} settings.
- Note 7: Measured with the DAC outputs at midscale with one channel transitioning 0 to full scale.
- **Note 8:** On power-up, the device initiates an internal 200µs (typ) calibration sequence. All commands issued during this time will be ignored.
- Note 9: Guaranteed by design.
- **Note 10:** Both channels active at V_{ES} , unloaded. Static logic inputs with $V_{IL} = V_{GND}$ and $V_{IH} = V_{DDIO}$.
- **Note 11:** An unconnected condition on the ADDR pin is sensed via a resistive pullup and pulldown operation; for proper operation, the ADDR pin should be tied to V_{DDIO}, GND, or left unconnected with minimal capacitance.

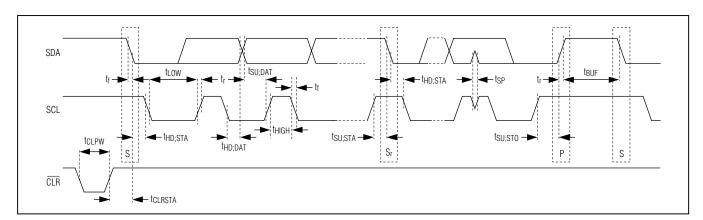
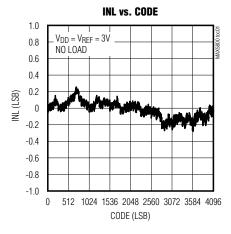


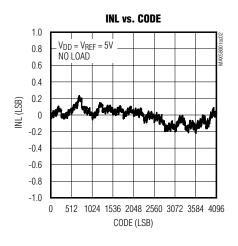
Figure 1. I²C Serial Interface Timing Diagram

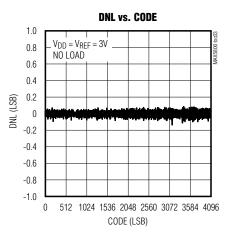
Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

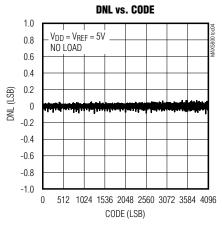
Typical Operating Characteristics

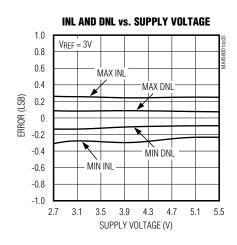
(MAX5802, 12-bit performance, $T_A = +25$ °C, unless otherwise noted.)

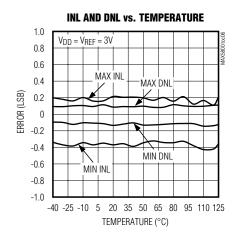








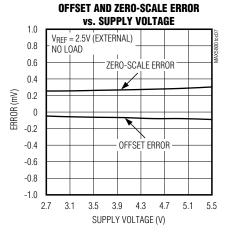




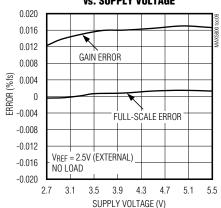
Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

Typical Operating Characteristics (continued)

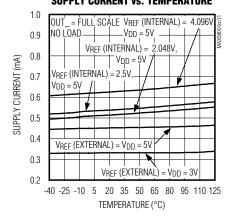
(MAX5802, 12-bit performance, $T_A = +25$ °C, unless otherwise noted.)



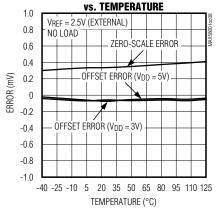
FULL-SCALE ERROR AND GAIN ERROR vs. SUPPLY VOLTAGE



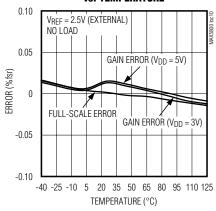
SUPPLY CURRENT vs. TEMPERATURE



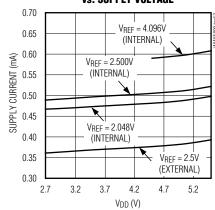
OFFSET AND ZERO-SCALE ERROR



FULL-SCALE ERROR AND GAIN ERROR vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



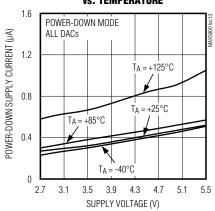
Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

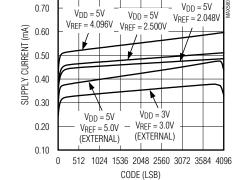
Typical Operating Characteristics (continued)

0.80

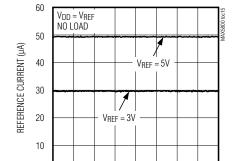
(MAX5802, 12-bit performance, TA = +25°C, unless otherwise noted.)





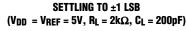


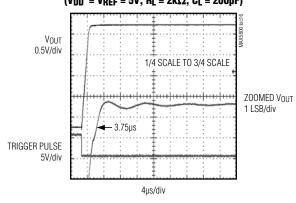
SUPPLY CURRENT vs. CODE

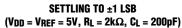


0

IREF (EXTERNAL) vs. CODE

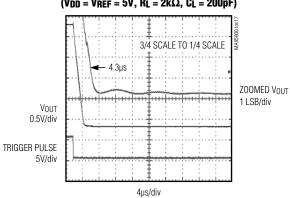




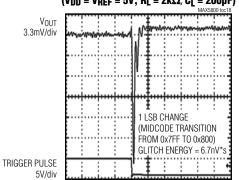


CODE (LSB)

512 1024 1536 2048 2560 3072 3584 4096



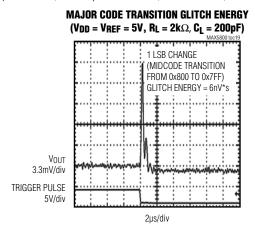
MAJOR CODE TRANSITION GLITCH ENERGY ($V_{DD} = V_{REF} = 5V$, $R_L = 2k\Omega$, $C_L = 200pF$)

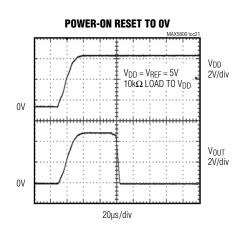


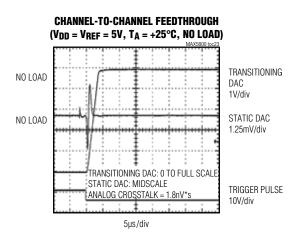
Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

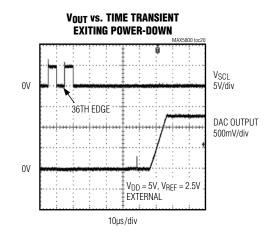
Typical Operating Characteristics (continued)

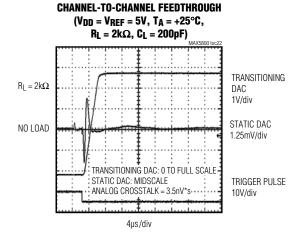
(MAX5802, 12-bit performance, $T_A = +25^{\circ}C$, unless otherwise noted.)

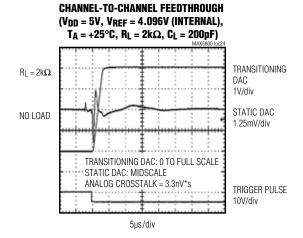








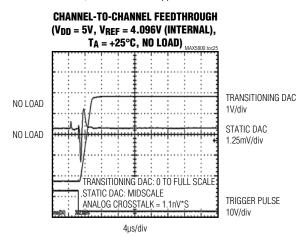


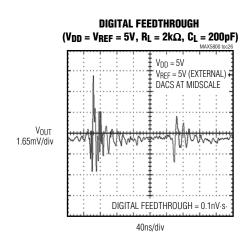


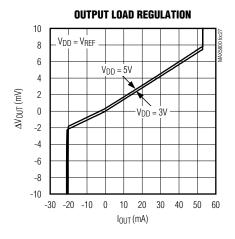
Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

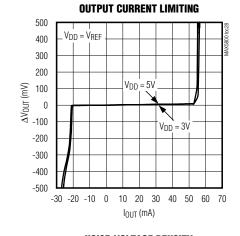
Typical Operating Characteristics (continued)

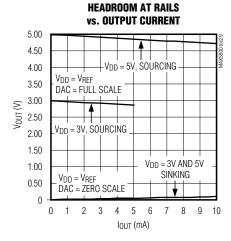
(MAX5802, 12-bit performance, $T_A = +25$ °C, unless otherwise noted.)

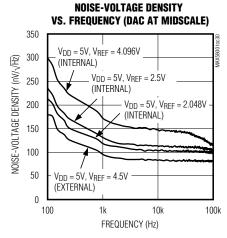










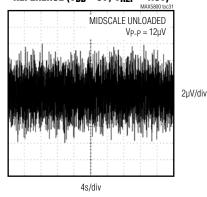


Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

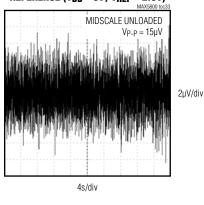
Typical Operating Characteristics (continued)

(MAX5802, 12-bit performance, $T_A = +25^{\circ}C$, unless otherwise noted.)

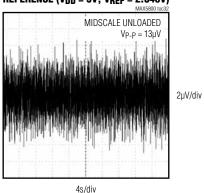
0.1Hz TO 10Hz OUTPUT NOISE, EXTERNAL REFERENCE (VDD = 5V, VREF = 4.5V)



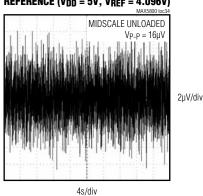
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD} = 5V, \ V_{REF} = 2.5V$)

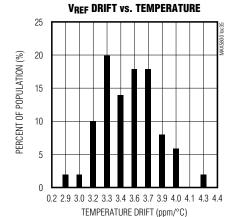


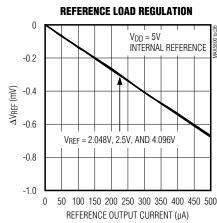
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD} = 5V$, $V_{REF} = 2.048V$)

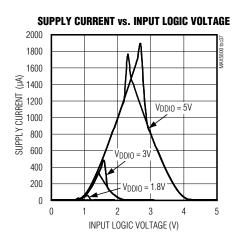


0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD}=5V,\,V_{REF}=4.096V$)



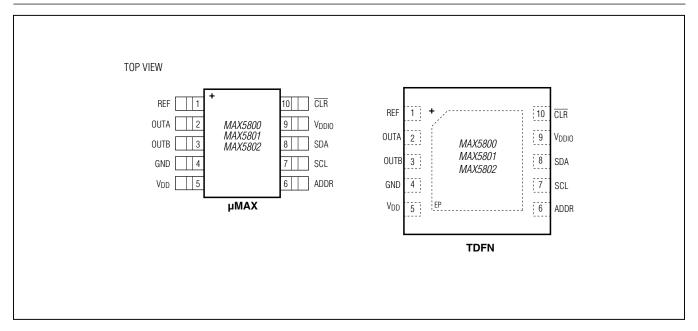






Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	REF	Reference Voltage Input/Output
2	OUTA	Buffered Channel A DAC Output
3	OUTB	Buffered Channel B DAC Output
4	GND	Ground
5	V _{DD}	Supply Voltage Input. Bypass V _{DD} with at least a 0.1µF capacitor to GND.
6	ADDR	I ² C Interface Address Selection Bit
7	SCL	I ² C Interface Clock Input
8	SDA	I ² C Bidirectional Serial Data
9	V _{DDIO}	Digital Interface Power-Supply Input
10	CLR	Active-Low Clear Input
_	EP	Exposed Pad (TDFN Only). Connect to ground.

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

Detailed Description

The MAX5800/MAX5801/MAX5802 are 2-channel, low-power, 8-/10-/12-bit buffered voltage-output DACs. The 2.7V to 5.5V wide supply voltage range and low-power consumption accommodates most low-power and low-voltage applications. The devices present a $100k\Omega$ load to the external reference. The internal output buffers allow rail-to-rail operation. An internal voltage reference is available with software selectable options of 2.048V, 2.5V, or 4.096V. The devices feature a fast 400kHz l²C-compatible interface. The MAX5800/MAX5801/MAX5802 include a serial-in/parallel-out shift register, internal CODE and DAC registers, a power-on-reset (POR) circuit to initialize the DAC outputs to code zero, and control logic. \overline{CLR} is available to asynchronously clear the device independent of the serial interface.

DAC Outputs (OUT_)

The MAX5800/MAX5801/MAX5802 include internal buffers on both DAC outputs. The internal output buffers provide improved load regulation for the DAC outputs. The output buffers slew at 1V/µs (typ) and drive up to $2k\Omega$ in parallel with 500pF. The analog supply voltage (VDD) determines the maximum output voltage range of the devices as VDD powers the output buffer. Under no-load conditions, the output buffers drive from GND to VDD, subject to offset and gain errors. With a $2k\Omega$ load to GND, the output buffers drive from GND to within 200mV of VDD. With a $2k\Omega$ load to VDD, the output buffers drive from VDD to within 200mV of GND.

The DAC ideal output voltage is defined by:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N}$$

where D = code loaded into the DAC register, V_{REF} = reference voltage, N = resolution.

Internal Register Structure

The user interface is separated from the DAC logic to minimize digital feedthrough. Within the serial interface is an input shift register, the contents of which can be routed to control registers, individual, or multiple DACs as determined by the user command.

Within each DAC channel there is a CODE register followed by a DAC latch register (see the *Detailed Functional Diagram*). The contents of the CODE register

hold pending DAC output settings which can later be loaded into the DAC registers. The CODE register can be updated using both CODE and CODE_LOAD user commands. The contents of the DAC register hold the current DAC output settings. The DAC register can be updated directly from the serial interface using the CODE_LOAD commands or can upload the current contents of the CODE register using LOAD commands.

The contents of both CODE and DAC registers are maintained during power-down states, so that when the DACs are powered on, they return to their previously stored output settings. Any CODE or LOAD commands issued during power-down states continue to update the register contents. SW_CLEAR and SW_RESET commands reset the contents of all CODE and DAC registers to their zero-scale defaults.

Internal Reference

The MAX5800/MAX5801/MAX5802 include an internal precision voltage reference that is software selectable to be 2.048V, 2.500V, or 4.096V. When an internal reference is selected, that voltage is available on the REF pin for other external circuitry (see the Typical Operating Circuits) and can drive a 25k Ω load.

External Reference

The external reference input has a typical input impedance of $100k\Omega$ and accepts an input voltage from +1.24V to V_{DD} . Connect an external voltage supply between REF and GND to apply an external reference. The MAX5800/MAX5801/MAX5802 power up and reset to external reference mode. Visit www.maximintegrated.com/products/references for a list of available external voltage-reference devices.

Clear Input (CLR)

The MAX5800/MAX5801/MAX5802 feature an asynchronous active-low $\overline{\text{CLR}}$ logic input that simultaneously sets both DAC outputs to zero. Driving $\overline{\text{CLR}}$ low clears the contents of both the CODE and DAC registers and also aborts the on-going I²C command. To allow a new I²C command, drive $\overline{\text{CLR}}$ high, satisfying the t_{CLRSTA} timing requirement.

Interface Power Supply (V_{DDIO})

The MAX5800/MAX5801/MAX5802 feature a separate supply pin (V_{DDIO}) for the digital interface (1.8V to 5.5V). Connect V_{DDIO} to the I/O supply of the host processor.

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

I²C Serial Interface

The MAX5800/MAX5801/MAX5802 feature an I2C-/ SMBus[™]-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL enable communication between the MAX5800/ MAX5801/MAX5802 and the master at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX5800/MAX5801/MAX5802 by transmitting the proper slave address followed by the command byte and then the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX5800/ MAX5801/MAX5802 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX5800/MAX5801/MAX5802 must transmit the proper slave address followed by a series of nine SCL pulses for each byte of data requested. The MAX5800/ MAX5801/MAX5802 transmit data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or Repeated START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically $4.7k\Omega$ is required on SDA. SCL operates only as an input. A pullup resistor, typically $4.7k\Omega$, is required on SCL if there are multiple masters on the bus. or if the single master has an open-drain SCL output.

Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX5800/MAX5801/MAX5802 from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals. The MAX5800/MAX5801/MAX5802 can accommodate bus voltages higher than VDDIO up to a limit of 5.5V; bus voltages lower than VDDIO are not recommended and may result in significantly increased interface currents. The MAX5800/MAX5801/MAX5802 digital inputs are double buffered. Depending on the command issued through the serial interface, the CODE register(s) can be loaded without affecting the DAC register(s) using the write command. To update the DAC registers, use the software LOAD command.

I²C START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with

SMBus is a trademark of Intel Corp.

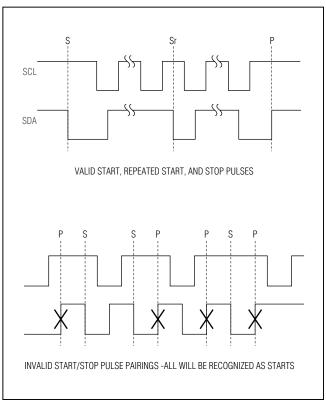


Figure 2. I²C START, Repeated START, and STOP Conditions

SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the MAX5800/MAX5801/MAX5802. The master terminates transmission and frees the bus, by issuing a STOP condition. The bus remains active if a Repeated START condition is generated instead of a STOP condition.

I²C Early STOP and Repeated START Conditions

The MAX5800/MAX5801/MAX5802 recognize a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. Transmissions ending in an early STOP condition will not impact the internal device settings. If the STOP occurs during a readback byte, the transmission is terminated and a later read mode request will begin transfer of the requested register data from the beginning (this applies to combined format I²C read mode transfers only, interface verification mode transfers will be corrupted). See Figure 2.

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

I²C Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the R/W bit. See Figure 4. The five most significant bits are 00011 with the 2 LSBs determined by ADDR as shown in Table 1. Setting the R/W bit to 1 configures the MAX5800/MAX5801/MAX5802 for read mode. Setting the R/W bit to 0 configures the MAX5800/MAX5801/MAX5802 for write mode. The slave address is the first byte of information sent to the MAX5800/MAX5801/MAX5802 after the START condition.

The MAX5800/MAX5801/MAX5802 have the ability to detect an unconnected state on the ADDR input for additional address flexibility; if leaving the ADDR input unconnected, be certain to minimize all loading on the pin (i.e. provide a landing for the pin, but do not allow any board traces).

I²C Broadcast Address

A broadcast address is provided for the purpose of updating or configuring all MAX5800/MAX5801/MAX5802 devices on a given I²C bus. All MAX5800/MAX5801/MAX5802 devices acknowledge and respond to the broadcast device address 00010000. The devices will respond to the broadcast address, regardless of the state of the address pins. The broadcast mode is intended for use in write mode only (as indicated by $R/\overline{W}=0$ in the address given).

I²C Acknowledge

In write mode, the acknowledge bit (ACK) is a clocked 9th bit that the MAX5800/MAX5801/MAX5802 use to hand-

shake receipt of each byte of data as shown in Figure 3. The MAX5800/MAX5801/MAX5802 pull down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication.

Table 1. I²C Slave Address LSBs

A[6:2] = 00011											
ADDR	A 1	A0									
V _{DDIO}	0	0									
N.C.	1	0									
GND	1	1									

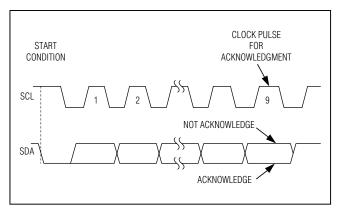


Figure 3. I²C Acknowledge

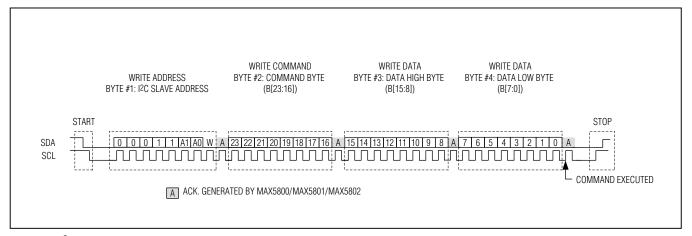


Figure 4. I²C Single Register Write Sequence

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

In read mode, the master pulls down SDA during the 9th clock cycle to acknowledge receipt of data from the MAX5800/MAX5801/MAX5802. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX5800/MAX5801/MAX5802, followed by a STOP condition.

I²C Command Byte and Data Bytes

A command byte follows the slave address. A command byte is typically followed by two data bytes unless it is the last byte in the transmission. If data bytes follow the command byte, the command byte indicates the address of the register that is to receive the following two data bytes. The data bytes are stored in a temporary register and then transferred to the appropriate register during the ACK periods between bytes. This avoids any glitching or digital feedthrough to the DACs while the interface is active.

I²C Write Operations

A master device communicates with the MAX5800/MAX5801/MAX5802 by transmitting the proper slave address followed by command and data words. Each transmit sequence is framed by a START or Repeated START condition and a STOP condition as described above. Each word is 8 bits long and is always followed by an acknowledge clock (ACK) pulse as shown in the Figure 4 and Figure 5. The first byte contains the address of the MAX5800/MAX5801/MAX5802 with R/W = 0 to indicate a write. The second byte contains the register (or com-

mand) to be written and the third and fourth bytes contain the data to be written. By repeating the register address plus data pairs (Byte #2 through Byte #4 in Figure 4 and Figure 5), the user can perform multiple register writes using a single I²C command sequence. There is no limit as to how many registers the user can write with a single command. The MAX5800/MAX5801/MAX5802 support this capability for all user-accessible write mode commands.

Combined Format I²C Readback Operations

Each readback sequence is framed by a START or Repeated START condition and a STOP condition. Each word is 8 bits long and is followed by an acknowledge clock pulse as shown in Figure 6. The first byte contains the address of the MAX5800/MAX5801/MAX5802 with $R/\overline{W} = 0$ to indicate a write. The second byte contains the register that is to be read back. There is a Repeated START condition, followed by the device address with $R/\overline{W} = 1$ to indicate a read and an acknowledge clock. The master has control of the SCL line but the MAX5800/ MAX5801/MAX5802 take over the SDA line. The final two bytes in the frame contain the register data readback followed by a STOP condition. If additional bytes beyond those required to readback the requested data are provided, the MAX5800/MAX5801/MAX5802 will continue to readback ones.

Readback of individual CODE registers is supported for the CODE command (B[23:20] = 0000). For this command, which supports a DAC address, the requested

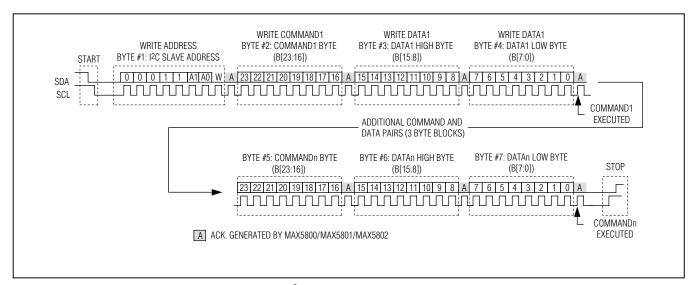


Figure 5. Multiple Register Write Sequence (Standard I²C Protocol)

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

channel CODE register content will be returned; if both DACs are selected, CODEA content will be returned.

Readback of individual DAC registers is supported for all LOAD commands (B[23:20] = 0001, 0010, or 0011). For these commands, which support a DAC address, the requested DAC register content will be returned. If both DACs are selected. DACA content will be returned.

Modified readback of the POWER register is supported for the POWER command (B[23:20] = 0100). The power status of each DAC is reported in locations B[1:0], with a 1 indicating the DAC is powered down and a 0 indicating the DAC is operational (see Table 2).

Readback of all other registers is not directly supported. All requests to read unsupported registers reads back the device's reference status and the device ID and revision information in the format as shown in Table 2.

Interface Verification I²C Readback Operations

While the MAX5800/MAX5801/MAX5802 support standard I²C readback of selected registers, it is also capable of functioning in an interface verification mode. This mode is accessed any time a readback operation follows an executed write mode command. In this mode, the last executed three-byte command is read back in its entirety. This behavior allows verification of the interface.

Sample command sequences are shown in Figure 7. The first command transfer is given in write mode with $R/\overline{W}=0$ and must be run to completion to qualify for interface verification readback. There is now a STOP/START pair or Repeated START condition required, followed by the readback transfer with $R/\overline{W}=1$ to indicate a read and an acknowledge clock from the MAX5800/MAX5801/MAX5802. The master still has control of the

Table 2. Standard I²C User Readback Data

	CON	IMAN	ID BY	TE (F	REQU	EST)		READBACK DATA HIGH BYTE									REA	DBAC	CK DA	ATA L	OW E	BYTE	
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	В9	B8	В7	В6	B5	B4	В3	B2	B1	В0
0	0	0	0	D	AC se	electic	n			C	ODEr	า[11:4	!]			(CODE	n[3:0]]	0	0	0	0
0	0	0	1	DAC selection							DACn	[11:4]					DACr	า[3:0]		0	0	0	0
0	0	1	0	D	AC se	electio	n			- 1	DACn	[11:4]					DACr	า[3:0]		0	0	0	0
0	0	1	1	DAC selection						ı	DACn	[11:4]					DACr	า[3:0]		0	0	0	0
0	1	0	0	0	0	Х	Χ	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PWB	PWA
1	0	0	0	0	0	0	0			С	ODEA	\[11:4	1]			(CODE	A[3:0]	0	0	0	0
1	0	0	0	0	0	0	1			[DACA	[11:4]]				DACA	4[3:0]		0	0	0	0
1	0	1	0	0	0	1	0			[DACA	[11:4]]				DACA	4[3:0]		0	0	0	0
1	0	1	1	0	0 0 1 1 DACA[11:4] DACA[3:0]						DACA[11:4]								0	0	0	0	
	Any other command								1001 1000								000		RE'	V_ID[2 (011)	1	REF N RF[

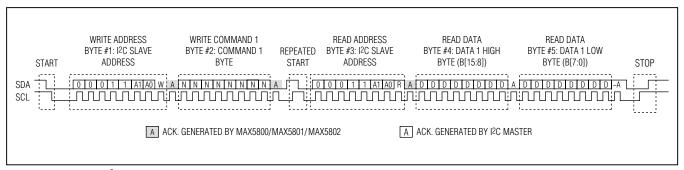


Figure 6. Standard I²C Register Read Sequence

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

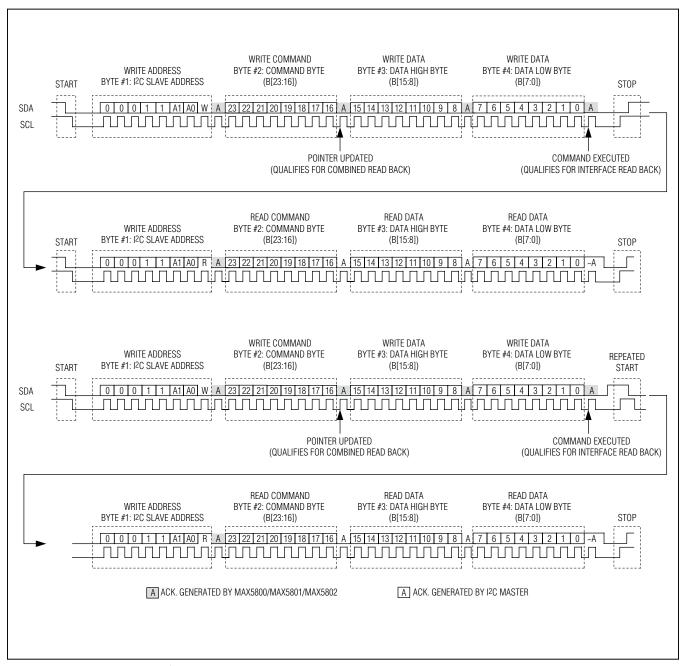


Figure 7. Interface Verification I²C Register Read Sequences

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

SCL line but the MAX5800/MAX5801/MAX5802 take over the SDA line. The final three bytes in the frame contain the command and register data written in the first transfer presented for readback, followed by a STOP condition. If additional bytes beyond those required to read back the requested data are provided, the MAX5800/MAX5801/MAX5802 will continue to read back ones.

It is not necessary for the write and read mode transfers to occur immediately in sequence. I²C transfers involving other devices do not impact the MAX5800/MAX5801/MAX5802 readback mode. Toggling between readback modes is based on the length of the preceding write mode transfer. Combined format I²C readback operation is resumed if a write command greater than two bytes but less than four bytes is supplied. For commands written using multiple register write sequences, only the last command executed is read back. For each command written, the readback sequence can only be completed one time; partial and/or multiple attempts to readback executed in succession will not yield usable data.

I²C Compatibility

The MAX5800/MAX5801/MAX5802 are fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain which pulls the data line low to transmit data or ACK pulses. Figure 8 shows a typical I²C application.

I²C User-Command Register Map

This section lists the user accessible commands and registers for the MAX5800/MAX5801/MAX5802. Each serial operation word is 24-bits long. The DAC data is left justified as shown in Table 3.

 $\begin{tabular}{ll} \hline \textbf{Table 4} provides detailed information about the Command Registers. \end{tabular}$

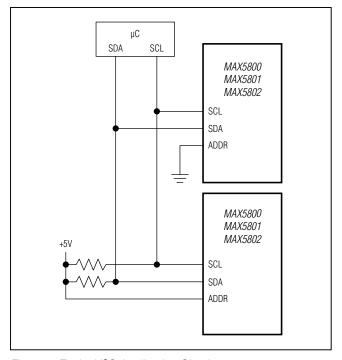


Figure 8. Typical I²C Application Circuit

Table 3. Format DAC Data Bit Positions

PART	B15	B14	B13	B12	B11	B10	В9	В8	В7	В6	В5	В4	В3	B2	B1	В0
MAX5800	D7	D6	D5	D4	D3	D2	D1	D0	Χ	Х	Χ	Χ	Χ	Χ	Χ	Х
MAX5801	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Χ	Х	Χ	Χ	Х	Х
MAX5802	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Χ	Χ	Χ	Χ

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

C SELECTION C SEL	COMMAND B23 B22 B20 B19	B23	B22	B21	B20	_	B18	B17 B16	3 B15	B14	B13	B12	B13 B12 B11 B10	B10	B3	B8	87	Be	B5	8	B	B2	19	80	DESCRIPTION	
0	DAC COMM	ĬĀ.	၂၀				1										1				1	1	1	1		
CODE REGISTER CODE REGISTE	CODEn	0	0	0	0	DAC	SELE	ECTION			ŏ	DAT	REGIS A[11:∠	TER 1			8	DE R	EGIS' \[3:0]	TER	×	×	×	×	Writes data to the selected CODE register(s)	
CODE REGISTER CODE REGISTER CODE REGISTER X X X X X X X X X	LOADn	0	0	0	-	DAC	SELE	ECTION	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	Transfers data from the selected CODE register(s) to the selected DAC register(s)	
UPATA[11:4] CODE REGISTER X	CODEn_ LOAD_ALL	0	0	-	0	DAC	SELE	ECTION			ŏ	DAT,	REGIS A[11:∠	iTER 4]			8	DATA	EGIS' 4[3:0]	TER	×	×	×	×	Simultaneously writes data to the selected CODE register(s) while updating all DAC registers	
Mode Mode Mode Mode Normal 0 0 0 Mode Normal Normal 0 0 0 Normal Normal 0 0 0 ADA0 Normal 0 0 0 X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X </td <td>CODEn_ LOADn</td> <td>0</td> <td>0</td> <td>-</td> <td>-</td> <td>DAC</td> <td>SELE</td> <td>ECTION</td> <td></td> <td></td> <td> ŏ</td> <td>ODE F DAT,</td> <td>REGIS A[11:∠</td> <td>iTER 1]</td> <td></td> <td></td> <td>8</td> <td>DAT</td> <td>EGIS' \[3:0]</td> <td>TER _</td> <td>×</td> <td>×</td> <td>×</td> <td>×</td> <td>Simultaneously writes data to the selected CODE register(s) while updating selected DAC register(s)</td> <td></td>	CODEn_ LOADn	0	0	-	-	DAC	SELE	ECTION			ŏ	ODE F DAT,	REGIS A[11:∠	iTER 1]			8	DAT	EGIS' \[3:0]	TER _	×	×	×	×	Simultaneously writes data to the selected CODE register(s) while updating selected DAC register(s)	
O O O O O O O O O O O O O O O O O O O	CONFIGUR,	ATIC	Š	OMM	IAND	တ်																				
X X X	POWER	0	-	0	0	0		Power Mode 00 = Normal 01 = PD 1kΩ 110 = PD 100kΩ Hi-Z		×	×	×	×	×	D∀CB	ADAC	×	×	×	×	×	×	×	×	Sets the power mode of the selected DACs (DACs selected with a 1 in the corresponding DACn bit are updated, DACs with a 0 in the corresponding DACn bit are not impacted)	
	SW_CLEAR		-	0	-	0	0			×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	Executes a software clear (all CODE and DAC registers cleared to their default values)	
	SW_RESET	0	-	0	-	0	0			×	×	×	×		×	×	×	×	×	×	×	×	×	×	Executes a software reset (all CODE, DAC, and control registers returned to their default values)	

Table 4. I2C Commands Summary

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

COMMAND 823 822 821 820 819	B23	B22	B21	B20	B19	B18	B17	B17 B16 B15	B15	B14	B13	B14 B13 B12 B11 B10	11	B10	89	88	B7	Be	B5	B4 B	83	R3	1 B0	DESCRIPTION
CONFIG	0	-	-	0	0	0	0	LD_EN	×	×	×	×	×	×	+					+		+		Sets the of the Only I select by the IDER is ope control ITALER
REF	0	-	-	-	0	PAG O= DAC ON		REF Mode 00 = EXT 01 = 2.5V 10 = 2.0V 11 = 4.1V	×	×	×	×	×	×	×	×	×	×	×	×	×	× ×	×	Sets the reference operating mode. REF Power (B18): 0 = Internal reference is only powered if at least one DAC is powered 1 = Internal reference is always powered
ALL DAC COMMANDS	MOX	IAND	SC																					
CODE_ALL	-	0	0	0	0	0	0	0			100	CODE REGISTER DATA[11:4]	EGIST [11:4]	Ë			000	CODE REGISTER DATA[3:0]	3.0]		×	×	×	Writes data to all CODE registers
LOAD_ALL	-	0	0	0	0	0	0	-	×	×	×	×	×	×	×	×	×	×	×	×	×	× ×	×	Updates all DAC latches with current CODE register data
CODE_ ALL_ LOAD_ALL	-	0	0	0	0	0	-	×			100	CODE REGISTER DATA[11:4]	EGIST [11:4]	ĘŖ			COD	CODE REGISTER DATA[3:0]	SISTE 3:0]		×	× ×	×	Simultaneously writes data to all CODE registers while updating all DAC registers
NO OPERATION COMMANDS	TION	00	MMA	NDS																				
;	-	0	0	-	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×		×	×	
No Operation	-	0	-	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	^ ×	×	×	×	These commands will have
	-	-	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×		× ×	×	
Reserved Commands: Any commands not specifically listed above are reserved for Maxim internal use only	omm	ands	: Any	com	manc	ds not	sbec	ifically	y listed	dabo	ve are	ese :	irved	for Ma	xim in	iterna	l use	only.						

Table 4. I2C Commands Summary (continued)

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

CODEn Command

The CODEn command (B[23:20] = 0000) updates the CODE register contents for the selected DAC(s). Changes to the CODE register content based on this command will not affect DAC outputs directly unless the DAC latch has been configured to be transparent. Issuing the CODEn command with DAC SELECTION = ALL DACs is equivalent to CODE_ALL (B[23:16] = 10000000). See Table 4 and Table 5.

LOADn Command

The LOADn command (B[23:20] = 0001) updates the DAC register content for the selected DAC(s) by uploading the current contents of the CODE register. The LOADn command can be used with DAC SELECTION = ALL DACs to issue a software load for both DACs, which is equivalent to the LOAD_ALL (B[23:16] = 10000001) command. See Table 4 and Table 5.

CODEn_LOAD_ALL Command

The CODEn_LOAD_ALL command (B[23:20] = 0010) updates the CODE register contents for the selected DAC(s) as well as the DAC register content of both DACs. Channels for which the CODE register content has not been modified since the last load to DAC register operation will not be updated to reduce digital crosstalk. Issuing this command with DAC_ADDRESS = ALL is equivalent to the CODE_ALL_LOAD_ALL command. The CODEn_LOAD_ALL command by definition will modify at least one CODE register. To avoid this, use the LOADn command with DAC SELECTION = ALL DACs or use the LOAD_ALL command. See Table 4 and Table 5.

CODEn_LOADn Command

The CODEn_LOADn command (B[23:20] = 0011) updates the CODE register contents for the selected DAC(s) as well as the DAC register content of the selected DAC(s). Channels for which the CODE register content has not been modified since the last load to DAC register operation will not be updated to reduce digital crosstalk. Issuing this command with DAC SELECTION = ALL DACs is equivalent to the CODE_ALL_LOAD_ALL command. See Table 4 and Table 5.

CODE_ALL Command

The CODE_ALL command (B[23:16] = 10000000) updates the CODE register contents for both DACs. See Table 4.

LOAD ALL Command

The LOAD_ALL command (B[23:16] = 10000001) updates the DAC register content for both DACs by uploading the current contents of the CODE registers. See Table 4.

CODE_ALL_LOAD_ALL Command

The CODE_ALL_LOAD_ALL command (B[23:16] = 1000001x) updates the CODE register contents for both DACs as well as the DAC register content of both DACs. See Table 4

Table 5. DAC Selection

B19	B18	B17	B16	DAC SELECTED
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	X	No effect
X	1	X	X	ALL DACs
1	X	X	X	ALL DACs

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

POWER Command

The MAX5800/MAX5801/MAX5802 feature a software-controlled power-mode (POWER) command (B[23:18] = 010000). The POWER command updates the power-mode settings of the selected DACs while the power settings of the rest of the DACs remain unchanged. The new power setting is determined by bits B[17:16] while the affected DAC(s) are selected by bits B[9:8]. If all DACs are powered down, the device enters a STANDBY mode.

In power-down, the DAC output is disconnected from the buffer and is grounded with either one of the two selectable internal resistors or set to high impedance. See <u>Table 7</u> for the selectable internal resistor values in power-down mode. In power-down mode, the DAC register retains its value so

that the output is restored when the device powers up. The serial interface remains active in power-down mode.

In STANDBY mode, the internal reference can be powered down or it can be set to remain powered-on for external use. Also, in STANDBY mode, devices using the external reference do not load the REF pin. See Table 6.

SW_RESET and SW_CLEAR Command

The SW_RESET (B[23:16] = 01010001) and SW_CLEAR (B[23:16] = 01010000) commands provide a means of issuing a software reset or software clear operation. Use SW_CLEAR to issue a software clear operation to return all CODE and DAC registers to the zero-scale value. Use SW_RESET to reset all CODE, DAC, and configuration registers to their default values.

Table 6. POWER Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	В9	В8	В7	В6	B 5	В4	В3	B2	B1	В0
0	1	0	0	0	0	PD1	PD0	Χ	Х	Χ	Χ	Χ	Х	В	Α	Χ	Χ	Χ	Χ	Χ	Χ	Χ	X
	POV	WER (Comm	nand		10 = 1	de:) =			Don't	Care			Sele 0 = N	ect: DAC cted DAC				Don't	Care			
De	efault '	Value	s (all	DACs	;)	0	0	Χ	Х	Χ	Χ	Χ	Х	1	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х

Table 7. Selectable DAC Output Impedance in Power-Down Mode

PD1 (B17)	PD0 (B16)	OPERATING MODE
0	0	Normal operation
0	1	Power-down with internal $1k\Omega$ pulldown resistor to GND.
1	0	Power-down with internal $100k\Omega$ pulldown resistor to GND.
1	1	Power-down with high-impedance output.

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

CONFIG Command

The CONFIG command (B[23:17] = 0110000) updates the LOAD functions of selected DACs. Issue the command with B16 = 0 to allow the DAC latches to operate normally or with B16 = 1 to disable the DAC latches, making them perpetually transparent. Mode settings of the selected DACs are updated while the mode settings of the rest of the DACs remain unchanged; DAC(s) are selected by bits B[9:8]. See Table 8.

REF Command

The REF command (B[23:19] = 01110) updates the global reference setting used for both DAC channels. Set B[17:16] = 00 to use an external reference for the DACs

or set B[17:16] to 01, 10, or 11 to select either the 2.5V, 2.048V, or 4.096V internal reference, respectively.

If RF2 (B18) is set to zero (default) in the REF command, the reference will be powered down any time both DAC channels are powered down (in STANDBY mode). If RF2 (B18 = 1) is set to one, the reference will remain powered even if both DAC channels are powered down, allowing continued operation of external circuitry. In this mode, the $1\mu A$ shutdown state is not available. See Table 9.

Table 8. CONFIG Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	В9	В8	В7	В6	B5	В4	В3	B2	В1	В0
0	1	1	0	0	0	0	LDB	Х	Χ	Χ	Χ	Χ	Χ	В	Α	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х
	С	ONFI	G Cor	mmar	nd		0 = Normal 1 = Transparent			Don't	Care			Sele 1 = 1 Sele 0 = 1	AC ect: DAC ected DAC ot ected				Don't	Care			
	Defa	ult Val	lues (a	all DA	Cs)		0	Χ	Χ	Χ	Χ	Χ	Χ	1	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ

Table 9. REF Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	В9	В8	В7	В6	В5	В4	ВЗ	B2	B1	В0
0	1	1	1	0	RF2	RF1	RF0	Χ	Χ	Χ	Χ	Χ	Х	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х
	REF	Comr	nand		0 = Off in Standby 1 = On in Standby	10 =					Don't	Care							Don't	Care			
	Defau	ılt Val	ues		0	0	0	Χ	Χ	Х	X	Χ	X	Χ	Χ	Χ	Х	Χ	Х	Χ	Χ	Χ	Χ

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

Applications Information

Power-On Reset (POR)

When power is applied to V_{DD} and V_{DDIO} , the DAC output is set to zero scale. To optimize DAC linearity, wait until the supplies have settled and the internal setup and calibration sequence completes (200 μ s, typ).

Power Supplies and Bypassing Considerations

Bypass V_{DD} and V_{DDIO} with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. Minimize lead lengths to reduce lead inductance. Connect the GND to the analog ground plane.

Layout Considerations

Digital and AC transient signals on GND can create noise at the output. Connect GND to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5800/MAX5801/MAX5802 GND. Carefully layout the traces between channels to reduce AC cross-coupling. Do not use wire-wrapped boards and sockets. Use shielding to minimize noise immunity. Do not run analog and digital signals parallel to one another, especially clock signals. Avoid routing digital lines underneath the MAX5800/MAX5801/MAX5802 package.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a straight line drawn between two codes once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL \leq 1 LSB, the DAC guarantees no missing codes and is monotonic. If the magnitude of the DNL \geq 1 LSB, the DAC output may still be monotonic.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function. The offset error is calculated from two measurements near zero code and near maximum code.

Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Zero-Scale Error

Zero-scale error is the difference between the DAC output voltage when set to code zero and ground. This includes offset and other die level nonidealities.

Full-Scale Error

Full-scale error is the difference between the DAC output voltage when set to full scale and the reference voltage. This includes offset, gain error, and other die level non-idealities.

Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

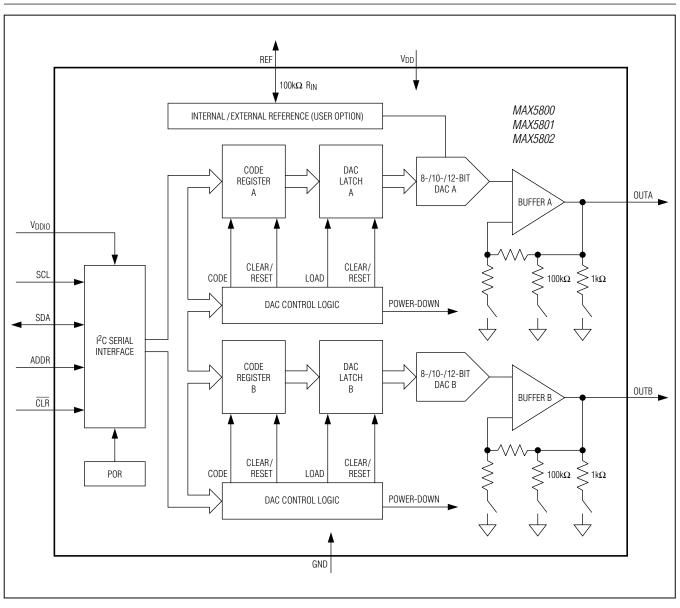
Digital-to-Analog Glitch Impulse

A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse.

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

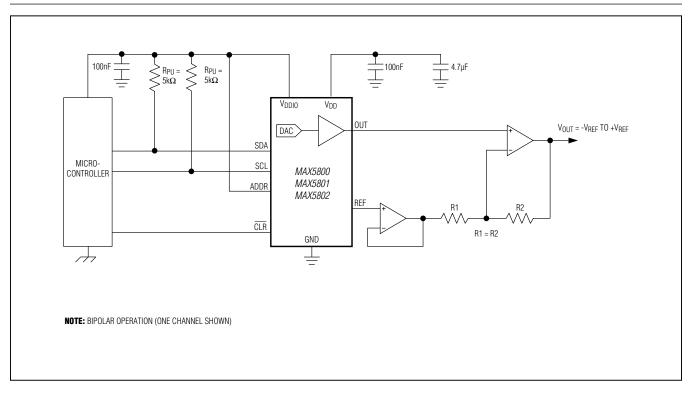
Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

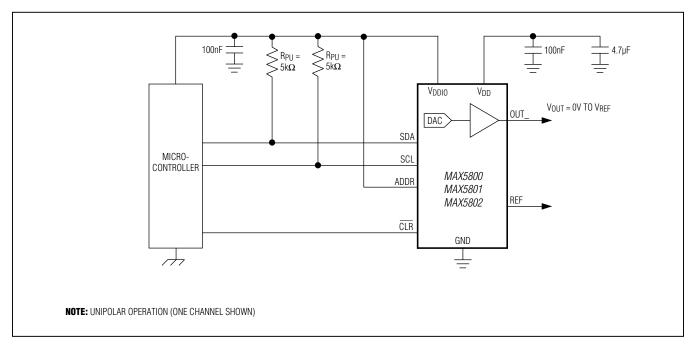
Detailed Functional Diagram



Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

Typical Operating Circuits





Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

Ordering Information

PART	PIN-PACKAGE	RESOLUTION (BIT)	INTERNAL REFERENCE TEMPCO (ppm/°C)
MAX5800ATB+T*	10 TDFN-EP**	8	10 (typ), 25 (max)
MAX5800AUB+T*	10 μMAX	8	10 (typ), 25 (max)
MAX5801ATB+T*	10 TDFN-EP**	10	10 (typ), 25 (max)
MAX5801AUB+T*	10 μMAX	10	10 (typ), 25 (max)
MAX5802AAUB+T	10 μMAX	12	3 (typ), 10 (max)
MAX5802BATB+T*	10 TDFN-EP**	12	10 (typ), 25 (max)
MAX5802BAUB+T*	10 μMAX	12	10 (typ), 25 (max)

Note: All devices are specified over the -40°C to +125°C temperature range.

Chip Information

Package Information

PROCESS: BICMOS

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10+2	<u>21-0061</u>	90-0330
10 TDFN-EP	T1033+1	21-0137	90-0003

⁺Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

^{*}Future product—Contact factory for availability.

^{**}EP = Exposed pad.

Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I²C Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/12	Initial release	_
1	12/12	Updated Electrical Characteristics and Ordering Information	2, 30



Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.



Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«**FORSTAR**» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А