

# Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to [Freescale.com](http://Freescale.com) and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

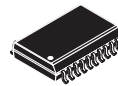
Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D



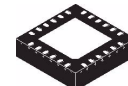
## MC9RS08KB12

### MC9RS08KB12 Series

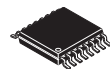
**Covers: MC9RS08KB12**  
**MC9RS08KB8**  
**MC9RS08KB4**  
**MC9RS08KB2**



20-Pin SOIC  
Case 751D



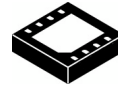
24-Pin QFN  
Case 1982-01



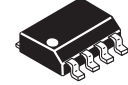
16-Pin TSSOP  
Case 948F



16-Pin SOIC N/B  
Case 751B



8-Pin DFN  
Case 1452-02



8-Pin SOIC  
Case 751

- 8-Bit RS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 1.8 V to 5.5 V across temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Subset of HC08 instruction set with added BGND instruction
  - Single Global interrupt vector
- On-Chip Memory
  - Up to 12 KB flash read/program/erase over full operating voltage and temperature, 12 KB/8 KB/4 KB/2 KB flash are optional
  - Up to 254-byte random-access memory (RAM), 254-byte/126-byte RAM are optional
  - Security circuitry to prevent unauthorized access to flash contents
- Power-Saving Modes
  - Wait mode — CPU shuts down; system clocks continue to run; full voltage regulation
  - Stop mode — CPU shuts down; system clocks are stopped; voltage regulator in standby
  - Wakeup from power-saving modes using RTI, KBI, ADC, ACMP, SCI and LVD
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies up to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal low power oscillator
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash-block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - **ADC** — 12-channel, 10-bit resolution; 2.5  $\mu\text{s}$  conversion time; automatic compare function; 1.7 mV/ $^{\circ}\text{C}$  temperature sensor; internal bandgap reference channel; operation in stop; hardware trigger
  - **ACMP** — Analog comparator; full rail-to-rail supply operation; option to compare to fixed internal bandgap reference voltage; can operate in stop mode
  - **TPM** — One 2-channel timer/pulse-width modulator module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - **IIC** — Inter-integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; capable of higher baud rates with reduced loading
  - **SCI** — One serial communications interface module with optional 13-bit break; LIN extensions
  - **MTIM** — Two 8-bit modulo timers; optional clock sources
  - **RTI** — One real-time clock with optional clock sources
  - **KBI** — Keyboard interrupts; up to 8 ports
- Input/Output
  - 18 GPIOs in 24- and 20-pin packages; 14 GPIOs in 16-pin package; 6 GPIOs in 8-pin package; including one output-only pin and one input-only pin
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
  - MC9RS08KB12/MC9RS08KB8/MC9RS08KB4
    - 24-pin QFN, 20-pin SOIC, 16-pin SOIC NB or TSSOP
  - MC9RS08KB2
    - 8-pin SOIC or DFN

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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## Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	4/13/2009	Updated on shared review comments, added package information.
2	5/22/2009	Completed most of the TBDs, corrected the block diagram.
3	8/31/2009	Completed all the TBDs. Changed $V_{LVD}$ and added $R_{PD}$ in the <a href="#">Table 7</a> . Changed $SI_{DD}$ , ADC adder from stop, RTI adder from stop with 1 kHz clock source enabled and LVI adder from stop at 5 V in the <a href="#">Table 8</a> .
4	6/23/2011	Split the 10-Bit ADC Characteristics to <a href="#">Table 15</a> and <a href="#">Table 16</a> for the $V_{DDAD}$ ranges. Corrected the note 4 in the <a href="#">Table 8</a> .
5	1/30/2012	Added 24-pin QFN package.

## Related Documentation

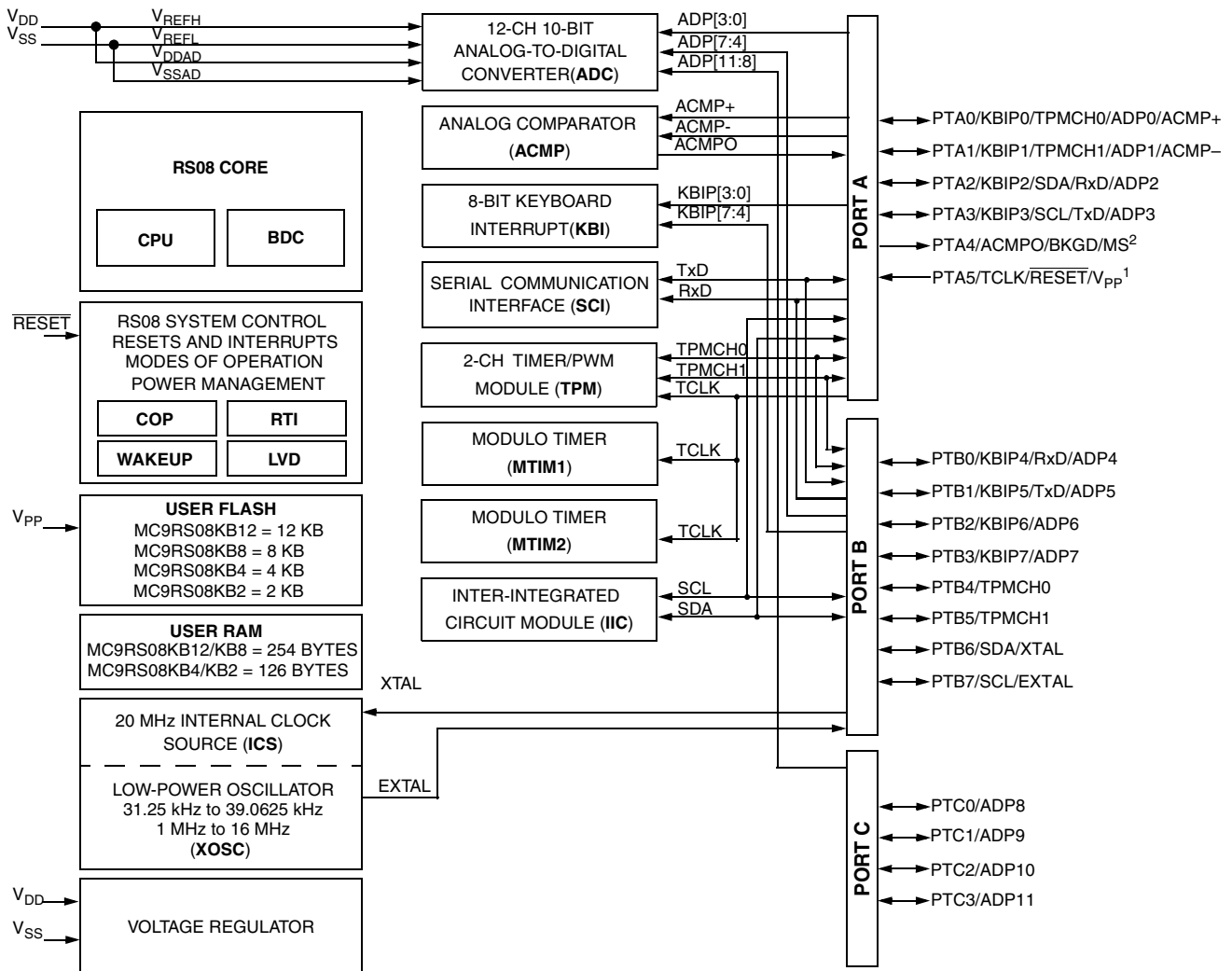
Find the most current versions of all documents at: <http://www.freescale.com>

### Reference Manual (MC9RS08KB12RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

# 1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of the MC9RS08KB12 MCU.



**NOTES:**

1. PTA5/TCLK/RESET/V<sub>PP</sub> is an input-only pin when used as port pin
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin

**Figure 1. MC9RS08KB12 Series Block Diagram**

# 2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KB12 series.

**Table 1. Pin Availability by Package Pin-Count**

Pin Number				<-- Lowest Priority --> Highest				
24	20	16	8	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	3	3	3					V <sub>DD</sub>
2	—	—	—	NC				
3	4	4	4					V <sub>SS</sub>
4	5	5	—	PTB7	SCL <sup>1</sup>			EXTAL
5	6	6	—	PTB6	SDA <sup>1</sup>			XTAL
6	7	7	—	PTB5	TPMCH1 <sup>2</sup>			
7	8	8	—	PTB4	TPMCH0 <sup>2</sup>			
8	9	—	—	PTC3			ADP11	
9	10	—	—	PTC2			ADP10	
10	11	—	—	PTC1			ADP9	
11	12	—	—	PTC0			ADP8	
12	13	9	—	PTB3	KBIP7		ADP7	
13	14	10	—	PTB2	KBIP6		ADP6	
14	15	11	—	PTB1	KBIP5	TxD <sup>3</sup>	ADP5	
15	16	12	—	PTB0	KBIP4	RxD <sup>3</sup>	ADP4	
16	17	13	5	PTA3	KBIP3	SCL <sup>1</sup>	TxD <sup>3</sup>	ADP3
17	18	14	6	PTA2	KBIP2	SDA <sup>1</sup>	RxD <sup>3</sup>	ADP2
18	19	15	7	PTA1	KBIP1	TPMCH1 <sup>2</sup>	ADP1	ACMP–
19	20	16	8	PTA0	KBIP0	TPMCH0 <sup>2</sup>	ADP0	ACMP+
20	—	—	—	NC				
21	—	—	—	NC				
22	—	—	—	NC				
23	1	1	1	PTA5		TCLK	$\overline{\text{RESET}}$	V <sub>PP</sub>
24	2	2	2	PTA4	ACMPO	BKGD	MS	

<sup>1</sup> IIC pins can be remapped to PTB6 and PTB7, default reset location is PTA2 and PTA3. It can be configured only once.

<sup>2</sup> TPM pins can be remapped to PTB4 and PTB5, default reset location is PTA0 and PTA1.

<sup>3</sup> SCI pins can be remapped to PTA2 and PTA3, default reset location is PTB0 and PTB1. It can be configured only once.

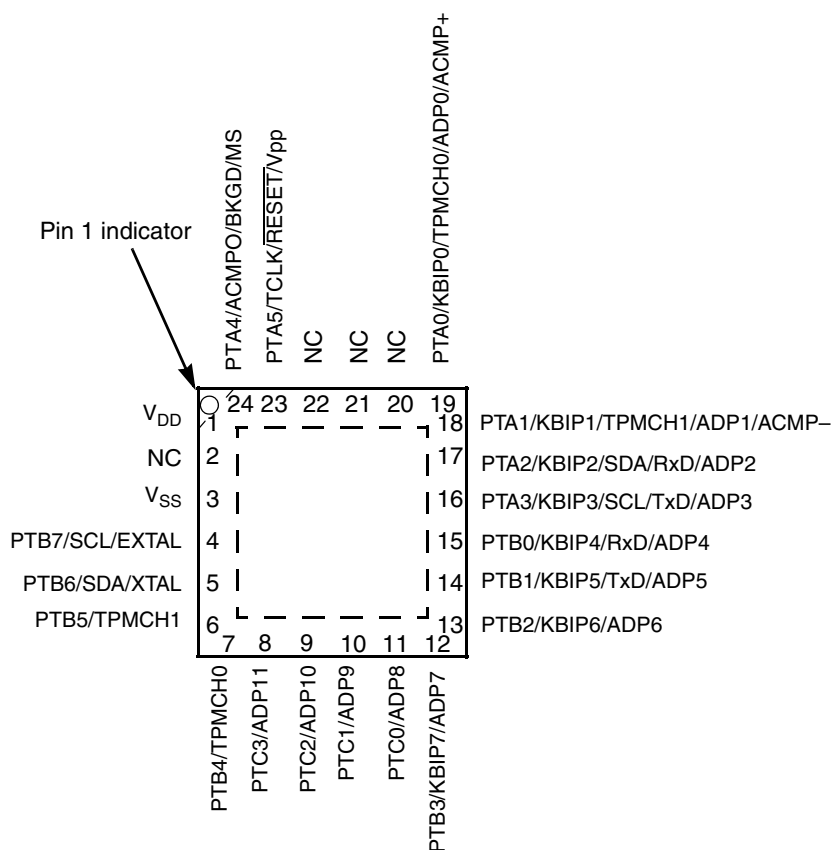


Figure 2. MC9RS08KB12 Series 24-Pin QFN Package

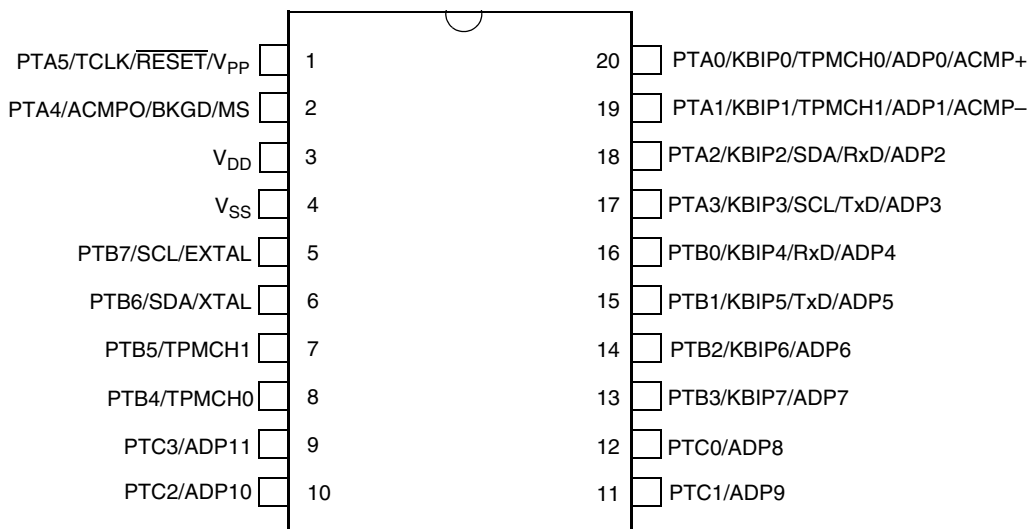


Figure 3. MC9RS08KB12 Series 20-Pin SOIC Package

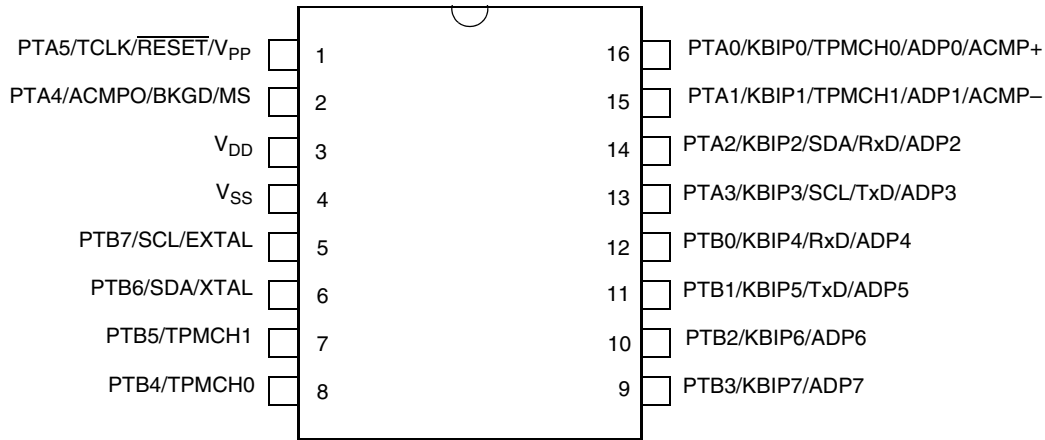


Figure 4. MC9RS08KB12 Series 16-Pin SOIC NB/TSSOP Package

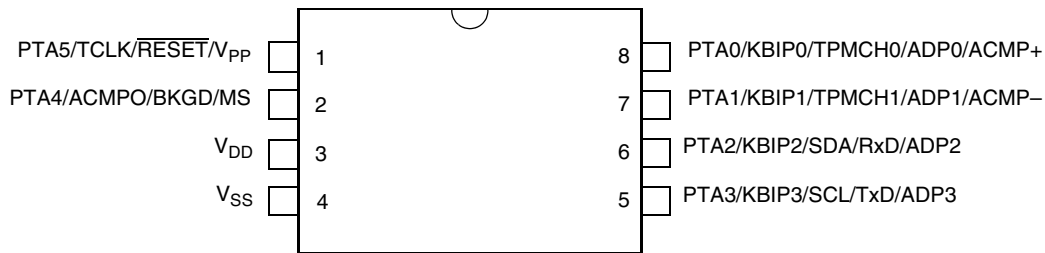


Figure 5. MC9RS08KB12 Series 8-Pin SOIC/DFN Package

### 3 Electrical Characteristics

#### 3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KB12 series of microcontrollers available at the time of publication.

#### 3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

<b>P</b>	Those parameters are guaranteed during production testing on each individual device.
<b>C</b>	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
<b>T</b>	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.



**Table 2. Parameter Classifications**

<b>D</b>	Those parameters are derived mainly from simulations.
----------	-------------------------------------------------------

### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## 3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance,  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

**Table 3. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to 5.8	V
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Digital input voltage	$V_{In}$	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	±25	mA
Storage temperature range	$T_{stg}$	-55 to 150	°C

<sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.

<sup>2</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  except the  $\overline{RESET}/V_{PP}$  pin which is internally clamped to  $V_{SS}$  only.

<sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

## 3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of

## Electrical Characteristics

unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 4. Thermal Characteristics**

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	$T_A$	$T_L$ to $T_H$ -40 to 85	°C
Maximum junction temperature	$T_{JMAX}$	150	°C
Thermal resistance 24-pin QFN	$\theta_{JA}$	113	°C/W
Thermal resistance 20-pin SOIC	$\theta_{JA}$	83	°C/W
Thermal resistance 16-pin SOIC NB	$\theta_{JA}$	103	°C/W
Thermal resistance 16-pin TSSOP	$\theta_{JA}$	29	°C/W
Thermal resistance 8-pin SOIC	$\theta_{JA}$	150	°C/W
Thermal resistance 8-pin DFN	$\theta_{JA}$	110	°C/W

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

$T_A$  = Ambient temperature, °C

$\theta_{JA}$  = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$ , Watts chip internal power

$P_{I/O}$  = Power dissipation on input and output pins user determined

For most applications,  $P_{I/O} \ll P_{int}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving [Equation 1](#) and [Equation 2](#) for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from [Equation 3](#) by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving [Equation 1](#) and [Equation 2](#) iteratively for any value of  $T_A$ .

### 3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge.

Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 5. ESD and Latch-Up Test Conditions**

<b>Model</b>	<b>Description</b>	<b>Symbol</b>	<b>Value</b>	<b>Unit</b>
Human body	Series resistance	R1	1500	$\Omega$
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	1	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

**Table 6. ESD and Latch-Up Protection Characteristics**

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{HBM}$	$\pm 2000$	—	V
2	Charge device model (CDM)	$V_{CDM}$	$\pm 500$	—	V
3	Latch-up current at $T_A = 85^\circ\text{C}$	$I_{LAT}$	$\pm 100$	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

### 3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

**Table 7. DC Characteristics (Temperature Range =  $-40$  to  $85^\circ\text{C}$  Ambient)**

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage (run, wait and stop modes.) $0 < f_{BUS} < 10$ MHz	$V_{DD}$	1.8	—	5.5	V
2	C	Minimum RAM retention supply voltage applied to $V_{DD}$	$V_{RAM}$	$0.8^1$	—	—	V
3	P	Low-voltage detection threshold ( $V_{DD}$ falling) ( $V_{DD}$ rising)	$V_{LVD}$	1.80 1.88	1.86 1.94	1.95 2.05	V
4	C	Power on RESET (POR) voltage	$V_{POR}^1$	0.9	—	1.7	V
5	C	Input high voltage ( $V_{DD} > 2.3\text{V}$ ) (all digital inputs)	$V_{IH}$	$0.70 \times V_{DD}$	—	—	V
6	C	Input high voltage ( $1.8\text{V} \leq V_{DD} \leq 2.3\text{V}$ ) (all digital inputs)	$V_{IH}$	$0.85 \times V_{DD}$	—	—	V
7	C	Input low voltage ( $V_{DD} > 2.3\text{V}$ ) (all digital inputs)	$V_{IL}$	—	—	$0.30 \times V_{DD}$	V
8	C	Input low voltage ( $1.8\text{V} \leq V_{DD} \leq 2.3\text{V}$ ) (all digital inputs)	$V_{IL}$	—	—	$0.30 \times V_{DD}$	V
9	C	Input hysteresis (all digital inputs)	$V_{hys}^1$	$0.06 \times V_{DD}$	—	—	V
10	P	Input leakage current (per pin) $V_{In} = V_{DD}$ or $V_{SS}$ , all input only pins	$I_{InI}$	—	0.025	1.0	$\mu\text{A}$
11	P	High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or $V_{SS}$ , all input/output	$I_{IOZ}$	—	0.025	1.0	$\mu\text{A}$
12	P	Internal pullup resistors <sup>2</sup> (all port pins)	$R_{PU}$	20	45	65	k $\Omega$
13	P	Internal pulldown resistors <sup>2</sup> (all port pins)	$R_{PD}$	20	45	65	k $\Omega$
14	C	Output high voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 1$ mA 1.8 V, $I_{Load} = 0.5$ mA	$V_{OH}$	$V_{DD} - 0.8$	—	—	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = 5$ mA 3 V, $I_{Load} = 3$ mA 1.8 V, $I_{Load} = 2$ mA			$V_{DD} - 0.8$	—	
15	C	Maximum total IOH for all port pins	$I_{OHT}$	—	—	40	mA

**Table 7. DC Characteristics (Temperature Range = -40 to 85°C Ambient) (continued)**

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
16	C	Output low voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 1$ mA 1.8 V, $I_{Load} = 0.5$ mA	$V_{OL}$	—	—	0.8	V
		Output low voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = 5$ mA 3 V, $I_{Load} = 3$ mA 1.8 V, $I_{Load} = 2$ mA		—	—		
17	C	Maximum total IOI for all port pins	$I_{OLT}$	—	—	40	mA
18	C	DC injection current <sup>3, 4, 5, 6</sup> $V_{In} < V_{SS}$ , $V_{In} > V_{DD}$ Single pin limit		—	—	0.2	mA
		Total MCU limit, includes sum of all stressed pins		—	—	0.8	
19	C	Input capacitance (all non-supply pins)	$C_{In}$	—	—	7	pF

<sup>1</sup> This parameter is characterized and not tested on each device.

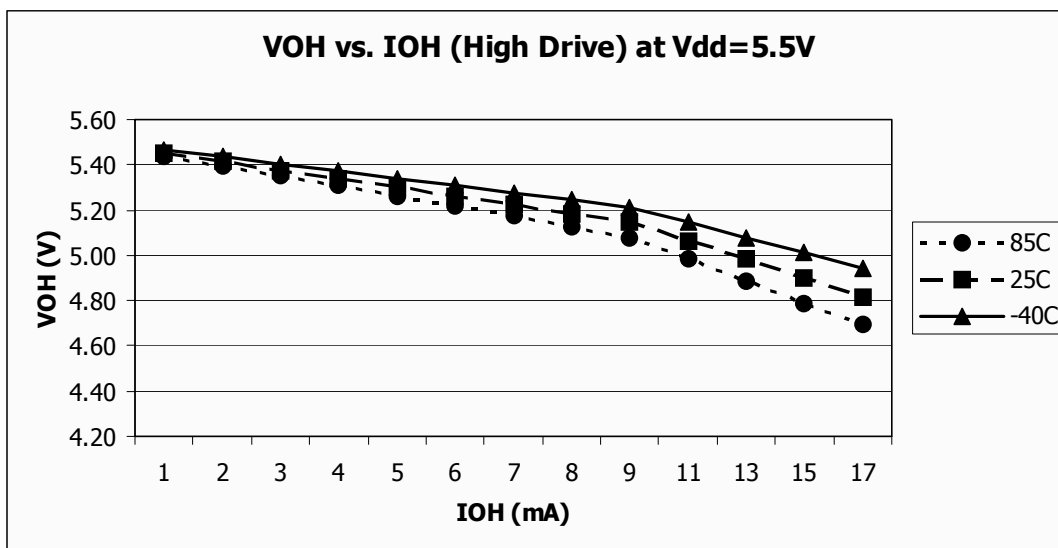
<sup>2</sup> Measurement condition for pull resistors:  $V_{In} = V_{SS}$  for pullup and  $V_{In} = V_{DD}$  for pulldown.

<sup>3</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  except the  $\overline{RESET}/V_{PP}$  which is internally clamped to  $V_{SS}$  only.

<sup>4</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>5</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>6</sup> This parameter is characterized and not tested on each device.



**Figure 6. Typical  $V_{OH}$  vs.  $I_{OH}$   
 $V_{DD} = 5.5$  V (High Drive)**

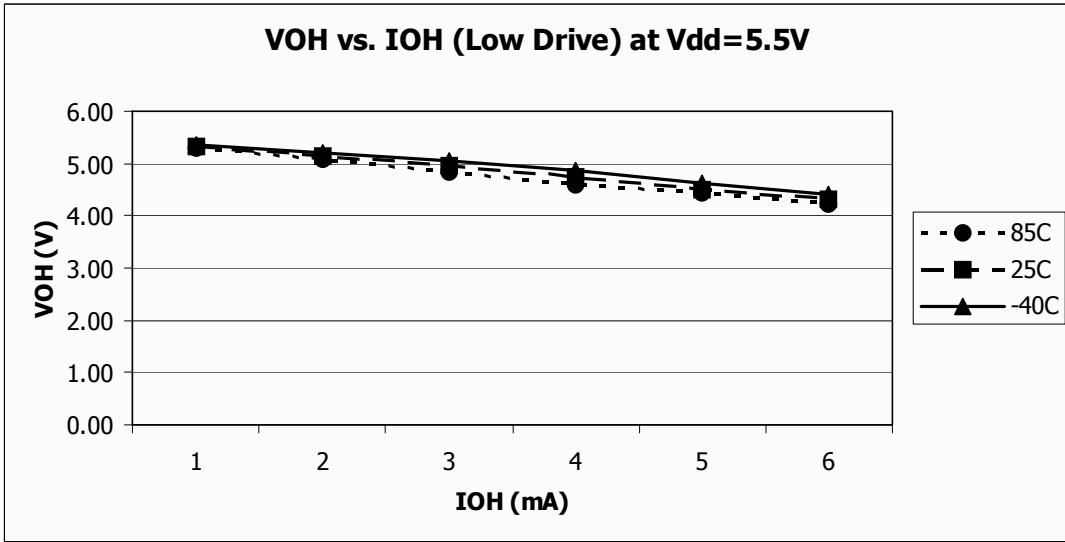


Figure 7. Typical  $V_{OH}$  vs.  $I_{OH}$   
 $V_{DD} = 5.5V$  (Low Drive)

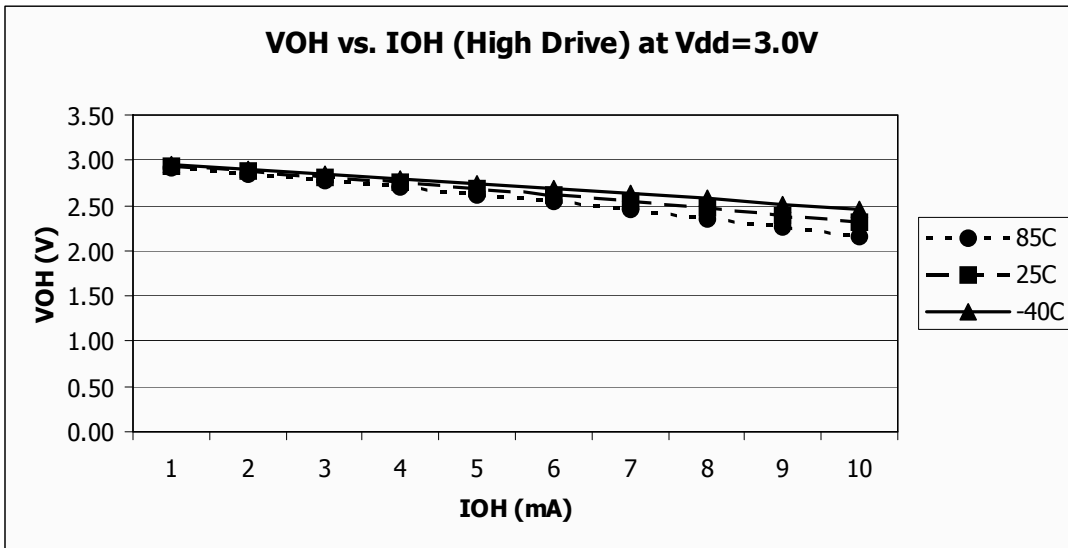


Figure 8. Typical  $V_{OH}$  vs.  $I_{OH}$   
 $V_{DD} = 3.0V$  (High Drive)

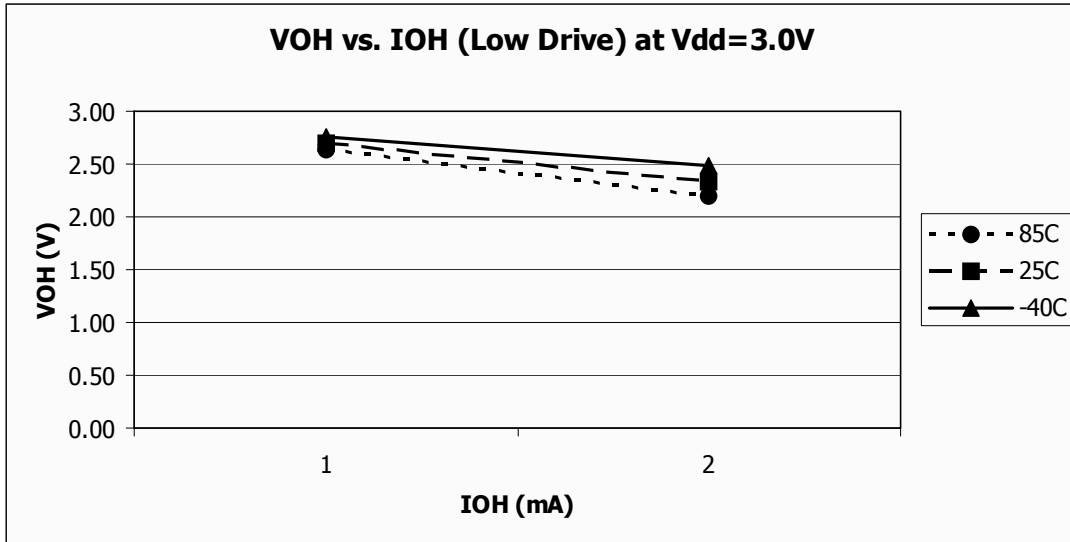


Figure 9. Typical  $V_{OH}$  vs.  $I_{OH}$   
 $V_{DD} = 3.0\text{ V}$  (Low Drive)

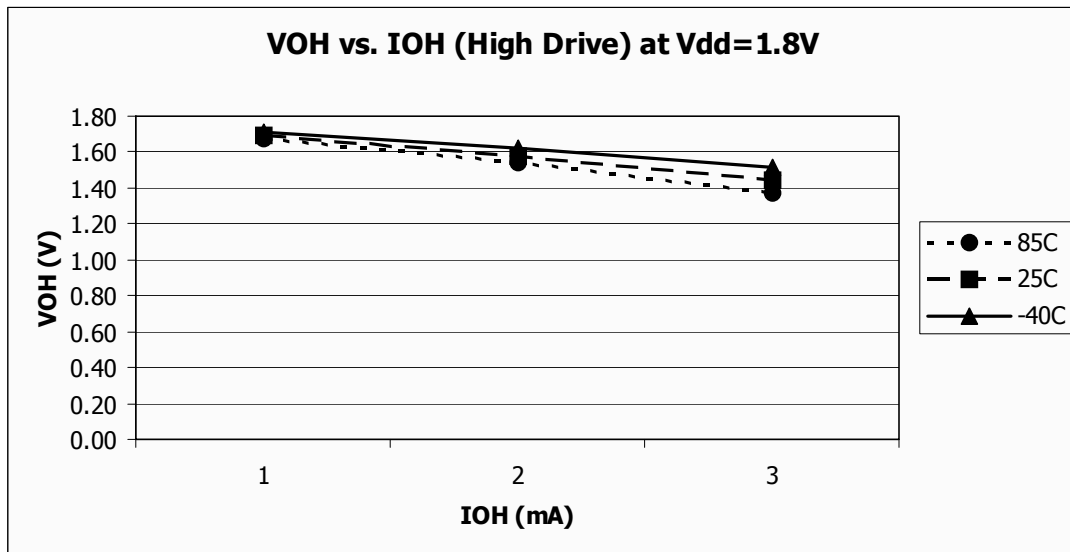


Figure 10. Typical  $V_{OH}$  vs.  $I_{OH}$   
 $V_{DD} = 1.8\text{ V}$  (High Drive)

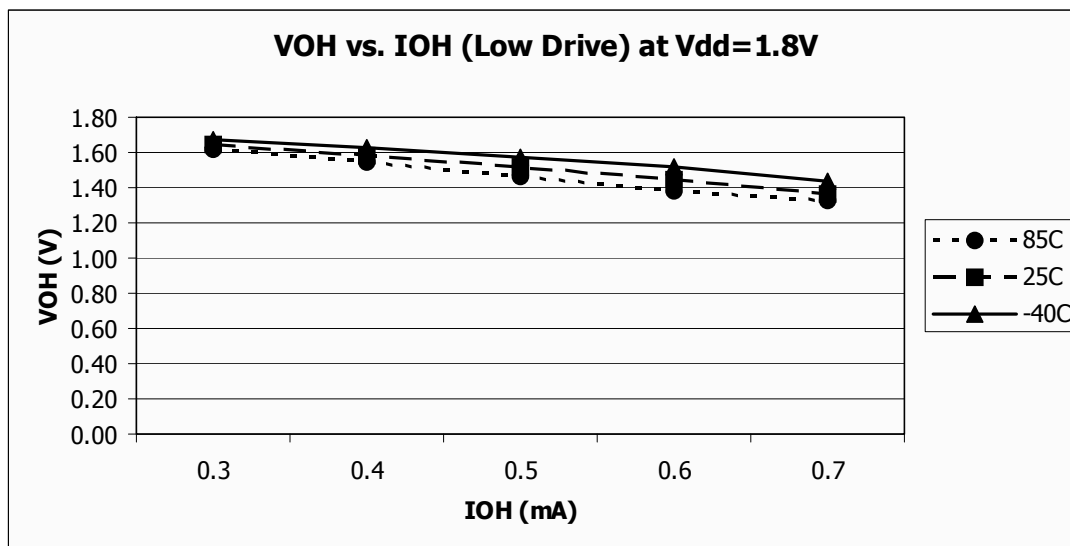


Figure 11. Typical  $V_{OH}$  vs.  $I_{OH}$   
 $V_{DD} = 1.8\text{ V}$  (Low Drive)

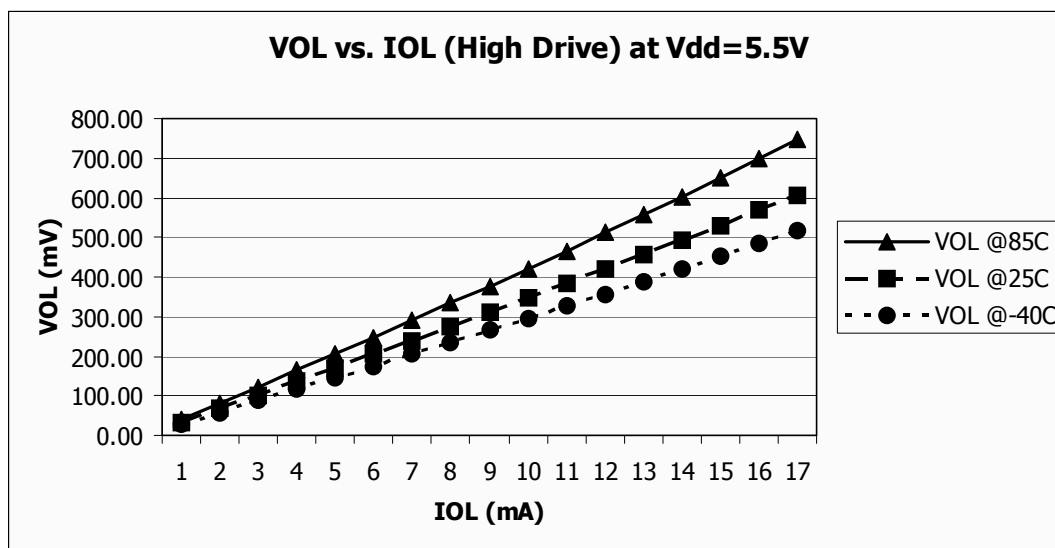


Figure 12. Typical  $V_{OL}$  vs.  $I_{OL}$   
 $V_{DD} = 5.5\text{ V}$  (High Drive)



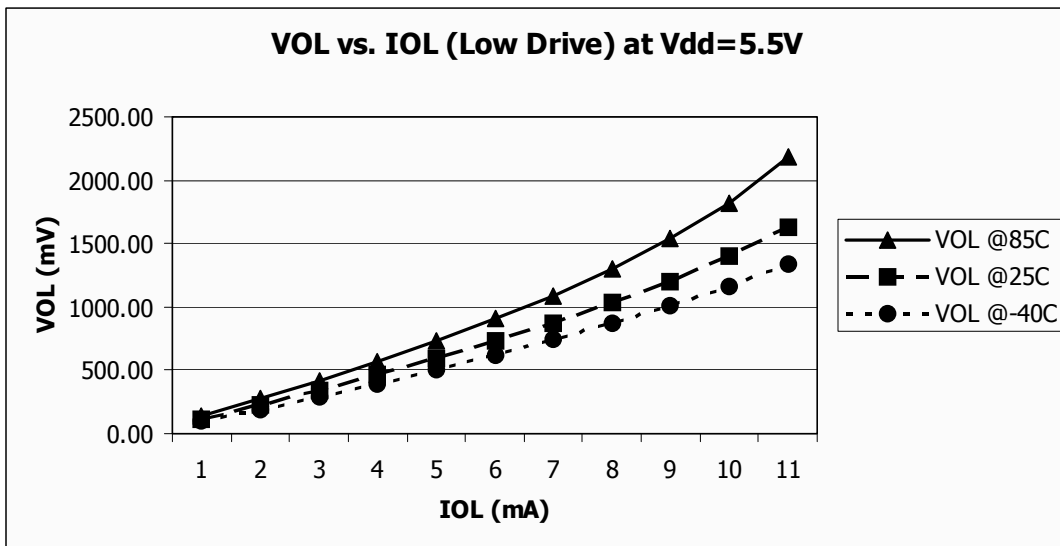


Figure 13. Typical  $V_{OL}$  vs.  $I_{OL}$   
 $V_{DD} = 5.5\text{ V}$  (Low Drive)

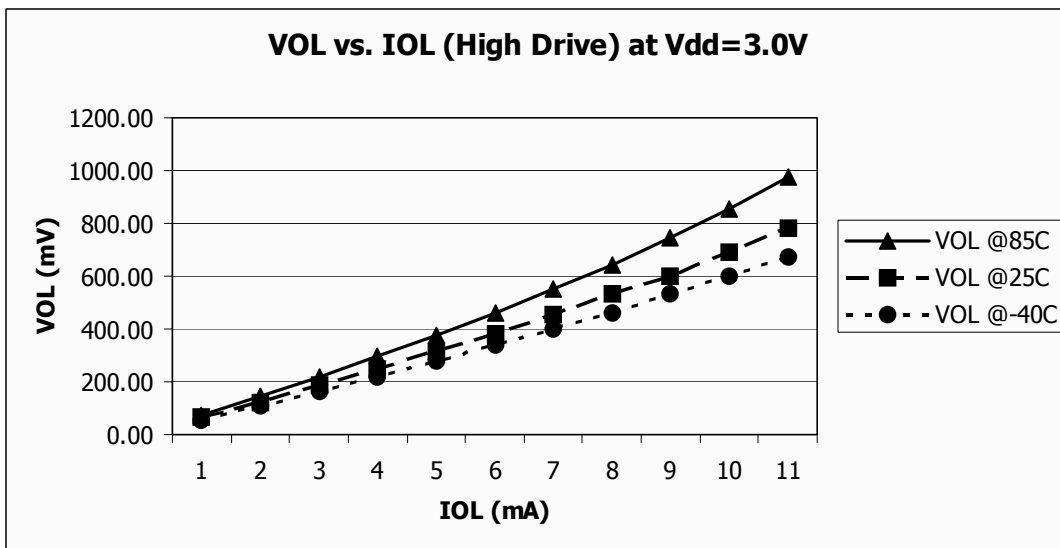


Figure 14. Typical  $V_{OL}$  vs.  $I_{OL}$   
 $V_{DD} = 3.0\text{ V}$  (High Drive)

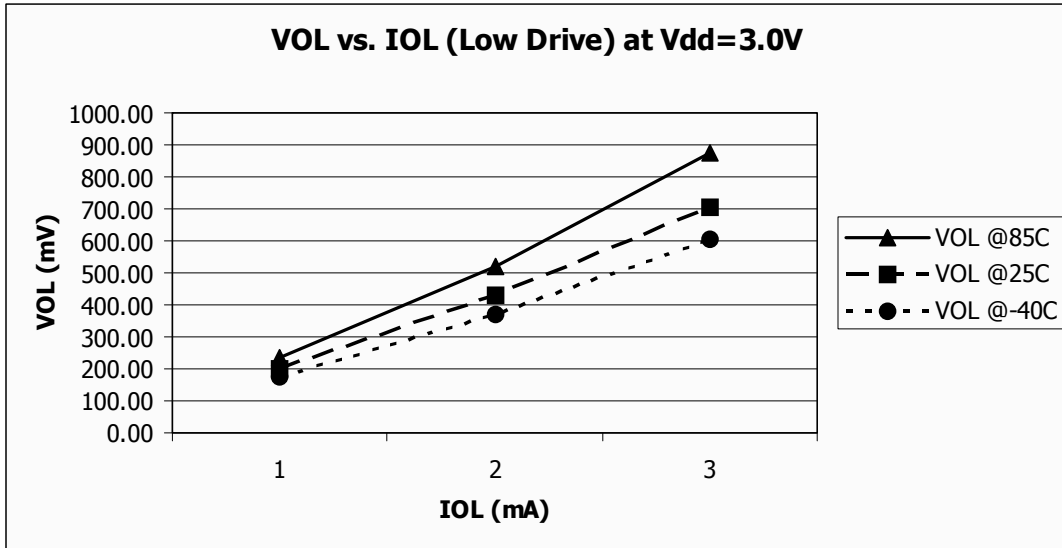


Figure 15. Typical  $V_{OL}$  vs.  $I_{OL}$   
 $V_{DD} = 3.0\text{ V}$  (Low Drive)

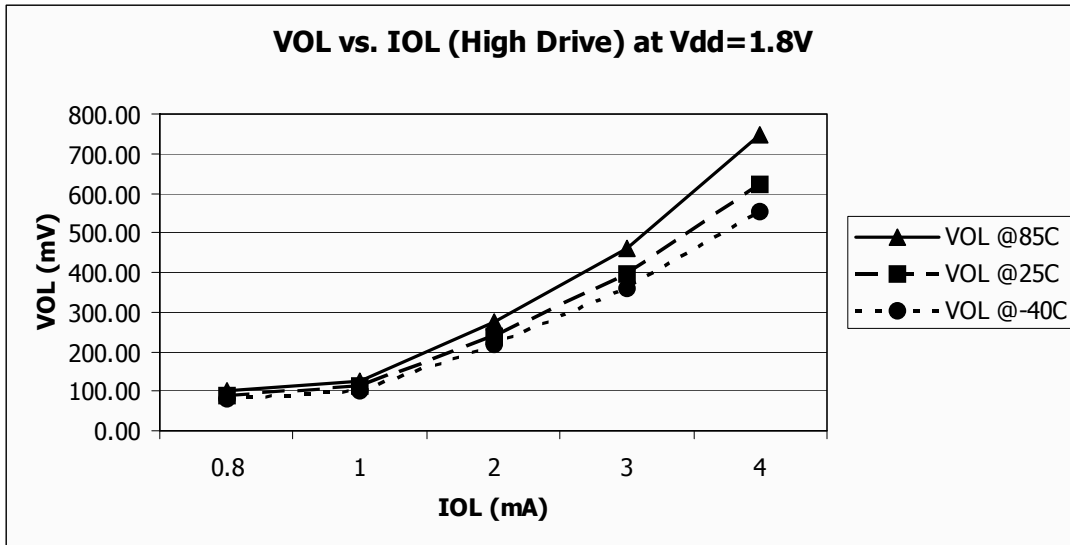


Figure 16. Typical  $V_{OL}$  vs.  $I_{OL}$   
 $V_{DD} = 1.8\text{ V}$  (High Drive)

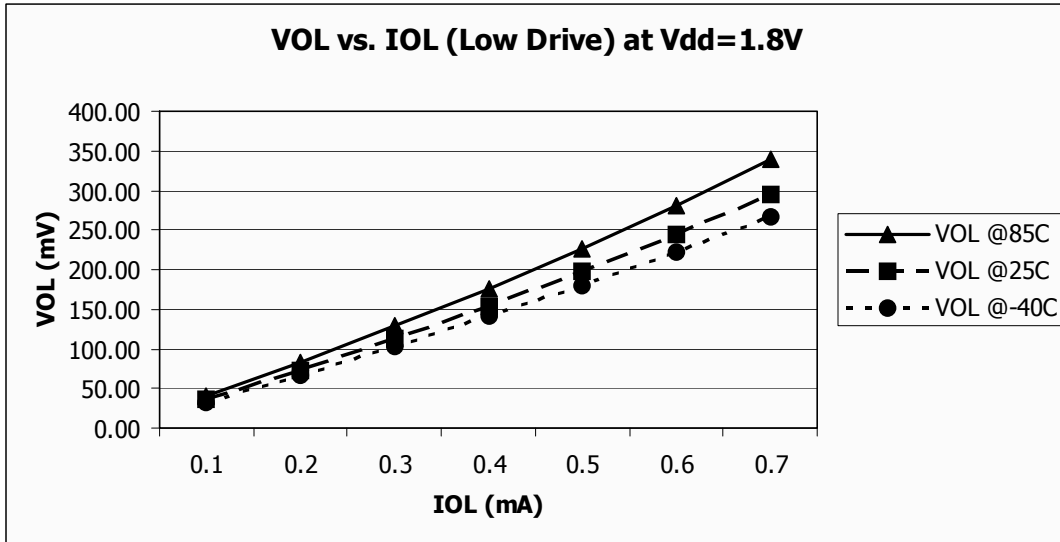


Figure 17. Typical  $V_{OL}$  vs.  $I_{OL}$   
 $V_{DD} = 1.8\text{ V}$  (Low Drive)

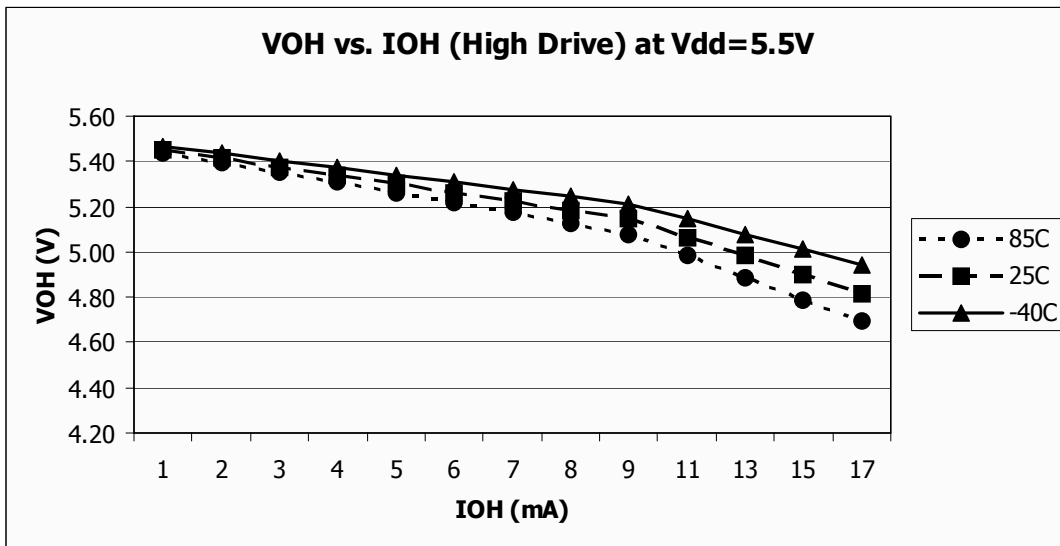


Figure 18. Typical  $I_{OH}$  vs.  $V_{DD}-V_{OH}$   
 $V_{DD} = 5.5\text{ V}$  (High Drive)

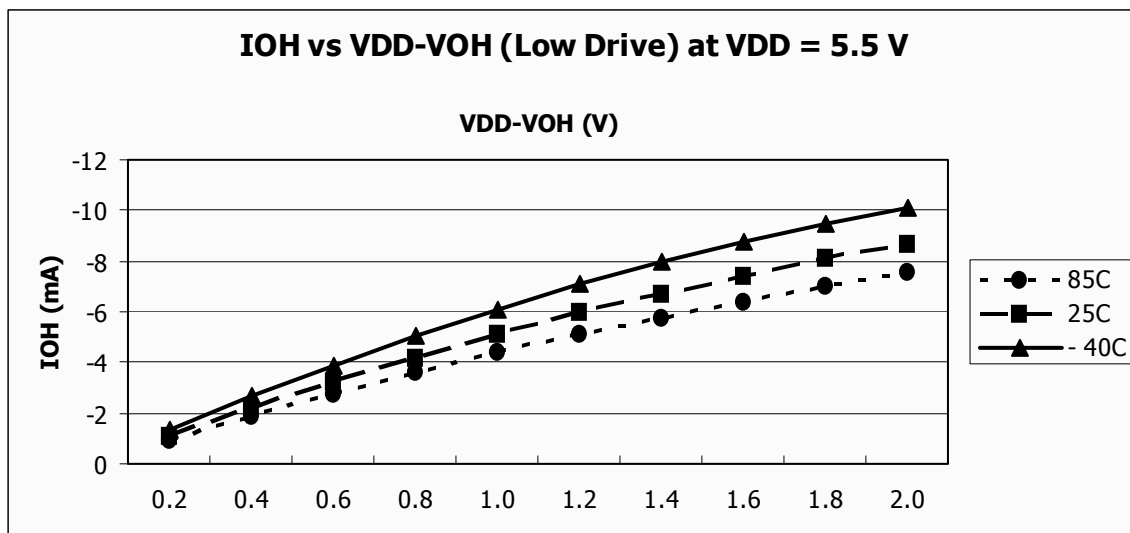


Figure 19. Typical I<sub>OH</sub> vs. V<sub>DD</sub>-V<sub>OH</sub>  
V<sub>DD</sub> = 5.5 V (Low Drive)

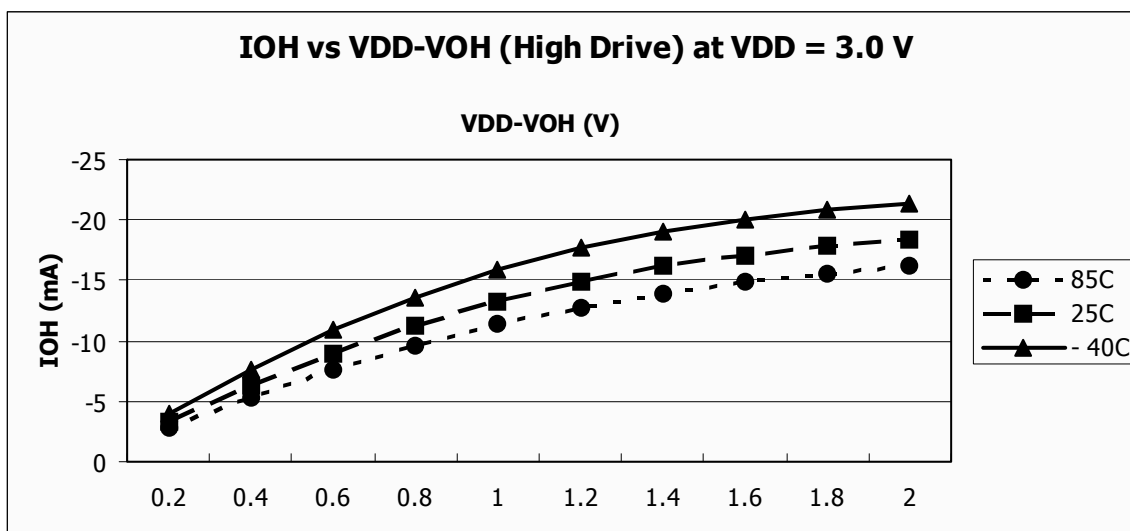


Figure 20. Typical I<sub>OH</sub> vs. V<sub>DD</sub>-V<sub>OH</sub>  
V<sub>DD</sub> = 3 V (High Drive)

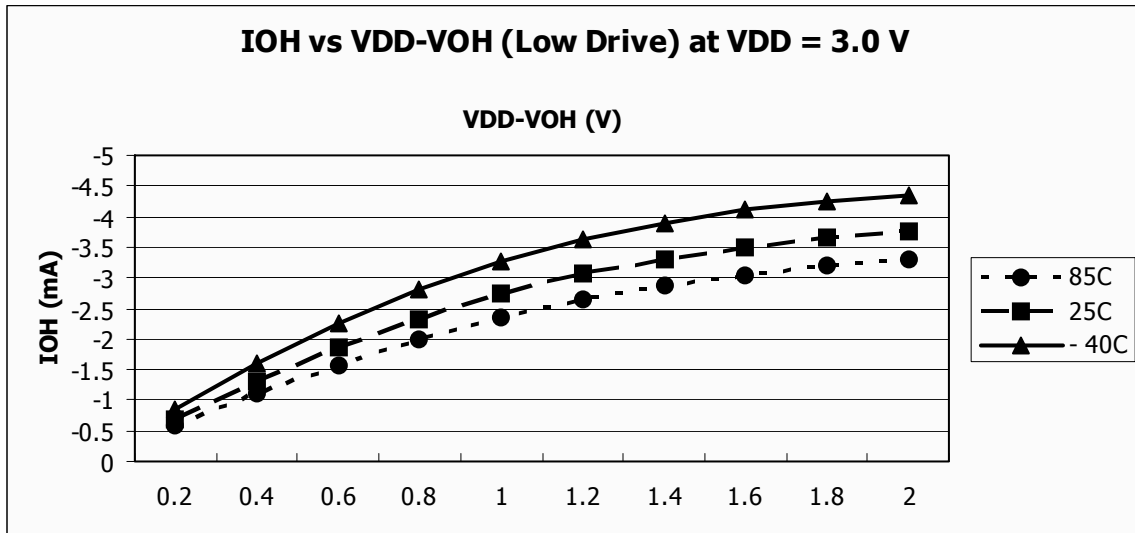


Figure 21. Typical  $I_{OH}$  vs.  $V_{DD}-V_{OH}$   
 $V_{DD} = 3\text{ V}$  (Low Drive)

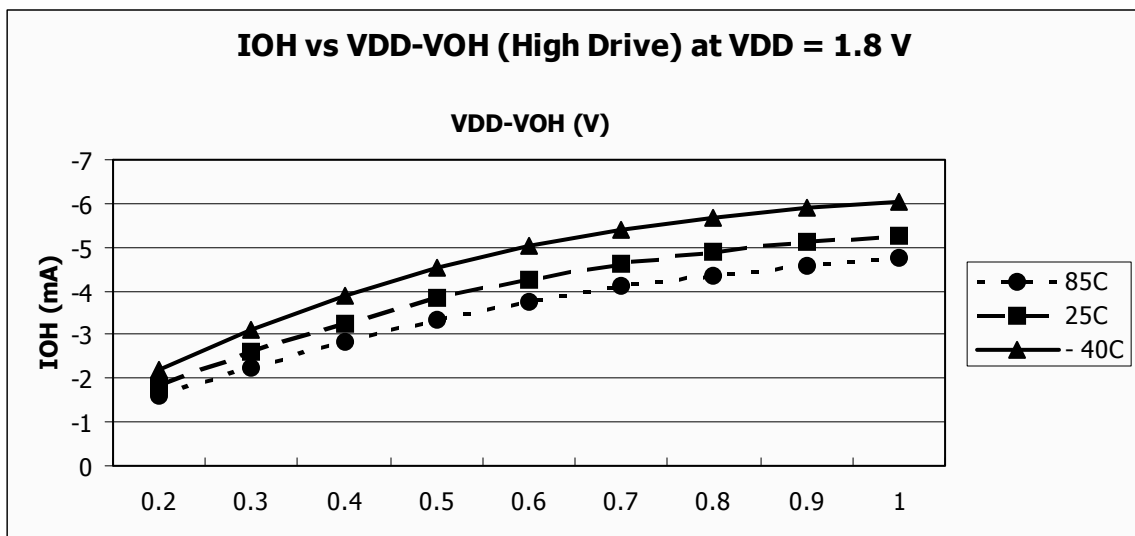


Figure 22. Typical  $I_{OH}$  vs.  $V_{DD}-V_{OH}$   
 $V_{DD} = 1.8\text{ V}$  (High Drive)

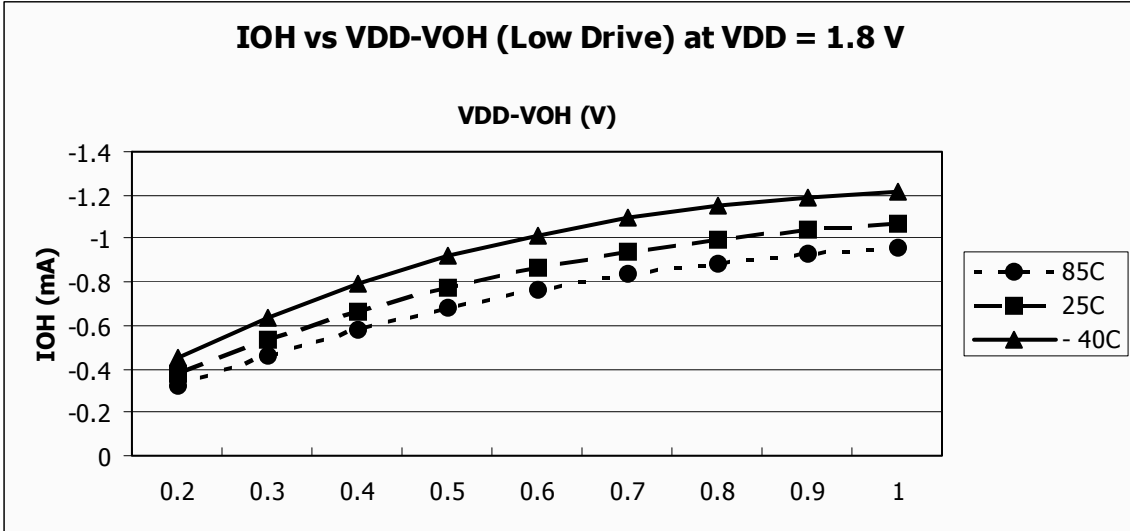


Figure 23. Typical  $I_{OH}$  vs.  $V_{DD}-V_{OH}$   
 $V_{DD} = 1.8\text{ V}$  (Low Drive)

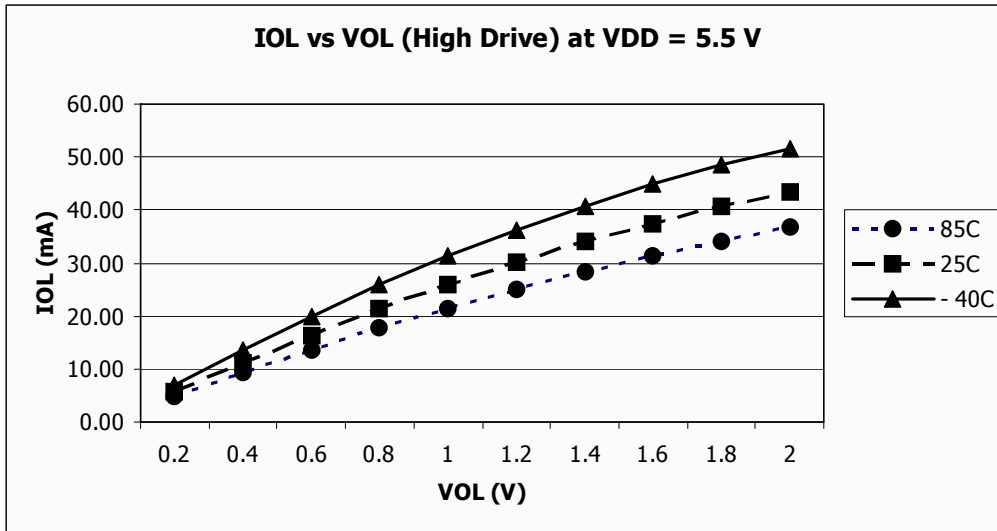


Figure 24. Typical  $I_{OL}$  vs.  $V_{OL}$   
 $V_{DD} = 5.5\text{ V}$  (High Drive)

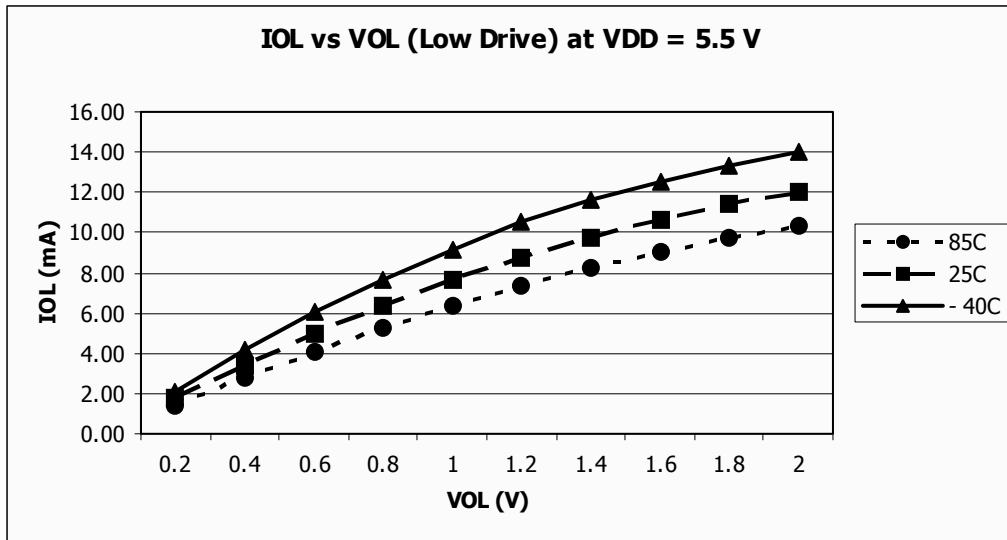


Figure 25. Typical I<sub>OL</sub> vs. V<sub>OL</sub>  
V<sub>DD</sub> = 5.5 V (Low Drive)

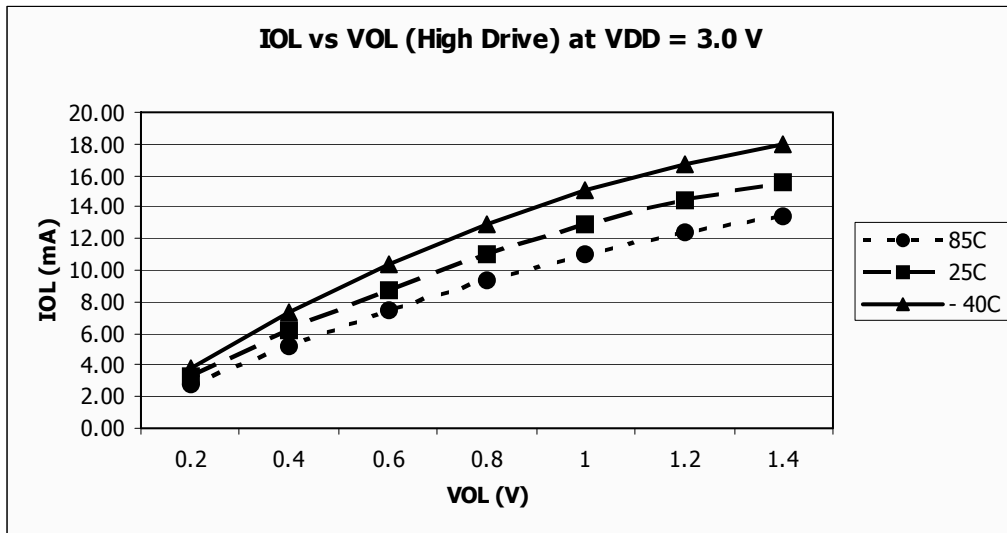


Figure 26. Typical I<sub>OL</sub> vs. V<sub>OL</sub>  
V<sub>DD</sub> = 3 V (High Drive)

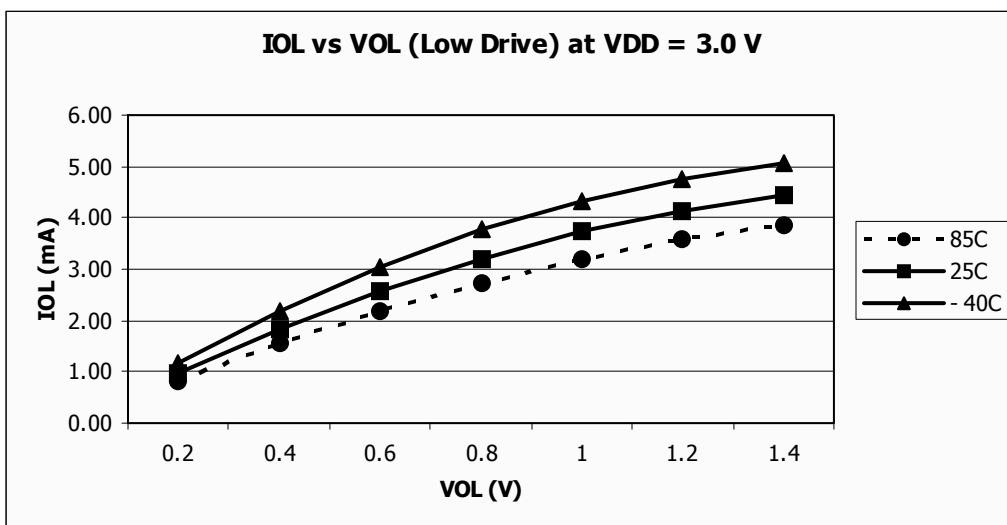


Figure 27. Typical  $I_{OL}$  vs.  $V_{OL}$   
 $V_{DD} = 3\text{ V}$  (Low Drive)

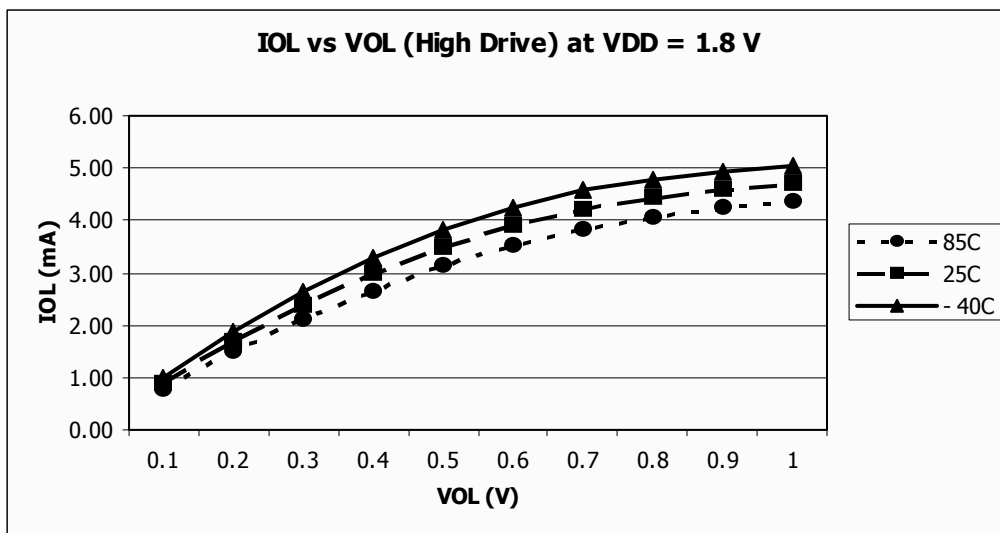


Figure 28. Typical  $I_{OL}$  vs.  $V_{OL}$   
 $V_{DD} = 1.8\text{ V}$  (High Drive)



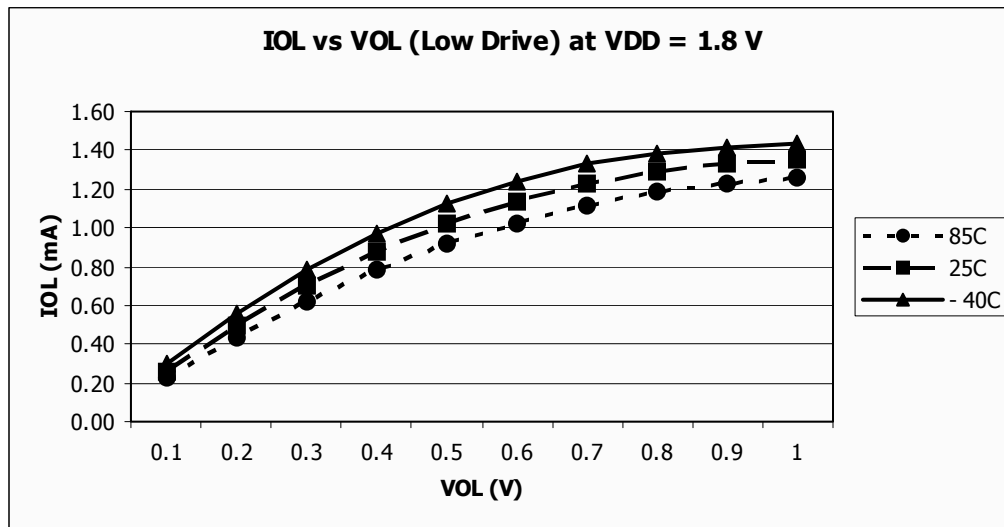


Figure 29. Typical  $I_{OL}$  vs.  $V_{OL}$   
 $V_{DD} = 1.8$  V (Low Drive)

### 3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

N	C	Parameter	Symbol	$V_{DD}$ (V)	Typical	Max <sup>1</sup>	Temp. (°C)	Unit
1	P	Run supply current <sup>2</sup> measured at ( $f_{Bus} = 10$ MHz)	$R_{I_{DD10}}$	5	3.45 3.48 3.53	7	-40 25 85	mA
2	C			3	3.39 3.42 3.49	—	-40 25 85	
3	C			1.80	2.40 2.42 2.44	—	-40 25 85	
4	C	Run supply current <sup>3</sup> measured at ( $f_{Bus} = 1.25$ MHz)	$R_{I_{DD1}}$	5	0.93 0.96 0.99	—	-40 25 85	mA
5	T			3	0.91 0.92 0.92	—	-40 25 85	
6	T			1.80	0.66 0.67 0.68	—	-40 25 85	

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V <sub>DD</sub> (V)	Typical	Max <sup>1</sup>	Temp. (°C)	Unit
7	C	Wait mode supply current <sup>3</sup> measured at (f <sub>Bus</sub> = 2.00 MHz)	W <sub>I</sub> DD2	5	841.13 859.98 873.69	—	−40 25 85	μA
8	T			3	840.21 850.60 846.67	—	−40 25 85	
9	T			1.80	630.64 635.10 643.67	—	−40 25 85	
10	C	Wait mode supply current <sup>3</sup> measured at (f <sub>Bus</sub> = 1.00 MHz)	W <sub>I</sub> DD1	5	667.86 683.38 688.02	—	−40 25 85	μA
11	T			3	666.34 672.79 669.15	—	−40 25 85	
12	T			1.80	505.39 509.28 502.52	—	−40 25 85	
13	P	Stop mode supply current	S <sub>I</sub> DD	5	1.15 1.40 7.67	11	−40 25 85	μA
14	C			3	1.05 1.26 4.52	—	−40 25 85	
15	C			1.80	0.39 0.56 4.21	—	−40 25 85	
16	C	ADC adder from stop <sup>3</sup>	—	5	128.86 140.44 154.97	—	−40 25 85	μA
17	T			3	102.98 111.71 118.33	—	−40 25 85	
18	T			1.80	54.77 66.33 74.42	—	−40 25 85	
19	C	ACMP adder from stop (ACME = 1)	—	5	14.43 15.96 16.77	—	−40 25 85	μA
20	T			3	14.37 14.72 14.45	—	−40 25 85	
21	T			1.80	13.05 14.02 12.92	—	−40 25 85	

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V <sub>DD</sub> (V)	Typical	Max <sup>1</sup>	Temp. (°C)	Unit
22	C	RTI adder from stop with 1 kHz clock source enabled <sup>4</sup>	—	5	0.10 0.10 0.17	—	–40 25 85	μA
23	T			3	0.02 0.06 0.02	—	–40 25 85	
24	T			1.80	0.40 0.45 0.20	—	–40 25 85	
25	T	RTI adder from stop with 32.768KHz external clock source reference enabled	—	5	0.70 1.08 1.94	—	–40 25 85	μA
26	T			3	0.56 0.56 0.62	—	–40 25 85	
27	T			1.80	0.70 0.86 0.50	—	–40 25 85	
28	C	LVI adder from stop (LVDE = 1 and LVDSE = 1)	—	5	58.93 68.27 76.60	—	–40 25 85	μA
29	T			3	58.89 61.98 63.45	—	–40 25 85	
30	T			1.80	52.84 54.52 52.49	—	–40 25 85	

<sup>1</sup> Maximum value is measured at the nominal V<sub>DD</sub> voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

<sup>2</sup> Not include any DC loads on port pins.

<sup>3</sup> Required asynchronous ADC clock and LVD to be enabled.

<sup>4</sup> Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 672.79 μA at 3 V and 509.28 μA at 1.8 V with f<sub>BUS</sub> = 1 MHz.

### 3.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications (Temperature Range = -40 to 85°C Ambient)

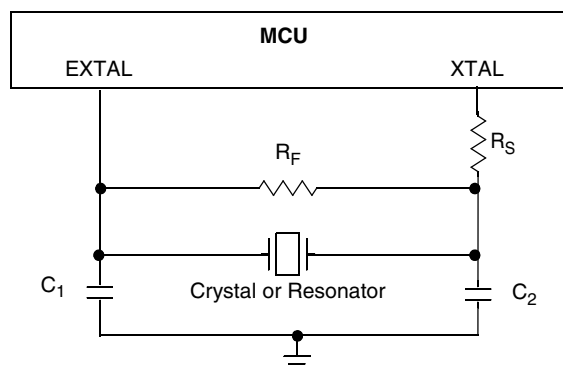
Num	C	Rating	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	$f_{lo}$	32	—	38.4	kHz
		High range (RANGE = 1) FEE or FBE mode <sup>2</sup>	$f_{hi}$	1	—	5	MHz
		High range (RANGE = 1, HGO = 1) FBELP mode	$f_{hi-hgo}$	1	—	16	MHz
		High range (RANGE = 1, HGO = 0) FBELP mode	$f_{hi-lp}$	1	—	8	MHz
2	D	Load capacitors	$C_1, C_2$	See crystal or resonator manufacturer's recommendation.			
3	D	Feedback resistor	$R_F$	—	10	—	M $\Omega$
		Low range (32 kHz to 100 kHz)					
		High range (1 MHz to 16 MHz)		—	1	—	
4	D	Series resistor	$R_S$	—	0	—	k $\Omega$
		Low range, low gain (RANGE = 0, HGO = 0)					
		Low range, high gain (RANGE = 0, HGO = 1)					
		High range, low gain (RANGE = 1, HGO = 0)					
		High range, high gain (RANGE = 1, HGO = 1)					
		$\geq 8$ MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
5	C	Crystal start-up time <sup>3</sup>					
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	ms
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—	
		High range, low gain (RANGE = 1, HGO = 0) <sup>4</sup>	$t_{CSTH-LP}$	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1) <sup>4</sup>	$t_{CSTH-HGO}$	—	20	—	
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)	$f_{extal}$	0.03125	—	5	MHz
		FEE or FBE mode <sup>2</sup>					
		FBELP mode		0	—	40	

<sup>1</sup> Typical data was characterized at 5.0 V, 25 °C or is recommended value.

<sup>2</sup> The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

<sup>3</sup> This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

<sup>4</sup> 4 MHz crystal.



### 3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

### 3.9.1 Control Timing

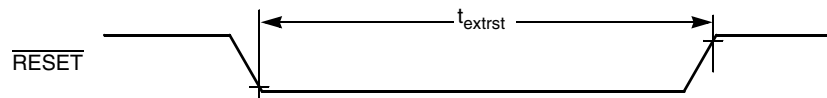
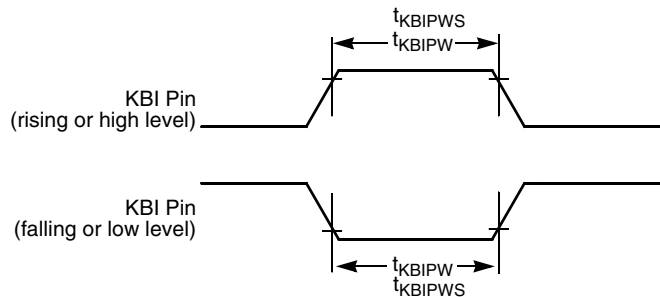
**Table 10. Control Timing**

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	D	Bus frequency ( $t_{cyc} = 1/f_{Bus}$ )	$f_{Bus}$	0	—	10	MHz
2	D	Real time interrupt internal oscillator period	$t_{RTI}$	700	1000	1300	$\mu$ s
3	D	External $\overline{RESET}$ pulse width <sup>1</sup>	$t_{extrst}$	150	—	—	ns
4	D	KBI pulse width <sup>2</sup>	$t_{KBIPW}$	$1.5 t_{cyc}$	—	—	ns
5	D	KBI pulse width in stop <sup>1</sup>	$t_{KBIPWS}$	100	—	—	ns
6	D	Port rise and fall time (load = 50 pF) <sup>3</sup>	$t_{Rise}, t_{Fall}$	—	11	—	ns
		Slew rate control disabled (PTxSE = 0)			35	—	
		Slew rate control enabled (PTxSE = 1)					

<sup>1</sup> This is the shortest pulse guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

<sup>2</sup> This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

<sup>3</sup> Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

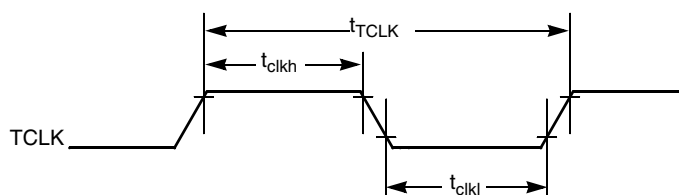

**Figure 30. Reset Timing**

**Figure 31. KBI Pulse Width**

### 3.9.2 TPM/MTIM Module Timing

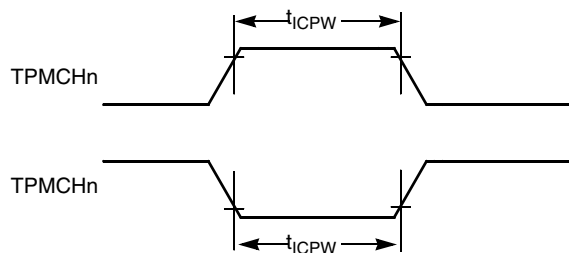
Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table 11. TPM Input Timing**

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	$f_{TPMext}$	DC	$f_{Bus}/4$	MHz
2	D	External clock period	$t_{TPMext}$	4	—	$t_{cyc}$
3	D	External clock high time	$t_{clkh}$	1.5	—	$t_{cyc}$
4	D	External clock low time	$t_{clkl}$	1.5	—	$t_{cyc}$
5	D	Input capture pulse width	$t_{ICPW}$	1.5	—	$t_{cyc}$



**Figure 32. Timer External Clock**



**Figure 33. Timer Input Capture Pulse**

### 3.10 Analog Comparator (ACMP) Electrical

**Table 12. Analog Comparator Electrical Specifications**

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	$V_{DD}$	1.80	—	5.5	V
2	P	Supply current (active)	$I_{DDAC}$	—	20	35	$\mu A$
3	D	Analog input voltage <sup>1</sup>	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DD}$	V
4	C	Analog input offset voltage <sup>1</sup>	$V_{AIO}$	—	20	40	mV
5	C	Analog Comparator hysteresis <sup>1</sup>	$V_H$	3.0	9.0	15.0	mV
6	C	Analog source impedance <sup>1</sup>	$R_{AS}$	—	—	10	$k\Omega$
7	P	Analog input leakage current	$I_{ALKG}$	—	—	1.0	$\mu A$
8	C	Analog Comparator initialization delay	$t_{AINIT}$	—	—	1.0	$\mu s$

**Table 12. Analog Comparator Electrical Specifications (continued)**

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
9	P	Analog Comparator bandgap reference voltage	$V_{BG}$	1.1	1.208	1.3	V

<sup>1</sup> These data are characterized but not production tested.

### 3.11 Internal Clock Source Characteristics

**Table 13. Internal Clock Source Specifications**

Num	C	Characteristic	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	C	Average internal reference frequency — untrimmed	$f_{int\_ut}$	25	31.25	41.66	kHz
2	P	Average internal reference frequency — trimmed	$f_{int\_t}$	31.25	32.768	39.0625	kHz
3	C	DCO output frequency range — untrimmed	$f_{dco\_ut}$	12.8	16	21.33	MHz
4	P	DCO output frequency range — trimmed	$f_{dco\_t}$	16	16.77	20	MHz
5	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	0.2	% $f_{dco}$
6	C	Total deviation of trimmed DCO output frequency over voltage and temperature	$\Delta f_{dco\_t}$	—	—	2	% $f_{dco}$
7	C	FLL acquisition time <sup>2,3</sup>	$t_{acquire}$	—	—	1	ms
8	C	Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1	$t_{wakeup}$	—	100 86	—	$\mu$ s

<sup>1</sup> Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.

<sup>2</sup> This parameter is characterized and not tested on each device.

<sup>3</sup> This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

### 3.12 ADC Characteristics

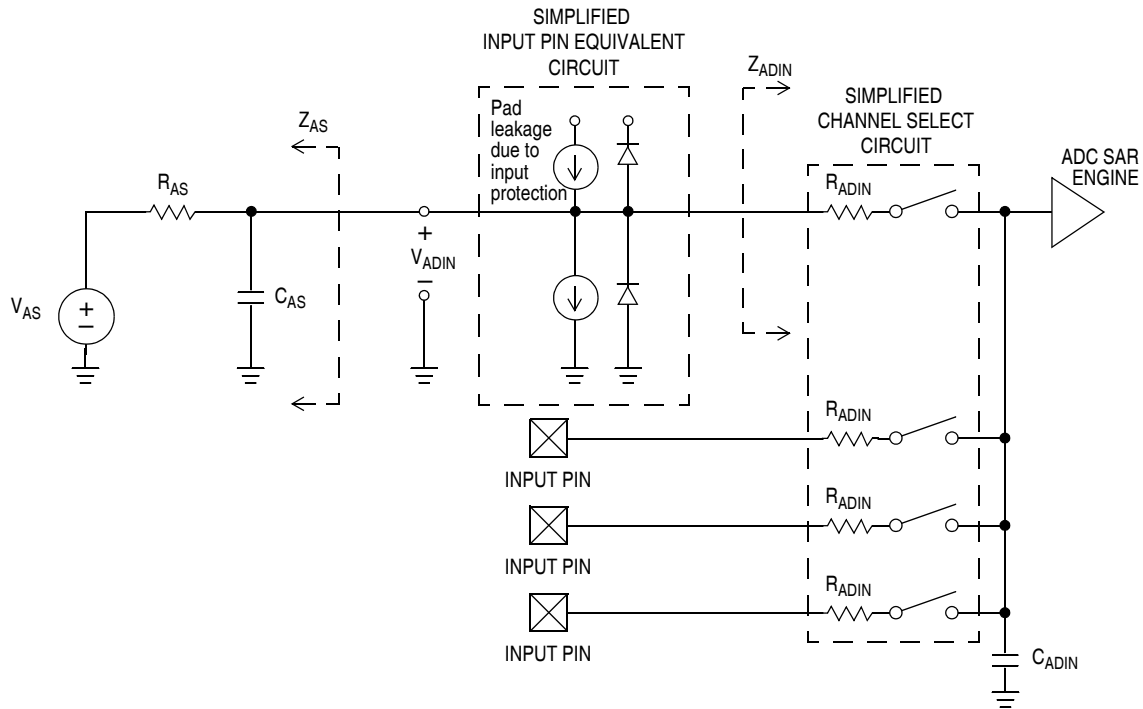
**Table 14. 10-Bit ADC Operating Conditions**

Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDAD}$	1.8	—	5.5	V	
Input voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	
Input capacitance		$C_{ADIN}$	—	4.5	5.5	pF	
Input resistance		$R_{ADIN}$	—	3	5	k $\Omega$	
Analog source resistance	10-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	$R_{AS}$	—	—	5	k $\Omega$	External to MCU
	8-bit mode (all valid $f_{ADCK}$ )		—	—	10		

**Table 14. 10-Bit ADC Operating Conditions (continued)**

Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
ADC conversion clock Freq.	High speed (ADLPC=0)	$f_{ADCK}$	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

<sup>1</sup> Typical values assume  $V_{DDAD} = 5.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.



**Figure 34. ADC Input Impedance Equivalency Diagram**

**Table 15. 10-Bit ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ ,  $2.7$  V <  $V_{DDAD} < 5.5$  V)**

C	Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		$I_{DDAD}$	—	133	—	$\mu$ A	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		$I_{DDAD}$	—	218	—	$\mu$ A	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		$I_{DDAD}$	—	327	—	$\mu$ A	



**Table 15. 10-Bit ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ ,  $2.7\text{ V} < V_{DDAD} < 5.5\text{ V}$ )**

C	Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
C	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		$I_{DDAD}$	—	0.582	1	mA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	$f_{ADACK}$	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	$t_{ADC}$	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	$t_{ADS}$	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	$E_{TUE}$	—	$\pm 1.5$	$\pm 3.5$	LSB <sup>2</sup>	Includes quantization
		8-bit mode		—	$\pm 0.7$	$\pm 1.5$		
T	Differential Non-Linearity	10-bit mode	DNL	—	$\pm 0.5$	$\pm 1.0$	LSB <sup>2</sup>	
		8-bit mode		—	$\pm 0.3$	$\pm 0.5$		
Monotonicity and No-Missing-Codes guaranteed								
C	Integral Non-Linearity	10-bit mode	INL	—	$\pm 0.5$	$\pm 1.0$	LSB <sup>2</sup>	
		8-bit mode		—	$\pm 0.3$	$\pm 0.5$		
P	Zero-Scale Error	10-bit mode	$E_{ZS}$	—	$\pm 1.5$	$\pm 2.5$	LSB <sup>2</sup>	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	$\pm 0.5$	$\pm 0.7$		
P	Full-Scale Error	10-bit mode	$E_{FS}$	—	$\pm 1$	$\pm 1.5$	LSB <sup>2</sup>	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	$\pm 0.5$	$\pm 0.5$		
D	Quantization Error	10-bit mode	$E_Q$	—	—	$\pm 0.5$	LSB <sup>2</sup>	
		8-bit mode		—	—	$\pm 0.5$		
D	Input Leakage Error	10-bit mode	$E_{IL}$	—	$\pm 0.2$	$\pm 2.5$	LSB <sup>2</sup>	Pad leakage <sup>2*</sup> $R_{AS}$
		8-bit mode		—	$\pm 0.1$	$\pm 1$		

<sup>1</sup> Typical values assume  $V_{DDAD} = 5.0\text{ V}$ ,  $\text{Temp} = 25\text{ }^\circ\text{C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> Based on input pad leakage current. Refer to pad electricals.

**Table 16. 10-Bit ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ ,  $1.8\text{ V} < V_{DDAD} < 2.7\text{ V}$ )**

C	Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	8-bit mode	$I_{DDAD}$	—	88	—	$\mu\text{A}$	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	8-bit mode	$I_{DDAD}$	—	152	—	$\mu\text{A}$	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	8-bit mode	$I_{DDAD}$	—	214	—	$\mu\text{A}$	
T	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	8-bit mode	$I_{DDAD}$	—	390	—	$\mu\text{A}$	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	$f_{ADACK}$	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	$t_{ADC}$	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	$t_{ADS}$	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	$E_{TUE}$	—	—	—	LSB <sup>2</sup>	Includes quantization
		8-bit mode		—	$\pm 3.5$	—		
T	Differential Non-Linearity	10-bit mode	DNL	—	—	—	LSB <sup>2</sup>	
		8-bit mode		—	$\pm 1.0$	—		
Monotonicity and No-Missing-Codes guaranteed								
C	Integral Non-Linearity	10-bit mode	INL	—	—	—	LSB <sup>2</sup>	
		8-bit mode		—	$\pm 1.5$	—		
C	Zero-Scale Error	10-bit mode	$E_{ZS}$	—	—	—	LSB <sup>2</sup>	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	$\pm 1.5$	—		
C	Full-Scale Error	10-bit mode	$E_{FS}$	—	—	—	LSB <sup>2</sup>	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	$\pm 1.0$	—		
D	Quantization Error	10-bit mode	$E_Q$	—	—	—	LSB <sup>2</sup>	
		8-bit mode		—	—	$\pm 0.5$		

**Table 16. 10-Bit ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ ,  $1.8\text{ V} < V_{DDAD} < 2.7\text{ V}$ )**

C	Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
D	Input Leakage Error	10-bit mode	$E_{IL}$	—	—	—	LSB <sup>2</sup>	Pad leakage <sup>2*</sup> $R_{AS}$
		8-bit mode		—	±0.1	±1		

<sup>1</sup> Typical values assume  $V_{DDAD} = 1.8\text{ V}$ ,  $\text{Temp} = 25\text{ °C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> Based on input pad leakage current. Refer to pad electricals.

### 3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

**Table 17. Flash Characteristics**

No.	C	Characteristic	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	D	Supply voltage for program/erase	$V_{DD}$	2.7	—	5.5	V
2	D	Program/Erase voltage	$V_{PP}$	11.8	12	12.2	V
3	C	VPP current	$I_{VPP\_prog}$ $I_{VPP\_erase}$	—	—	200	μA
		Program Mass erase		—	—	100	μA
4	D	Supply voltage for read operation $0 < f_{Bus} < 10\text{ MHz}$	$V_{Read}$	1.8	—	5.5	V
5	P	Byte program time	$t_{prog}$	20	—	40	μs
6	P	Mass erase time	$t_{me}$	500	—	—	ms
7	C	Cumulative program HV time <sup>2</sup>	$t_{hv}$	—	—	8	ms
8	C	Total cumulative HV time (total of $t_{me}$ & $t_{hv}$ applied to device)	$t_{hv\_total}$	—	—	2	hours
9	D	HVEN to program setup time	$t_{pgs}$	10	—	—	μs
10	D	PGM/MASS to HVEN setup time	$t_{nvs}$	5	—	—	μs
11	D	HVEN hold time for PGM	$t_{nvh}$	5	—	—	μs
12	D	HVEN hold time for MASS	$t_{nvh1}$	100	—	—	μs
13	D	$V_{PP}$ to PGM/MASS setup time	$t_{vps}$	20	—	—	ns
14	D	HVEN to $V_{PP}$ hold time	$t_{vph}$	20	—	—	ns
15	D	$V_{PP}$ rise time <sup>3</sup>	$t_{vrs}$	200	—	—	ns
16	D	Recovery time	$t_{rcv}$	1	—	—	μs
17	D	Program/erase endurance $T_L$ to $T_H = -40\text{ °C}$ to $85\text{ °C}$	—	1000	—	—	cycles
18	C	Data retention	$t_{D\_ret}$	15	—	—	years

<sup>1</sup> Typicals are measured at  $25\text{ °C}$ .

<sup>2</sup>  $t_{hv}$  is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

<sup>3</sup> Fast  $V_{PP}$  rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the  $V_{PP}$  power source is recommended. An example  $V_{PP}$  filter is shown in [Figure 35](#).

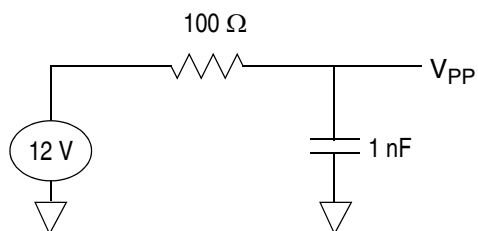
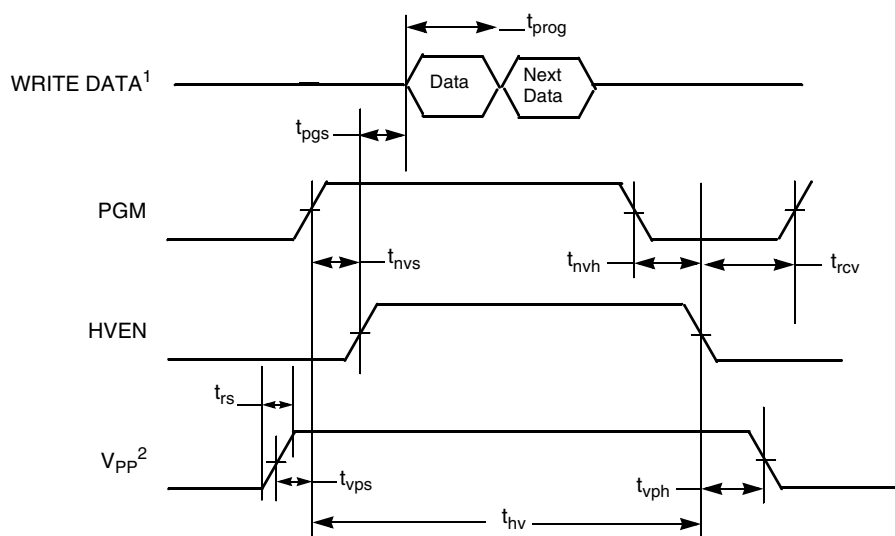
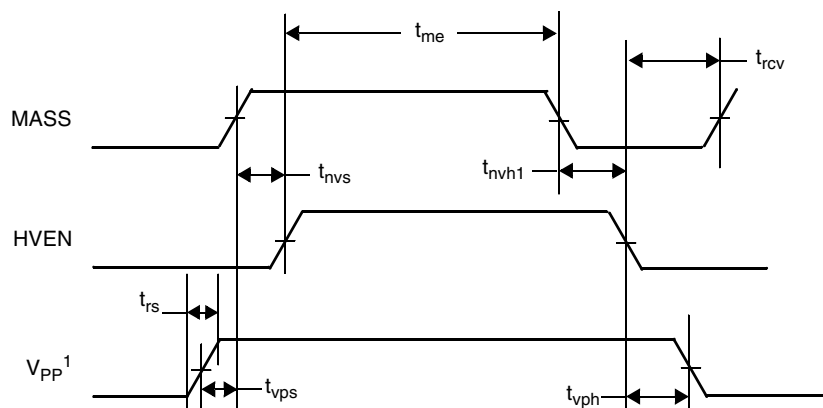


Figure 35. Example V<sub>PP</sub> Filtering



- <sup>1</sup> Next Data applies if programming multiple bytes in a single row, refer to *MC9RS08KB12 Series Reference Manual*.
- <sup>2</sup> V<sub>DD</sub> must be at a valid operating voltage before voltage is applied or removed from the V<sub>PP</sub> pin.

Figure 36. Flash Program Timing



- <sup>1</sup> V<sub>DD</sub> must be at a valid operating voltage before voltage is applied or removed from the V<sub>PP</sub> pin.

Figure 37. Flash Mass Erase Timing

## **3.14 EMC Performance**

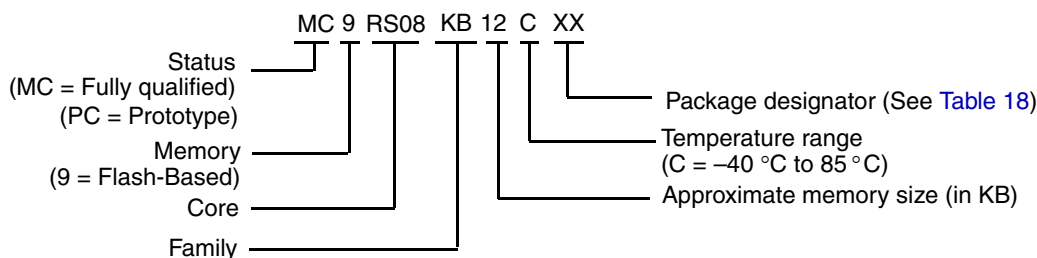
Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

### **3.14.1 Radiated Emissions**

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

## 4 Ordering Information

This section contains ordering numbers for MC9RS08KB12 series devices. See below for an example of the device numbering system.



## 5 Package Information and Mechanical Drawings

Table 18 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9RS08KB12 Series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in Table 18, or
- Open a browser to the Freescale® website (<http://www.freescale.com>), and enter the appropriate document number (from Table 18) in the “Enter Keyword” search box at the top of the page.

**Table 18. Device Numbering System**

Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
<b>MC9RS08KB12</b> <b>MC9RS08KB8</b> <b>MC9RS08KB4</b>	12 KB	254 bytes	24 QFN	FK	<a href="#">98ASA00087D</a>
	8 KB	254 bytes	20 SOIC WB	WJ	<a href="#">98ASB42343B</a>
	4 KB	126 bytes	16 SOIC NB	SG	<a href="#">98ASB42566B</a>
			16 TSSOP	TG	<a href="#">98ASH70247A</a>
<b>MC9RS08KB2</b>	2 KB	126 bytes	8 SOIC NB	SC	<a href="#">98ASB42564B</a>
			8 DFN	DC	<a href="#">98ARL10557D</a>

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