3 A, 61 V monolithic current source with dimming capability

Datasheet - production data

HTSSOP16 (R_{TH} = 40 °C)

Features

- Up to 3 A DC output current
- 4.5 V to 61 V operating input voltage
- $R_{DS,ON}$ = 250 mΩ typ.
- Adjustable f_{SW} (250 kHz - 1.5 MHz)
- Dimming function with dedicated pin
- Low I_Q shutdown (10 µA typ. from VIN)
- Low I_Q operating (2.4 mA typ.)
- ± 3% output current accuracy
- Synchronization
- Enable with dedicated pin
- Adjustable soft-start time
- Adjustable current limitation
- Low dropout operation (12 µs max.)
- VBIAS improves efficiency at light-load
- Output voltage sequencing
- Auto recovery thermal shutdown
- MLCC output capacitor

Applications

- HB LED driving applications
- Halogen bulb replacement

Description

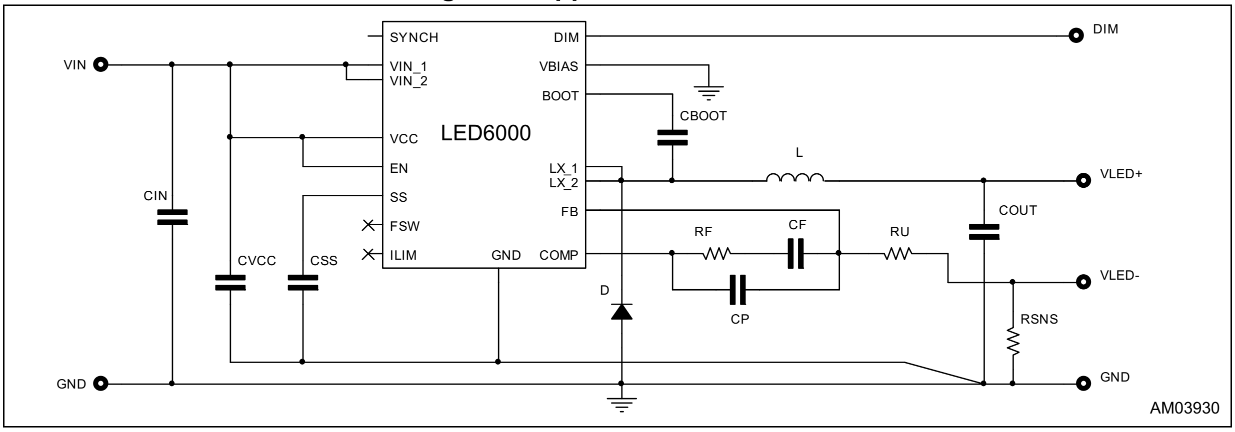
The LED6000 is a step-down monolithic switching regulator designed to source up to 3 A DC current for high power LED driving. The 250 mV typical RSENSE voltage drop enhances the efficiency. Digital dimming is implemented by driving the dedicated DIM pin.

The adjustable current limitation, designed to select the inductor RMS in accordance with the nominal output LED current, and the adjustability of the switching frequency allow the size of the application to be compact. The embedded switchover feature on the VBIAS pin maximizes efficiency. Multiple devices can be synchronized by sharing the SYNCH pin to prevent beating noise in low-noise applications, and to reduce the input current RMS value.

The device is fully protected against overheating, overcurrent and output short-circuit.

The LED6000 is available in an HTSSOP16 exposed pad package.

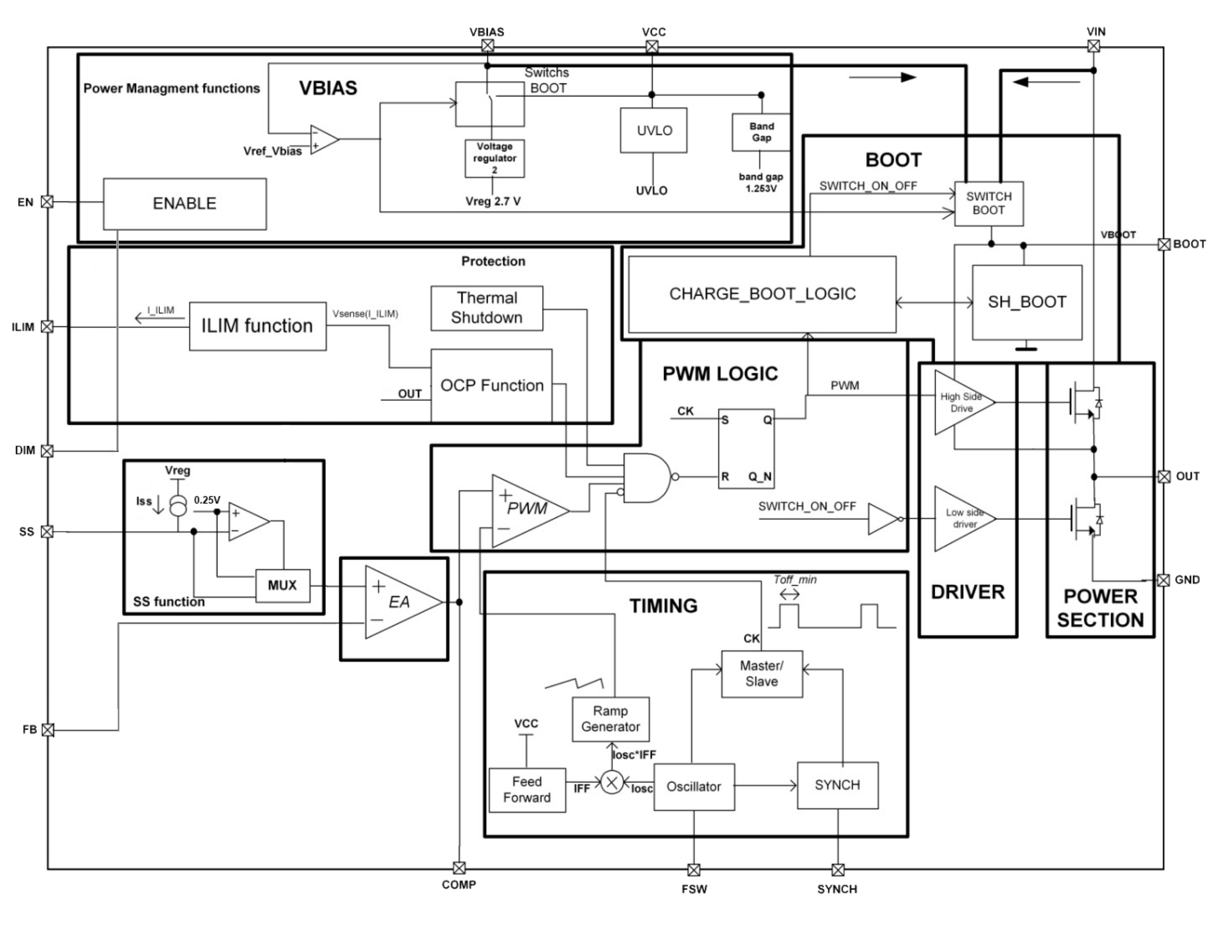
Figure 1. Application schematic



Contents

1 Block diagram

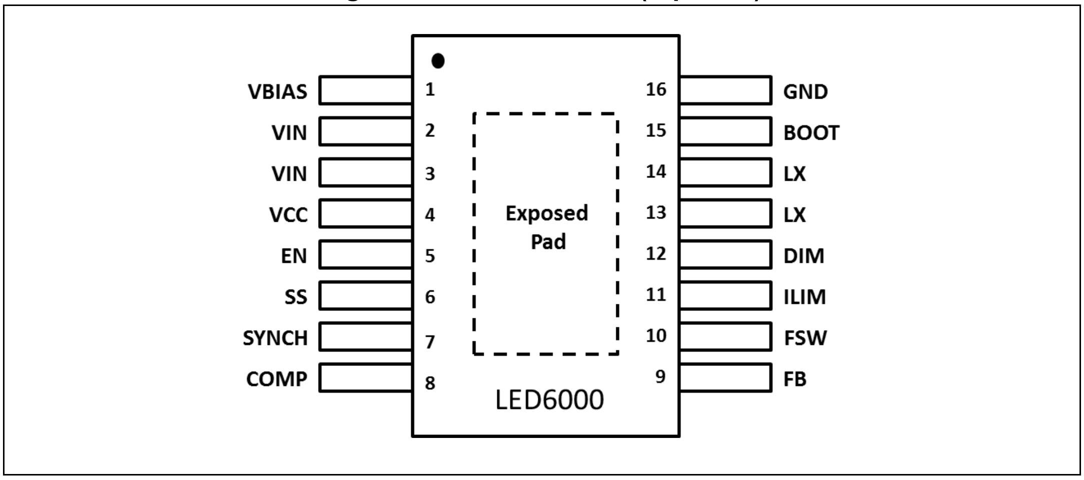
Figure 2. Block diagram



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top view)



2.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	VBIAS	Auxiliary input that can be used to supply a part of the analog circuitry to increase the efficiency at the light-load. Connect to GND if not used or bypass with a 1 µF ceramic capacitor if supplied by an auxiliary rail.
2	VIN	DC input voltage
3	VIN	DC input voltage
4	VCC	Filtered DC input voltage to the internal circuitry. Bypass to the signal GND by a 1 µF ceramic capacitor.
5	EN	Active high enable pin. Connect to the VCC pin if not used.
6	SS	An internal current generator (5 µA typ.) charges the external capacitor to implement the soft-start.
7	SYNCH	Master / slave synchronization
8	COMP	Output of the error amplifier. The designed compensation network is connected at this pin.
9	FB	Inverting input of the error amplifier
10	FSW	A pull-down resistor to GND selects the switching frequency.
11	ILIM	A pull-down resistor to GND selects the peak current limitation.
12	DIM	A PWM signal in this input pin implements the LED PWM current dimming. It's pulled-down by an internal 2 µA current.
13	LX	Switching node
14	LX	Switching node
15	BOOT	Connect an external capacitor (100 nF typ.) between BOOT and LX pins. The gate charge required to drive the internal n-DMOS is recovered by an internal regulator during the off-time.
16	GND	Signal GND
--	E. P.	The exposed pad must be connected to the signal GND.

2.3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
VIN		-0.3	61	V
VCC		-0.3	61	V
BOOT	V_{BOOT} - GND	-0.3	65	V
	V_{BOOT} - V_{LX}	-0.3	4	V
VBIAS		-0.3	VCC	V
EN		-0.3	VCC	V
DIM		-0.3	VCC	V
LX		-0.3	VIN + 0.3	V
SYNCH		-0.3	5.5	V
SS		-0.3	3.6	V
FSW		-0.3	3.6	V
COMP		-0.3	3.6	V
ILIM		-0.3	3.6	V
FB		-0.3	3.6	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	°C
I_{HS}	High-side RMS current		3	A

2.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction ambient (device soldered on the STMicroelectronics® demonstration board)	40	°C/W

2.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	KV
	CDM	500	V

3 Electrical characteristics

All the population tested at T_J = 25 °C, V_{IN} = V_{CC} = 24 V, VBIAS = GND, V_{DIM} = V_{EN} = 3 V and R_{ILIM} = N. M. unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		(1)	4.5		61	V
$R_{DSON\ HS}$	High-side RDSON	I_{LX} = 0.5 A			0.25	0.32	Ω
		I_{LX} = 0.5 A	(1)		0.25	0.42	Ω
f_{SW}	Switching frequency	FSW pin floating;		233	250	267	kHz
		FSW pin floating	(1)	225	250	275	kHz
	Selected switching frequency	R_{FSW} = 10 kΩ		1350	1500	1650	kHz
I_{PK}	Peak current limit	ILIM pin floating; V_{FB} = 0.2 V	(2)	3.5	4.1	4.7	A
	Selected peak current limit	R_{ILIM} = 100 kΩ; V_{FB} = 0.2 V	(2)	0.68	0.85	1.01	A
I_{SKIP}	Pulse skipping peak current	ILIM pin floating	(2)		0.40		A
		R_{ILIM} = 100 kΩ	(2)		0.15		A
T_{ONMIN}	Minimum on-time				120	150	ns
T_{ONMAX}	Maximum on-time	Refer to *Section 4: Functional description* for T_{ONMAX} details.			12		µs
T_{OFFMIN}	Minimum off-time		(3)		360		ns
VCC / VBIAS							
V_{CCH}	VCC UVLO rising threshold		(1)	3.85	4.10	4.30	V
V_{CCHYST}	VCC UVLO hysteresis		(1)	160	250	340	mV
SWO	VBIAS threshold	Switch internal supply from V_{CC} to V_{BIAS}. V_{BIAS} ramping up from 0 V.	(1)	2.82	2.90	2.98	V
		Hysteresis	(3)		80		mV
	VCC -VBIAS threshold	Switch internal supply from V_{CC} to V_{BIAS}. V_{IN} = V_{CC} = 24 V, V_{BIAS} falling from 24 V to GND.	(1)	3.35	4.05	4.90	V
		Hysteresis	(3)		750		mV
Power consumption							
I_{SHTDWN}	Shutdown current from VIN	V_{EN} = GND			10	15	µA
I_{QUIESC}	Quiescent current from VIN and VCC	LX floating, V_{FB} = 1 V, VBIAS = GND, FSW floating.			2.4	3.4	mA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
I_{QOPVIN}	Quiescent current from VIN and VCC	LX floating, V_{FB} = 1 V, VBIAS = 3.3 V, FSW floating			0.9	1.4	mA
$I_{QOPVBIAS}$	Quiescent current from VBIAS				1.5	2.4	mA
Enable							
V_{ENL}	Device OFF level			0.06		0.30	V
V_{ENH}	Device ON level			0.35		0.90	V
Soft-start							
$T_{SSSETUP}$	Soft-start setup time	Delay from UVLO rising to switching activity	(3)		640		µs
I_{SSCH}	C_{SS} charging current	V_{SS} = GND		4.3	5.0	5.7	µA
Error amplifier							
V_{FB}	Voltage feedback			0.242	0.250	0.258	V
			(1)	0.240	0.250	0.260	V
V_{COMPH}		V_{FB} = GND; V_{SS} = 3.2 V		3.20	3.35	3.50	V
V_{COMPL}		V_{FB} = 3.2 V; V_{SS} = 3.2 V				0.1	V
I_{FB}	FB biasing current	V_{FB} = 3.6 V			5	50	nA
$I_{OSOURCE}$		V_{FB} = GND; SS pin floating; V_{COMP} = 2 V	(3)		3.1		mA
I_{OSINK}	Output stage sinking capability	Unity gain buffer configuration (FB connected to COMP). No load on COMP pin.	(3)		5		mA
A_{V0}	Error amplifier gain		(3)		100		dB
GBWP		Unity gain buffer configuration (FB connected to COMP). No load on COMP pin.	(3)		23		MHz
Synchronization (fan out: 5 slave devices max.)							
$f_{SYN\ MIN}$	Synchronization frequency	Pin FSW floating		280			kHz
V_{SYNOUT}	Master output amplitude	I_{LOAD} = 4 mA		2.45			V
		I_{LOAD} = 0 A; pin SYNCH floating				3.8	
V_{SYNOW}	Output pulse width	I_{LOAD} = 0 A; pin SYNCH floating		150	215	280	ns
V_{SYNIH}	SYNCH slave high level input threshold			2.0			V
V_{SYNIL}	SYNCH slave low level input threshold					1.0	
I_{SYN}	Slave SYNCH pull-down current	V_{SYNCH} = 5 V		450	700	950	µA
V_{SYNIW}	Input pulse width			150			ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Dimming						
V_{DIMH}	DIM rising threshold			1.23	1.7	V
V_{DIML}	DIM falling threshold		0.75	1.00		V
V_{DIMPD}	DIM pull-down current	V_{DIM} = 2 V	0.5	1.5	2.5	µA
T_{DIMTO}	Dimming timeout	[3]		42		ms
Thermal shutdown						
T_{SHDWN}	Thermal shutdown temperature	[3]		170		°C
T_{HYS}	Thermal shutdown hysteresis	[3]		15		°C

1. Specifications referred to T_J from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
3. Not tested in production.

4 Functional description

The LED6000 device is based on a voltage mode, constant frequency control loop. The LEDs current, monitored through the voltage drop on the external current sensing resistor, RSNS, is compared to an internal reference (0.25 V) providing an error signal on the COMP pin. The COMP voltage level is then compared to a fixed frequency sawtooth ramp, which finally controls the on- and off-time of the power switch.

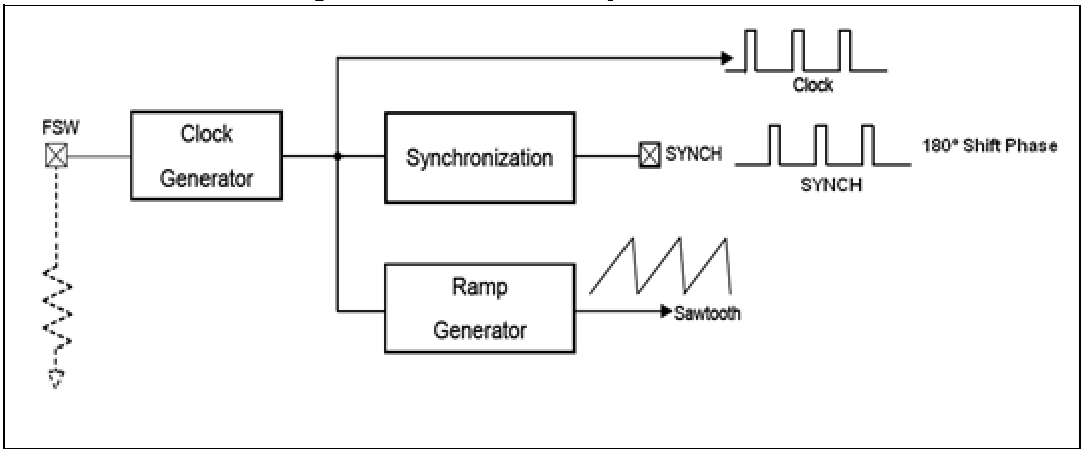
The main internal blocks are shown in *Figure 2: Block diagram on page 4* and can be summarized as follow.

- The fully integrated oscillator that provides the sawtooth ramp to modulate the duty cycle and the synchronization signal. Its switching frequency can be adjusted by an external resistor. The input voltage feedforward is implemented.
- The soft-start circuitry to limit the inrush current during the startup phase.
- The voltage mode error amplifier.
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switch.
- The high-side driver for the embedded N-channel power MOSFET switch and bootstrap circuitry. A dedicated high resistance low-side MOSFET, for anti-boot discharge management purposes, is also present.
- The peak current limit sensing block, with a programmable threshold, to handle the overload including a thermal shutdown block, to prevent the thermal runaway.
- The bias circuitry, which includes a voltage regulator and an internal reference, to supply the internal circuitry and provide a fixed internal reference and manages the current dimming feature. The switchover function from VCC to VBIAS can be implemented for higher efficiency. This block also implements voltage monitor circuitry (UVLO) that checks the input and internal voltages.

4.1 Oscillator and synchronization

Figure 4 shows the block diagram of the oscillator circuit. The internal oscillator provides a constant frequency clock, whose frequency depends on the resistor externally connected between the FSW pin and ground.

Figure 4. Oscillator and synchronization

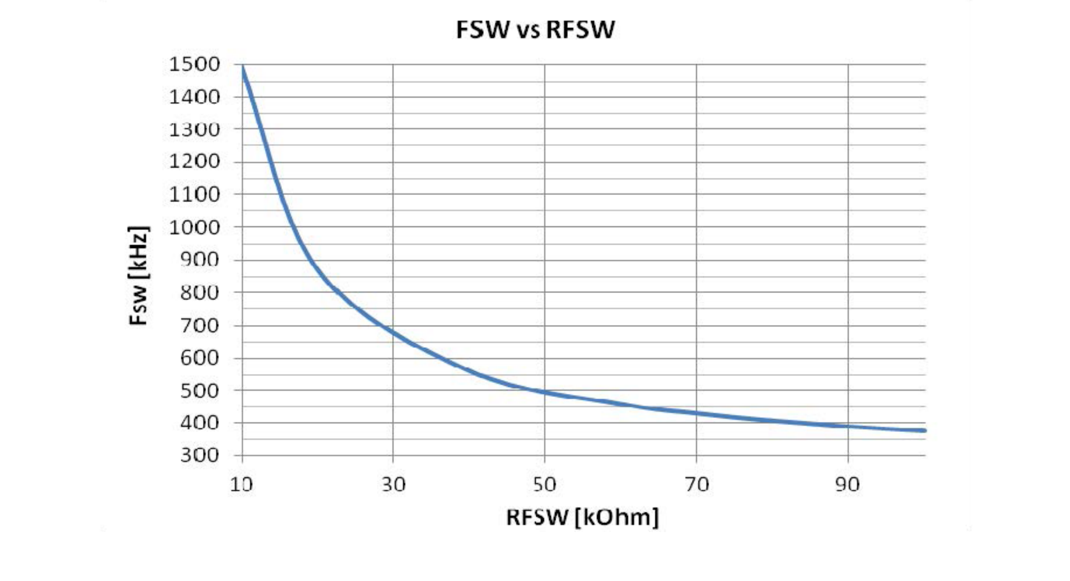


If the FSW pin is left floating, the programmed frequency is 250 kHz (typ.); if the FSW pin is connected to an external resistor, the programmed switching frequency can be increased up to 1.5 MHz, as shown in *Figure 5*. The required R_{FSW} value (expressed in kΩ) is estimated by *Equation 1*:

Equation 1

$$F_{SW} = 250kHz + \frac{12500}{R_{FSW}}$$

Figure 5. Switching frequency programmability



To improve the line transient performance, keeping the PWM gain constant versus the input voltage, the input voltage feedforward is implemented by changing the slope of the sawtooth ramp, according to the input voltage change (*Figure 6* a).

The slope of the sawtooth also changes if the oscillator frequency is programmed by the external resistor. In this way a frequency feedforward is implemented (*Figure 6* b) in order to keep the PWM modulator gain constant versus the switching frequency.

On the SYNCH pin the synchronization signal is generated. This signal has a phase shift of 180° with respect to the clock. This delay is useful when two devices are synchronized connecting the SYNCH pins together. When SYNCH pins are connected, the device with a higher oscillator frequency works as a master, so the slave device switches at the frequency of the master but with a delay of half a period. This helps reducing the RMS current flowing through the input capacitor. Up to five LED6000s can be connected to the same SYNCH pin; however, the clock phase shift from master switching frequency to the slave input clock is 180°.

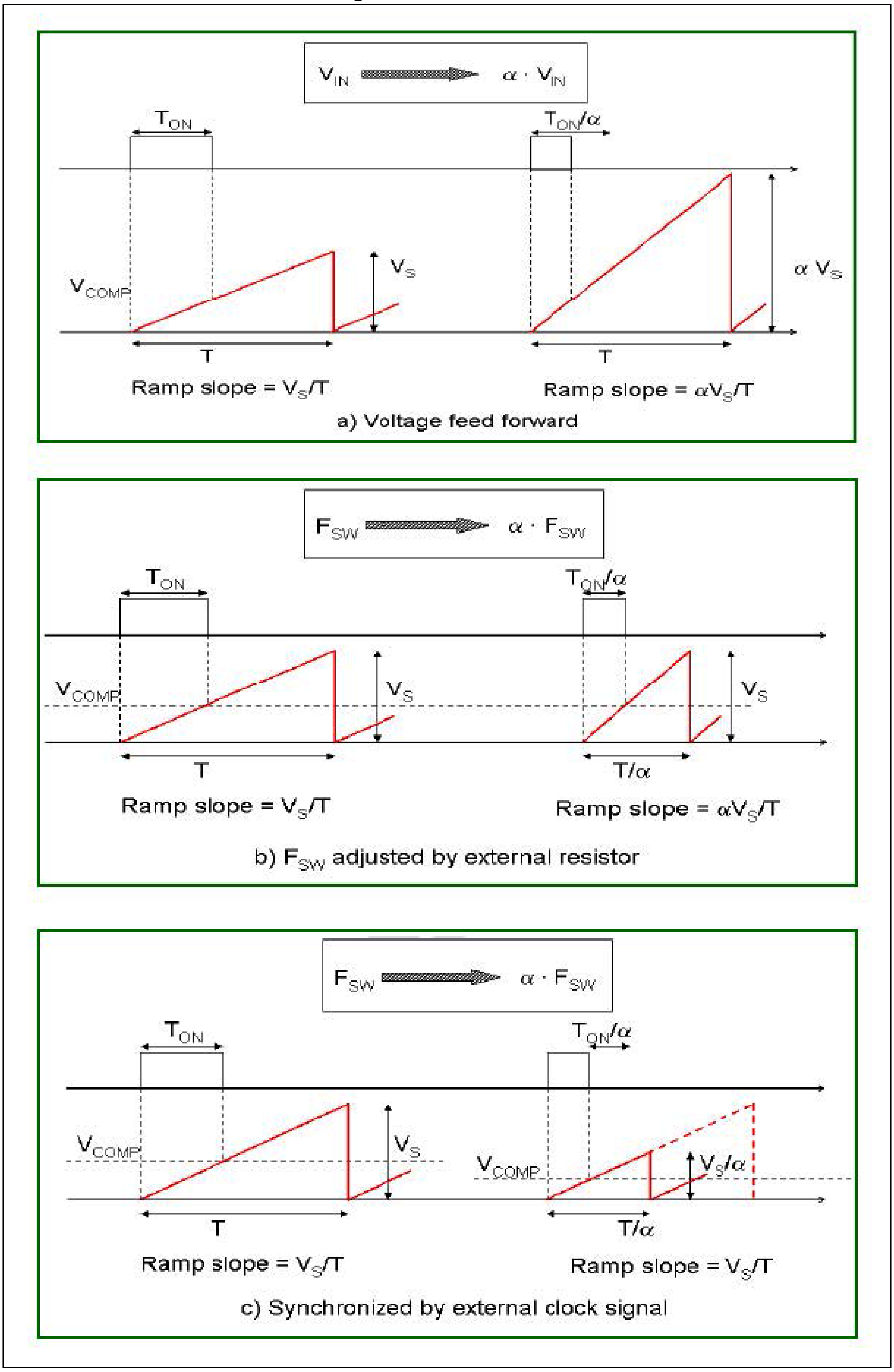
The LED6000 device can be synchronized to work at a higher frequency, in the range of 250 kHz - 1500 kHz, providing an external clock signal on the SYNCH pin. The synchronization changes the sawtooth amplitude, also affecting the PWM gain (*Figure 6* c). This change must be taken into account when the loop stability is studied. In order to minimize the change of the PWM gain, the free-running frequency should be set (with a resistor on the FSW pin) only slightly lower than the external clock frequency.

This pre-adjusting of the slave IC switching frequency keeps the truncation of the ramp sawtooth negligible.

In case two or more (up to five) LED6000 SYNCH pins are tied together, the LED6000 IC with higher programmed switching frequency is typically the master device; however, the SYNCH circuit is also able to synchronize with a slightly lower external frequency, so the frequency pre-adjustment with the same resistor on the FSW pin, as suggested above, is required for a proper operation.

The SYNCH signal is provided as soon as EN is asserted high; however, if DIM is kept low for more than T_{DIMTO} timeout, the SYNCH signal is no more available until DIM re-assertion high.

Figure 6. Feedforward

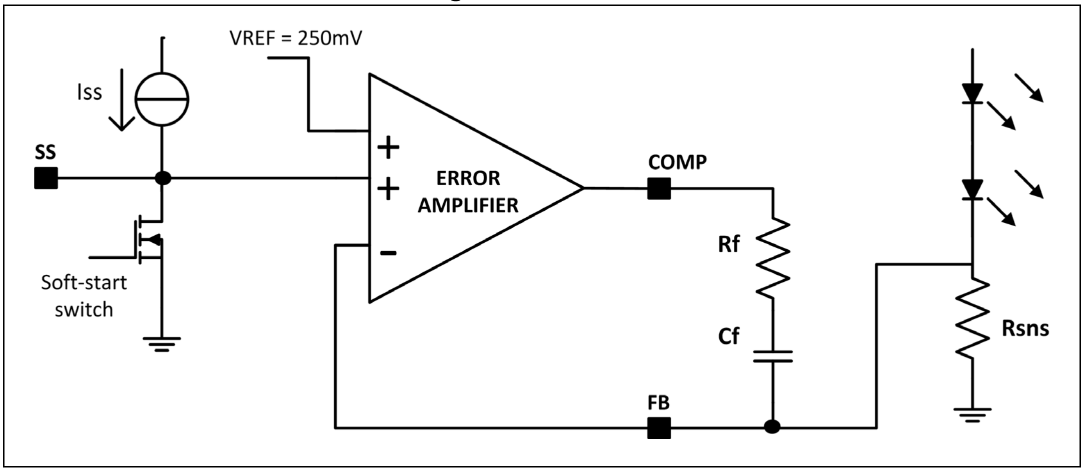


4.2 Soft-start

The soft-start is essential to assure a correct and safe startup of the step-down converter. It avoids an inrush current surge and makes the output voltage to increase monotonically.

The soft-start is performed as soon as the EN and DIM pin are asserted high; when this occurs, an external capacitor, connected between the SS pin and ground, is charged by a constant current (5 µA typ.). The SS voltage is used as reference of the switching regulator and the output voltage of the converter tracks the ramp of the SS voltage. When the SS pin voltage reaches the 0.25 V level, the error amplifier switches to the internal 0.25 V reference to regulate the output voltage.

Figure 7. Soft-start



During the soft-start period the current limit is set to the nominal value.

The dV_{SS}/dt slope is programmed in agreement with *Equation 2*:

Equation 2

$$C_{SS} = \frac{I_{SS} \cdot T_{SS}}{V_{REF}} = \frac{5\mu A \cdot T_{SS}}{0.25V}$$

Before starting the C_{SS} capacitor charge, the soft-start circuitry turns-on the discharge switch shown in *Figure 7* for $T_{SSDISCH}$ minimum time, in order to completely discharge the C_{SS} capacitor.

As a consequence, the maximum value for the soft-start capacitor, which assures an almost complete discharge in case of the EN signal toggle, is provided by:

Equation 3

$$C_{SS\_MAX} \leq \frac{T_{SSDISCH}}{5 \cdot R_{SSDISCH}} \cong 270nF$$

given $T_{SSDISCH}$ = 530 µs and $R_{SSDISCH}$ = 380 Ω typical values.

The enable feature allows to put the device into the standby mode. With the EN pin lower than V_{ENL} the device is disabled and the power consumption is reduced to 10 µA (typ.). If the EN pin is higher than V_{ENH}, the device is enabled. If the EN pin is left floating, an internal pull-down current ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also VCC compatible.

4.3 Digital dimming

The switching activity is inhibited as long as the DIM pin is kept below the V_{DIML} threshold.

When the DIM is asserted low, the HS MOS is turned-off as soon as the minimum on-time is expired and the COMP pin is parked close to the maximum ramp peak value, in order to limit the input inrush current when the IC restarts the switching activity. The internal oscillator and, consequently, the IC quiescent current are reduced only if the DIM is kept low for more than T_{DIMTO} timeout.

The inductor current dynamic performance, when dimming input goes high, depends on the designed system response. The best dimming performance is obtained by maximizing the bandwidth and phase margin, when possible.

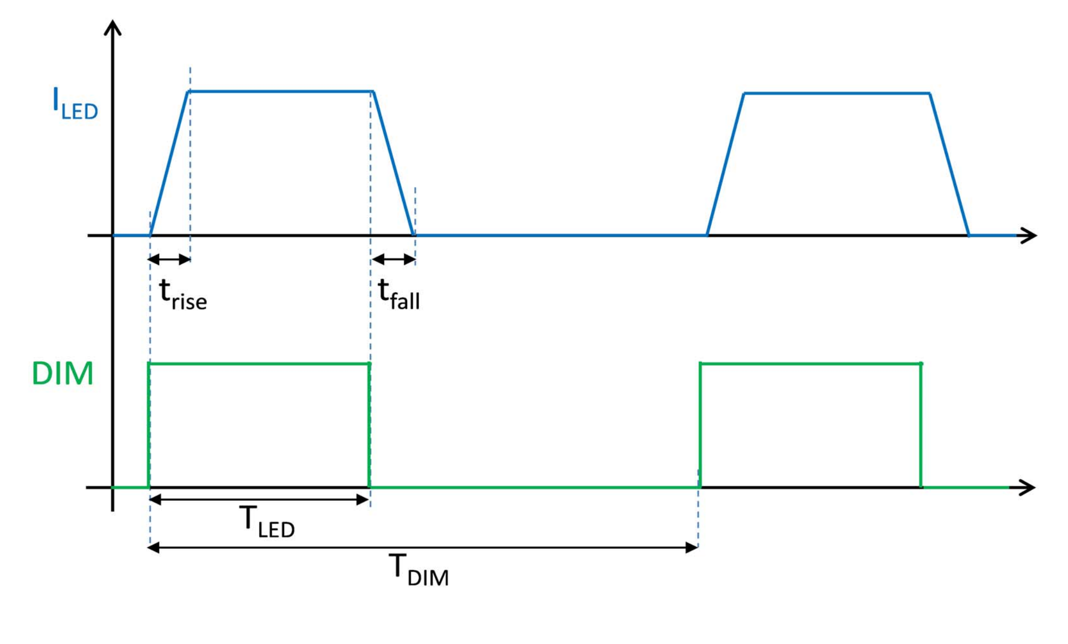
As a general rule, the output capacitor minimization improves dimming performance in terms of the shorter LEDs current rising time and reduced inductor peak current.

An oversized output capacitor value requires an extra current for the fast charge so generating an inductor current overshoot and oscillations.

Refer also to *Section 5.2 on page 25* for output capacitor design hints.

The dimming performance depends on the current pulse shape specification of the final application.

Figure 8. Dimming operation



The ideal current pulse has rectangular shape; however, in any case it degenerates into a trapezoid or, at worst, into a triangle, depending on the ratio (t_{RISE} + t_{FALL})/ T_{LED}.

Figure 9. Dimming operation (rising edge) - VIN = 44 V, 12 LED

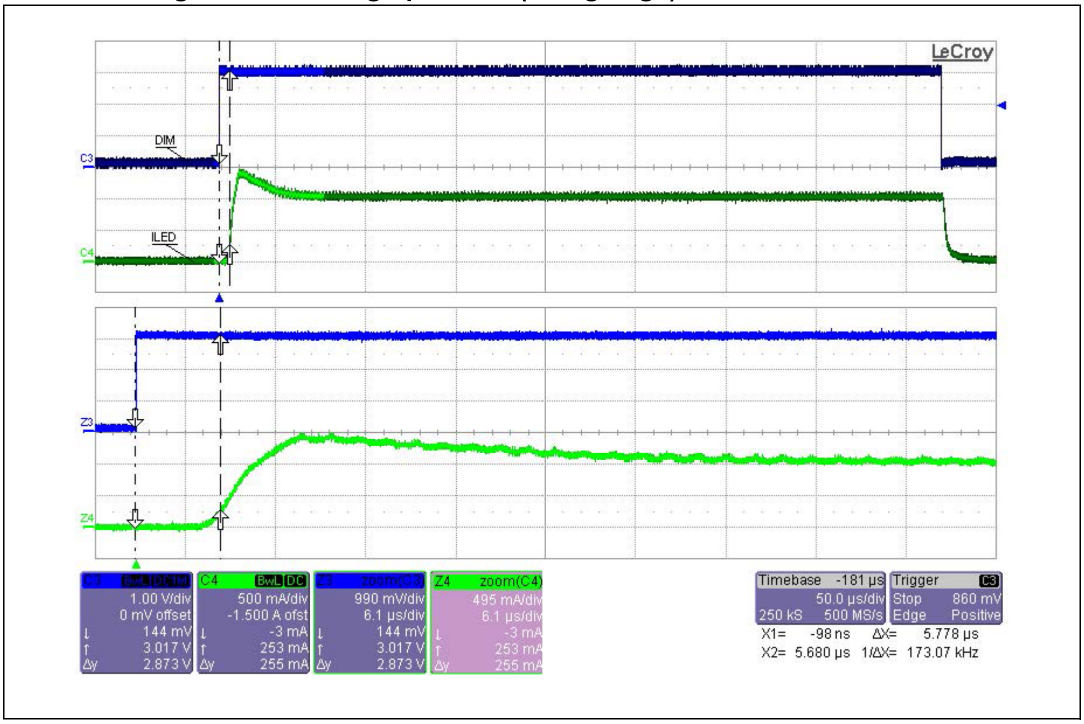
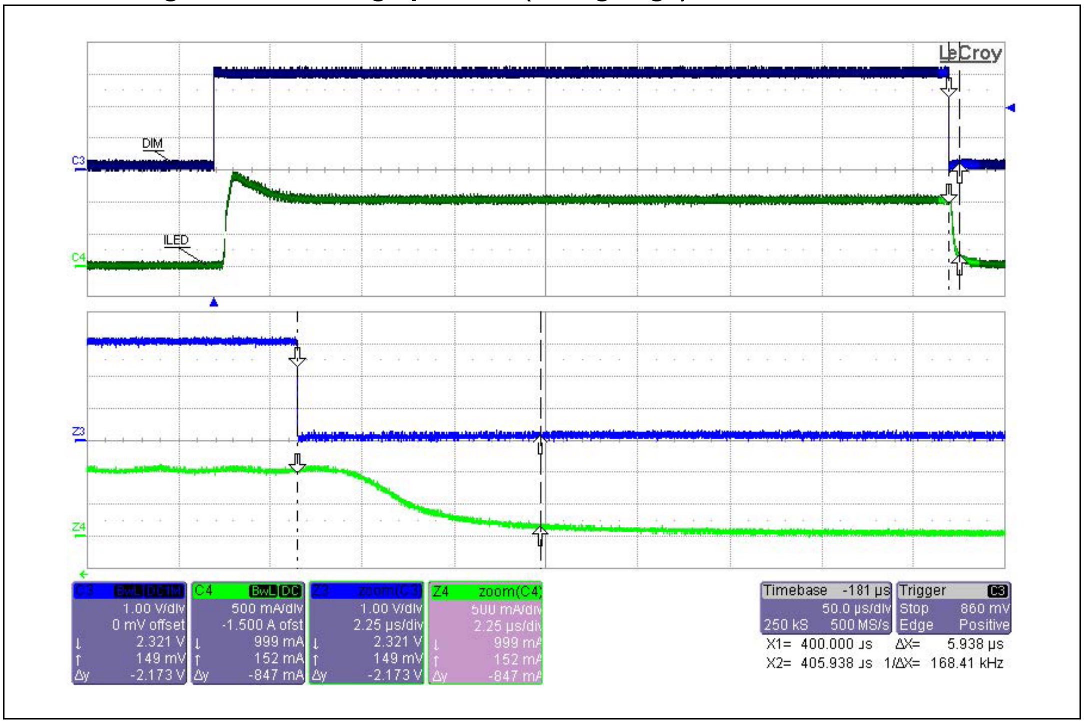
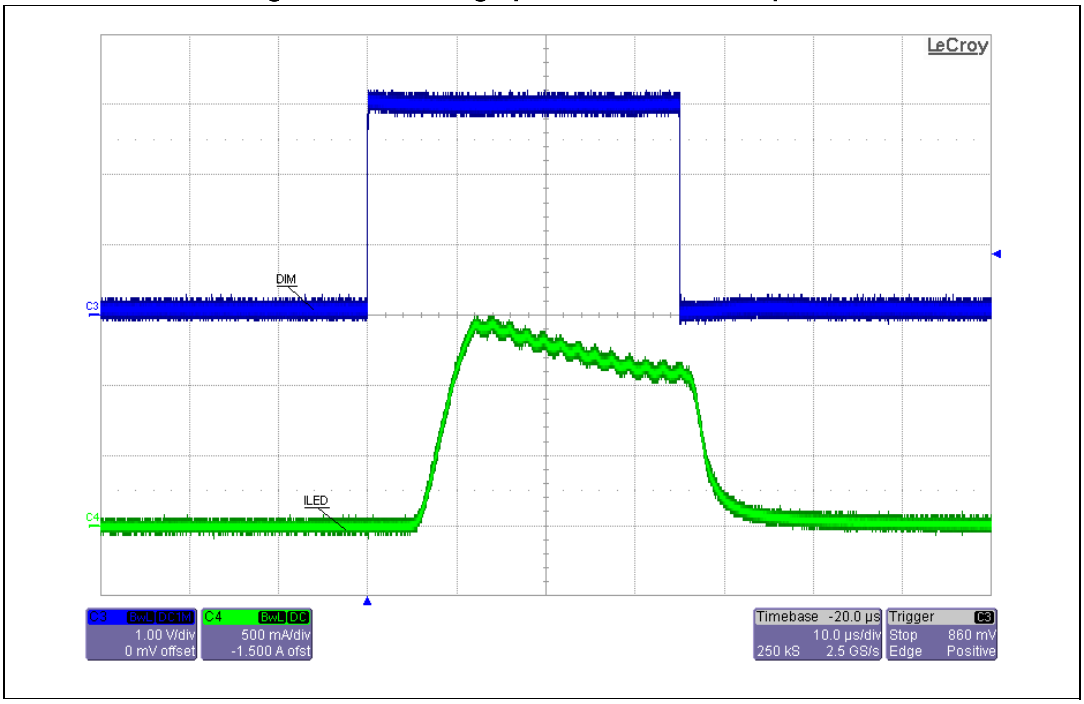


Figure 10. Dimming operation (falling edge) - VIN = 44 V, 12 LED



In *Figure 11* a very short DIM pulse is shown, measured in the standard demonstration board, V_{IN} = 44 V, 12 LEDs. The programmed LED current, 1 A, is reached at the end of the DIM pulse (35 µs).

Figure 11. Dimming operation - short DIM pulse



The above consideration is crucial when short DIM pulses are expected in the final application. Once the external power components and the compensation network are selected, a direct measurement to determine t_{RISE} and t_{FALL} is necessary to certify the achieved dimming performance.

When the DIM is forced above the V_{DIMH} threshold after T_{DIMTO} has elapsed, a new soft-start sequence is performed.

4.4 Error amplifier and light-load management

The error amplifier (E/A) provides the error signal to be compared with the sawtooth to perform the pulse width modulation. Its non-inverting input is internally connected to a 0.25 V voltage reference and its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device the error amplifier is a voltage mode operational amplifier, therefore, with the high DC gain and low output impedance.

The uncompensated error amplifier characteristics are summarized in *Table 6*.

Table 6. Error amplifier characteristics

Parameters	Value
Low frequency gain (A_0)	100 dB
GBWP	23 MHz
Output voltage swing	0 to 3.5 V
Source/sink current capability	3.1 mA / 5 mA

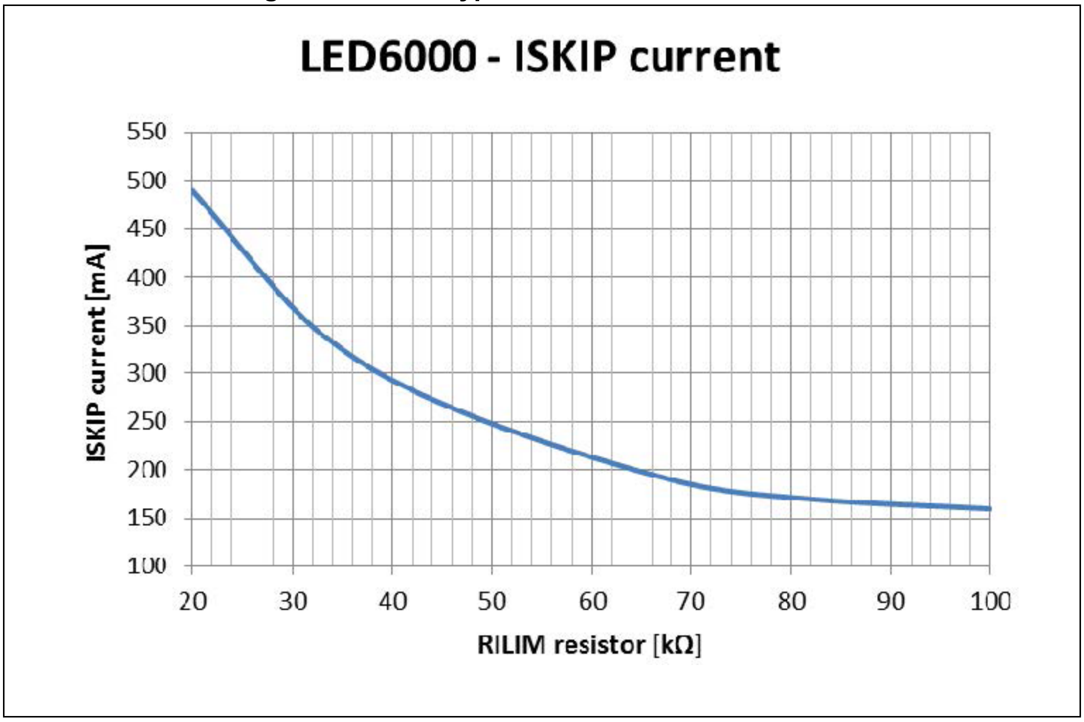
In the continuous conduction working mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different kinds of compensation networks can be used depending on the ESR value of the output capacitor.

If the zero introduced by the output capacitor helps to compensate the double pole of the LC filter, a type II compensation network can be used. Otherwise, a type III compensation network must be used (see *Section 5.3 on page 27* for details on the compensation network design).

In case of the light-load (i.e.: if the output current is lower than the half of the inductor current ripple) the LED6000 enters the pulse-skipping working mode. The HS MOS is kept off if the COMP level is below 200 mV (typ.); when this bottom level is reached the integrated switch is turned on until the inductor current reaches I_{SKIP} value. So, in the discontinuous conduction working mode (DCM), the HS MOS on-time is only related to the time necessary to charge the inductor up to the I_{SKIP} level.

The I_{SKIP} threshold is reduced with increasing the RILIM resistor value, as shown also in *Table 5 on page 8* and plotted in *Figure 12*, so allowing the LED6000 device work in the continuous conduction mode also in case lower current LEDs are selected.

Figure 12. ISKIP typical current and RILIM value



However, due to the current sensing comparator delay, the actual inductor charge current is slightly impacted by the V_{IN} and selected inductor value.

In order to let the bootstrap capacitor recharge, in case of an extremely light-load the LED6000 is able to pull-down the LX net through an integrated small LS MOS. In this way the bootstrap recharge current can flow from the V_{IN} through the C_{BOOT}, LX and LS MOS.

This mechanism is activated if the HS MOS has been kept turned-off for more than 3 ms (typ.).

4.5 Low VIN operation

In normal operation (i.e.: VOUT programmed lower than input voltage) when the HS MOS is turned off, a minimum off time (T_{OFFMIN}) interval is performed.

In case the input voltage falls close or below the programmed output voltage (low dropout, LDO) the LED6000 control loop is able to increase the duty cycle up to 100%. However, in order to keep the boot capacitor properly recharged, a maximum HS MOS on-time is limited (T_{ONMAX}). When this limit is reached the HS MOS is turned-off and an integrated switch working as a pull-down resistor between the LX and GND is turned on, until one of the following conditions is met:

- A negative current limit (300 mA typ.) is reached
- A timeout (1 µs typ.) is reached.

So doing the LED6000 device is able to work in the low dropout operation, due to the advanced boot capacitor management, and the effective maximum duty cycle is about 12 µs / 13 µs = 92%.

4.6 Overcurrent protection

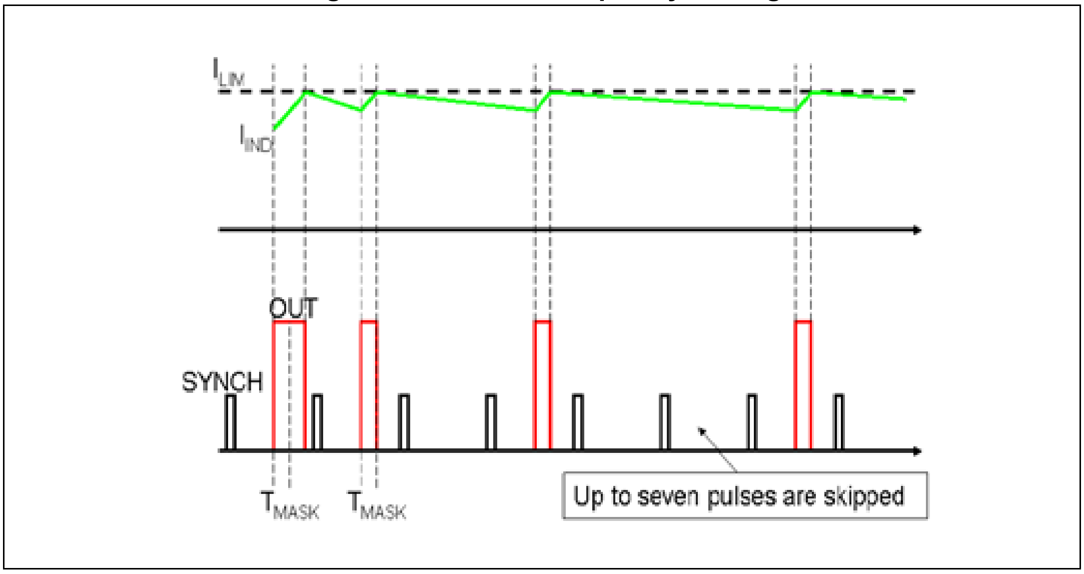
The LED6000 implements overcurrent protection by sensing the current flowing through the power MOSFET. Due to the noise created by the switching activity of the power MOSFET, the current sensing circuitry is disabled during the initial phase of the conduction time. This avoids erroneous detection of fault condition. This interval is generally known as “masking time” or “blanking time”. The masking time is about 120 ns.

If the overcurrent limit is reached, the power MOSFET is turned off implementing pulse by pulse overcurrent protection. In the overcurrent condition, the device can skip turn-on pulses in order to keep the output current constant and equal to the current limit. If, at the end of the “masking time”, the current is higher than the overcurrent threshold, the power MOSFET is turned off and one pulse is skipped. If, at the following switching on, when the “masking time” ends, the current is still higher than the overcurrent threshold, the device skips two pulses. This mechanism is repeated and the device can skip up to seven pulses (refer to *Figure 13*).

If at the end of the “masking time” the current is lower than the overcurrent threshold, the number of skipped cycles is decreased by one unit.

As a consequence, the overcurrent protection acts by turning off the power MOSFET and reducing the switching frequency down to one eighth of the default switching frequency, in order to keep constant the output current close to the current limit.

Figure 13. OCP and frequency scaling



This kind of overcurrent protection is effective if the inductor can be completely discharged during HS MOS turn-off time, in order to avoid the inductor current to run away. In case of the output short-circuit the maximum switching frequency can be computed by the following equation:

Equation 4

$$F_{SW,MAX} \le \frac{8 \cdot (V_F + R_{DCR} \cdot I_{LIM})}{V_{IN} - (R_{ON} + R_{DCR}) \cdot I_{LIM}} \cdot \frac{1}{T_{ON,MIN}}$$

Assuming V_F = 0.6 V the free-wheeling diode direct voltage, R_{DCR} = 30 mΩ inductor parasitic resistance, I_{LIM} = I_{PK} = 4 A the peak current limit, R_{ON} = 0.25 Ω HS MOS resistance and $T_{ON,MIN}$ = 120 ns minimum HS MOS on duration, the maximum F_{SW} frequency which avoids the inductor current runaway in case of the output short-circuit and VIN = 61 V is 801 kHz.

If the programmed switching frequency is higher than the above computed limit, an estimation of the inductor current in case of the output short-circuit fault is provided by *Equation 5*:

Equation 5

$$I_{LIM} = \frac{F_{SW} \cdot T_{ON} \cdot V_{IN} - 8 \cdot V_F}{8 \cdot R_{DCR} + F_{SW} \cdot T_{ON,MIN}\left(R_{ON} + R_{DCR}\right)}$$

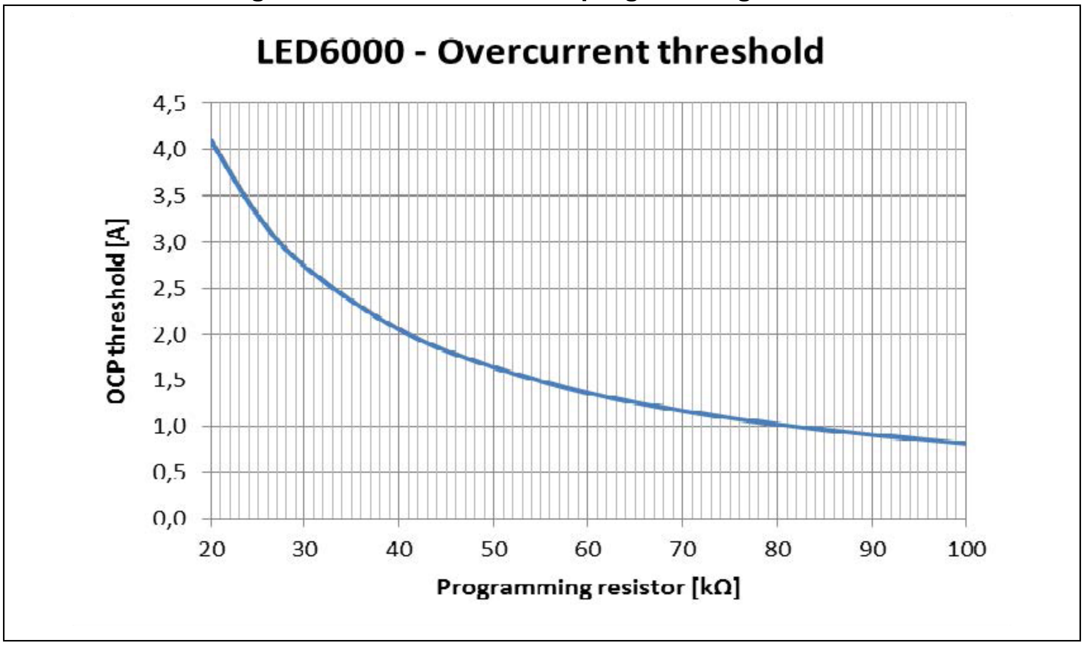
The peak current limit threshold (I_{LIM}) can be programmed in the range 0.85 A - 4.0 A by selecting the proper R_{ILIM} resistor, as suggested in *Equation 6*.

Equation 6

$$R_{ILIM} = 20k\Omega \cdot \frac{I_{PK}}{I_{LIM}}$$

I_{PK} is the default LED6000 current limit in case of R_{ILIM} not mounted, as shown in *Table 5 on page 8*.

Figure 14. Current limit and programming resistor



4.7 Overtemperature protection

It is recommended that the device never exceeds the maximum allowable junction temperature. This temperature increase is mainly caused by the total power dissipated by the integrated power MOSFET.

To avoid any damage to the device when reaching high temperature, the LED6000 implements a thermal shutdown feature: when the junction temperature reaches 170 °C (typ.) the device turns off the power MOSFET and shuts-down.

When the junction temperature drops to 155 °C (typ.), the device restarts with a new soft-start sequence.

5 Application notes - step-down conversion

5.1 Input capacitor selection

The input capacitor must be rated for the maximum input operating voltage and the maximum RMS input current.

Since the step-down converters input current is a sequence of pulses from 0A to I_{OUT}, the input capacitor must absorb the equivalent RMS current which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency.

The RMS input current (flowing through the input capacitor) in step-down conversion is roughly estimated by:

Equation 7

$$I_{CIN,RMS} \cong I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The actual DC/DC conversion duty cycle, D = V_{OUT}/V_{IN}, is influenced by a few parameters:

Equation 8

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{IN,MIN} - V_{SW,MAX}}$$

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{IN,MAX} - V_{SW,MIN}}$$

where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal high-side MOSFET. Considering the range D_{MIN} to D_{MAX} it is possible to determine the maximum $I_{CIN,RMS}$ flowing through the input capacitor.

The input capacitor value must be dimensioned to safely handle the input RMS current and to limit the VIN and VCC ramp-up slew rate to 0.5 V/µs maximum, in order to avoid the device active ESD protections turn-on.

Different capacitors can be considered:

- **Electrolytic capacitors**

These are the most commonly used due to their low cost and wide range of operative voltage. The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

- **Ceramic capacitors**

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is their high cost.

- **Tantalum capacitor**

Small, good quality tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to a very high current, for example when they are connected to the power supply.

The amount of the input voltage ripple can be roughly overestimated by *Equation 9*.

Equation 9

$$V_{IN,PP} = \frac{D \cdot (1 - D) \cdot I_{OUT}}{C_{IN} \cdot F_{SW}} + R_{ES,IN} \cdot I_{OUT}$$

In case of MLCC ceramic input capacitors, the equivalent series resistance ($R_{ES,IN}$) is negligible.

In addition to the above considerations, a ceramic capacitor with an appropriate voltage rating and with a value 1 µF or higher should always be placed across VIN and power ground and across VCC and the IC GND pins, as close as possible to the LED6000 device. This solution is necessary for spike filtering purposes.

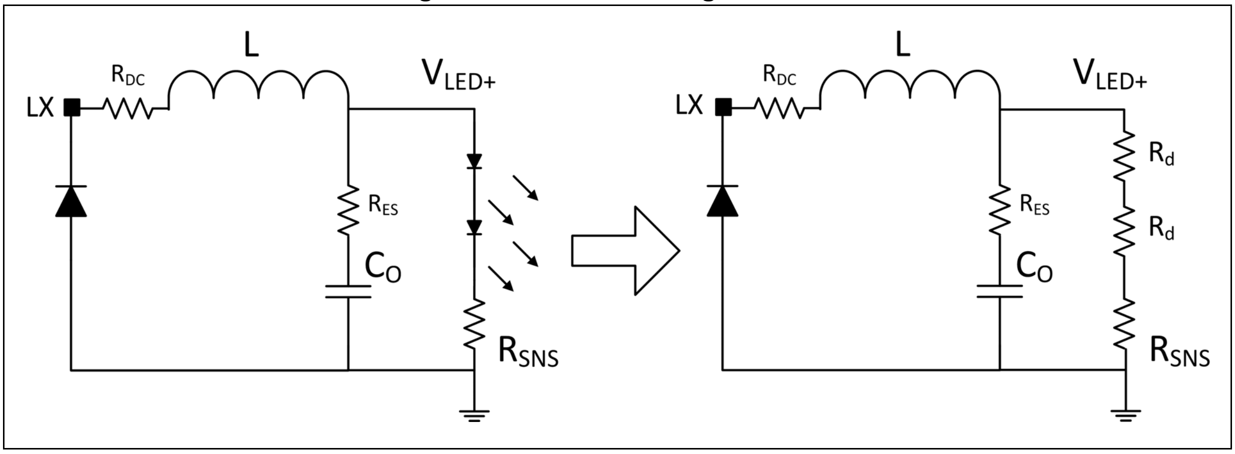
5.2 Output capacitor and inductor selection

The output capacitor is very important in order to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the choke but increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required.

The current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge and discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The allowed LED current ripple ($\Delta I_{LED,PP}$) is typically from 2% to 5% of the LED DC current.

Figure 15. LEDs small signal model



Based on the small signal model typically adopted for LEDs (as shown in *Figure 15*), the amount of the inductor current ripple which flows through the LEDs can be estimated by the following equation:

Equation 10

$$\Delta I_{LED}(s) = \Delta I_L(s) \cdot \frac{1 + sC_O R_{ES}}{1 + sC_O \cdot (R_{ES} + R_{SNS} + N \cdot R_d)}$$

The typical LED dynamic resistance, for high current LEDs, is about 0.9 Ω to 1 Ω.

The output capacitor, C_O, is typically an MLCC ceramic capacitor in the range of 1 µF and with equivalent series resistance lower than 10 mΩ, as a consequence the zero due to the time constant $C_O * R_{ES}$ is in the range of 10 MHz or above.

Starting from *Equation 10* it's possible to roughly estimate the required C_O value:

Equation 11

$$C_O \geq \frac{8}{\pi^2} \cdot \Delta I_{L,PP} \cdot \frac{1}{2\pi \cdot f_{SW} \cdot (R_{SNS} + N \cdot R_d) \cdot \Delta I_{LED,PP}}$$

In the above equation it has been assumed that the total inductor current ripple is well approximated by the first Fourier harmonic, $8/\pi^2 * \Delta I_{L,PP}$, due to the inductor current triangular shape.

The inductance value fixes the current ripple flowing through the output capacitor and LEDs. So the minimum inductance value, in order to have the expected current ripple, must be selected.

The rule to fix the current ripple value is to have a ripple at 30% - 60% of the programmed LEDs current.

In the continuous conduction mode (CCM), the required inductance value can be calculated by *Equation 12*.

Equation 12

$$L = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta I_L \cdot F_{SW}}$$

In order to guarantee a maximum current ripple in every condition, *Equation 12* must be evaluated in case of maximum input voltage, assuming V_{OUT} fixed.

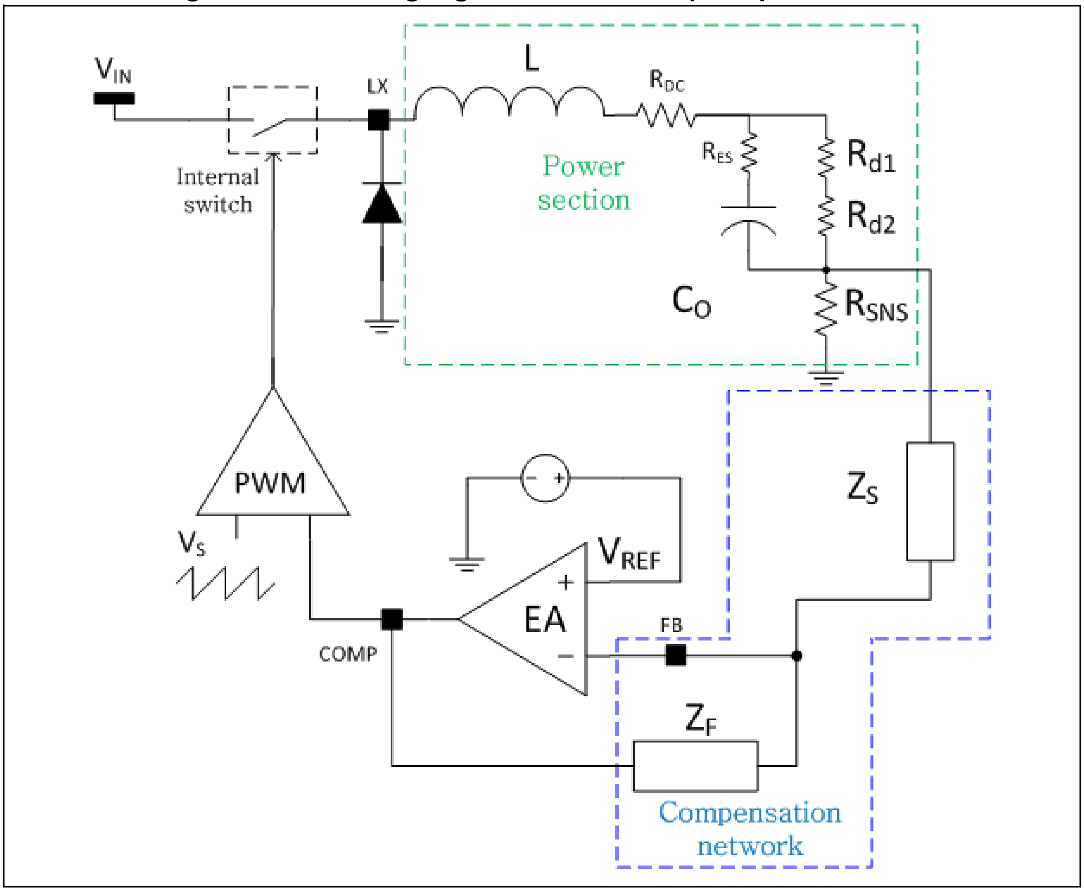
Increasing the value of the inductance helps to reduce the current ripple but, at the same time, strongly impacts the converter response time in case of high frequency dimming requirements. On the other hand, with a lower inductance value the regulator response time is improved but the power conversion efficiency is impacted and the output capacitor must be increased to limit the current ripple flowing through the LEDs.

As usually, the L-C_O choice is a trade-off among multiple design parameters.

5.3 Compensation strategy

The compensation network must assure stability and good dynamic performance. The loop of the LED6000 is based on the voltage mode control. The error amplifier is an operational amplifier with high bandwidth. So, by selecting the compensation network the E/A is considered as ideal, that is, its bandwidth is much larger than the system one.

Figure 16. Switching regulator control loop simplified model



The transfer function of the PWM modulator, from the error amplifier output (COMP pin) to the LX pin results in an almost constant gain, due to the voltage feedforward which generates a sawtooth with amplitude V_S directly proportional to the input voltage:

Equation 13

$$G_{PW0} = \frac{1}{V_S} = \frac{1}{k_{FF} \cdot V_{IN}}$$

For the LED6000 the feedforward gain is K_{FF} = 1/30.

The synchronization of the device with an external clock provided through the SYNCH pin can modify the PWM modulator gain (see *Section 4.1 on page 11* to understand how this gain changes and how to keep it constant in spite of the external synchronization).

The transfer function of the power section (i.e.: the voltage across R_{SNS} resulting as a variation of the duty cycle) is:

Equation 14

$$G_{LC}(s) = \frac{V_{SNS}(s)}{d(s)} = \frac{R_{SNS} \cdot V_{IN}}{R_{SNS} + s \cdot L + R_{DC} + N \cdot R_d \;//\; \dfrac{1 + s \cdot C_O \cdot R_{ES}}{s \cdot C_O}}$$

given L, R_{DC}, C_O, R_{ES}, R_{SNS} and R_d the parameters shown in *Figure 16*.

The power section transfer function can be rewritten as follows:

Equation 15

$$G_{LC}(s) = G_{LC0} \cdot \frac{1 + \dfrac{s}{2\pi \cdot f_z}}{1 + \dfrac{s}{2\pi \cdot Q \cdot f_{LC}} + \left(\dfrac{s}{2\pi \cdot f_{LC}}\right)^2}; \quad G_{LC0} \cong \frac{R_{SNS} \cdot V_{IN}}{R_{SNS} + N \cdot R_d}$$

Equation 16

$$f_z = \frac{1}{2\pi \cdot C_O \cdot (R_{ES} + N \cdot R_d)}; \quad f_{LC} \cong \frac{1}{2\pi\sqrt{LC_O}\sqrt{\dfrac{N \cdot R_d}{N \cdot R_d + R_{SNS}}}}$$

Equation 17

$$Q \cong \frac{\sqrt{LC_O} \cdot \sqrt{R_{SNS} + N \cdot R_d} \cdot \sqrt{N \cdot R_d}}{L + C_O \cdot R_{SNS} \cdot N \cdot R_d}$$

with the assumption that the inductor parasitic resistance, R_{DC}, and the output capacitor parasitic resistance, R_{ES}, are negligible compared to LED dynamic resistance, R_d.

The closed loop gain is then given by:

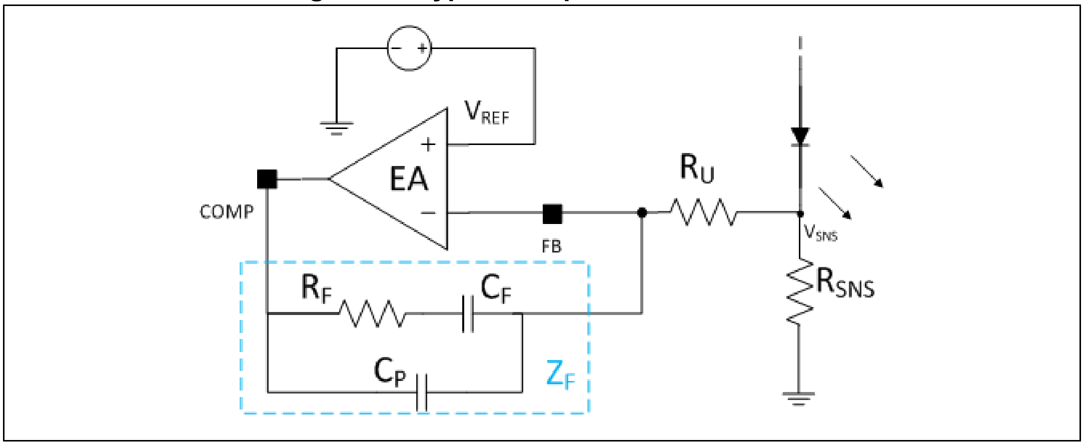
Equation 18

$$G_{LOOP}(s) = G_{LC}(s) \cdot G_{PW0}(s) \cdot G_{COMP}(s)$$

As shown in Equation 16, f_z depends on the output capacitor parasitic resistance and on the LEDs dynamic resistance. Following the considerations summarized in Section 5.2 on page 25, in the typical application the programmed control loop bandwidth (BW) might be higher than f_z, so this zero helps stabilize the loop. If this assumption is verified, a type II compensation network is required for loop stabilization.

In Figure 17 the type II compensation network is shown.

Figure 17. Type II compensation network



The type II compensation network transfer function, from V_{SNS} to COMP, is computed in Equation 19.

Equation 19

$$G_{COMPII}(s)=\frac{V_{COMP}(s)}{V_{SNS}(s)}=-\frac{Z_F(s)}{R_U}=-\frac{1}{R_U}\cdot\frac{1+sC_FR_F}{s\cdot(C_F+C_P)\cdot(1+sC_F//C_PR_F)}=-1\cdot\frac{1+\frac{s}{2\pi\cdot f_{Z1}}}{\frac{s}{2\pi\cdot f_{P0}}\cdot\left(1+\frac{s}{2\pi\cdot f_{P1}}\right)}$$

Equation 20

$$f_{Z1}=\frac{1}{2\pi\cdot C_FR_F};\quad f_{P0}=\frac{1}{2\pi\cdot(C_F+C_P)\cdot R_U};\quad f_{P1}=\frac{1}{2\pi\cdot C_F//C_PR_F}$$

The following suggestions can be followed for a quite common compensation strategy, assuming that C_P << C_F.

- Starting from Equation 18, the control loop gain module at s = 2π * F_{BW} allows to fix the R_F/R_U ratio:

Equation 21

$$\left|G_{LOOP,II}(s=2\pi\cdot f_{BW})\right|=\frac{G_{LC0}}{k_{FF}}\cdot\frac{f_{LC}{}^2}{f_z\cdot f_{BW}}\cdot\frac{f_{P0}}{f_{Z1}}\cong\frac{G_{LC0}}{k_{FF}}\cdot\frac{f_{LC}{}^2}{f_z\cdot f_{BW}}\cdot\frac{R_F}{R_U}=1$$

After choosing the regulator bandwidth (typically F_{BW} < 0.2 * F_{SW}) and a value for R_U, usually between 1 kΩ and 50 kΩ, in order to achieve C_F and C_P not comparable with parasitic capacitance of the board, the R_F required value is computed by *Equation 21*.

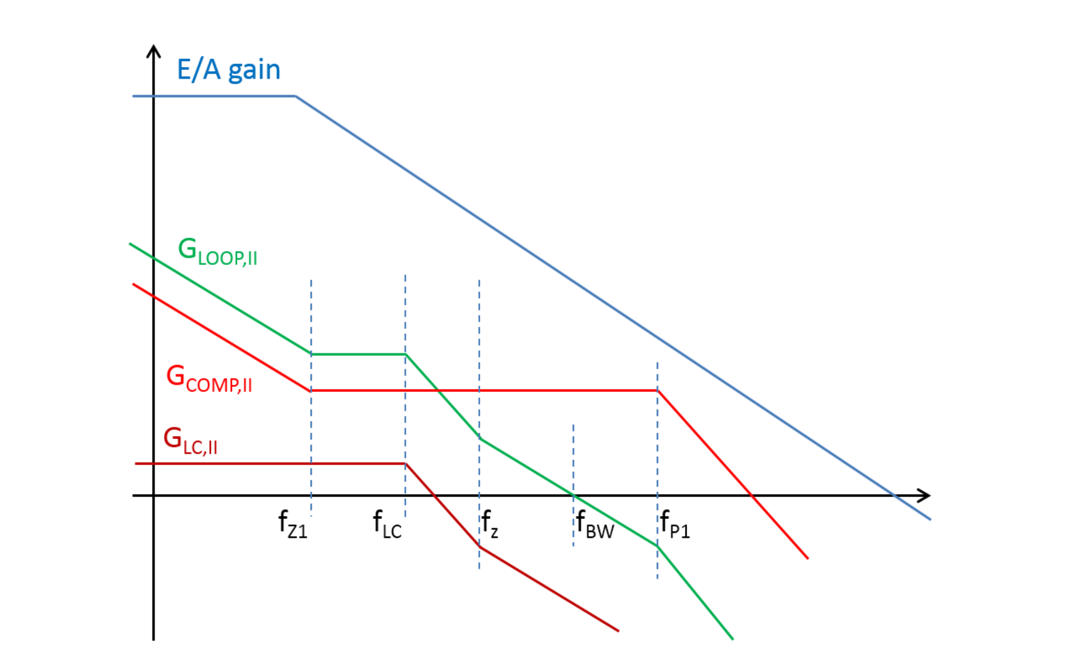
- Select C_F in order to place F_{Z1} below F_{LC} (typically 0.1 * F_{LC})
- Select C_P in order to place F_{P1} at 0.5 * F_{SW}

Equation 22

$$C_F = \frac{1}{2\pi \cdot R_F \cdot 0.1 \cdot f_{LC}}; \quad C_P = \frac{1}{2\pi \cdot R_F \cdot 0.5 \cdot f_{SW}}$$

The resultant control loop and other transfer functions gain are shown in *Figure 18*.

Figure 18. Type II compensation - Bode plot



5.4 Thermal considerations

The thermal design is important to prevent the thermal shutdown of the device if junction temperature goes above 170 °C (typ.). The three different sources of losses within the device are:

- Conduction losses due to the non-negligible RDSON of the power switch; these are equal to:

Equation 23

$$P_{HS,ON} = R_{HS,ON} \cdot D \cdot (I_{OUT})^2$$

where *D* is the duty cycle of the application and the maximum R_{DSON}, over the temperature, is 420 mΩ. Note that the duty cycle is theoretically given by the ratio between VOUT and VIN, but actually it is slightly higher in order to compensate the losses of the regulator. So the conduction losses increase compared with the ideal case.

- Switching losses due to power MOSFET turn ON and OFF; these can be calculated as:

Equation 24

$$P_{HS,SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot f_{SW} \cong V_{IN} \cdot I_{OUT} \cdot T_{TR} \cdot f_{SW}$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the power switch (V_{DS}) and the current flowing into it during turn ON and turn OFF phases. T_{TR} is the equivalent switching time. For this device the typical value for the equivalent switching time is 40 ns.

- Quiescent current losses, calculated as:

Equation 25

$$P_Q = V_{IN} \cdot I_{QOPVIN} + V_{BIAS} \cdot I_{QOPVBIAS}$$

where I_{QOPVIN} and $I_{QOPVBIAS}$ are the LED6000 quiescent current in case of the separate bias supply. If the switchover feature is not used, the IC quiescent current is the only one from VIN, I_{QUIESC}, as summarized in *Table 5 on page 8*.

The junction temperature T_J can be calculated as:

Equation 26

$$T_J = T_A + R_{th,JA} \cdot P_{TOT}$$

where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen. R_{thJA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The R_{thJA}, measured on the demonstration board described in the following paragraph, is about 40 °C/W for the HTSSOP16 package.

5.5 Layout considerations

The PCB layout of the switching DC/DC regulators is very important to minimize the noise injected in high impedance nodes and interference generated by the high switching current loops. Two separated ground areas must be considered: the signal ground and the power ground.

In a step-down converter the input loop (including the input capacitor, the power MOSFET and the freewheeling diode) is the most critical one. This is due to the fact that high value pulsed currents are flowing through it. In order to minimize the EMI, this loop must be as short as possible. The input loop, including also the output capacitor, must be referred to the power ground. All the other components are referred to the signal ground.

The feedback pin (FB) connection to the external current sensing resistor is a high impedance node, so the interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. To reduce the pick-up noise, the compensation network involving FB and COMP pins should be placed very close to the device.

To filter the high frequency noise, a small bypass capacitor (1 µF or higher) must be added as close as possible to the input voltage pin of the device, for both VIN and VCC pins.

Thanks to the exposed pad of the device, the ground plane helps to reduce the junction to ambient thermal resistance; so a wide ground plane enhances the thermal performance of the converter, allowing high power conversion.

The exposed pad must be connected to the signal GND pin. The connection to the ground plane must be achieved by taking care of the above mentioned input loop, in order to avoid a high current flowing through the signal GND.

Refer to *Section 5.6* for the LED6000 layout example.

5.6 Demonstration board

In this section the LED6000 step-down demonstration board is described.

The default settings are:

- Input voltage up to 60 V
- Programmed LED current 1 A (HB LEDs)
- F_{SW} = 500 kHz
- V_{BIAS} = GND

Figure 19. LED6000 demonstration board schematic (step-down)

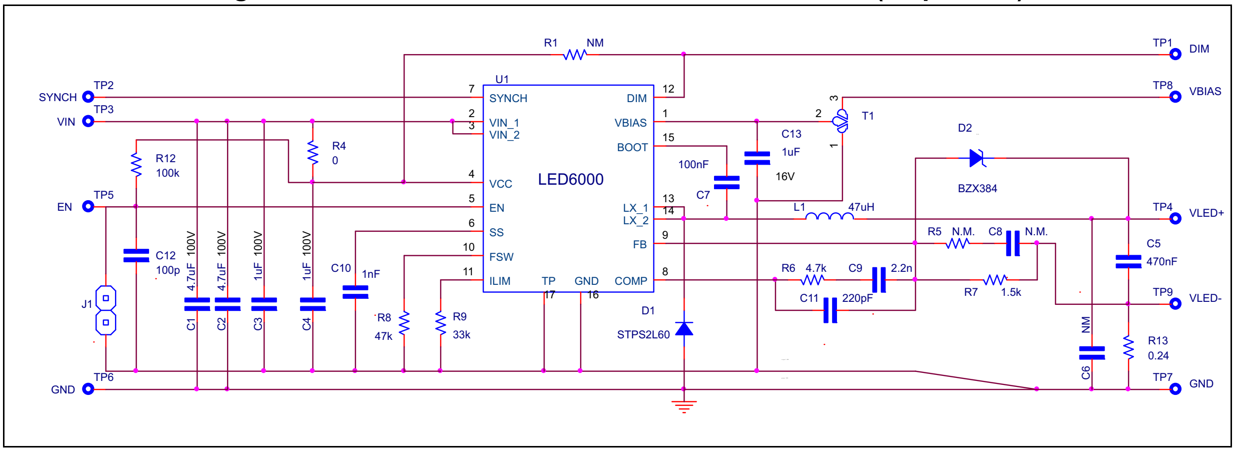


Table 7. LED6000 demonstration board component list

Reference	Part	Package	Note	Manufacturer P/N
C1, C2	4.7 µF	1210	X7S/100 V/10%	TDK C3225X7S2A475K
C3, C4	1 µF	0805	X7S/100 V/10%	TDK C2012X7S2A105K
C5	470 nF	1206	X7R/100 V/10%	TDK C3225X7R2A474M
C6, C8	N. M.			
C7	100 nF	0603	X7R/16 V/10%	
C9	2.2 nF	0603	X7R/25 V/10%	
C10	1 nF	0603	X7R/16 V/10%	
C11	220 pF	0603	NP0/50 V/5%	
C12	100 pF	0603	100 V	
C13	1 µF	0805	X5R/16 V/20%	
R1, R5	N. M.			
R4	0 Ω	0603		

Table 7. LED6000 demonstration board component list (continued)

Reference	Part	Package	Note	Manufacturer P/N
R6	4.7 kΩ	0603	1% tolerance	
R7	1.5 kΩ	0603	1% tolerance	
R8	47 kΩ	0603	1% tolerance	
R9	33 kΩ	0603	1% tolerance	
R12	100 kΩ	0603	1% tolerance	
R13	0.24 Ω	1210	1%, 0.5 W	PANASONIC ERJ14BQFR24U
L1	47 µH	10 x 10	2.2 A sat. / 128 mΩ	COILCRAFT MSS1038-473
D1	STPS2L60	SMBflat	60 V - 2 A Schottky rectifier	STM STPS2L60UF
D2	N. M.			
U1	LED6000	HTSSOP16		STM LED6000

Figure 20. LED6000 demonstration board layout (component side)

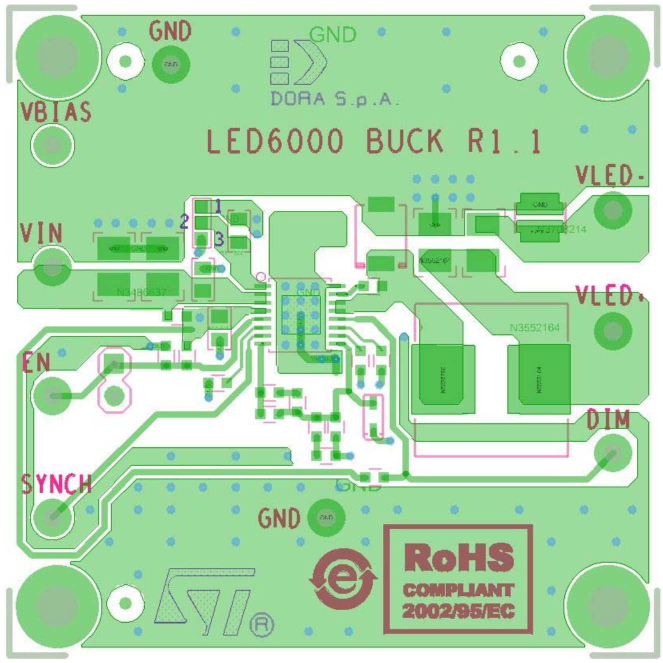
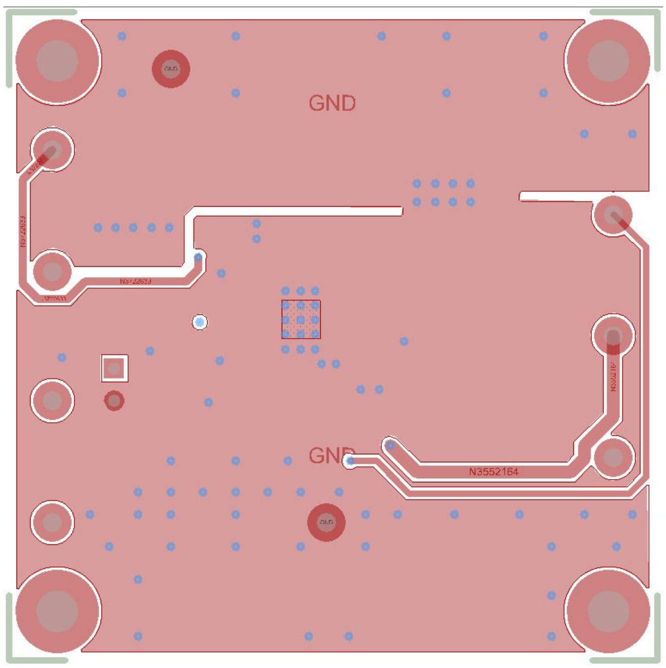


Figure 21. LED6000 demonstration board layout (bottom side)



6 Application notes - alternative topologies

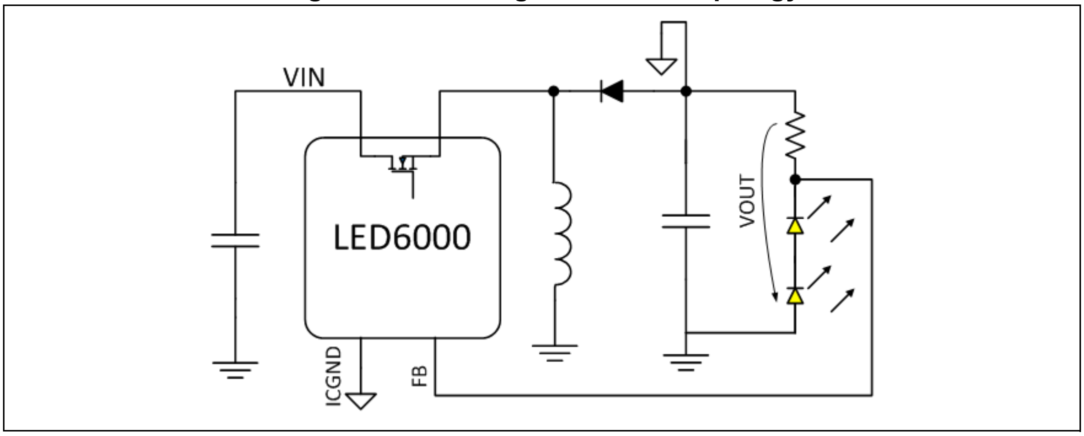
Thanks to the wide input voltage range and the adjustable compensation network, the LED6000 device is suitable to implement boost and buck-boost topologies.

6.1 Inverting buck-boost

The buck-boost topology fits the application with an input voltage range that overlaps the output voltage, V_{OUT}, which is the voltage drop across the LEDs and the sensing resistor.

The inverting buck-boost (see *Figure 22*) requires the same components count as the buck conversion and it is more efficient than the positive buck-boost, since no additional power MOSFET is required.

Figure 22. Inverting buck-boost topology



A current generator based on this topology implies two main application constraints:

- The output voltage is negative so the LEDs must be reversed
- The device GND floats with the negative output voltage. The device is supplied between V_{IN} and V_{OUT} (< 0). As a consequence:

Equation 27

$$V_{IN} + |V_{OUT}| < V_{IN,MAX}$$

$V_{IN,MAX}$ = 61 V is the maximum operating input voltage for the LED6000, as shown in *Table 5 on page 8*.

In buck-boost topology working in the continuous conduction mode (CCM), the HS MOS on-time interval, D, is given by:

Equation 28

$$D = \frac{|V_{OUT}|}{V_{IN} + |V_{OUT}|}$$

However, due to power losses (mainly switching and conduction losses), the real duty cycle is always higher than this. The real value (which can be measured in the application) should be used in the following formulas.

The peak current flowing in the embedded switch is:

Equation 29

$$I_{SW} = \frac{I_{OUT}}{1-D} + \frac{I_{RIPPLE}}{2} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \cdot D}{2 \cdot L \cdot f_{SW}}$$

While its average current level is equal to:

Equation 30

$$I_{SW} = \frac{I_{OUT}}{1-D}$$

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

The switch peak current must be lower than the minimum current limit of the overcurrent protection and the average current must be lower than the rated DC current of the device.

In addition to these constraints, the thermal considerations summarized in *Section 5.4 on page 30* must also be evaluated.

Figure 23. Inverting buck-boost schematic

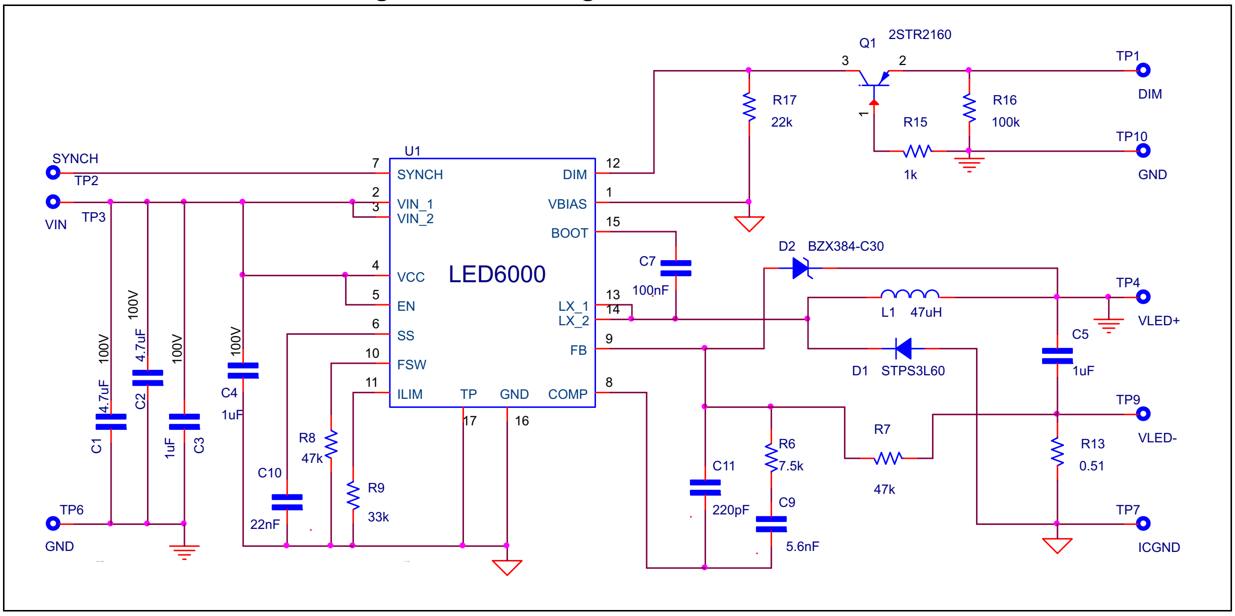


Figure 23 shows the schematic circuit for an LED current source based on inverting buck-boost topology. The input voltage ranges from 15 to 30 V and it can drive a string composed of 8 LEDs with 0.5 A DC.

This schematic also includes additional circuitry:

- A level shifter network for the proper dimming operation, since the LED6000 local ground (ICGND) is referred to the negative output voltage given by the voltage drop across the LEDs and the sensing resistor. This function is implemented by Q1, R15, R16 and R17. However, due to limited control loop bandwidth, the dimming operation in buck-boost topology is quite limited in terms of the minimum achievable DIM pulse.
- An external overvoltage protection which avoids the IC damage in case of the LED open row fault. This function is implemented by a Zener diode, D2, R7 and the sensing resistor, R_{SNS} = R13.

In case the LED string is disconnected the maximum output voltage is given by:

Equation 31

$$V_{OUT,MAX} = V_{FB} + V_{D2}$$

Equation 31, in addition to *Equation 27*, must be verified in order avoid the LED6000 to be exposed to electrical stress outside the allowed range (see *Table 2 on page 7* for details).

The series resistor, R7, must be selected in order to limit the maximum current flowing through the D2, as shown in *Equation 32*.

Equation 32

$$I_{D2} = \frac{V_{FB}}{R_{SNS} + R_7}$$

The compensation network design strategy for buck-boost topology is described in *Section 6.4 on page 44*.

Figure 24. Inverting buck-boost PCB layout (component side)

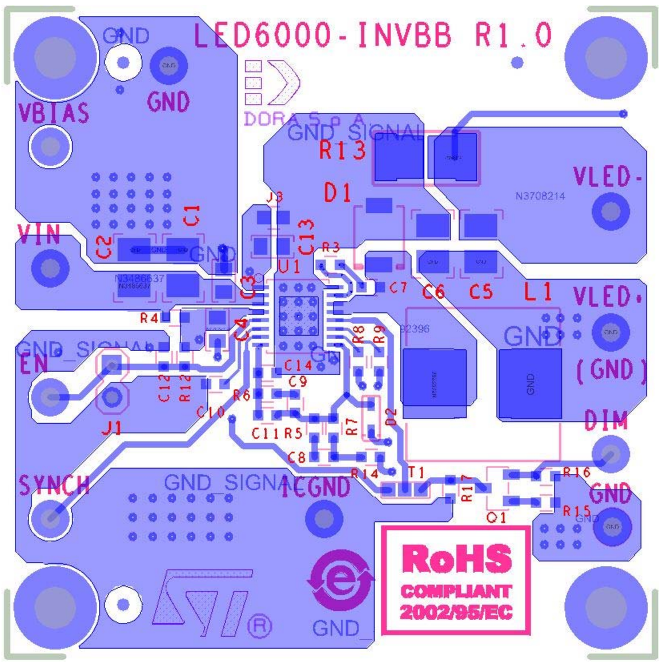
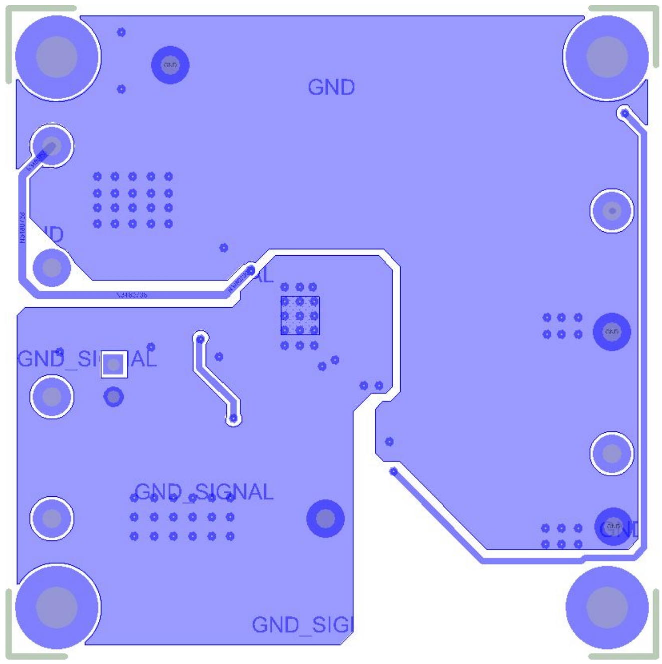


Figure 25. Inverting buck-boost PCB layout (bottom side)

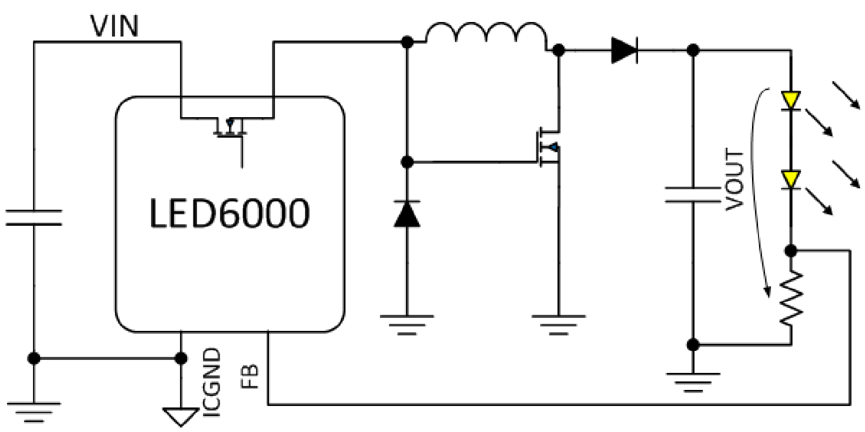


6.2 Positive buck-boost

The buck-boost topology fits the application with an input voltage range that overlaps the output voltage, V_{OUT}, which is the voltage drop across the LEDs and the sensing resistor.

The positive buck-boost (see *Figure 26*) can provide a positive output voltage, referred to ground, but it requires two additional power components, a MOSFET and a Schottky diode.

Figure 26. Positive buck-boost topology

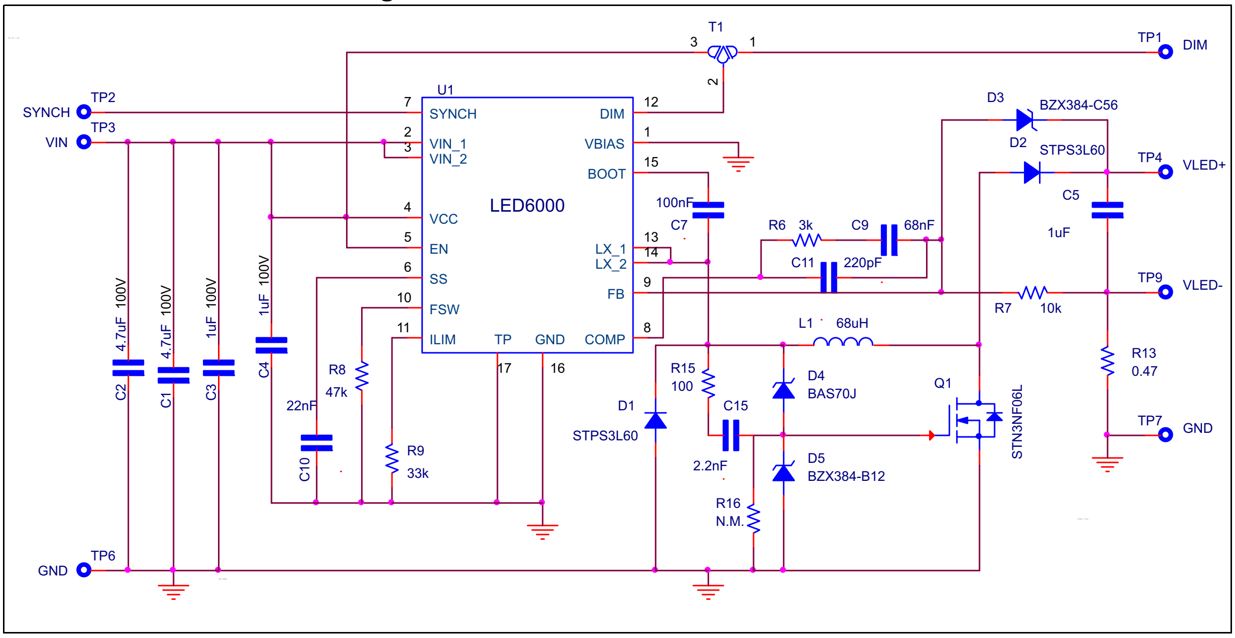


The main drawback of this topology, compared to inverting buck-boost, is the slightly lower efficiency. In the positive buck-boost *Equation 27 on page 35* is not applied, so the maximum input voltage is the maximum operating input voltage for the LED6000, as shown in *Table 5 on page 8*. In addition, the maximum output voltage can be higher than 61 V, assuming that the external MOS FET and Schottky diode are properly rated.

The other considerations summarized in *Section 6.1 on page 35* are also applied to this topology.

Figure 27 shows the schematic circuit for an LED current source based on positive buck-boost topology. The input voltage ranges from 24 to 54 V and it can drive a string composed of 14 LEDs with 0.55 A DC.

Figure 27. Positive buck-boost schematic



This schematic also includes two additional circuitry:

- A level shifter / clamping network for safe MOS driving and protection;
- An external overvoltage protection which avoids the IC damage in case of the LED open row fault. This function is implemented by a Zener diode, D3, R7 and the sensing resistor, R_{SNS} = R13.

In case the LED string is disconnected the maximum output voltage is given by:

Equation 33

$$V_{OUT,MAX} = V_{FB} + V_{D3}$$

The series resistor, R7, must be selected in order to limit the maximum current flowing through the D3, as shown in *Equation 34*.

Equation 34

$$I_{D3} = \frac{V_{FB}}{R_{SNS} + R_7}$$

The compensation network design strategy for buck-boost topology is described in *Section 6.4 on page 44*.

Figure 28. Positive buck-boost PCB layout (component side)

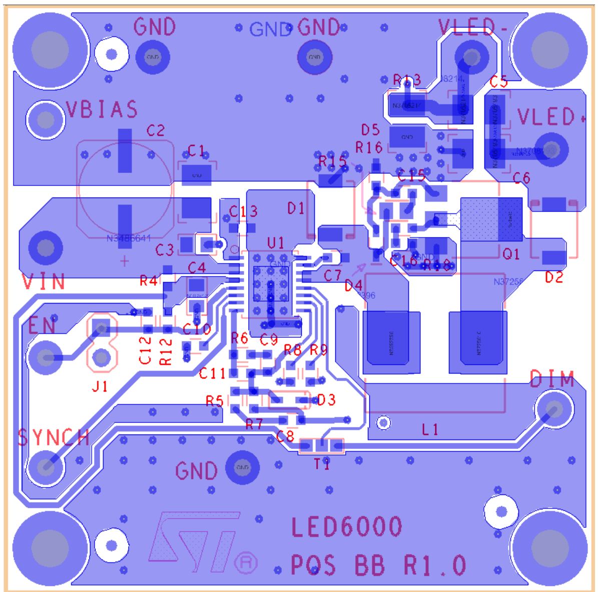
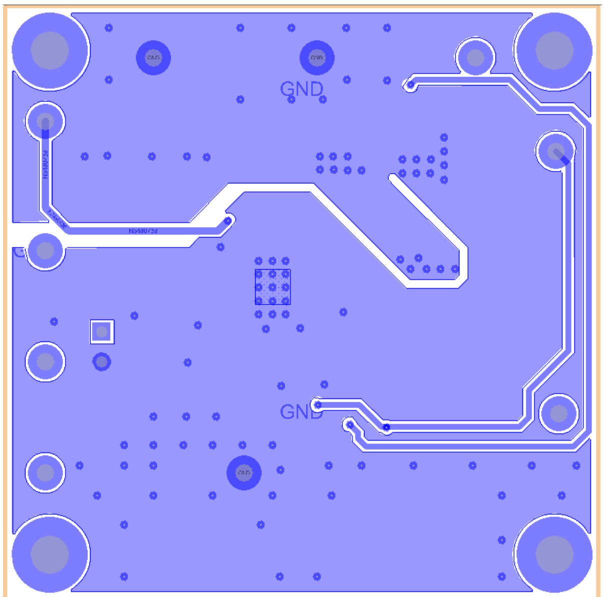


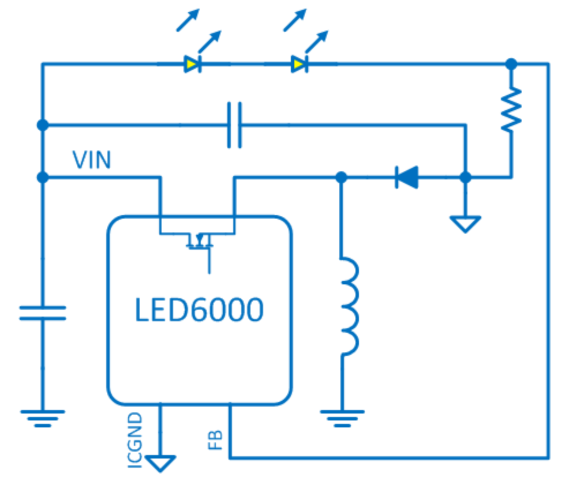
Figure 29. Positive buck-boost PCB layout (bottom side)



6.3 Floating boost

The floating-boost topology fits the application with an input voltage range always lower than the output voltage, V_{OUT}, which is the voltage drop across the LEDs and the sensing resistor. The floating boost (see *Figure 30*) requires the same components count as the buck conversion.

Figure 30. Floating-boost topology



In this topology the output voltage is referred to VIN and not to GND. The device is supplied by V_{OUT} as a consequence the maximum voltage drop across the LEDs string is 61 V.

In floating-boost topology working in the continuous conduction mode (CCM), the HS MOS on-time interval, D, is given by:

Equation 35

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

However, due conduction losses, the real duty cycle is always higher than the ideal one. The real value should be used in the following formulas.

The peak current flowing in the embedded switch is:

Equation 36

$$I_{SW} = \frac{I_{OUT}}{1-D} + \frac{I_{RIPPLE}}{2} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \cdot D}{2 \cdot L \cdot f_{SW}}$$

While its average current level is equal to:

Equation 37

$$I_{SW} = \frac{I_{OUT}}{1-D}$$

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

The switch peak current must be lower than the minimum current limit of the overcurrent protection and the average current must be lower than the rated DC current of the device.

In addition to these constraints, the thermal considerations summarized in *Section 5.4 on page 30* must also be evaluated.

Figure 31. Floating-boost reference schematic

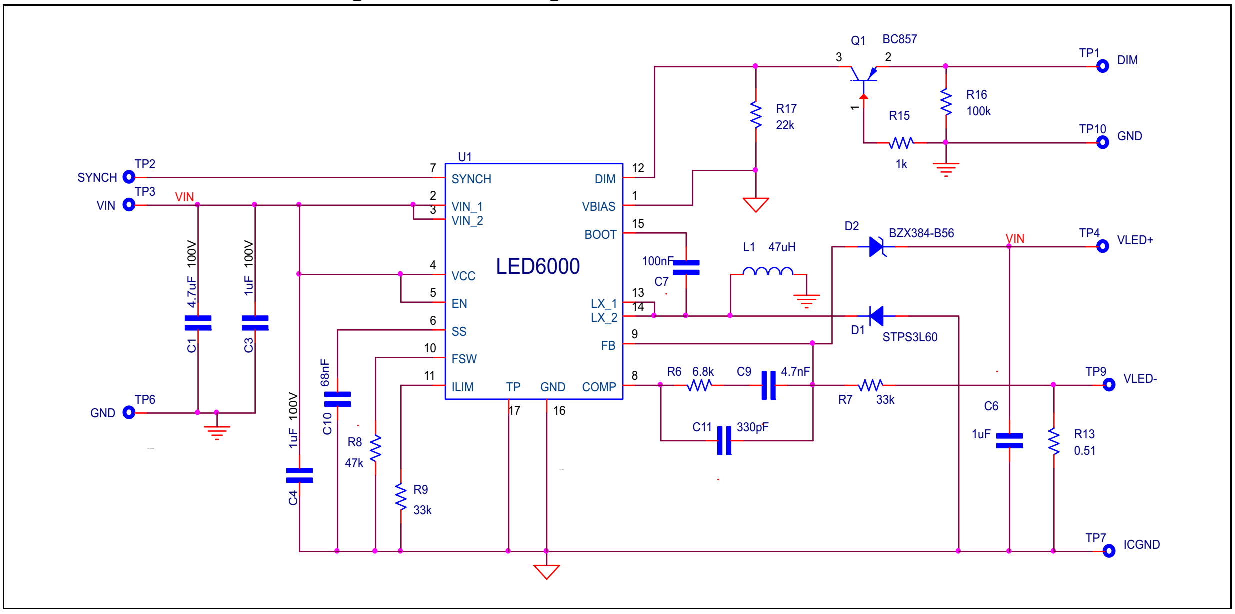


Figure 31 shows the schematic circuit for an LED current source based on floating-boost topology. The expected input voltage range is from 18 V to 36 V and it can drive a string composed of 15 LEDs with 0.5 A DC.

This schematic also includes two additional circuitry:

- A level shifter network for the proper dimming operation, since the LED6000 local ground is different from the board GND. This function is implemented by Q1, R15, R16 and R17. However, due to limited control loop bandwidth, the dimming operation in floating-boost topology is quite limited in terms of the minimum achievable DIM pulse.
- An external overvoltage protection which avoids the IC damage in case of the LED open row fault. This function is implemented by a Zener diode, D2, R7 and the sensing resistor, R_{SNS} = R13.

In case the LED string is disconnected the maximum output voltage is given by:

Equation 38

$$V_{OUT,MAX} = V_{FB} + V_{D2}$$

Equation 38 must be verified in order avoid the LED6000 to be exposed to electrical stress outside the allowed range (see *Table 2 on page 7* for details).

The series resistor, R7, must be selected in order to limit the maximum current flowing through the D2, as shown in *Equation 32 on page 37*.

The compensation network design strategy for floating-boost topology is described in *Section 6.4*.

Figure 32. Floating-boost PCB layout (component side)

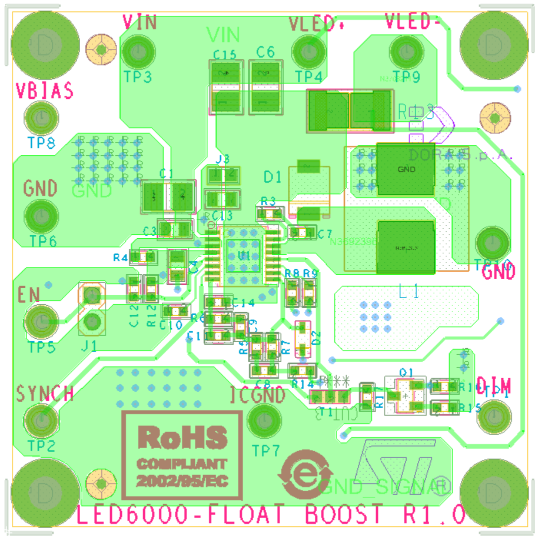
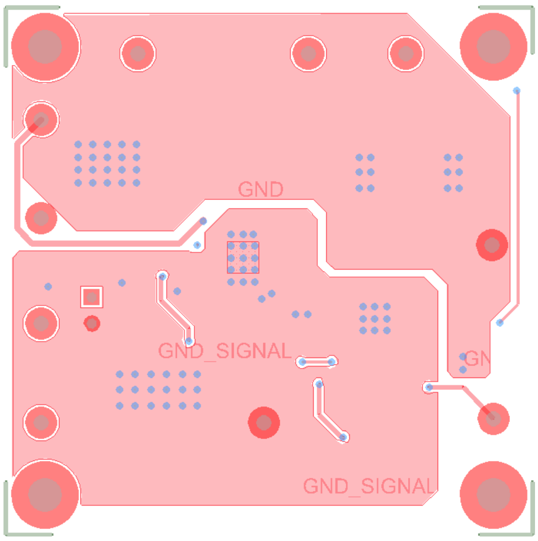


Figure 33. Floating-boost PCB layout (bottom side)



6.4 Compensation strategy for alternative topologies

The transfer function of the power section for buck-boost and floating-boost topology, driving N power LEDs with estimated R_d dynamic resistance, can be summarized by *Equation 39*:

Equation 39

$$G_{LC}(s) = \frac{V_{SNS}(s)}{d(s)} = G_0 \cdot \frac{\left(1 + \frac{s}{\omega_Z}\right) \cdot \left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_{LC} \cdot Q} + \frac{s^2}{\omega_{LC}{}^2}}$$

Table 8. Transfer function singularities

	ω_Z	ω_{RHPZ}	ω_{LC}
Buck boost	$\frac{1}{C_O \cdot N \cdot R_d}$	$\frac{(1-D)^2 \cdot V_O}{L \cdot D \cdot I_{LED}}$	$\frac{(1-D)}{L \cdot C_O}$
Floating boost	$\frac{1}{C_O \cdot N \cdot R_d}$	$\frac{(1-D)^2 \cdot V_O}{L \cdot I_{LED}}$	$\frac{(1-D)}{L \cdot C_O}$

Table 9. Transfer function parameters

	Q	G_0	D
Buck boost	$\sqrt{\frac{C_O}{L}} \cdot (1-D) \cdot N \cdot R_d$	$\frac{V_O}{D \cdot (1-D)} \cdot \frac{R_{SNS}}{R_{SNS} + N \cdot R_d}$	$\frac{V_O}{V_O + V_{IN}}$
Floating boost	$\sqrt{\frac{C_O}{L}} \cdot (1-D) \cdot N \cdot R_d$	$\frac{V_O}{1-D} \cdot \frac{R_{SNS}}{R_{SNS} + N \cdot R_d}$	$1 - \frac{V_{IN}}{V_O}$

This simplified model is based on the assumption that the output capacitor ESR is negligible compared to LED dynamic resistance, R_d, and the LED current sensing resistor, R_{SNS}. Further, the R_{SNS} is assumed negligible compared to the total LED dynamic resistance, N * R_d.

The closed loop transfer function is still given by *Equation 18 on page 28*, assuming for the power section the model summarized in *Equation 39*.

The singularity ω_{RHPZ}, computed at the maximum load and minimum input voltage, is the limitation in the loop bandwidth design (f_{BW}). Typically the maximum bandwidth is designed to be lower than:

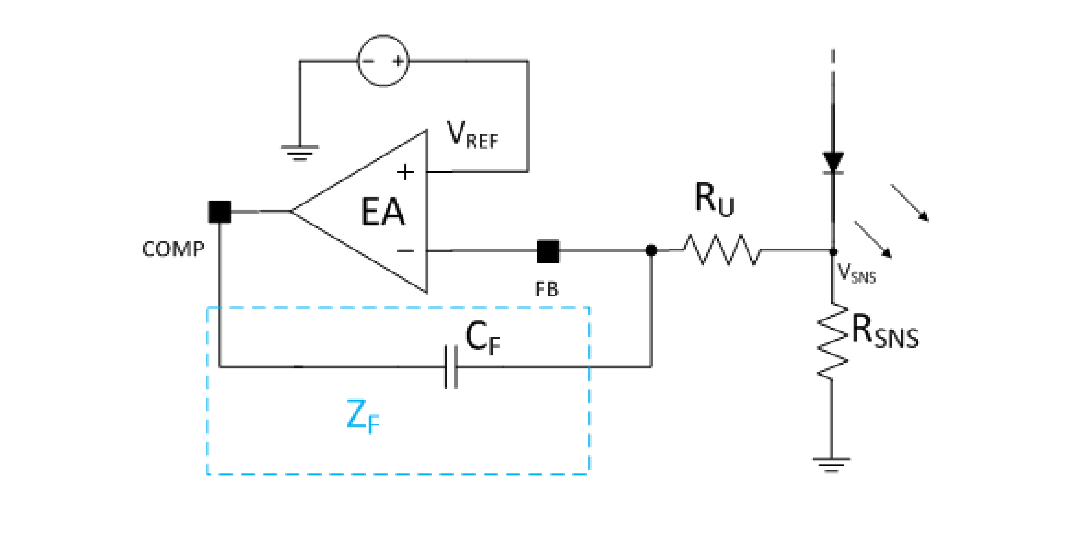
Equation 40

$$f_{BW} = \frac{1}{4} \cdot \frac{\omega_{RHPZ}}{2\pi}$$

In case ω_Z and ωL_C are lower than the target bandwidth, a type II compensation network is necessary for loop stabilization, following the compensation strategy described in *Section 5.3 on page 27*.

Otherwise, in case a very low bandwidth design is suitable, a simple type I compensation network is required. This approach is feasible if the target bandwidth is ¼ of f_{LC} or lower.

Figure 34. Type I compensation network



This kind of compensation network just provides one single low frequency pole, given by:

Equation 41

$$f_{PLF} = \frac{1}{2\pi \cdot C_F \cdot R_U}$$

Starting from *Equation 18 on page 28*, the control loop gain module at s = 2Π * F_{BW} allows to set f_{PLF} necessary value:

Equation 42

$$\left|G_{LOOP,I}(s = 2\pi \cdot f_{BW})\right| = \frac{G_0}{k_{FF} \cdot V_{IN}} \cdot \frac{f_{PLF}}{f_{BW}} = 1$$

A typical choice for R_U usually falls in the range from 1 kΩ to 50 kΩ, in order to provide for C_F a reasonable value (in the range from 1 nF to 100 nF) and to proper bias the overvoltage protection Zener diode.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

HTSSOP16 package information

Figure 35. HTSSOP16 package outline

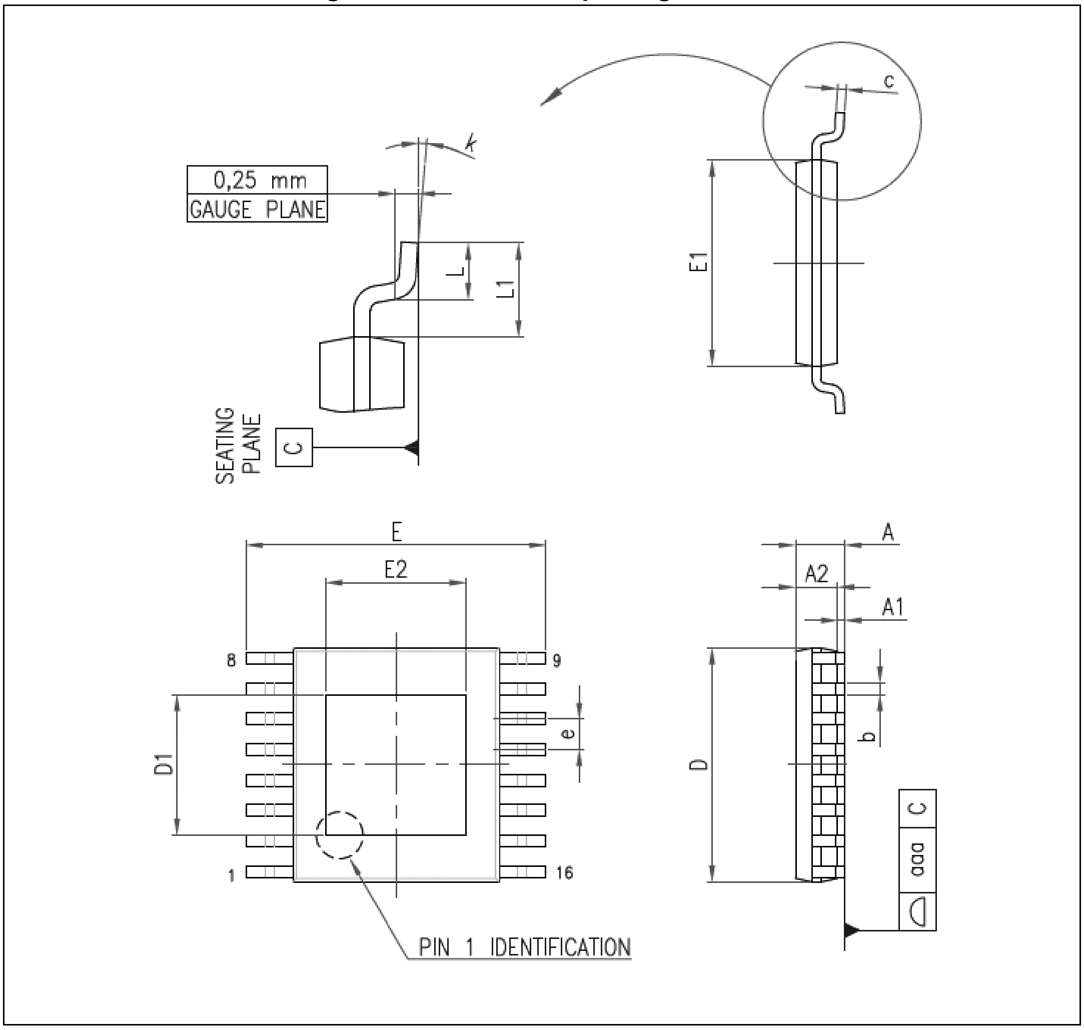


Table 10. HTSSOP16 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.80	3.00	3.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.80	3.00	3.20
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

8 Ordering information

Table 11. Order codes

Order code	Package	Packaging
LED6000PHR	HTSSOP16	Tube
LED6000PHTR	HTSSOP16	Tape and reel

9 Revision history

Table 12. Document revision history

Date	Revision	Changes
21-Apr-2015	1	Initial release.
15-May-2015	2	Updated document status to “production data” *on page 1*. Minor modifications throughout document.