



# VNN1NV04P-E, VNS1NV04P-E

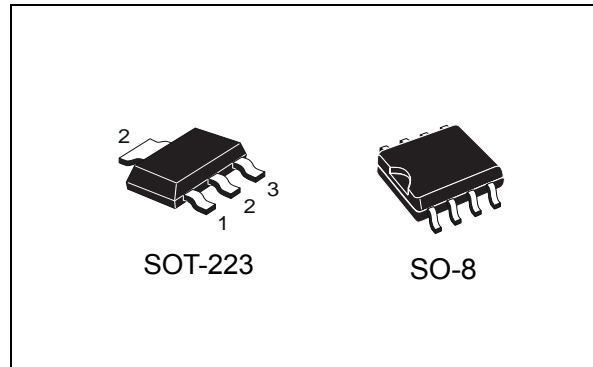
OMNIFET II

fully autoprotected Power MOSFET

## Features

Parameter	Symbol	Value
Max on-state resistance (per ch.)	$R_{ON}$	250 m $\Omega$
Current limitation (typ)	$I_{LIMH}$	1.7 A
Drain-source clamp voltage	$V_{CLAMP}$	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



## Description

The VNN1NV04P-E, VNS1NV04P-E are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
SOT-223	VNN1NV04P-E	VNN1NV04PTR-E
SO-8	VNS1NV04P-E	VNS1NV04PTR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

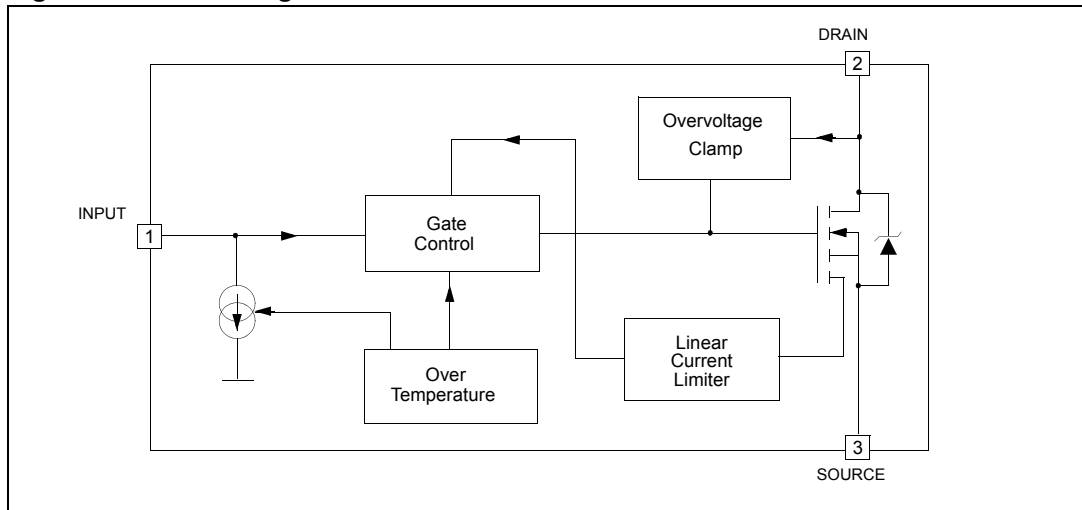
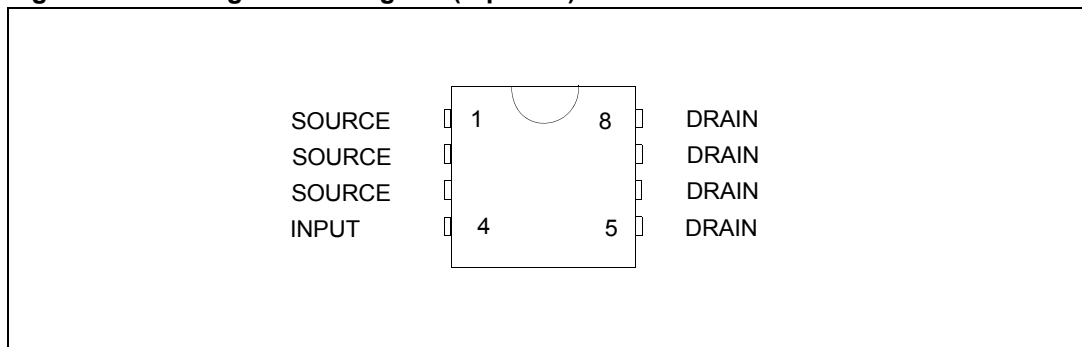


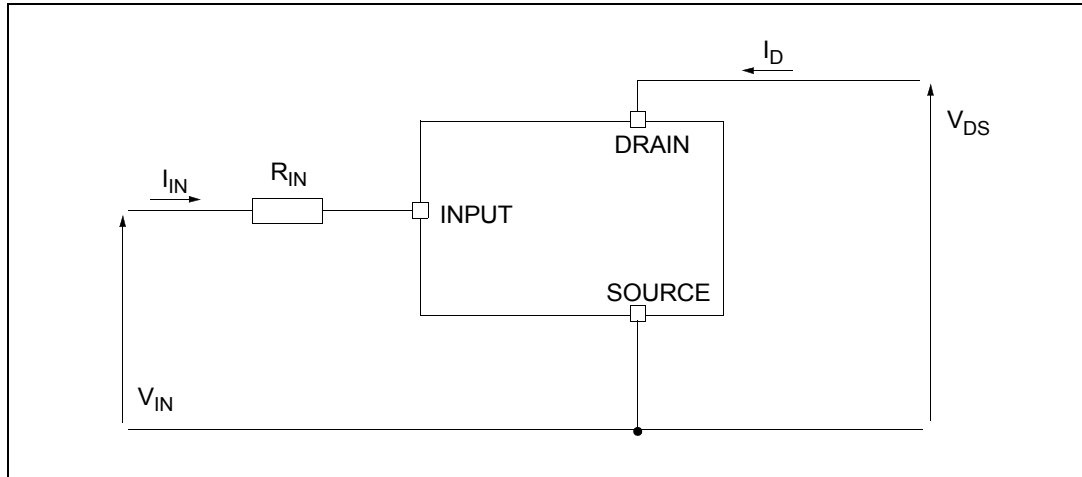
Figure 2. Configuration diagram (top view) (a)



a. For the pins configuration related to SOT-223 see outline at page 1.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Stress values that exceed those listed in the “Absolute maximum ratings” table can cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions greater than those, indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
$V_{DSn}$	Drain-source voltage ( $V_{INn}=0$ V)	Internally clamped		V
$V_{INn}$	Input voltage	Internally clamped		V
$I_{INn}$	Input current	+/-20		mA
$R_{IN\ MINn}$	Minimum input series impedance	330		$\Omega$
$I_{Dn}$	Drain current	Internally limited		A
$I_{Rn}$	Reverse DC output current	-3		A
$V_{ESD1}$	Electrostatic discharge ( $R=1.5$ K $\Omega$ , $C=100$ pF)	4000		V
$V_{ESD2}$	Electrostatic discharge on output pins only ( $R=330$ $\Omega$ , $C=150$ pF)	16500		V
$P_{tot}$	Total dissipation at $T_c=25$ °C	7	8.3	W
$T_j$	Operating junction temperature	Internally limited		°C
$T_c$	Case operating temperature	Internally limited		°C
$T_{stg}$	Storage temperature	-55 to 150		°C

## 2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max value		Unit
		SOT-223	SO-8	
$R_{thj-case}$	Thermal resistance junction-case	18		°C/W
$R_{thj-lead}$	Thermal resistance junction-lead		15	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	70 <sup>(1)</sup>	65 <sup>(1)</sup>	°C/W

1. When mounted on a standard single-sided FR4 board with 50 mm<sup>2</sup> of Cu (at least 35 μm thick) connected to all DRAIN pins

## 2.3 Electrical characteristics

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
<b>Off (-40 °C &lt; T<sub>j</sub> &lt; 150 °C, unless otherwise specified)</b>						
$V_{CLAMP}$	Drain-source clamp voltage	$V_{IN}=0\text{ V}; I_D=0.5\text{ A}$	40	45	55	V
$V_{CLTH}$	Drain-source clamp threshold voltage	$V_{IN}=0\text{ V}; I_D=2\text{ mA}$	36			V
$V_{INTH}$	Input threshold voltage	$V_{DS}=V_{IN}; I_D=1\text{ mA}$	0.5		2.5	V
$I_{ISS}$	Supply current from input pin	$V_{DS}=0\text{ V}; V_{IN}=5\text{ V}$		100	150	μA
$V_{INCL}$	Input-source clamp voltage	$I_{IN}=1\text{ mA}$ $I_{IN}=-1\text{ mA}$	6 -1.0	6.8	8 -0.3	V
$I_{DSS}$	Zero input voltage drain current ( $V_{IN}=0\text{ V}$ )	$V_{DS}=13\text{ V}; V_{IN}=0\text{ V}; T_j=25\text{ °C}$ $V_{DS}=25\text{ V}; V_{IN}=0\text{ V}$			30 75	μA
<b>On (-40 °C &lt; T<sub>j</sub> &lt; 150 °C, unless otherwise specified)</b>						
$R_{DS(on)}$	Static drain-source on resistance	$V_{IN}=5\text{ V}; I_D=0.5\text{ A}; T_j=25\text{ °C}$ $V_{IN}=5\text{ V}; I_D=0.5\text{ A}$			250 500	mΩ
<b>Dynamic (T<sub>j</sub>=25 °C, unless otherwise specified)</b>						
$g_{fs}^{(1)}$	Forward transconductance	$V_{DD}=13\text{ V}; I_D=0.5\text{ A}$		2		S
$C_{OSS}$	Output capacitance	$V_{DS}=13\text{ V}; f=1\text{ MHz}; V_{IN}=0\text{ V}$		90		pF
<b>Switching (T<sub>j</sub>=25 °C, unless otherwise specified)</b>						
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}; I_D=0.5\text{ A}$ $V_{gen}=5\text{ V}; R_{gen}=R_{IN\text{ MIN}}=330\text{ Ω}$ (see <a href="#">Figure 4</a> )		70	200	ns
$t_r$	Rise time			170	500	ns
$t_{d(off)}$	Turn-off delay time			350	1000	ns
$t_f$	Fall time			200	600	ns

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}; I_D=0.5\text{ A}$ $V_{gen}=5\text{ V}; R_{gen}=2.2\text{ K}\Omega$ (see <a href="#">Figure 4</a> )		0.25	1.0	$\mu\text{s}$	
$t_r$	Rise time			1.3	4.0	$\mu\text{s}$	
$t_{d(off)}$	Turn-off delay time			1.8	5.5	$\mu\text{s}$	
$t_f$	Fall time			1.2	4.0	$\mu\text{s}$	
$(di/dt)_{on}$	Turn-on current slope	$V_{DD}=15\text{ V}; I_D=1.5\text{ A}$ $V_{gen}=5\text{ V}; R_{gen}=R_{IN\text{ MIN}}=330\ \Omega$		5		$\text{A}/\mu\text{s}$	
$Q_i$	Total input charge	$V_{DD}=12\text{ V}; I_D=0.5\text{ A}; V_{IN}=5\text{ V}$ $I_{gen}=2.13\text{ mA}$ (see <a href="#">Figure 7</a> )		5		nC	
<b>Source drain diode (<math>T_j=25\text{ }^\circ\text{C}</math>, unless otherwise specified)</b>							
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD}=0.5\text{ A}; V_{IN}=0\text{ V}$		0.8		V	
$t_{rr}$	Reverse recovery time	$I_{SD}=0.5\text{ A}; di/dt=6\text{ A}/\mu\text{s}$ $V_{DD}=30\text{ V}; L=200\ \mu\text{H}$ (see <a href="#">Figure 5</a> )		205		ns	
$Q_{rr}$	Reverse recovery charge				100		nC
$I_{RRM}$	Reverse recovery current				0.7		A
<b>Protections (<math>-40\text{ }^\circ\text{C}&lt;T_j&lt;150\text{ }^\circ\text{C}</math>, unless otherwise specified)</b>							
$I_{lim}$	Drain current limit	$V_{IN}=5\text{ V}; V_{DS}=13\text{ V}$	1.7		3.5	A	
$t_{dlim}$	Step response current limit	$V_{IN}=5\text{ V}; V_{DS}=13\text{ V}$		2.0		$\mu\text{s}$	
$T_{jsh}$	Over temperature shutdown		150	175	200	$^\circ\text{C}$	
$T_{jrs}$	Over temperature reset		135			$^\circ\text{C}$	
$I_{gf}$	Fault sink current	$V_{IN}=5\text{ V}; V_{DS}=13\text{ V}; T_j=T_{jsh}$	10	15	20	mA	
$E_{as}$	Single pulse avalanche energy	Starting $T_j=25\text{ }^\circ\text{C}$ ; $V_{DD}=24\text{ V}$ $V_{IN}=5\text{ V}; R_{gen}=R_{IN\text{ MIN}}=330\ \Omega$ ; $L=50\text{ mH}$ (see <a href="#">Figure 6</a> and <a href="#">Figure 8</a> )	55			mJ	

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %



Figure 4. Switching time test circuit for resistive load

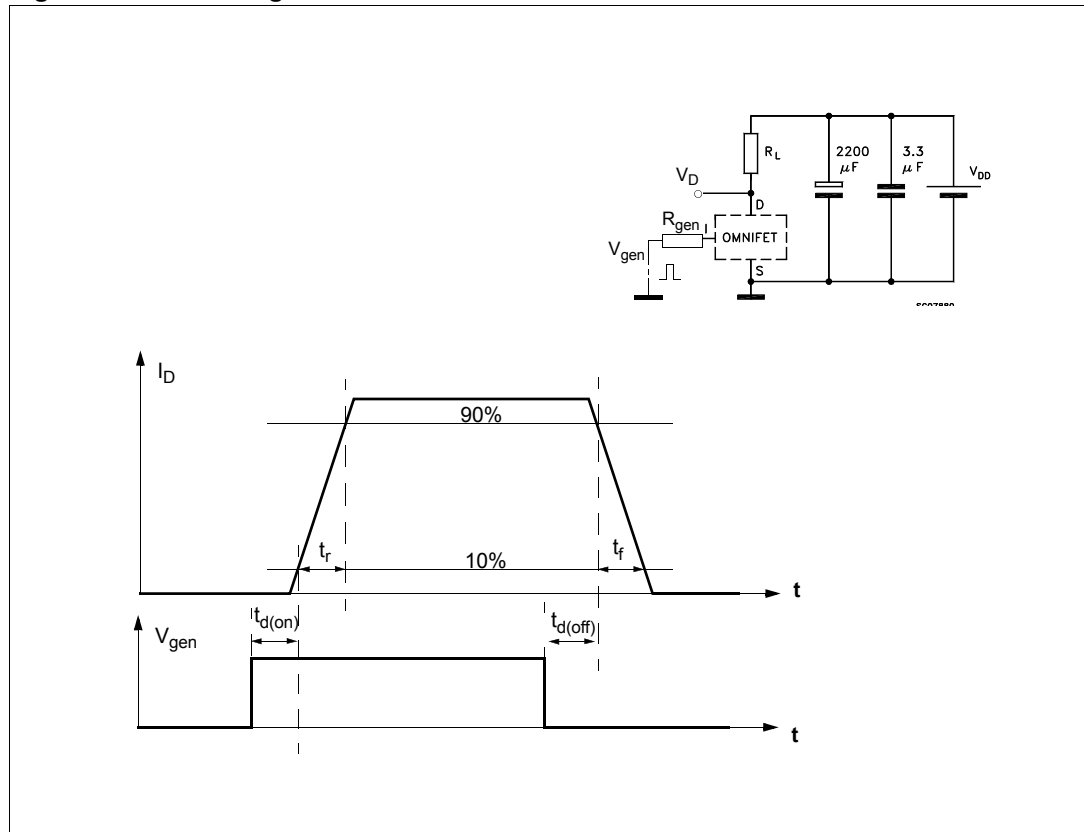


Figure 5. Test circuit for diode recovery times

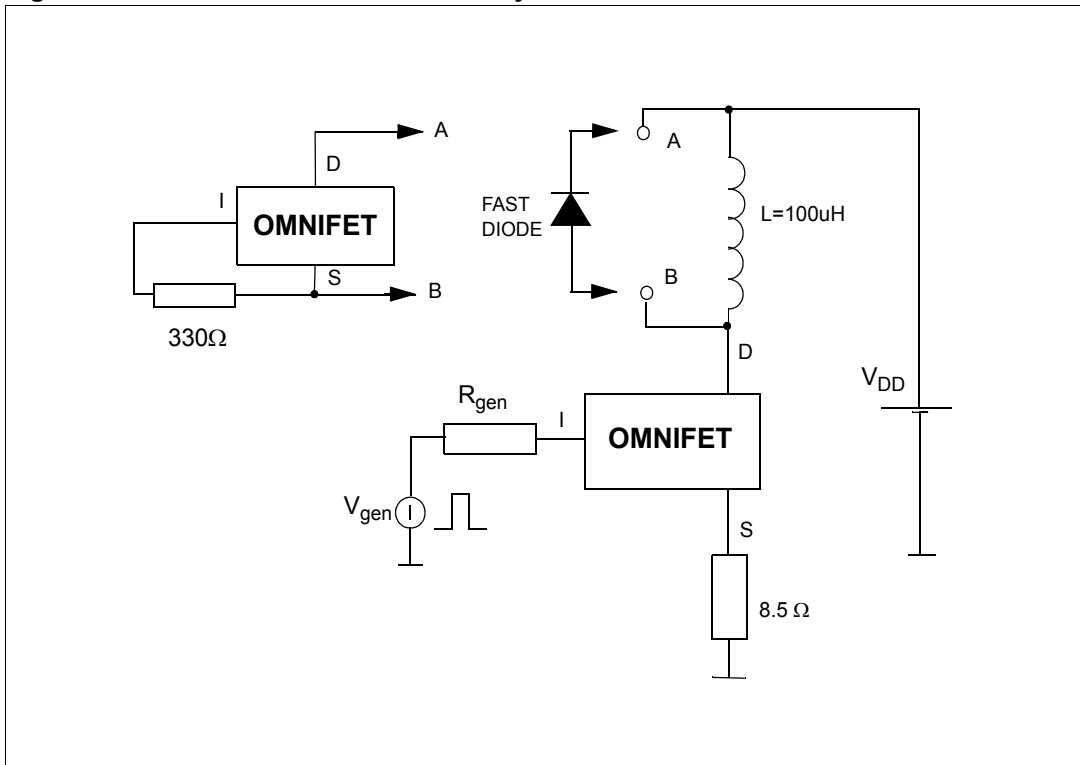


Figure 6. Unclamped inductive load test circuits

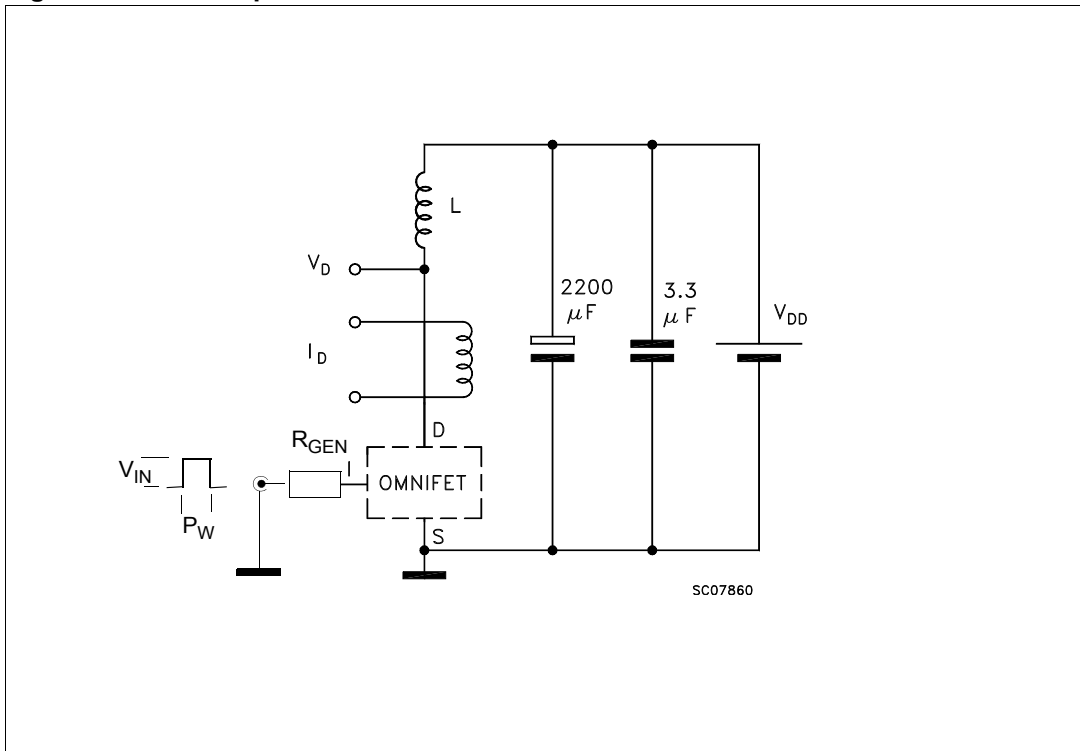


Figure 7. Input charge test circuit

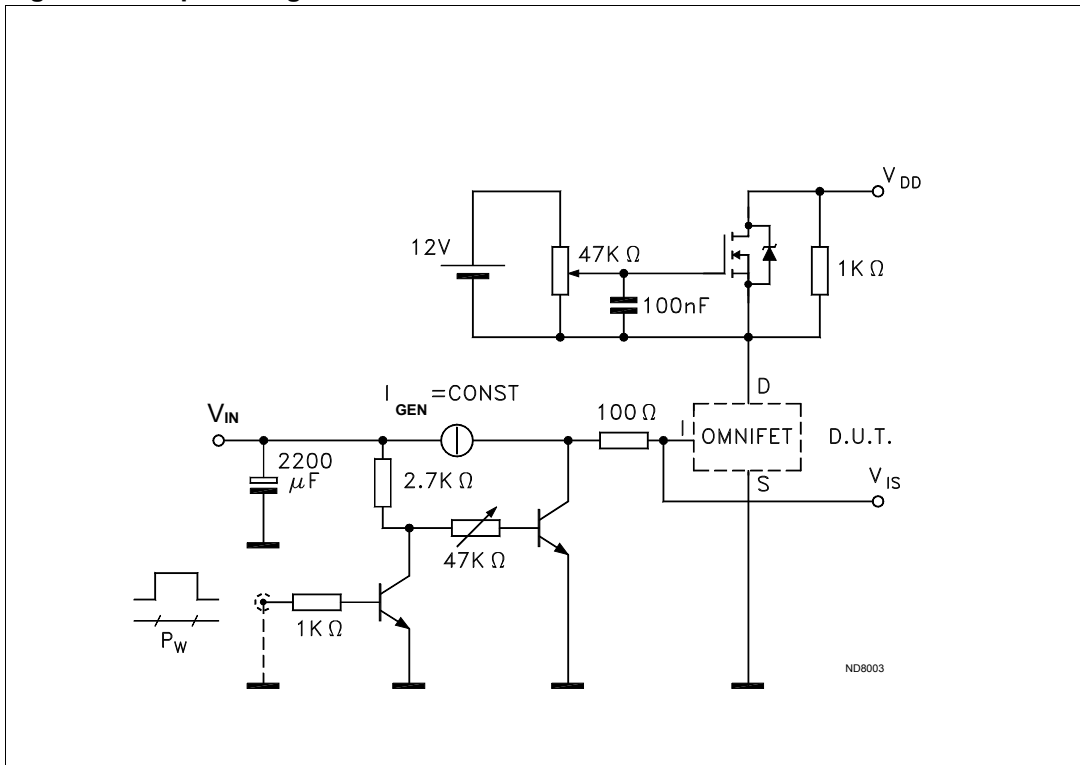
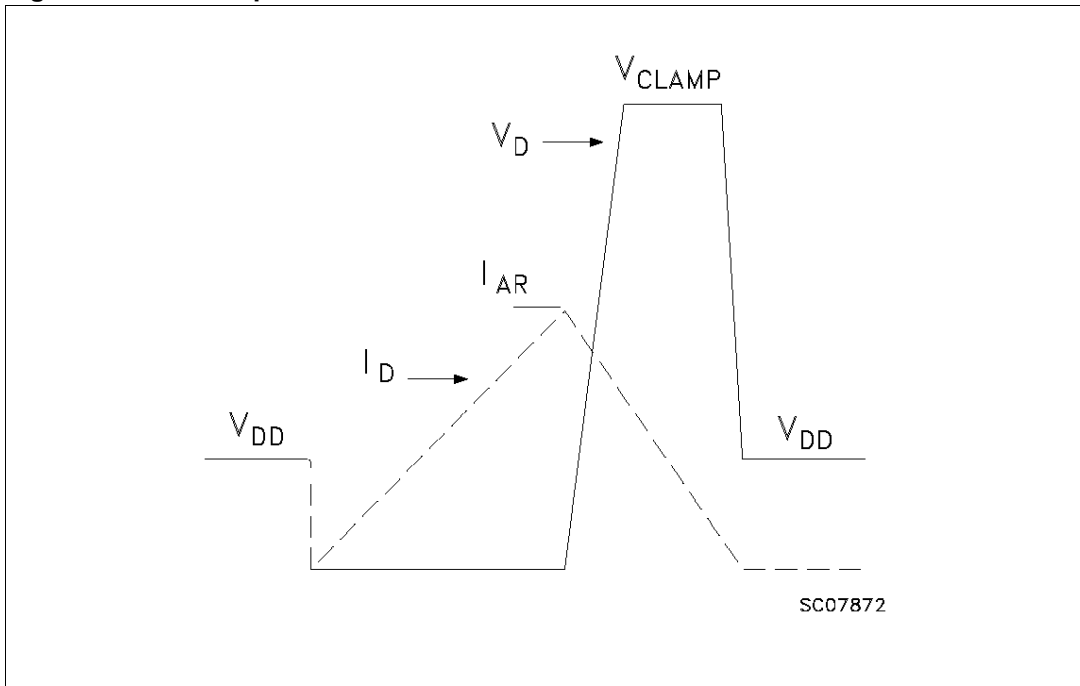
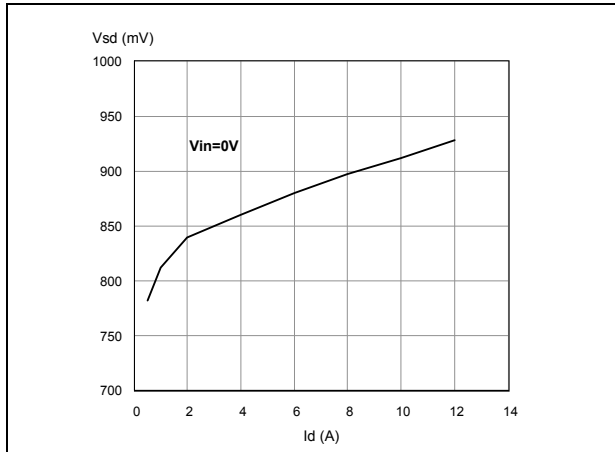


Figure 8. Unclamped inductive waveforms

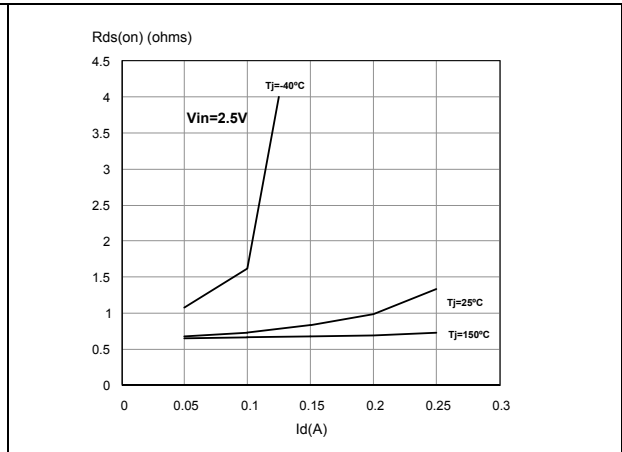


## 2.4 Electrical characteristics curves

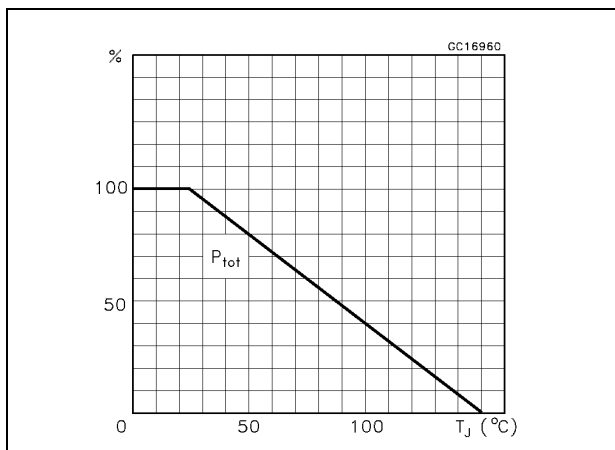
**Figure 9. Source-drain diode forward characteristics**



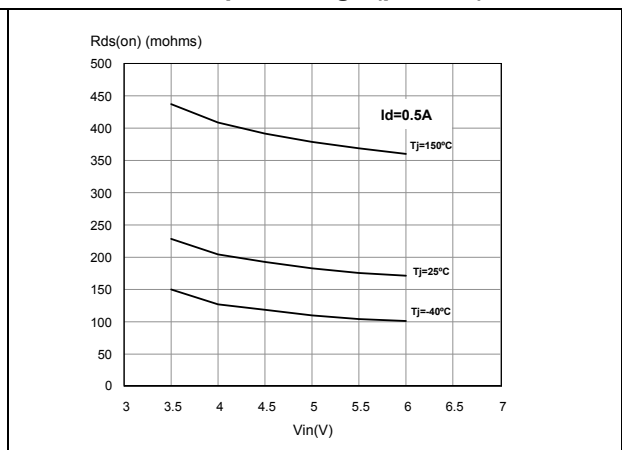
**Figure 10. Static drain-source on resistance**



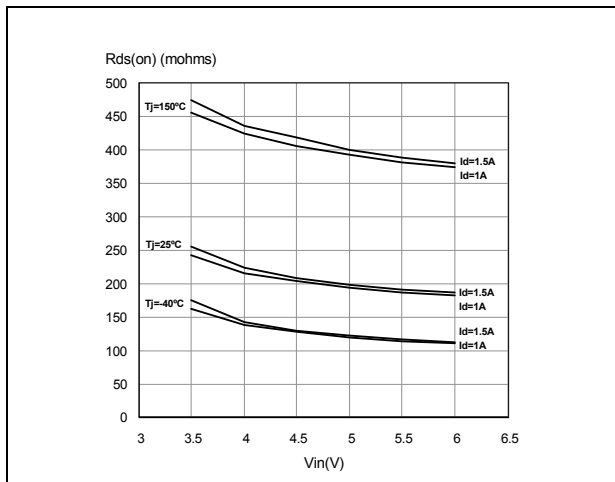
**Figure 11. Derating curve**



**Figure 12. Static drain-source on resistance vs input voltage (part 1/2)**



**Figure 13. Static drain-source on resistance vs input voltage (part 2/2)**



**Figure 14. Transconductance**

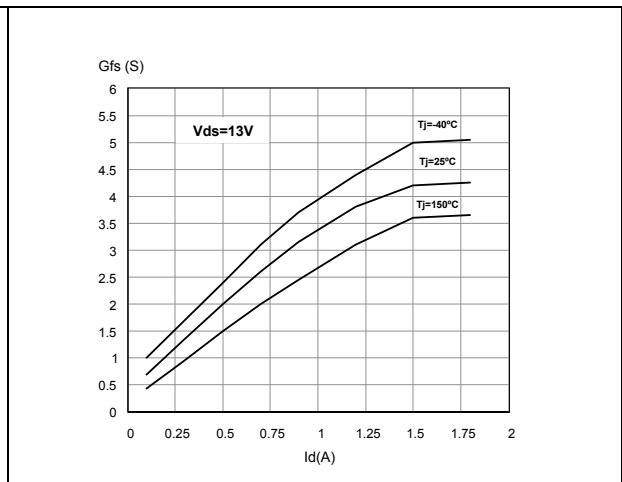


Figure 15. Static drain-source on resistance vs Id

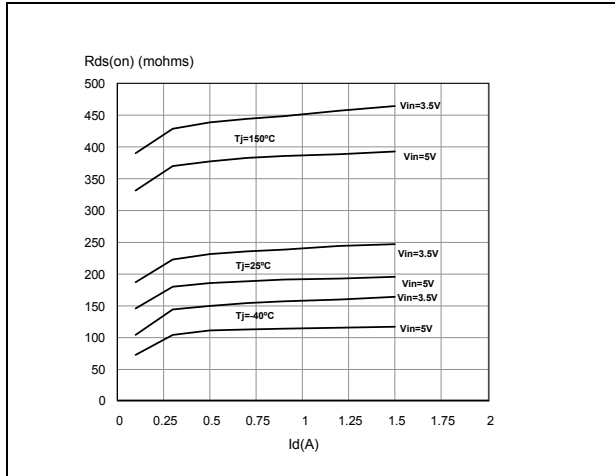


Figure 16. Transfer characteristics

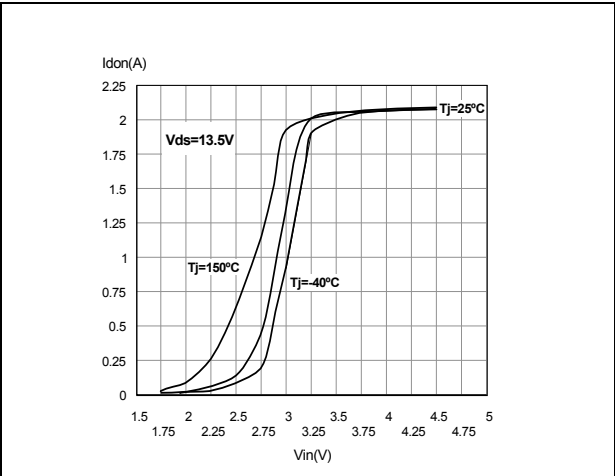


Figure 17. Turn-on current slope (part 1/2)

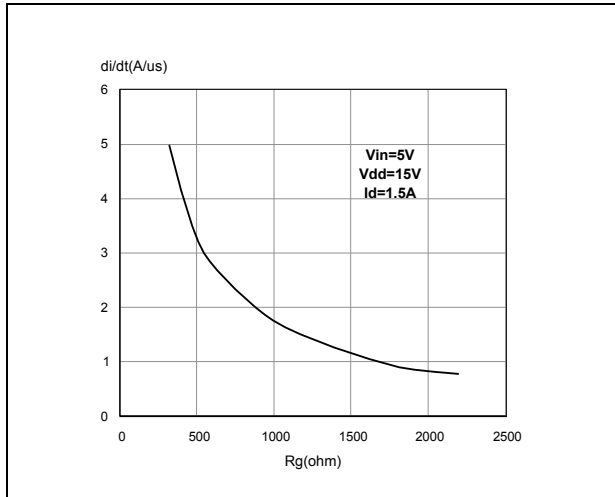


Figure 18. Turn-on current slope (part 2/2)

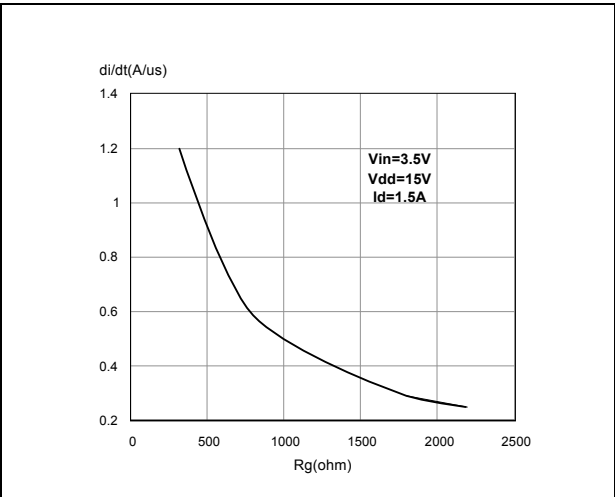


Figure 19. Input voltage vs input charge

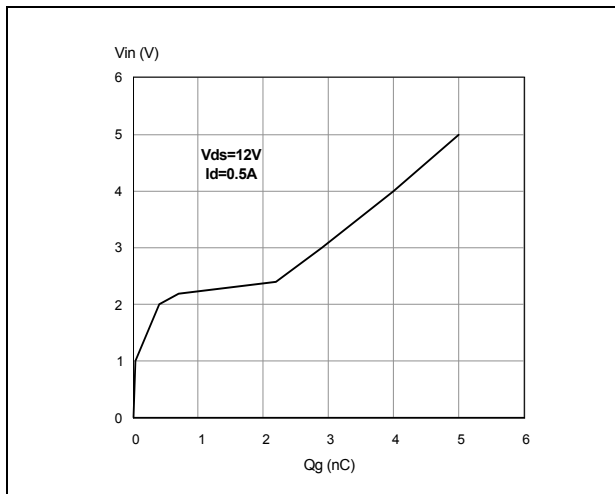


Figure 20. Turn-off drain source voltage slope (part 1/2)

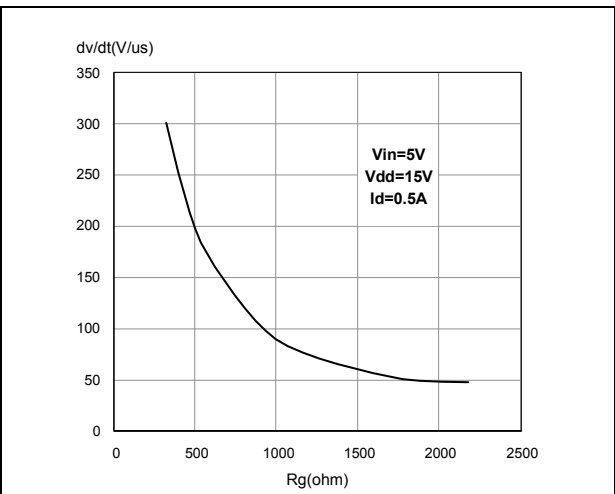


Figure 21. Turn-off drain-source voltage slope (part 2/2) Figure 22. Capacitance variations

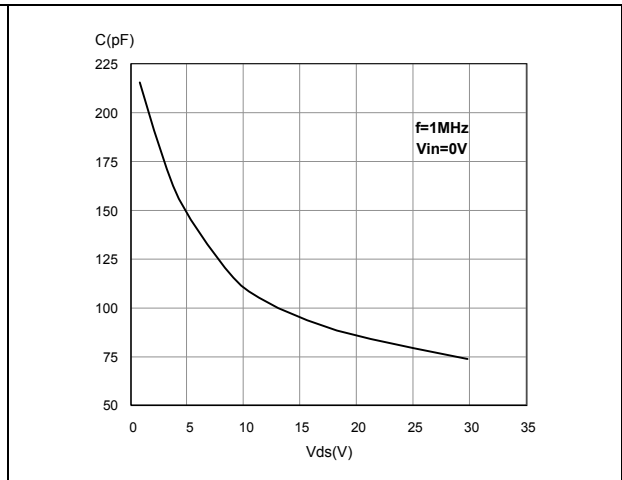
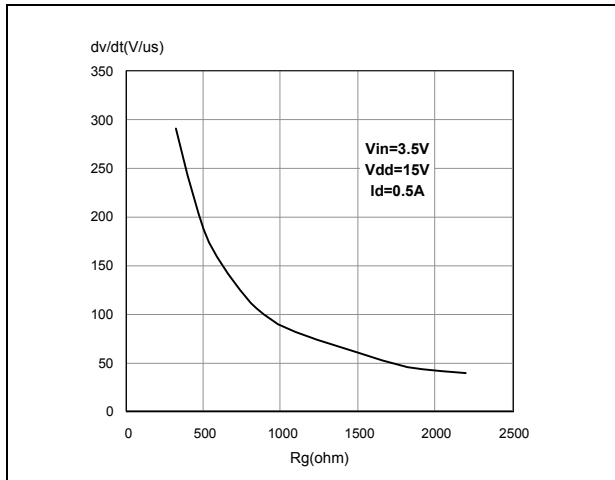


Figure 23. Switching time resistive load (part 1/2)

Figure 24. Switching time resistive load (part 2/2)

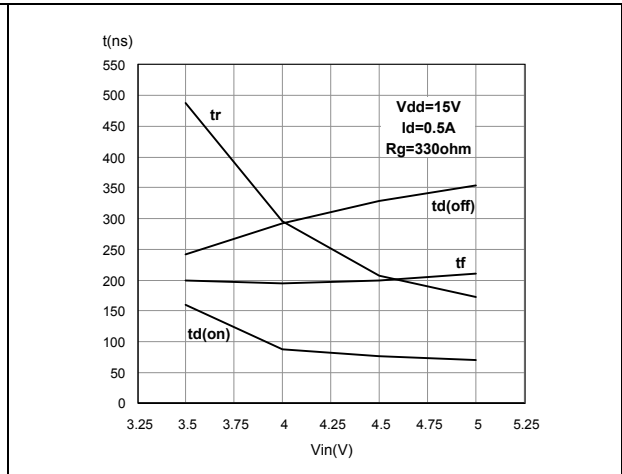
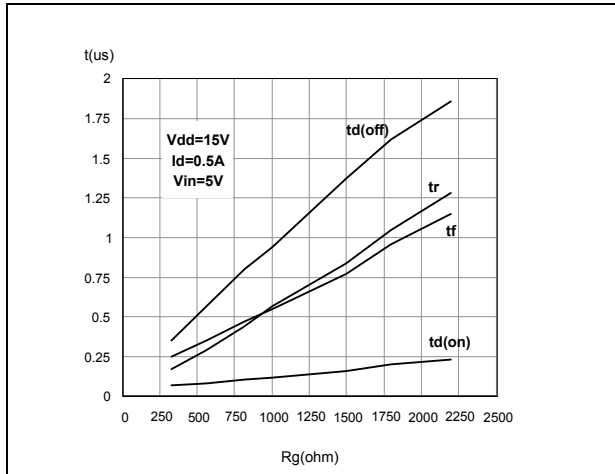
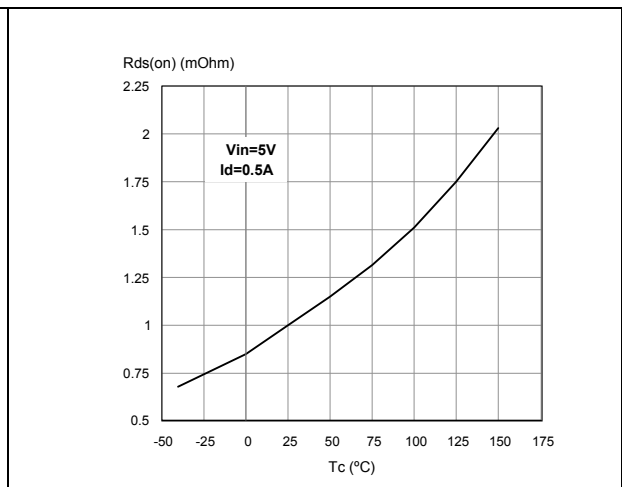
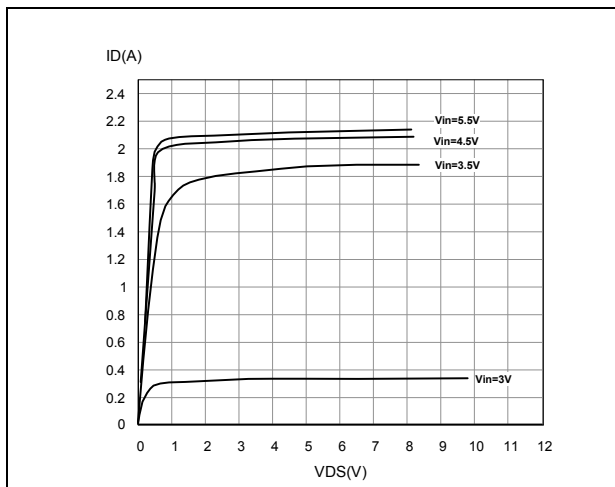
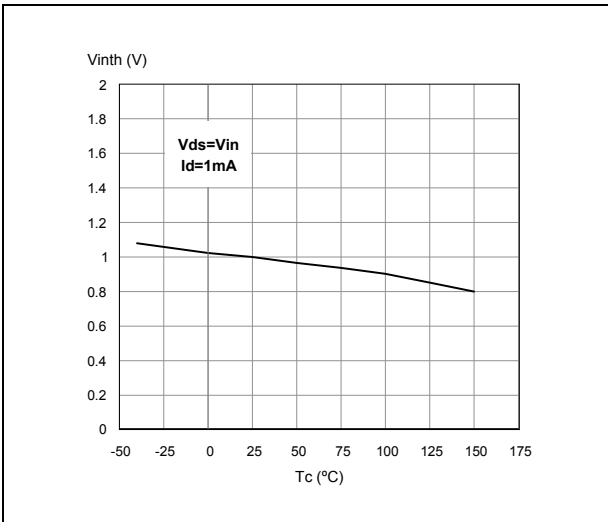


Figure 25. Output characteristics

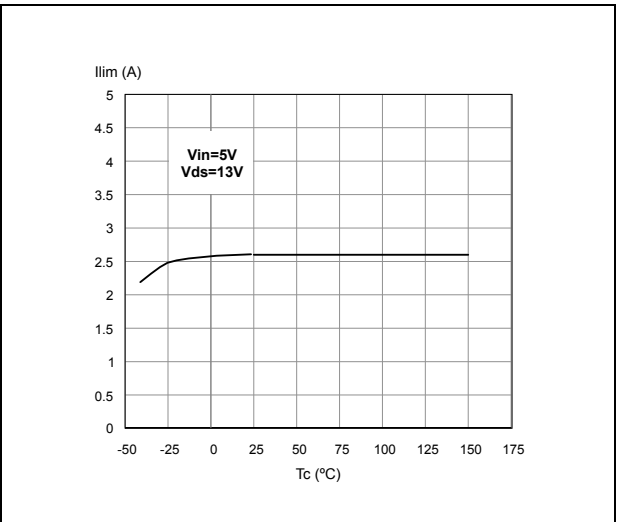
Figure 26. Normalized on resistance vs temperature



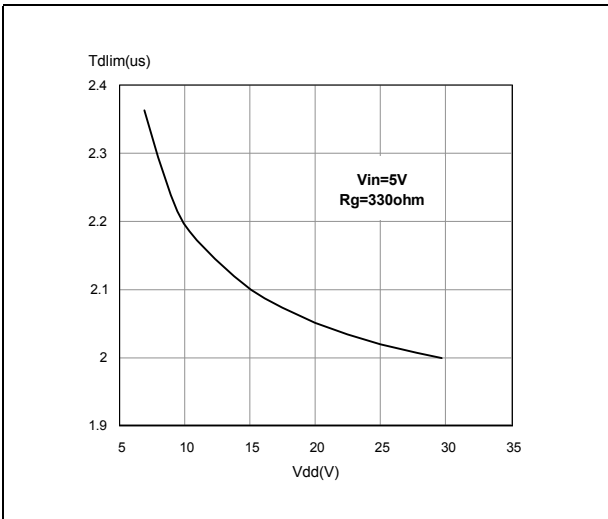
**Figure 27. Normalized input threshold voltage vs temperature**



**Figure 28. Normalized current limit vs junction temperature**



**Figure 29. Step response current limit**



### 3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC up to 50 kHz. The only difference from the user's standpoint is that a small DC current  $I_{ISS}$  (typ. 100  $\mu$ A) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- ? Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- ? Linear current limiter circuit: limits the drain current  $I_D$  to  $I_{lim}$  whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the over temperature threshold  $T_{jsh}$ .
- ? Over temperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Over temperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.
- ? Status feedback: in the case of an over temperature fault condition ( $T_j > T_{jsh}$ ), the device tries to sink a diagnostic current  $I_{gf}$  through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current  $I_{gf}$ , the input pin will fall to 0 V. This will not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current  $I_{ISS}$ .

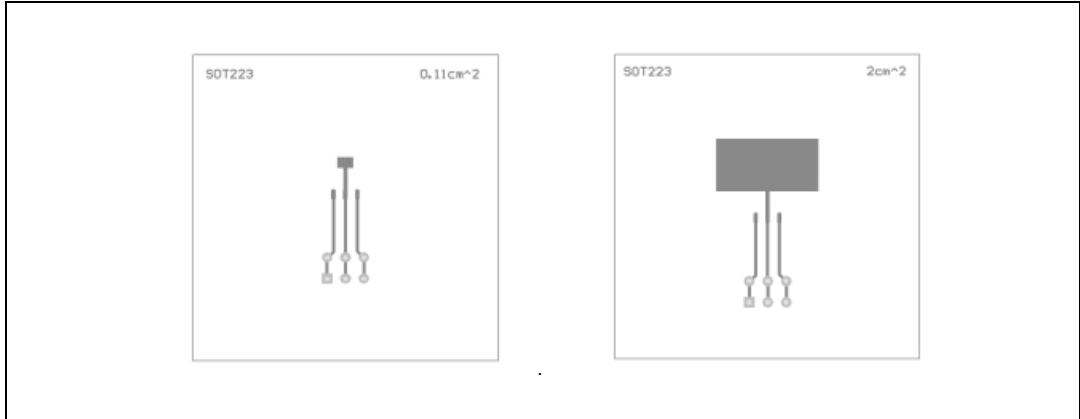
Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.



## 4 Package and PCB thermal data

### 4.1 SOT-223 thermal data

Figure 30. SOT-223 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35  $\mu$ m, Copper areas: from minimum pad layout to 0.8 cm<sup>2</sup>).

Figure 31. SOT-223  $R_{thj-amb}$  vs PCB copper area in open box free air condition

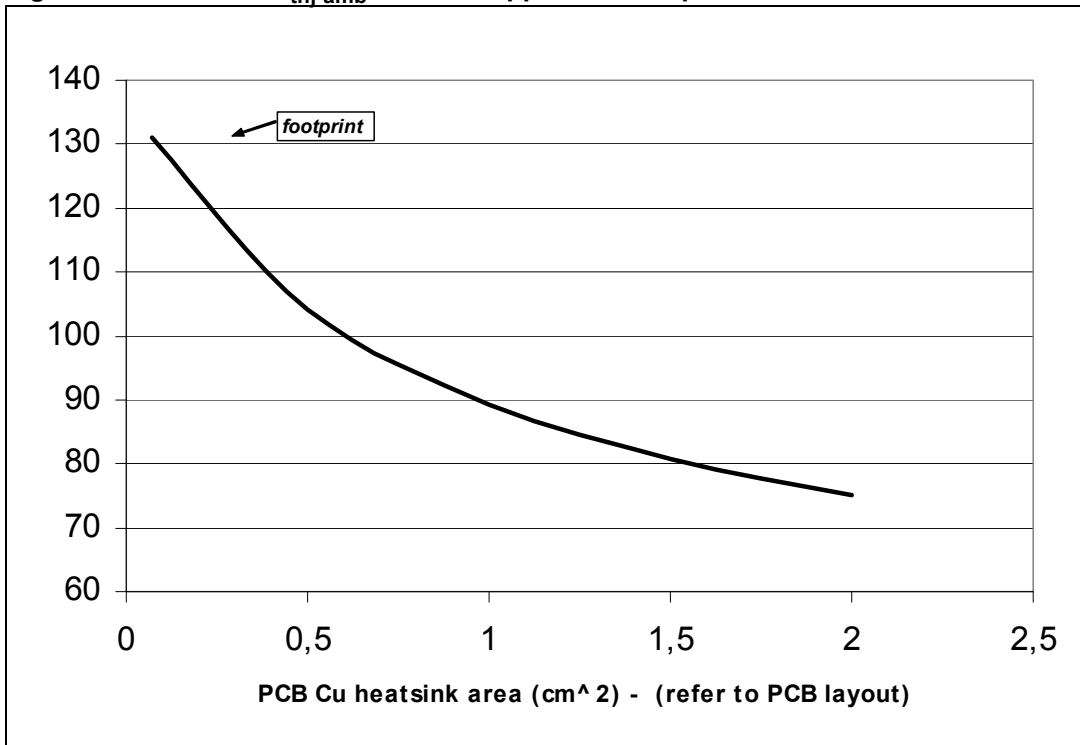
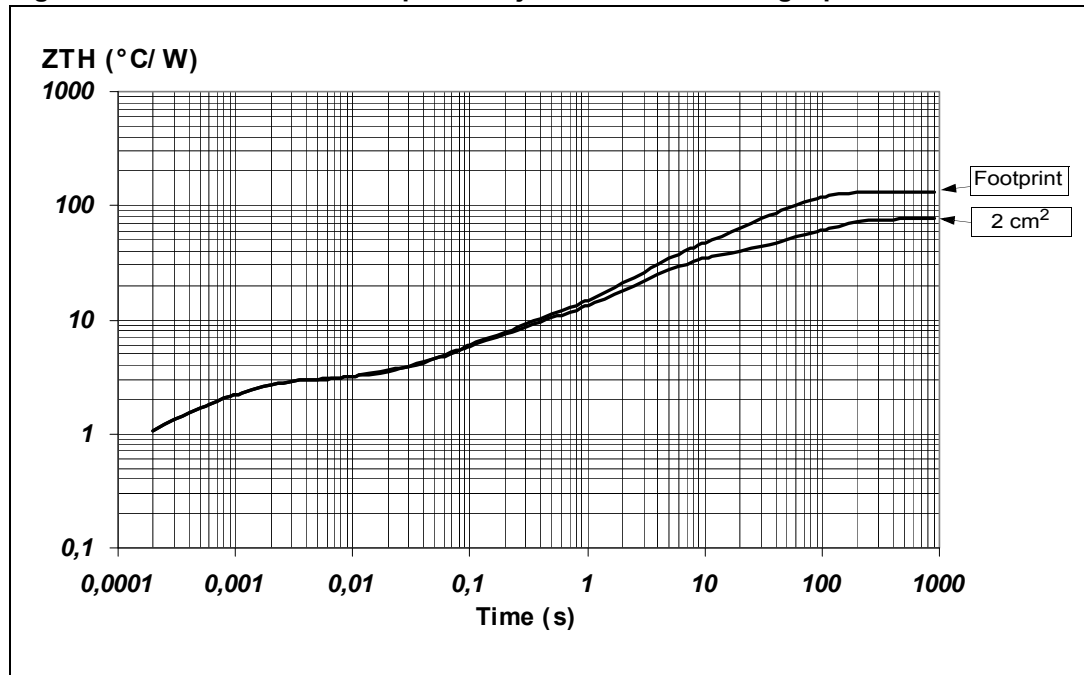


Figure 32. SOT-223 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 33. SOT-223 thermal fitting model of a single channel

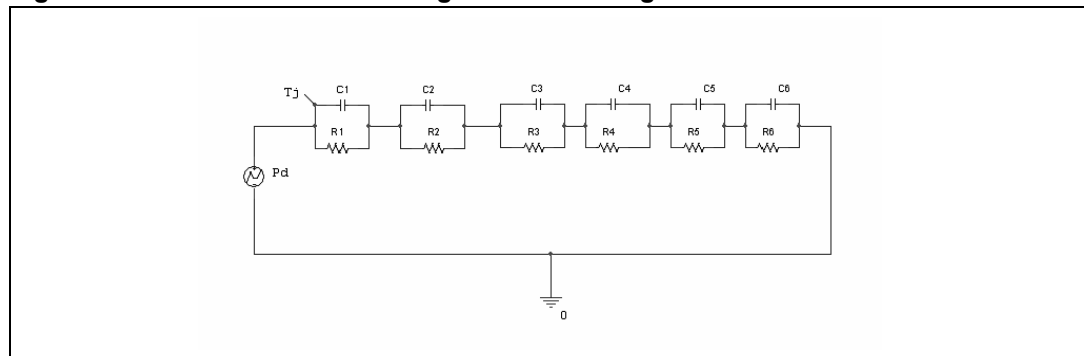


Table 5. SOT-223 thermal parameter

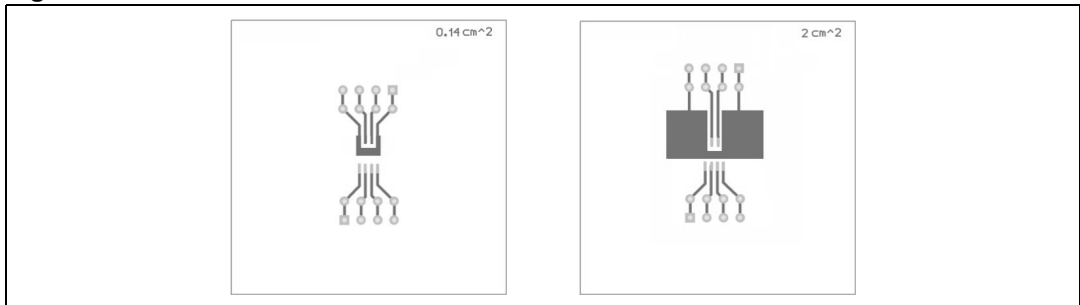
Area/island (cm <sup>2</sup> )	FP	2
R1 (°C/W)	0.8	
R2 (°C/W)	1.6	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	100	45

Table 5. SOT-223 thermal parameter (continued)

Area/island (cm <sup>2</sup> )	FP	2
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.03	
C4 (W·s/°C)	0.16	
C5 (W·s/°C)	1000	
C6 (W·s/°C)	0.5	2

## 4.2 SO-8 thermal data

Figure 34. SO-8 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness=35 μm, Copper areas: from minimum pad layout to 2 cm<sup>2</sup>).

Figure 35. SO-8  $R_{thj-amb}$  vs PCB copper area in open box free air condition

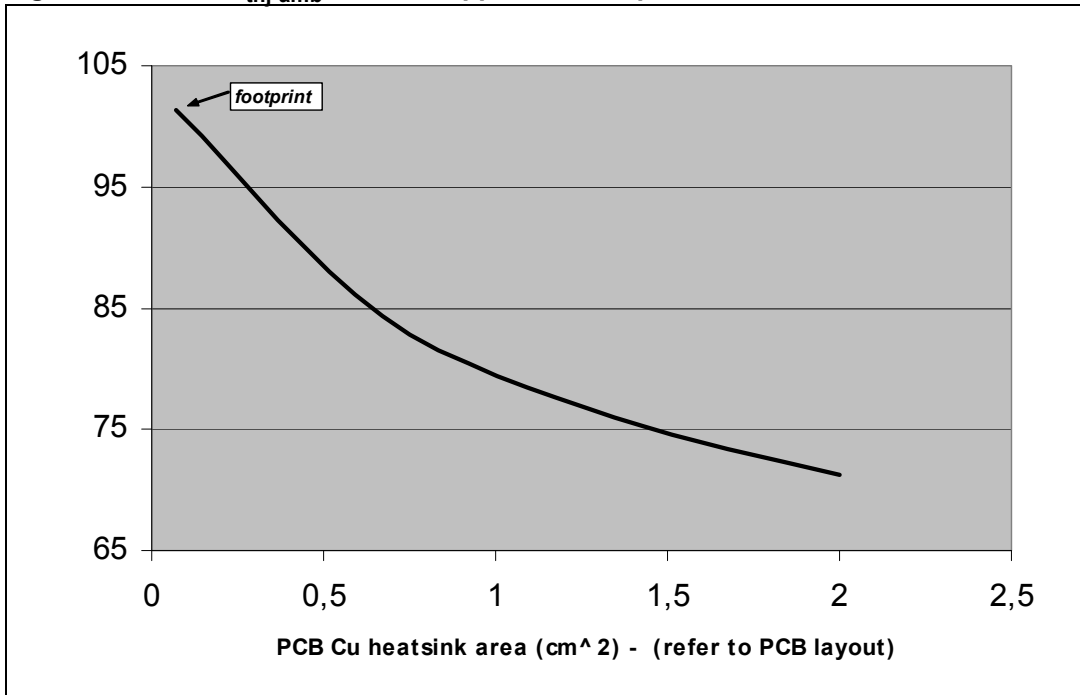
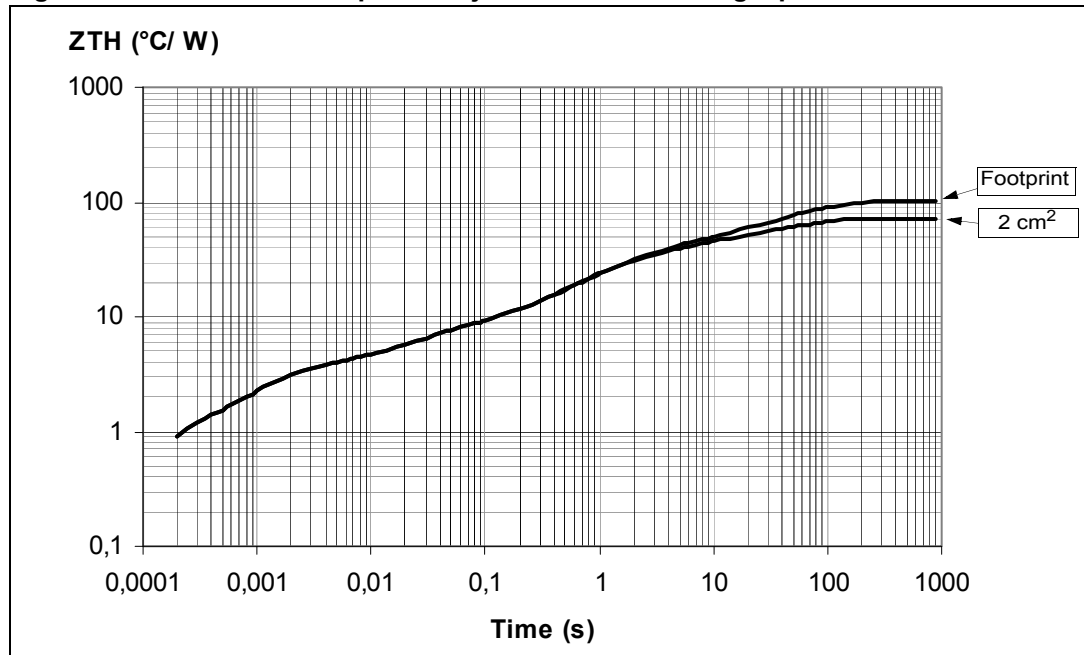


Figure 36. SO-8 thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 37. SO-8 thermal fitting model of a single channel

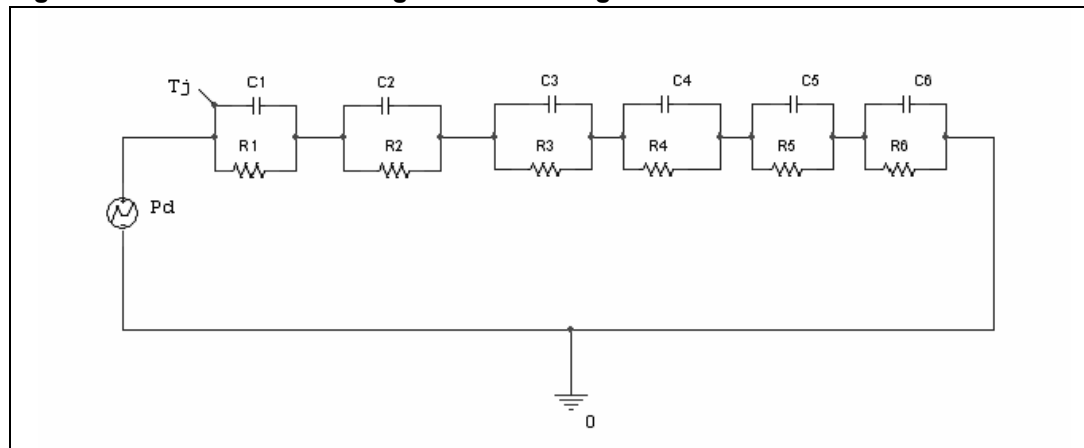


Table 6. SO-8 thermal parameter

Area/island (cm <sup>2</sup> )	FP	2
R1 (°C/W)	0.8	
R2 (°C/W)	2.6	
R3 (°C/W)	3.5	
R4 (°C/W)	21	

Table 6. SO-8 thermal parameter (continued)

Area/island (cm <sup>2</sup> )	FP	2
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

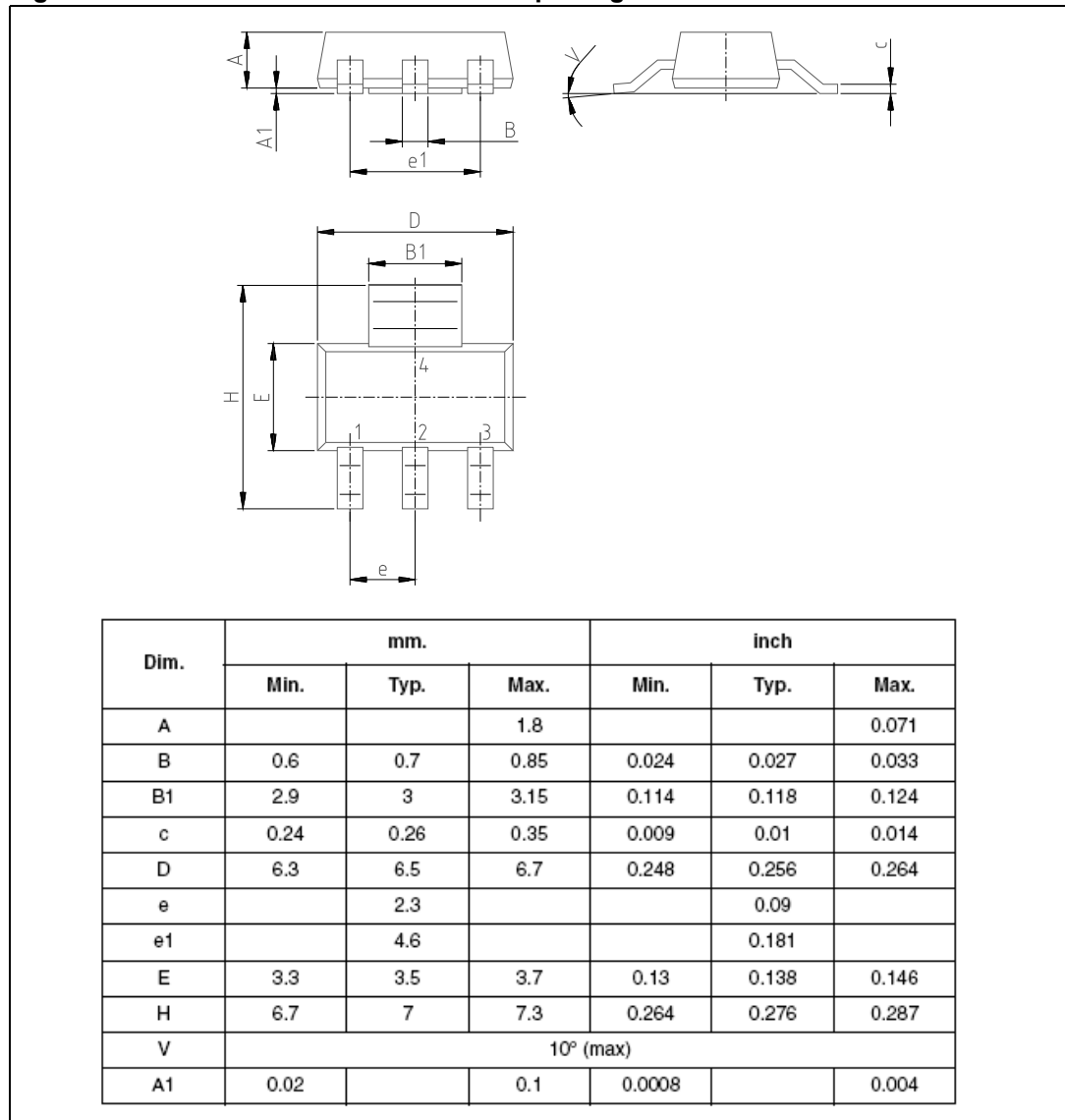
## 5 Package and packing information

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### 5.1 SOT-223 mechanical data

Figure 38. SOT-223 mechanical data and package outline



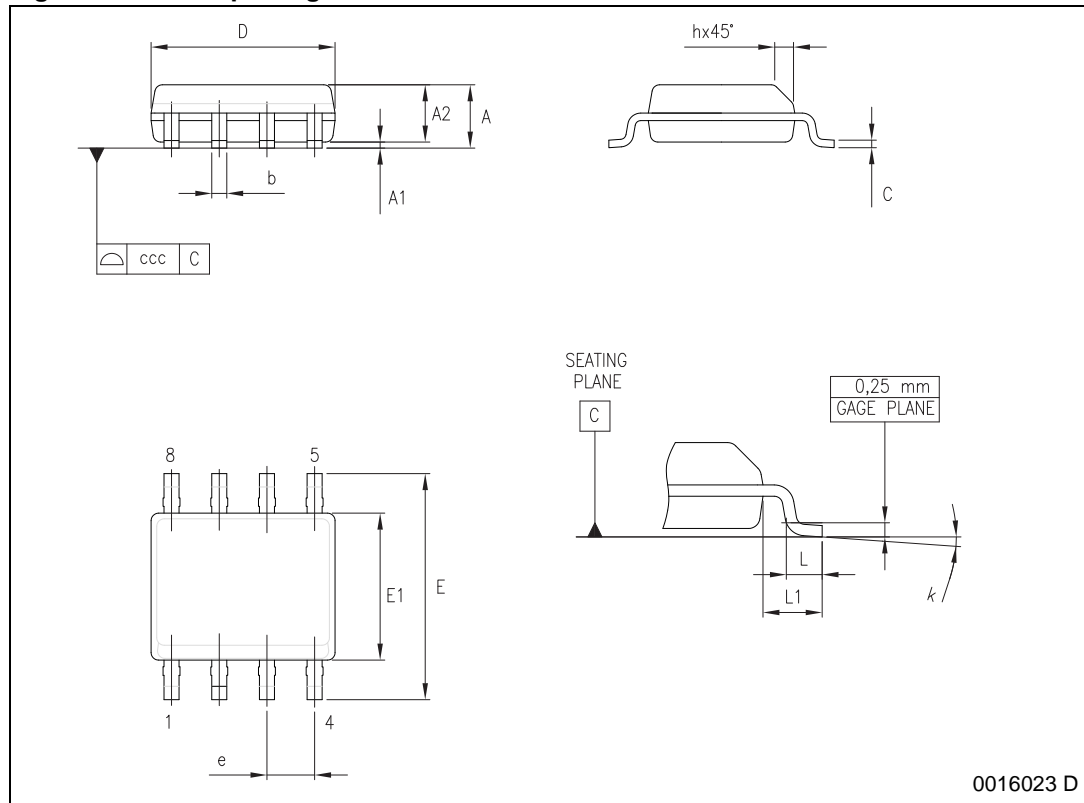
## 5.2 SO8 mechanical data

Table 7. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D <sup>(1)</sup>	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 <sup>(2)</sup>	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

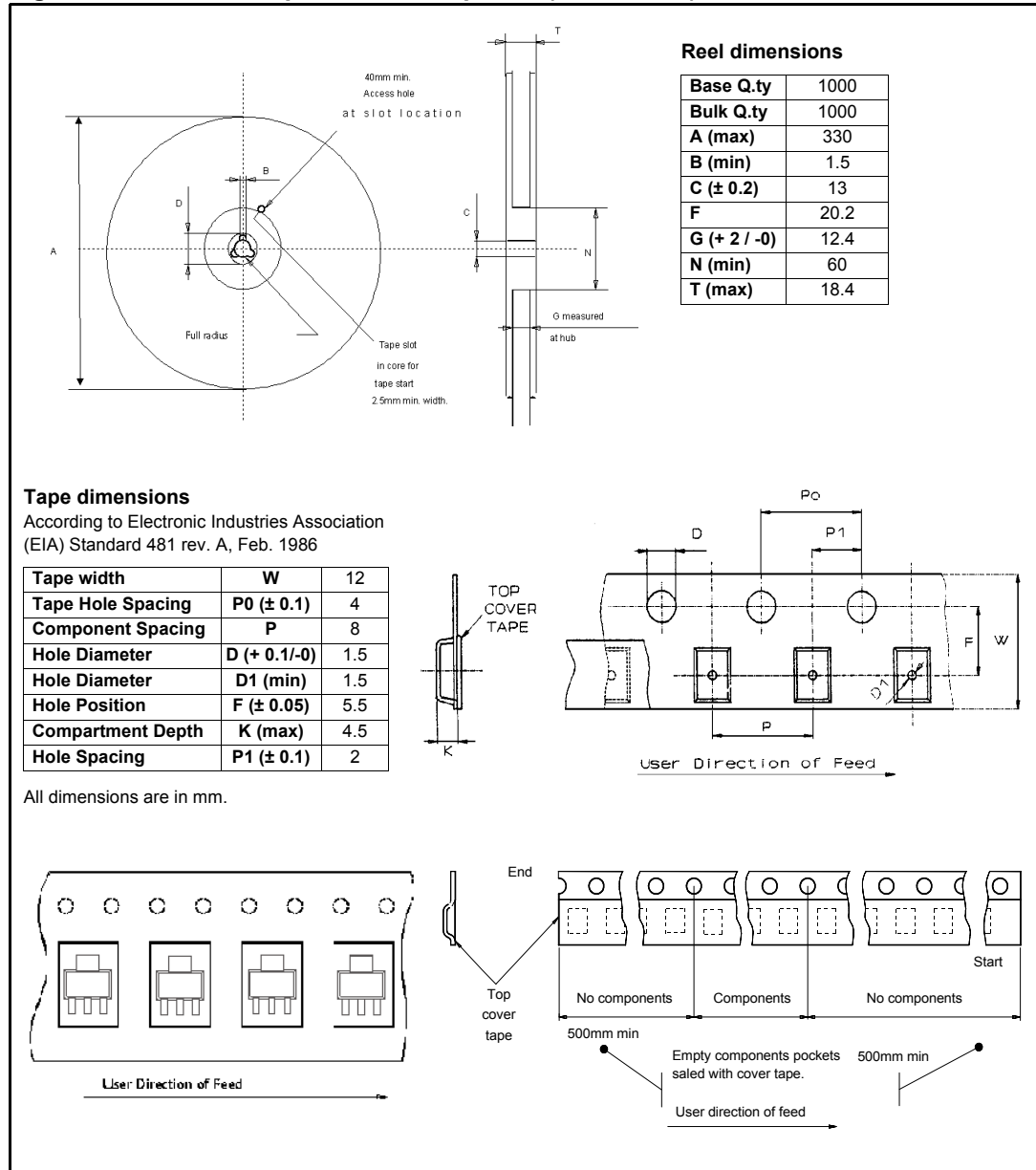
Figure 39. SO-8 package dimension





### 5.3 SOT-223 packing information

Figure 40. SOT-223 tape and reel shipment (suffix "TR")



### 5.4 SO8 packing information

Figure 41. SO-8 tube shipment (no suffix)

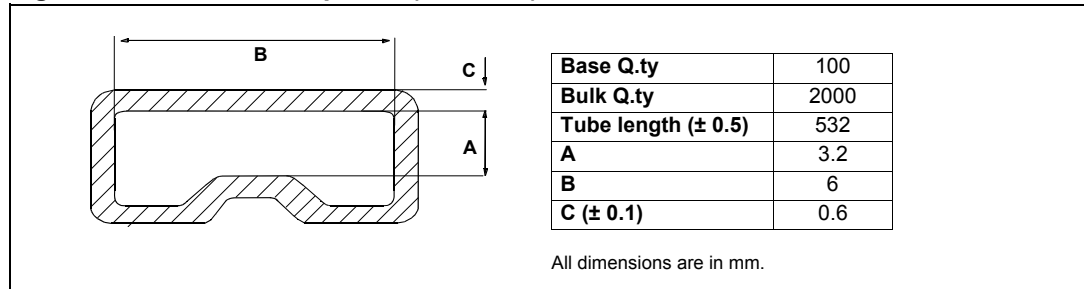
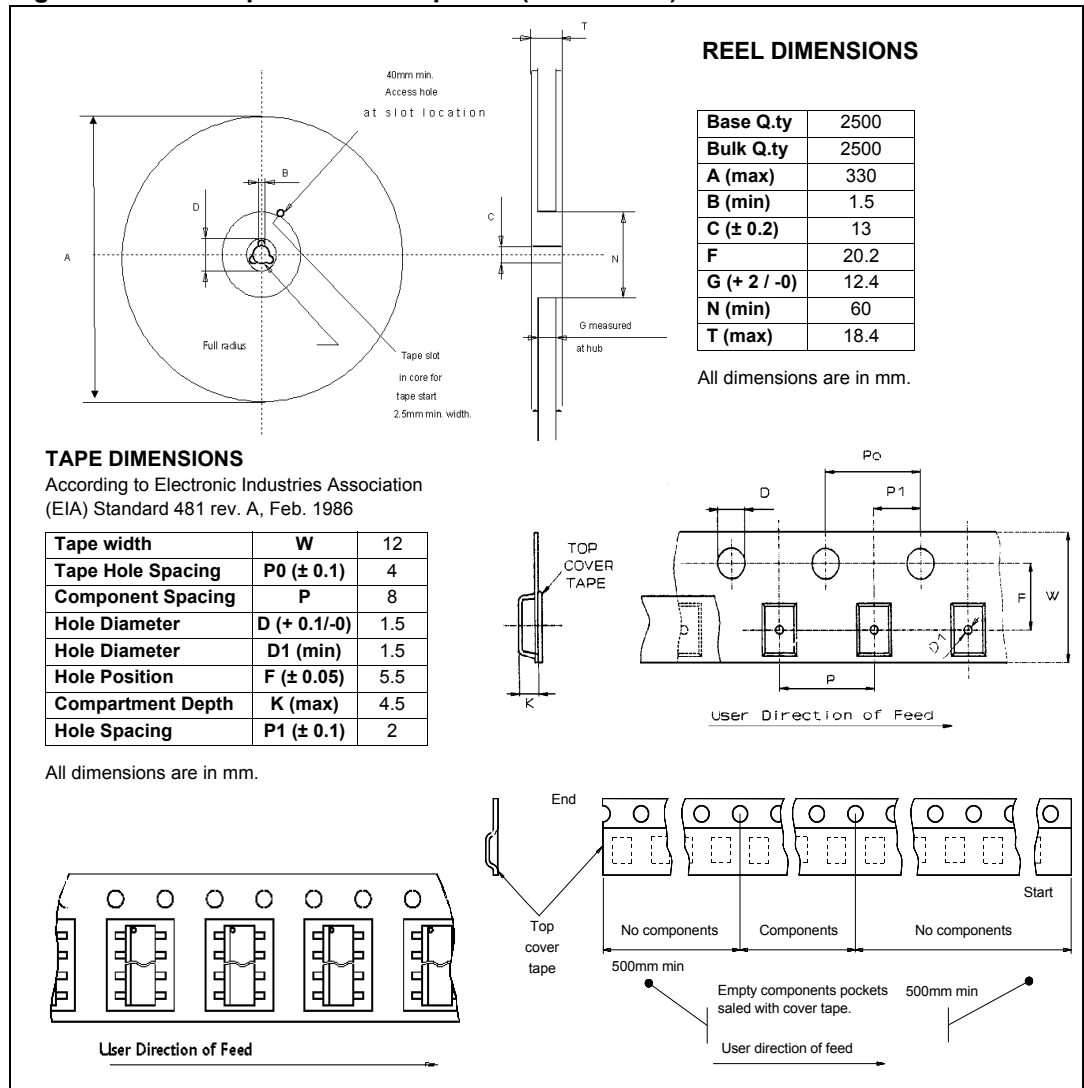


Figure 42. SO-8 tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 8. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
16-May-2009	1	Initial release.
29-Sep-2009	2	Removed target specification on cover page.
20-Sep-2013	3	Updated Disclaimer.

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