Dual 12-/14-/16-Bit 800 MSPS DAC with Low Power 32-Bit Complex NCO

Data Sheet

AD9785/AD9787/AD9788

FEATURES

Analog output: adjustable 8.7 mA to 31.7 mA, R_L = 25 Ω to 50 Ω
Low power, fine complex NCO allows carrier placement anywhere in DAC bandwidth while adding <300 mW power
Auxiliary DACs allow I and Q gain matching and offset control
Includes programmable I and Q phase compensation
Internal digital upconversion capability
Multiple chip synchronization interface
High performance, low noise PLL clock multiplier
Digital inverse sinc filter
100-lead, exposed pad TQFP package

APPLICATIONS

Wireless infrastructure
W-CDMA, CDMA2000, TD-SCDMA, WiMAX, GSM
Digital high or low IF synthesis
Transmit diversity
Wideband communications
LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9785/AD9787/AD9788 are 12-bit, 14-bit, and 16-bit, high dynamic range TxDAC® devices, respectively, that provide a sample rate of 800 MSPS, permitting multicarrier generation up to the Nyquist frequency. Features are included for optimizing direct conversion transmit applications, including complex digital modulation, as well as gain, phase, and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators, such as the ADL5375 family from Analog Devices, Inc. A serial peripheral interface (SPI) provides for programming and readback of many internal parameters. Full-scale output current can be programmed over a range of 10 mA to 30 mA. The AD9785/AD9787/AD9788 family is manufactured on a 0.18 µm CMOS process and operates from 1.8 V and 3.3 V supplies. It is enclosed in a 100-lead TQFP package.

PRODUCT HIGHLIGHTS

1. Low noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.
2. Proprietary DAC output switching technique enhances dynamic performance.
3. CMOS data input interface with adjustable setup and hold.
4. Low power complex 32-bit numerically controlled oscillators (NCOs).

TYPICAL SIGNAL CHAIN

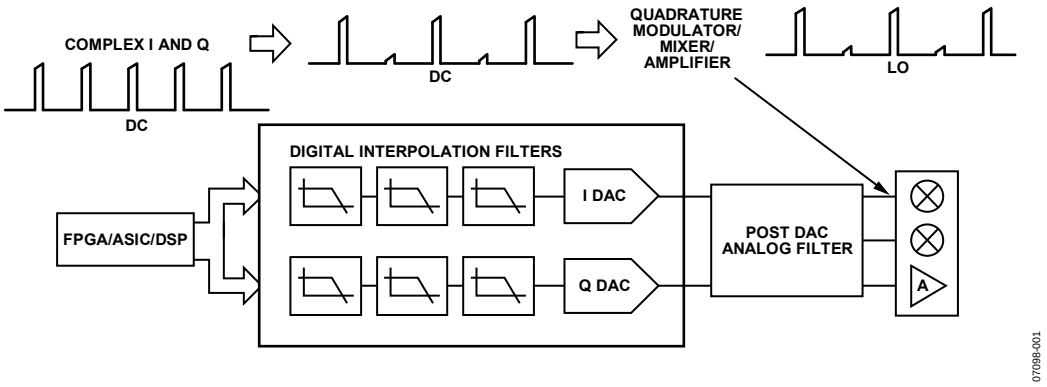


Figure 1.

Rev. C
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/2018—Rev. B to Rev. C

Change to Table 32 ... 45

2/2016—Rev. A to Rev. B

Changed SPI_CSB to SPI_CS ... Throughout
Changes to General Description Section ... 1
Changes to Figure 2 and Table 6 ... 7
Changes to Figure 3 and Table 7 ... 9
Changes to Figure 4 and Table 8 ... 11
Changes to Figure 52 ... 36
Updated Outline Dimensions ... 62
Changes to Ordering Guide ... 62

2/2009—Rev. 0 to Rev. A

Added Settling Time, to Within ±0.5 LSBs Parameter, Table 1 ... 3
Added REFCLK Frequency Range, PLL Enabled Parameter, Table 2 ... 4
Changes to SPI_SDIO—Serial Data I/O Section ... 23
Changes to Table 9 ... 24
Changes to Table 11 ... 26
Changes to Table 12 ... 27
Changes to Table 13 ... 28
Changes to Table 22 ... 32
Changes to Dual-Port Mode Section ... 33
Changes to Input Data RAM Section ... 37
Changes to Digital Amplitude and Offset Control Section ... 41
Changes to Direct Clocking Section ... 47

1/2008—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted. LVDS driver and receiver are compliant to the IEEE 1596 reduced range link, unless otherwise noted.

Table 1.

	AD9785			AD9787			AD9788			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.2			±0.5			±2.1		LSB
Integral Nonlinearity (INL)		±0.3			±1.0			±3.7		LSB
MAIN DAC OUTPUTS										
Offset Error	−0.001	0	+0.001	−0.001	0	+0.001	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)		±2			±2			±2		% FSR
Full-Scale Output Current	8.66	20.2	31.66	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
Gain DAC Monotonicity Guaranteed		10			10			10		Bits
Settling Time, to Within ±0.5 LSBs		20			20			20		ns
MAIN DAC TEMPERATURE DRIFT										
Offset		0.04			0.04			0.04		ppm/°C
Gain		100			100			100		ppm/°C
Reference Voltage		30			30			30		ppm/°C
AUX DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current[1]	−1.998		+1.998	−1.998		+1.998	−1.998		+1.998	mA
Output Compliance Range (Source)	0		1.6	0		1.6	0		1.6	V
Output Compliance Range (Sink)	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Resistance		1			1			1		MΩ
Aux DAC Monotonicity Guaranteed		10			10			10		Bits
REFERENCE										
Internal Reference Voltage		1.2			1.2			1.2		V
Output Resistance		5			5			5		kΩ
ANALOG SUPPLY VOLTAGES										
AVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
CVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES										
DVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
DVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
POWER CONSUMPTION										
1× Mode, f_{DATA} = 100 MSPS, PLL Off, IF = 2 MHz		375	450		375	450		375	450	mW
2× Mode, f_{DATA} = 100 MSPS, Inverse Sinc Off, PLL Off		533			533			533		mW
4× Mode, f_{DATA} = 100 MSPS, Inverse Sinc Off, PLL Off		754			754			754		mW
8× Mode, f_{DATA} = 100 MSPS, Inverse Sinc Off, PLL Off		1054			1054			1054		mW
Power-Down Mode		2.5	9.0		2.5	9.0		2.5	9.0	mW
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 Ω external resistor.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High		2.0			V
Input V_{IN} Logic Low				0.8	V
LVDS INPUT (SYNC_I+, SYNC_I–)	SYNC_I+ = V_{1A}, SYNC_I– = V_{1B}				
Input Voltage Range, V_{IA} or V_{IB}		825		1575	mV
Input Differential Threshold, V_{IDTH}		–100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
LVDS Input Rate ($f_{SYNC\_I} = f_{DATA}$)		30			MHz
Setup Time, SYNC_I to DAC Clock		0.45			ns
Hold Time, SYNC _I to DAC Clock		0.25			ns
LVDS DRIVER OUTPUTS (SYNC_O+, SYNC_O–)	SYNC_O+ = V_{OA}, SYNC_O– = V_{OB}, 100 Ω termination				
Output Voltage High, V_{OA} or V_{OB}		825		1575	mV
Output Voltage Low, V_{OA} or V_{OB}		1025			mV
Output Differential Voltage, $\|V_{OD}\|$		150	200	250	mV
Output Offset Voltage, V_{OS}		1150		1250	mV
Output Impedance, Single-Ended, R_O		80	100	120	Ω
DAC CLOCK INPUT (REFCLK+, REFCLK–)					
Differential Peak-to-Peak Voltage		400	800	1600	mV
Common-Mode Voltage		300	400	500	mV
Maximum Clock Rate					
DVDD18 = 1.8 V ± 5%		800			MHz
DVDD18 = 1.9 V ± 5%		900			MHz
REFCLK Frequency Range, PLL Enabled		30		250	MHz
MAXIMUM INPUT DATA RATE					
1× Interpolation			250		MSPS
2× Interpolation			250		MSPS
4× Interpolation					
DVDD18 = 1.8 V ± 5%		200			MSPS
DVDD18 = 1.9 V ± 5%		225			MSPS
8× Interpolation					
DVDD18 = 1.8 V ±5%		100			MSPS
DVDD18 = 1.9 V ± 5%		112.5			MSPS
SERIAL PERIPHERAL INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High		12.5			ns
Minimum Pulse Width Low		12.5			ns
Setup Time, SPI_SDIO to SCLK		2.8			ns
Hold Time, SPI_SDIO to SCLK		0.0			ns
Setup Time, $\overline{\text{SPI\_CS}}$ to SCLK		3.0			ns
Data Valid, SPI_SDO to SCLK		10.0			ns
INPUT DATA	All modes, –40°C to +85°C[1]				
Setup Time, Input Data to DATACLK		460			ns
Hold Time, Input Data to DATACLK		–1.5			ns
Setup Time, Input Data to REFCLK		–0.25			ns
Hold Time, Input Data to REFCLK		2.4			ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY (DACCLK CYCLES)					
1× Interpolation	With or without modulation		40		Cycles
2× Interpolation	With or without modulation		83		Cycles
4× Interpolation	With or without modulation		155		Cycles
8× Interpolation	With or without modulation		294		Cycles
Inverse Sinc			18		Cycles
POWER-UP TIME[2]			260		ms
DAC Wake-Up Time[3]	I_{OUT} current settling to 1%		22		ms
DAC Sleep Time[4]	I_{OUT} current to less than 1% of full scale		22		ms

[1] Timing vs. temperature and data valid windows are delineated in Table 25.
[2] Measured from $\overline{SPI\_CS}$ rising edge on Register 0x00; toggle Bit 4 from 0 to 1. VREF decoupling capacitor = 0.1 µF.
[3] Measured from $\overline{SPI\_CS}$ rising edge on Register 0x05 or Register 0x07; toggle Bit 15 or Bit 14 from 0 to 1.
[4] Measured from $\overline{SPI\_CS}$ rising edge on Register 0x05 or Register 0x07; toggle Bit 15 or Bit 14 from 1 to 0.

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 3.

	AD9785			AD9787			AD9788			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS-FREE DYNAMIC RANGE (IN-BAND SFDR)										
f_{DACCLK} = 200 MSPS, f_{OUT} = 70 MHz 1× Interpolation		80			82			83		dBc
f_{DACCLK} = 200 MSPS, f_{OUT} = 70 MHz 2× Interpolation		80			82			83		dBc
f_{DACCLK} = 200 MSPS, f_{OUT} = 70 MHz 4× Interpolation		78			80			81		dBc
f_{DACCLK} = 800 MSPS, f_{OUT} = 40 MHz 8× Interpolation		85			87			90		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)										
f_{DATA} = 200 MSPS, f_{OUT} = 50 MHz 1× Interpolation		80			82			83		dBc
f_{DATA} = 200 MSPS, f_{OUT} = 50 MHz 2× Interpolation		78			79			80		dBc
f_{DATA} = 200 MSPS, f_{OUT} = 100 MHz 4× Interpolation		78			79			80		dBc
f_{DATA} = 100 MSPS, f_{OUT} = 100 MHz 8× Interpolation		70			70			70		dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT TONE, 500 kHz TONE SPACING										
f_{DACCLK} = 200 MSPS, f_{OUT} = 80 MHz		−154			−157			−158		dBm/Hz
f_{DACCLK} = 400 MSPS, f_{OUT} = 80 MHz		−154			−158			−161		dBm/Hz
f_{DACCLK} = 800 MSPS, f_{OUT} = 80 MHz		−154			−159			−162		dBm/Hz
WCDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DACCLK} = 491.52 MSPS, f_{OUT} = 100 MHz 4× Interpolation		78			80			82		dBc
f_{DACCLK} = 491.52 MSPS, f_{OUT} = 200 MHz 4× Interpolation		72			74			76		dBc
WCDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DACCLK} = 491.52 MSPS, f_{OUT} = 100 MHz 4× Interpolation		80			82			88		dBc
f_{DACCLK} = 491.52 MSPS, f_{OUT} = 200 MHz 4× Interpolation		78			80			82		dBc

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD33 to AGND, DGND, CGND	−0.3 V to +3.6 V
DVDD33, DVDD18, CVDD18 to AGND, DGND, CGND	−0.3 V to +2.1 V
AGND to DGND, CGND	−0.3 V to +0.3 V
DGND to AGND, CGND	−0.3 V to +0.3 V
CGND to AGND, DGND	−0.3 V to +0.3 V
I120, VREF, IPTAT to AGND	−0.3 V to AVDD33 + 0.3 V
OUT1_P, OUT1_N, OUT2_P, OUT2_N, AUX1_P, AUX1_N, AUX2_P, AUX2_N to AGND	−1.0 V to AVDD33 + 0.3 V
P1D[15] to P1D[0], P2D[15] to P2D[0] to DGND	−0.3 V to DVDD33 + 0.3 V
DATACLK, TXENABLE to DGND	−0.3 V to DVDD33 + 0.3 V
REFCLK+, REFCLK−, RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I− to CGND	−0.3 V to CVDD18 + 0.3 V
RESET, IRQ, PLL_LOCK, SYNC_O+, $\overline{\text{SYNC\_O}}$−, SYNC_I+, SYNC_I−, $\overline{\text{SPI\_CS}}$, SCLK, SPI_SDIO, SPI_SDO to DGND	−0.3 V to DVDD33 + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

For this 100-lead, thermally enhanced TQFP, the exposed pad (EPAD) must be soldered to the ground plane. Note that these specifications are valid with no airflow movement.

Table 5. Thermal Resistance

Resistance	Unit	Conditions
θ_{JA}	19.1°C/W	EPAD soldered. No airflow.
θ_{JB}	12.4°C/W	EPAD soldered. No airflow.
θ_{JC}	7.1°C/W	EPAD soldered. No airflow.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

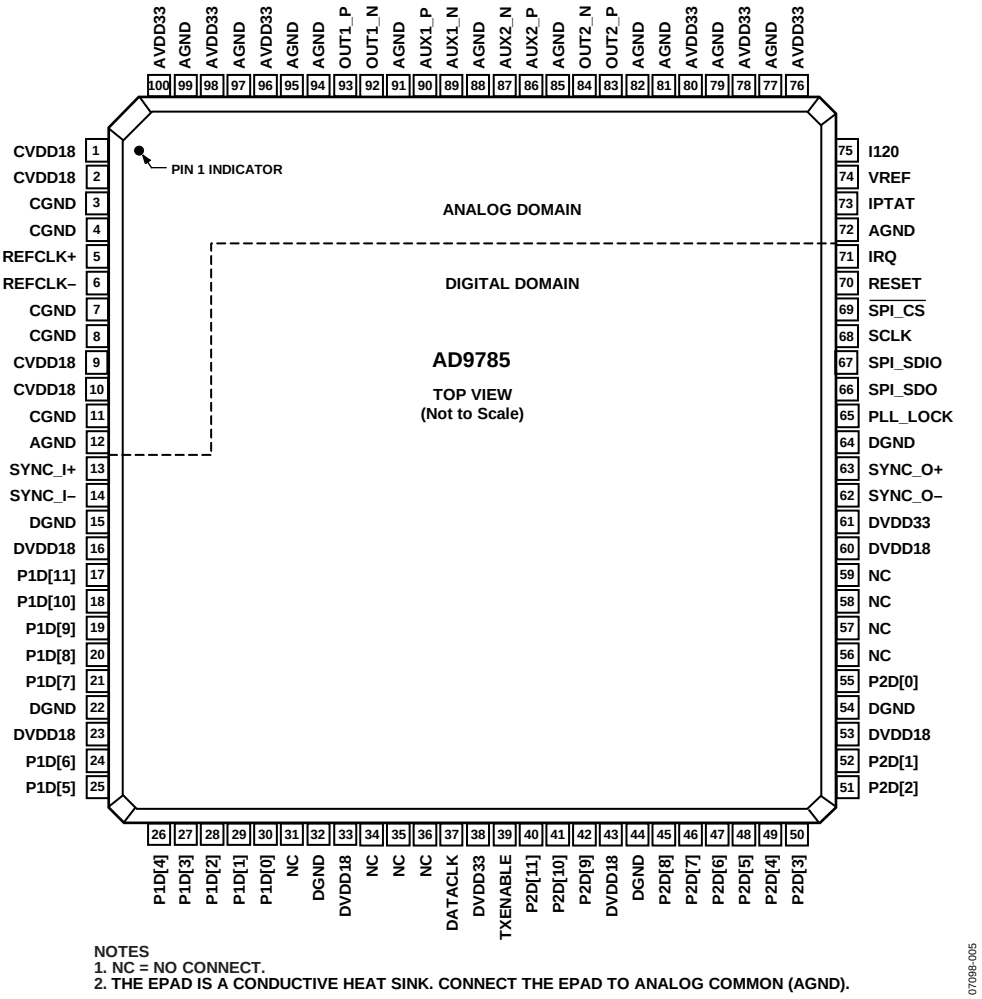


Figure 2. AD9785 Pin Configuration

Table 6. AD9785 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 9, 10	CVDD18	1.8 V Clock Supply.
3, 4, 7, 8, 11	CGND	Clock Common.
5	REFCLK+	Differential Clock Input, Positive.
6	REFCLK–	Differential Clock Input, Negative.
12, 72, 77, 79, 81, 82, 85, 88, 91, 94, 95, 97, 99	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input, Positive.
14	SYNC_I–	Differential Synchronization Input, Negative.
15, 22, 32, 44, 54, 64	DGND	Digital Common.
16, 23, 33, 43, 53, 60	DVDD18	1.8 V Digital Supply.
17	P1D[11]	Port 1, Data Input D11 (MSB).
18	P1D[10]	Port 1, Data Input D10.
19	P1D[9]	Port 1, Data Input D9.
20	P1D[8]	Port 1, Data Input D8.
21	P1D[7]	Port 1, Data Input D7.
24	P1D[6]	Port 1, Data Input D6.
25	P1D[5]	Port 1, Data Input D5.
26	P1D[4]	Port 1, Data Input D4.

Pin No.	Mnemonic	Description
27	P1D[3]	Port 1, Data Input D3.
28	P1D[2]	Port 1, Data Input D2.
29	P1D[1]	Port 1, Data Input D1.
30	P1D[0]	Port 1, Data Input D0 (LSB).
31, 34 to 36, 56 to 59	NC	No Connection Necessary. The NC pins are internally connected as digital inputs. They can be connected directly to ground.
37	DATACLK	Data Clock Output.
38, 61	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D[11]	Port 2, Data Input D11 (MSB).
41	P2D[10]	Port 2, Data Input D10.
42	P2D[9]	Port 2, Data Input D9.
45	P2D[8]	Port 2, Data Input D8.
46	P2D[7]	Port 2, Data Input D7.
47	P2D[6]	Port 2, Data Input D6.
48	P2D[5]	Port 2, Data Input D5.
49	P2D[4]	Port 2, Data Input D4.
50	P2D[3]	Port 2, Data Input D3.
51	P2D[2]	Port 2, Data Input D2.
52	P2D[1]	Port 2, Data Input D1.
55	P2D[0]	Port 2, Data Input D0 (LSB).
62	SYNC_O–	Differential Synchronization Output, Negative.
63	SYNC_O+	Differential Synchronization Output, Positive.
65	PLL_LOCK	PLL Lock Indicator.
66	SPI_SDO	SPI Port Data Output.
67	SPI_SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	$\overline{\text{SPI\_CS}}$	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76, 78, 80, 96, 98, 100	AVDD33	3.3 V Analog Supply.
83	OUT2_P	Differential DAC Current Output, Positive, Channel 2.
84	OUT2_N	Differential DAC Current Output, Negative, Channel 2.
86	AUX2_P	Auxiliary DAC Current Output, Positive, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Negative, Channel 2.
89	AUX1_N	Auxiliary DAC Current Output, Negative, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Positive, Channel 1.
92	OUT1_N	Differential DAC Current Output, Negative, Channel 1.
93	OUT1_P	Differential DAC Current Output, Positive, Channel 1.
	EPAD	Exposed Pad. The EPAD is a conductive heat sink. Connect the EPAD to analog common (AGND).

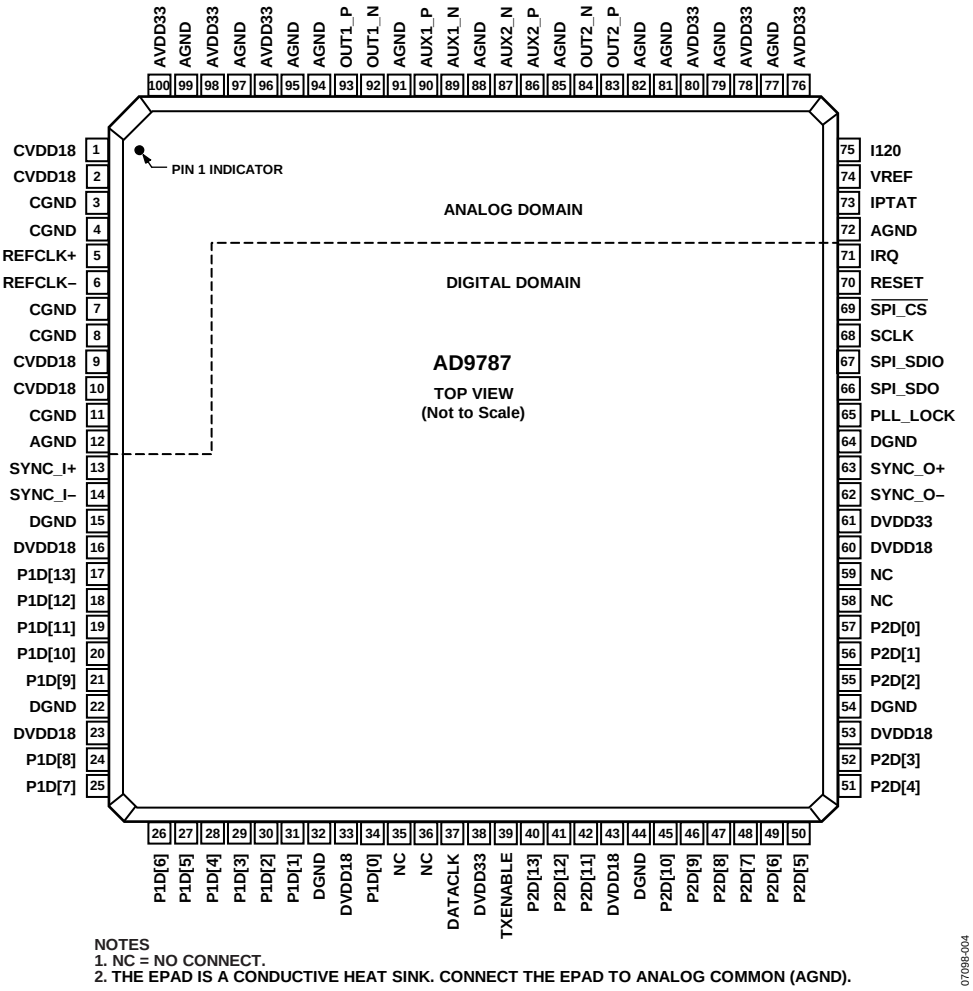


Figure 3. AD9787 Pin Configuration

Table 7. AD9787 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 9, 10	CVDD18	1.8 V Clock Supply.
3, 4, 7, 8, 11	CGND	Clock Common.
5	REFCLK+	Differential Clock Input, Positive.
6	REFCLK–	Differential Clock Input, Negative.
12, 72, 77, 79, 81, 82, 85, 88, 91, 94, 95, 97, 99	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input, Positive.
14	SYNC_I–	Differential Synchronization Input, Negative.
15, 22, 32, 44, 54, 64	DGND	Digital Common.
16, 23, 33, 43, 53, 60	DVDD18	1.8 V Digital Supply.
17	P1D[13]	Port 1, Data Input D13 (MSB).
18	P1D[12]	Port 1, Data Input D12.
19	P1D[11]	Port 1, Data Input D11.
20	P1D[10]	Port 1, Data Input D10.
21	P1D[9]	Port 1, Data Input D9.
24	P1D[8]	Port 1, Data Input D8.
25	P1D[7]	Port 1, Data Input D7.
26	P1D[6]	Port 1, Data Input D6.
27	P1D[5]	Port 1, Data Input D5.

Pin No.	Mnemonic	Description
28	P1D[4]	Port 1, Data Input D4.
29	P1D[3]	Port 1, Data Input D3.
30	P1D[2]	Port 1, Data Input D2.
31	P1D[1]	Port 1, Data Input D1.
34	P1D[0]	Port 1, Data Input D0 (LSB).
35, 36, 58, 59	NC	No Connection Necessary. The NC pins are internally connected as digital inputs. They can be connected directly to ground.
37	DATACLK	Data Clock Output.
38, 61	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D[13]	Port 2, Data Input D13 (MSB).
41	P2D[12]	Port 2, Data Input D12.
42	P2D[11]	Port 2, Data Input D11.
45	P2D[10]	Port 2, Data Input D10.
46	P2D[9]	Port 2, Data Input D9.
47	P2D[8]	Port 2, Data Input D8.
48	P2D[7]	Port 2, Data Input D7.
49	P2D[6]	Port 2, Data Input D6.
50	P2D[5]	Port 2, Data Input D5.
51	P2D[4]	Port 2, Data Input D4.
52	P2D[3]	Port 2, Data Input D3.
55	P2D[2]	Port 2, Data Input D2.
56	P2D[1]	Port 2, Data Input D1.
57	P2D[0]	Port 2, Data Input D0 (LSB).
62	SYNC_O–	Differential Synchronization Output, Negative.
63	SYNC_O+	Differential Synchronization Output, Positive.
65	PLL_LOCK	PLL Lock Indicator.
66	SPI_SDO	SPI Port Data Output.
67	SPI_SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	$\overline{\text{SPI\_CS}}$	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76, 78, 80, 96, 98, 100	AVDD33	3.3 V Analog Supply.
83	OUT2_P	Differential DAC Current Output, Positive, Channel 2.
84	OUT2_N	Differential DAC Current Output, Negative, Channel 2.
86	AUX2_P	Auxiliary DAC Current Output, Positive, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Negative, Channel 2.
89	AUX1_N	Auxiliary DAC Current Output, Negative, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Positive, Channel 1.
92	OUT1_N	Differential DAC Current Output, Negative, Channel 1.
93	OUT1_P	Differential DAC Current Output, Positive, Channel 1.
	EPAD	Exposed Paddle. The EPAD is a conductive heat sink. Connect the EPAD to analog common (AGND).

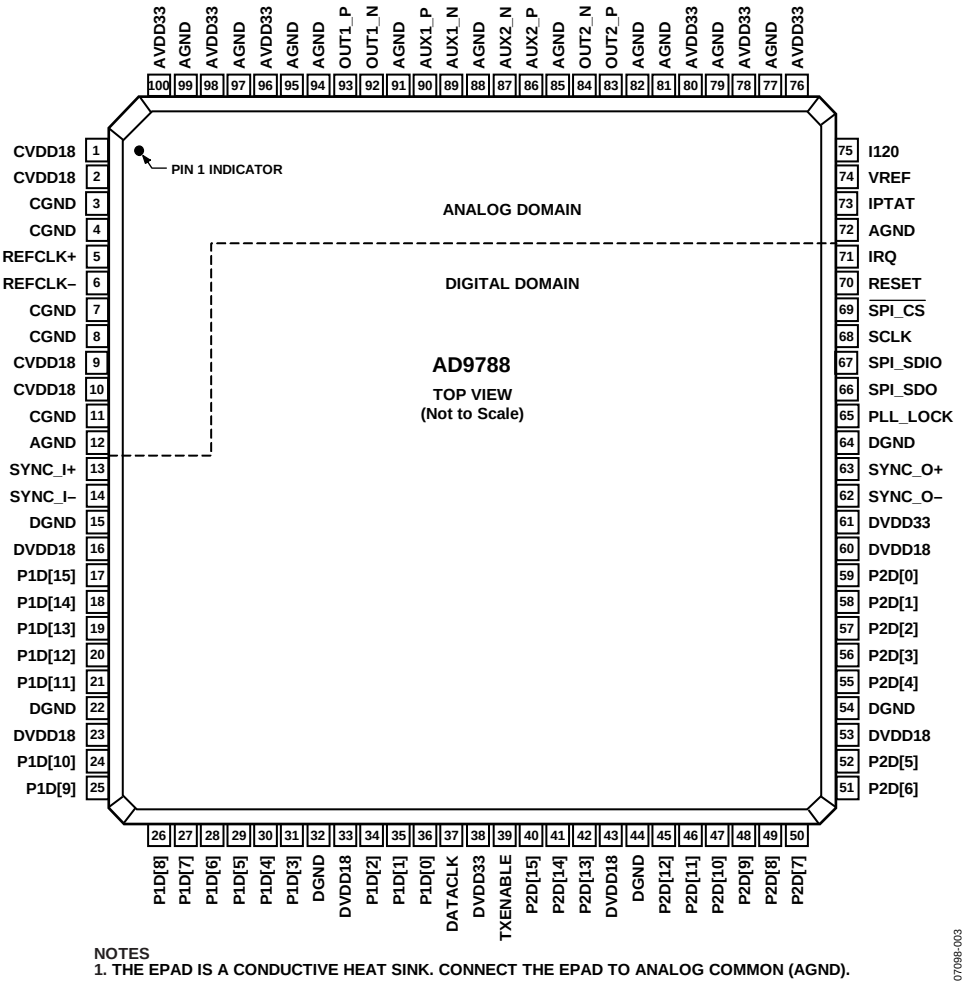


Figure 4. AD9788 Pin Configuration

Table 8. AD9788 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 9, 10	CVDD18	1.8 V Clock Supply.
3, 4, 7, 8, 11	CGND	Clock Common.
5	REFCLK+	Differential Clock Input, Positive.
6	REFCLK–	Differential Clock Input, Negative.
12, 72, 77, 79, 81, 82, 85, 88, 91, 94, 95, 97, 99	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input, Positive.
14	SYNC_I–	Differential Synchronization Input, Negative.
15, 22, 32, 44, 54, 64	DGND	Digital Common.
16, 23, 33, 43, 53, 60	DVDD18	1.8 V Digital Supply.
17	P1D[15]	Port 1, Data Input D15 (MSB).
18	P1D[14]	Port 1, Data Input D14.
19	P1D[13]	Port 1, Data Input D13.
20	P1D[12]	Port 1, Data Input D12.
21	P1D[11]	Port 1, Data Input D11.
24	P1D[10]	Port 1, Data Input D10.
25	P1D[9]	Port 1, Data Input D9.
26	P1D[8]	Port 1, Data Input D8.
27	P1D[7]	Port 1, Data Input D7.
28	P1D[6]	Port 1, Data Input D6.
29	P1D[5]	Port 1, Data Input D5.

Pin No.	Mnemonic	Description
30	P1D[4]	Port 1, Data Input D4.
31	P1D[3]	Port 1, Data Input D3.
34	P1D[2]	Port 1, Data Input D2.
35	P1D[1]	Port 1, Data Input D1.
36	P1D[0]	Port 1, Data Input D0 (LSB).
37	DATACLK	Data Clock Output.
38, 61	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D[15]	Port 2, Data Input D15 (MSB).
41	P2D[14]	Port 2, Data Input D14.
42	P2D[13]	Port 2, Data Input D13.
45	P2D[12]	Port 2, Data Input D12.
46	P2D[11]	Port 2, Data Input D11.
47	P2D[10]	Port 2, Data Input D10.
48	P2D[9]	Port 2, Data Input D9.
49	P2D[8]	Port 2, Data Input D8.
50	P2D[7]	Port 2, Data Input D7.
51	P2D[6]	Port 2, Data Input D6.
52	P2D[5]	Port 2, Data Input D5.
55	P2D[4]	Port 2, Data Input D4.
56	P2D[3]	Port 2, Data Input D3.
57	P2D[2]	Port 2, Data Input D2.
58	P2D[1]	Port 2, Data Input D1.
59	P2D[0]	Port 2, Data Input D0 (LSB).
62	SYNC_O–	Differential Synchronization Output, Negative.
63	SYNC_O+	Differential Synchronization Output, Positive.
65	PLL_LOCK	PLL Lock Indicator.
66	SPI_SDO	SPI Port Data Output.
67	SPI_SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	$\overline{\text{SPI\_CS}}$	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76, 78, 80, 96, 98, 100	AVDD33	3.3 V Analog Supply.
83	OUT2_P	Differential DAC Current Output, Positive, Channel 2.
84	OUT2_N	Differential DAC Current Output, Negative, Channel 2.
86	AUX2_P	Auxiliary DAC Current Output, Positive, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Negative, Channel 2.
89	AUX1_N	Auxiliary DAC Current Output, Negative, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Positive, Channel 1.
92	OUT1_N	Differential DAC Current Output, Negative, Channel 1.
93	OUT1_P	Differential DAC Current Output, Positive, Channel 1.
	EPAD	Exposed Paddle. The EPAD is a conductive heat sink. Connect the EPAD to analog common (AGND).

TYPICAL PERFORMANCE CHARACTERISTICS

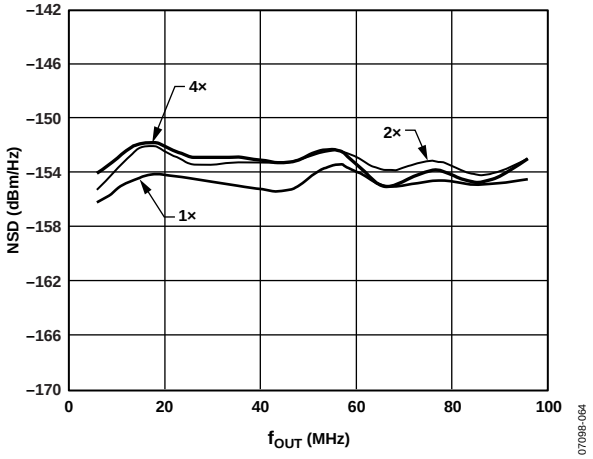


Figure 5. AD9785 Noise Spectral Density vs. f_{OUT}, Multitone Input, f_{DATA} = 200 MSPS

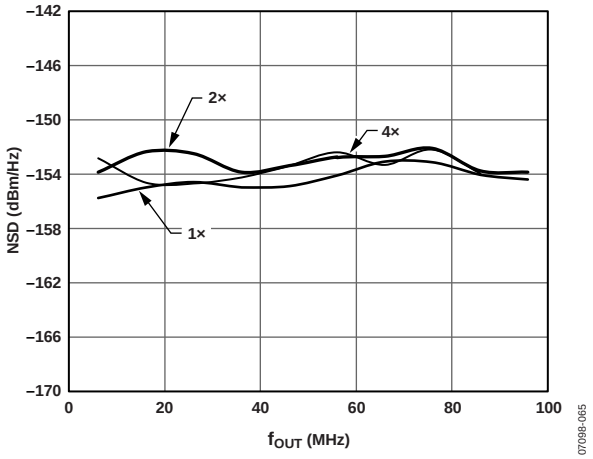


Figure 6. AD9785 Noise Spectral Density vs. f_{OUT}, Single-Tone Input, f_{DATA} = 200 MSPS

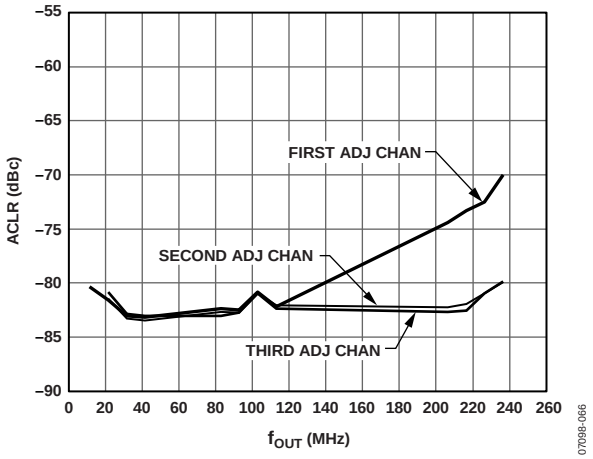


Figure 7. AD9785 ACLR, 4× Interpolation, f_{DATA} = 122.88 MSPS

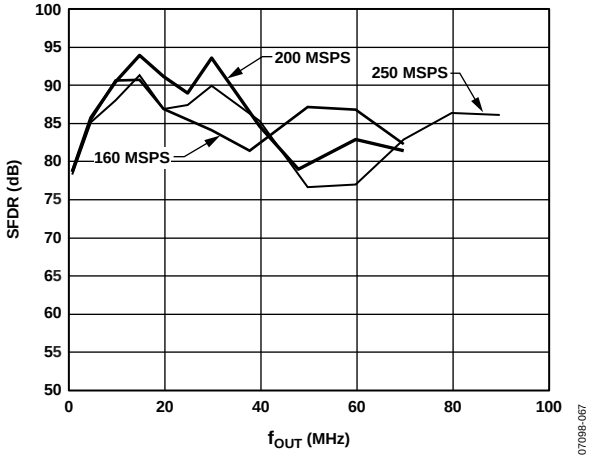


Figure 8. AD9785 In-Band SFDR vs. f_{OUT}, 2× Interpolation

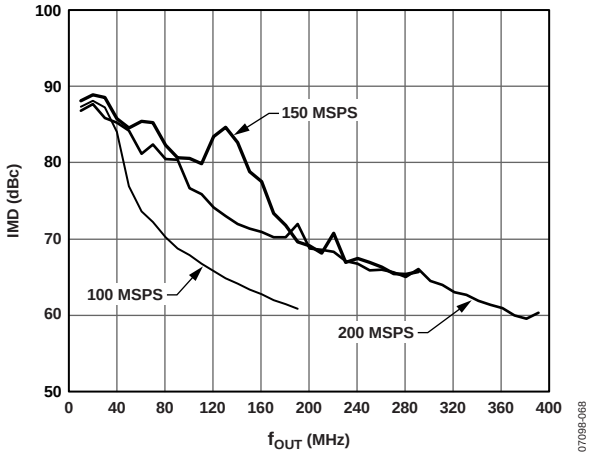


Figure 9. AD9785 IMD vs. f_{OUT}, 4× Interpolation

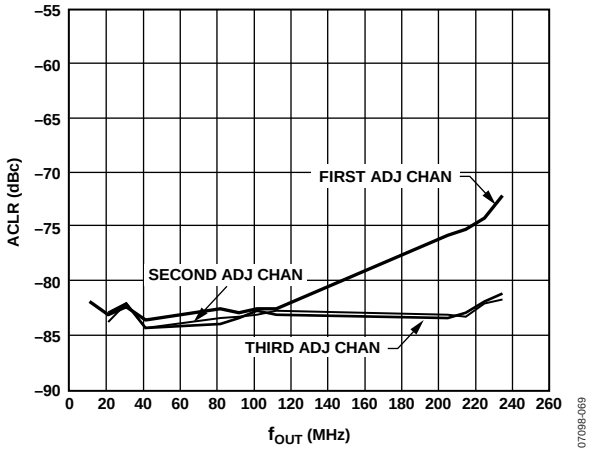


Figure 10. AD9787 ACLR, 4× Interpolation, f_{DATA} = 122.88 MSPS

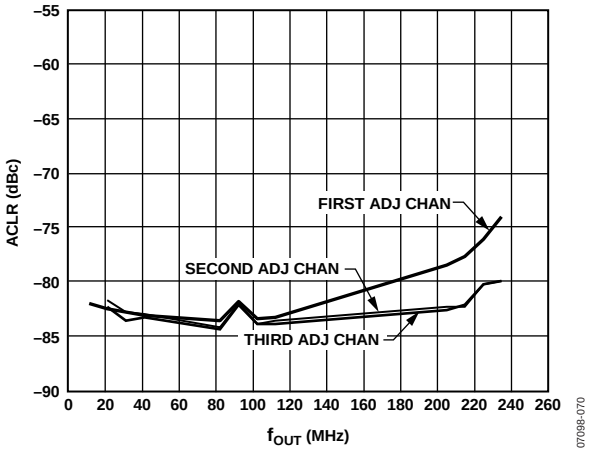


Figure 11. AD9787 ACLR, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = −3 dB

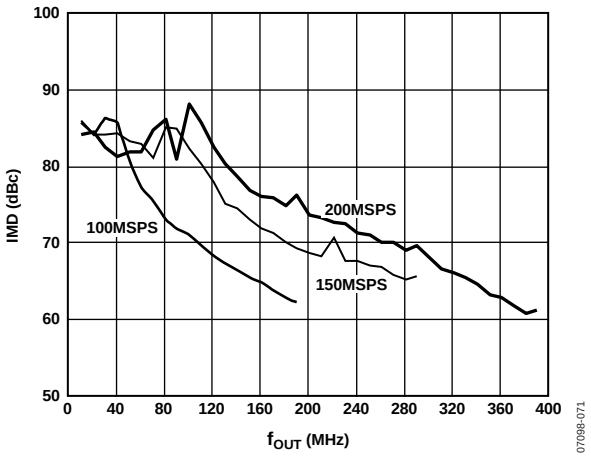


Figure 12. AD9787 IMD vs. f_{OUT}, 4× Interpolation

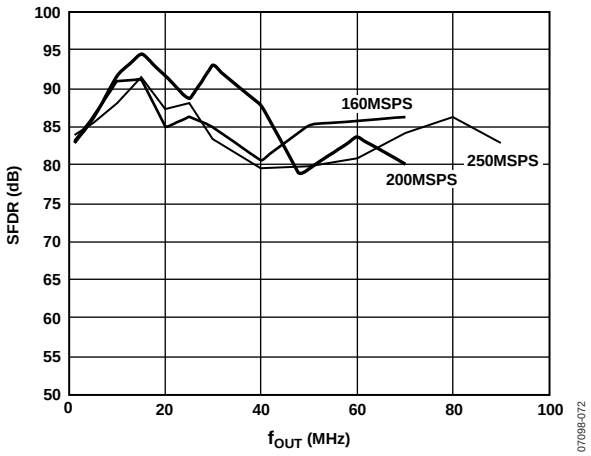


Figure 13. AD9787 In-Band SFDR vs. f_{OUT}, 2× Interpolation

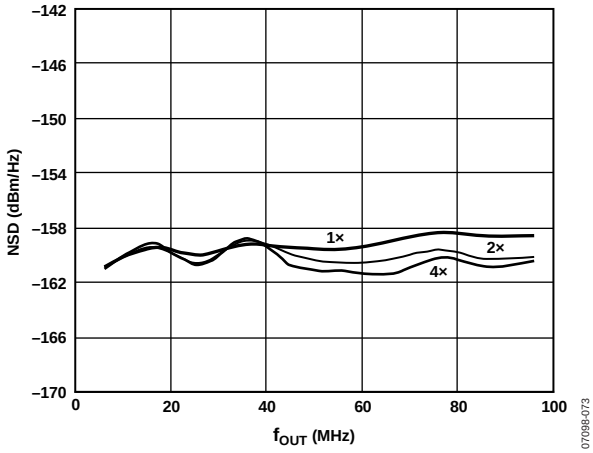


Figure 14. AD9787 Noise Spectral Density vs. f_{OUT} over Output Frequency of Multitone Input, f_{DATA} = 200 MSPS

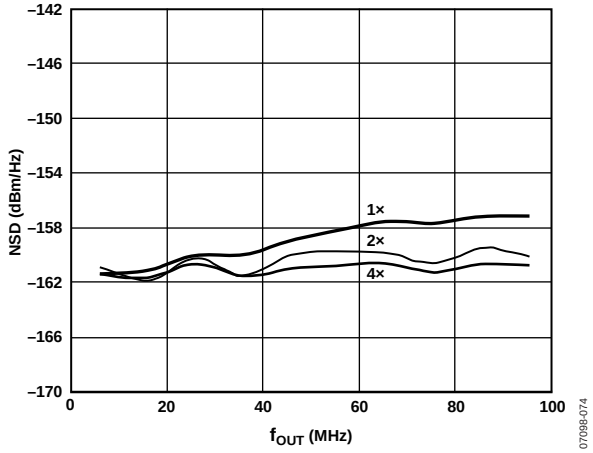


Figure 15. AD9787 Noise Spectral Density vs. f_{OUT}, Single-Tone Input, f_{DATA} = 200 MSPS

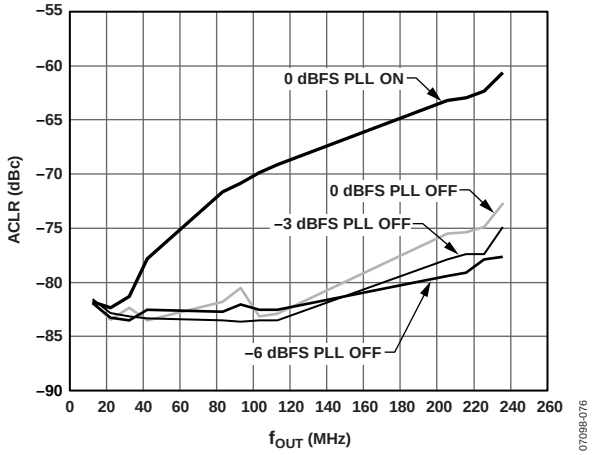


Figure 16. AD9788 ACLR for First Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, NCO Translates Baseband Signal to IF

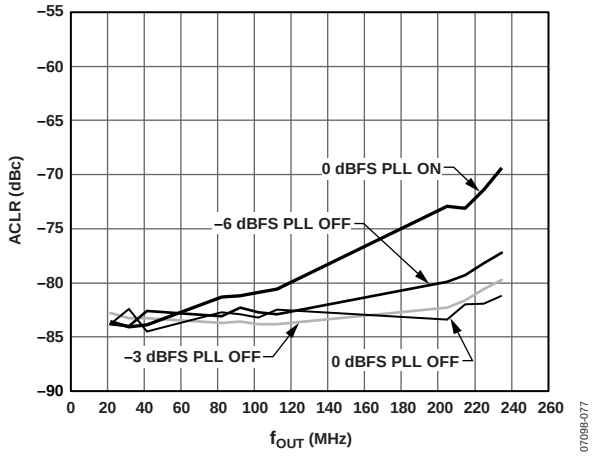


Figure 17. AD9788 ACLR for Second Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, NCO Translates Baseband Signal to IF

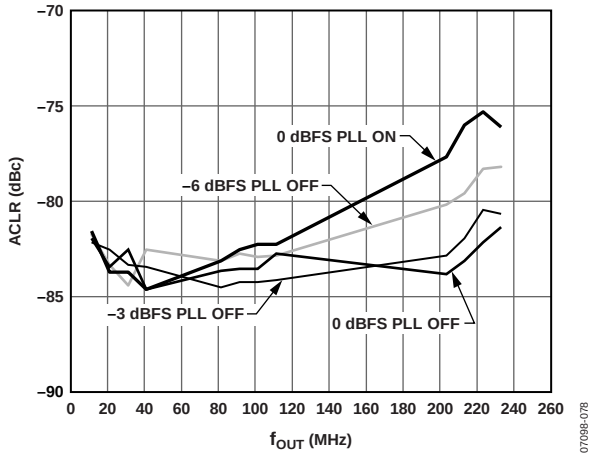


Figure 18. AD9788 ACLR for Third Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, NCO Translates Baseband Signal to IF

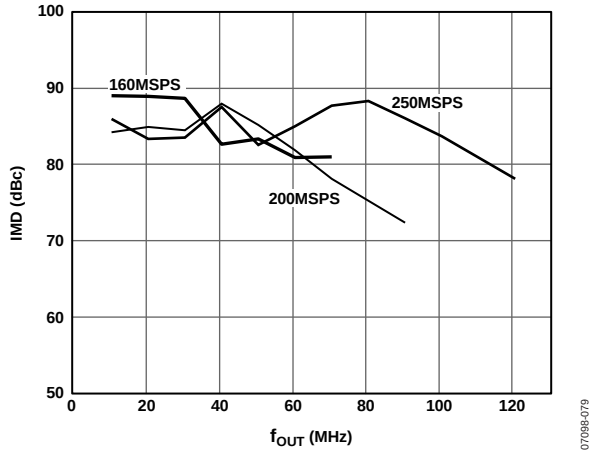


Figure 19. AD9788 IMD vs. f_{OUT}, 1× Interpolation

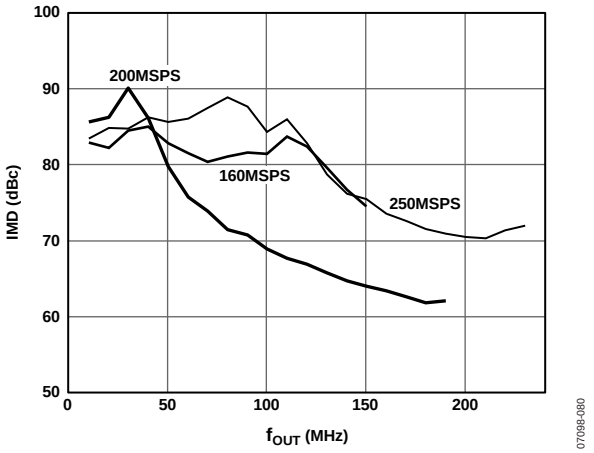


Figure 20. AD9788 IMD vs. f_{OUT}, 2× Interpolation

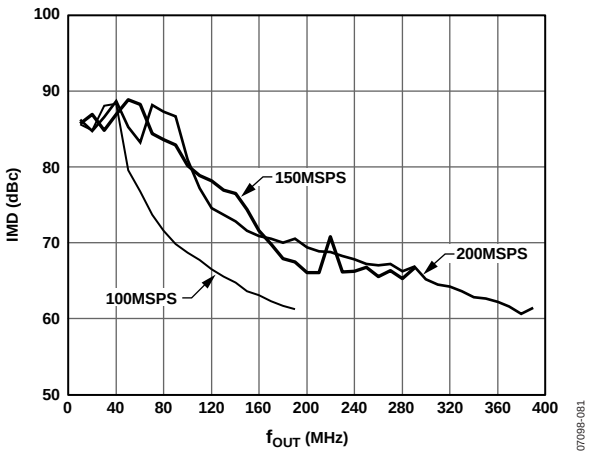


Figure 21. AD9788 IMD vs. f_{OUT}, 4× Interpolation

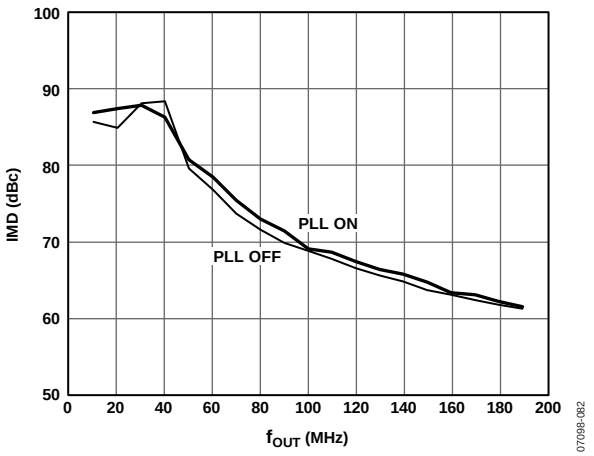


Figure 22. AD9788 IMD vs. f_{OUT}, 8× Interpolation, f_{DATA} = 100 MSPS, PLL On/PLL Off

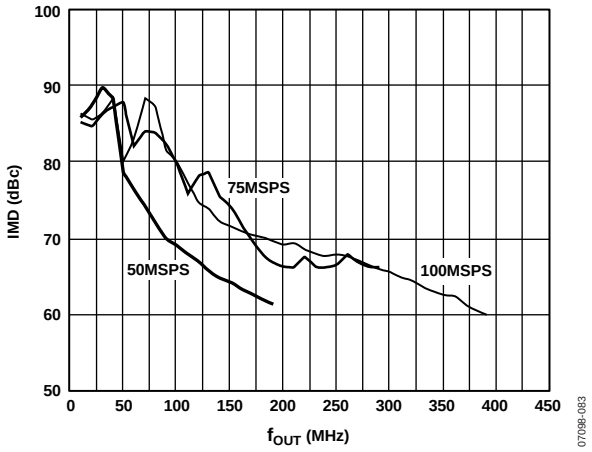


Figure 23. AD9788 IMD vs. f_{OUT}, 8× Interpolation

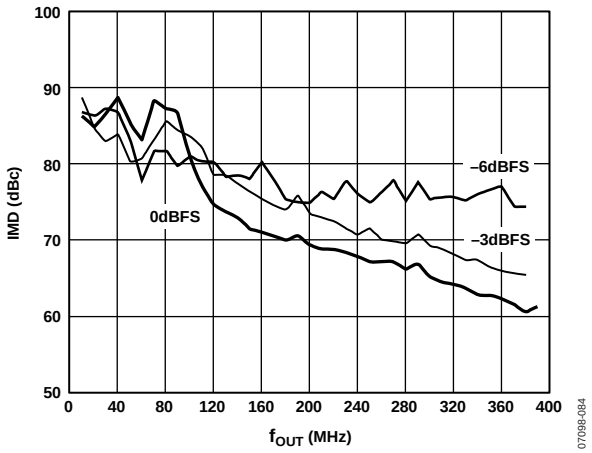


Figure 24. AD9788 IMD Performance vs. Digital Full-Scale Input, 4× Interpolation, f_{DATA} = 200 MSPS

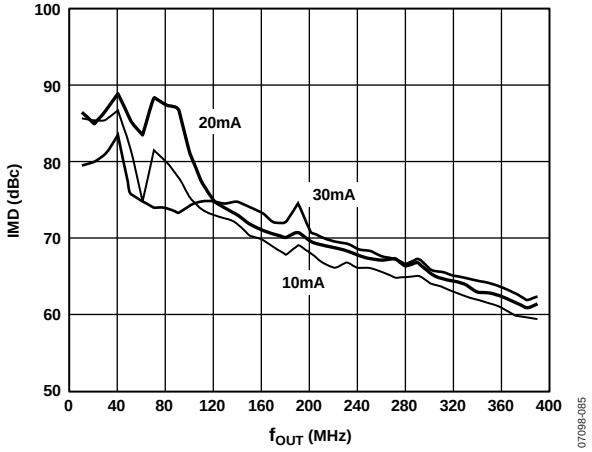


Figure 25. AD9788 IMD Performance vs. Full-Scale Output Current, 4× Interpolation, f_{DATA} = 200 MSPS

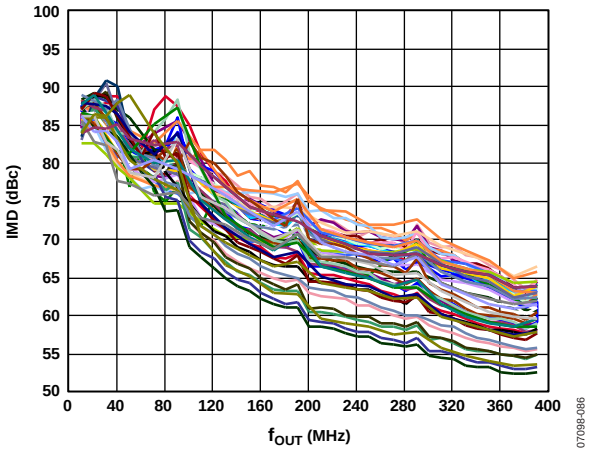


Figure 26. AD9788 IMD vs. f_{OUT}, over 50 Parts, 4× Interpolation, f_{DATA} = 200 MSPS

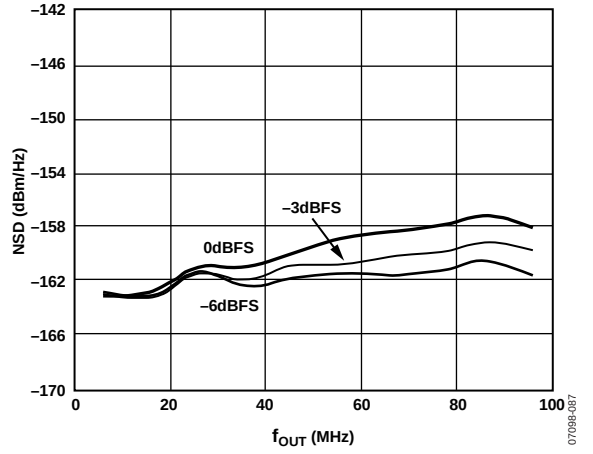


Figure 27. AD9788 Noise Spectral Density vs. Digital Full-Scale Single-Tone Input, f_{DATA} = 200 MSPS, 2× Interpolation

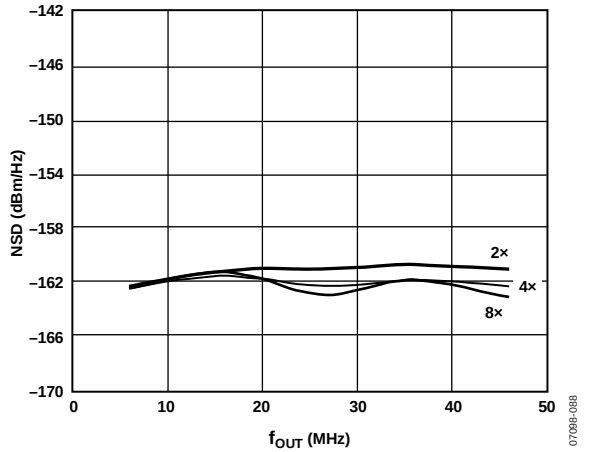


Figure 28. AD9788 Noise Spectral Density vs. f_{OUT}, Multitone Input, f_{DATA} = 100 MSPS

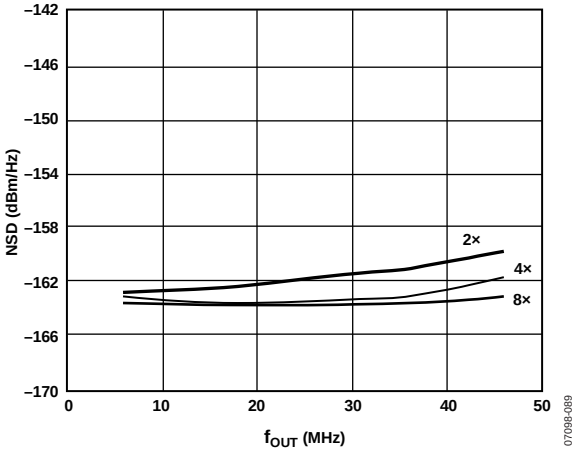


Figure 29. AD9788 Noise Spectral Density vs. f_{OUT}, Single-Tone Input, f_{DATA} = 100 MSPS

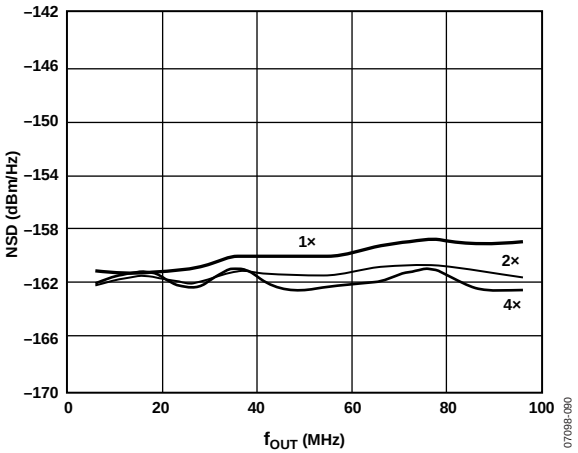


Figure 30. AD9788 Noise Spectral Density vs. f_{DAC}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

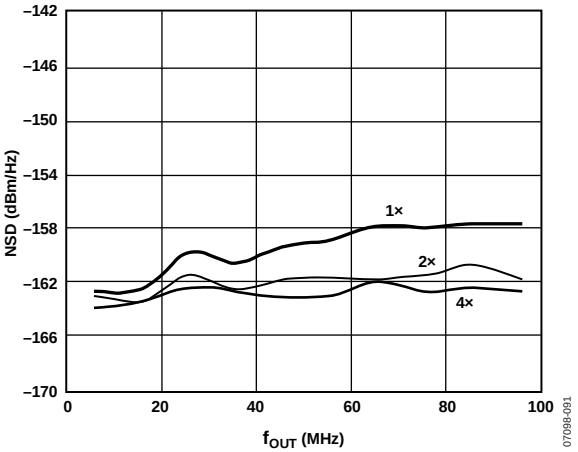


Figure 31. AD9788 Noise Spectral Density vs. f_{DAC}, Full-Scale Single-Tone Input at −6 dB, f_{DATA} = 200 MSPS

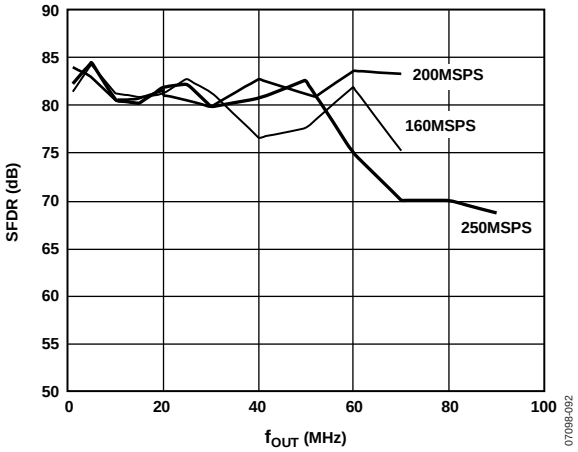


Figure 32. AD9788 In-Band SFDR vs. f_{OUT}, 1× Interpolation

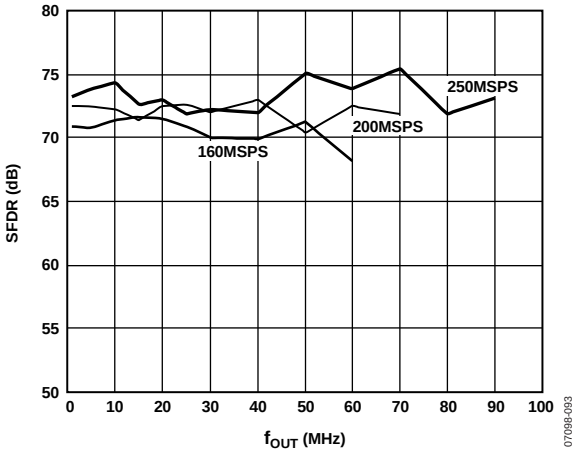


Figure 33. AD9788 Out-of-Band SFDR vs. f_{OUT}, 2× Interpolation

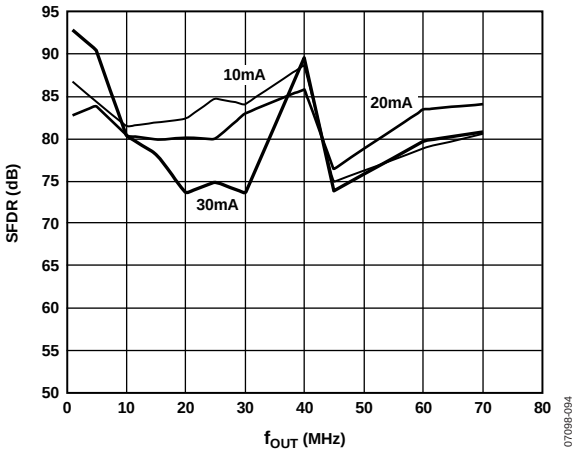


Figure 34. AD9788 In-Band SFDR vs. Full-Scale Output Current, 2× Interpolation, f_{DATA} = 200 MSPS

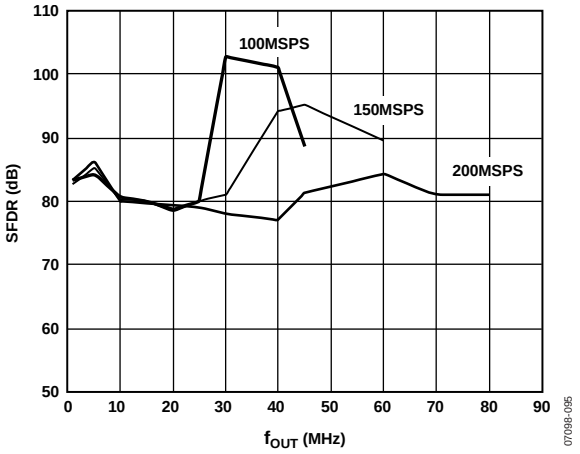


Figure 35. AD9788 In-Band SFDR vs. f_{OUT}, 4× Interpolation

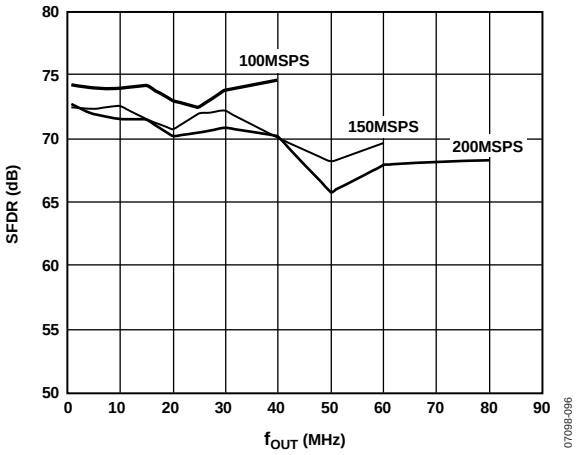


Figure 36. AD9788 Out-of-Band SFDR vs. f_{OUT}, 4× Interpolation

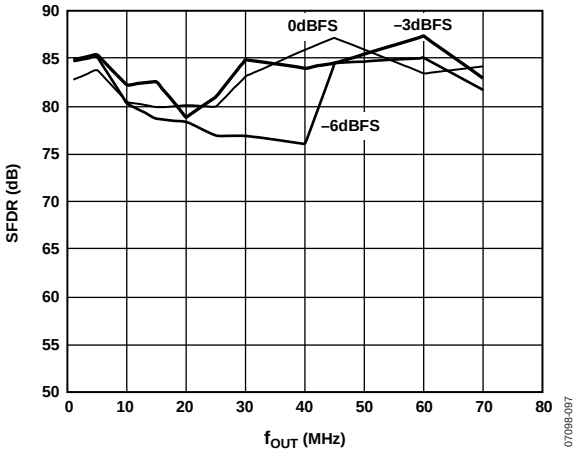


Figure 37. AD9788 In-Band SFDR vs. Digital Full-Scale Input, 2× Interpolation, f_{DATA} = 200 MSPS

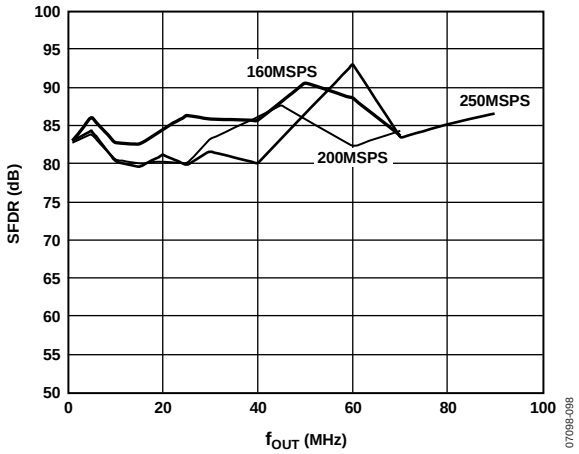


Figure 38. AD9788 In-Band SFDR vs. f_{OUT}, 2× Interpolation

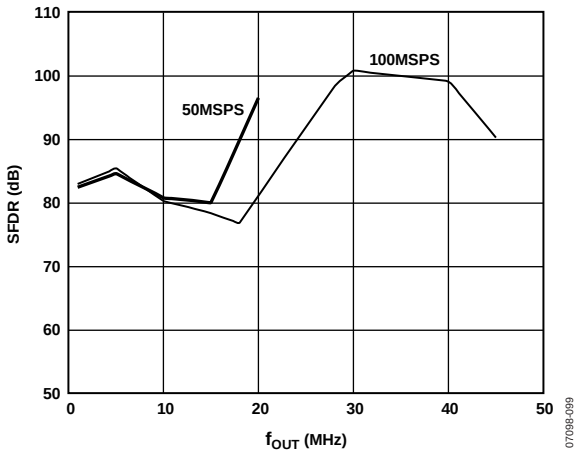


Figure 39. AD9788 In-Band SFDR vs. f_{OUT}, 8× Interpolation

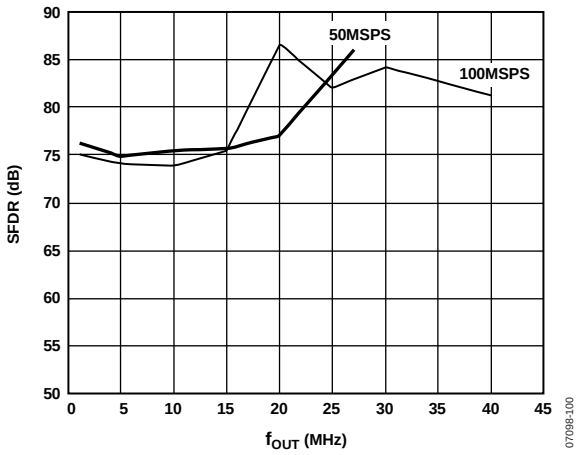


Figure 40. AD9788 Out-of-Band SFDR vs. f_{OUT}, 8× Interpolation

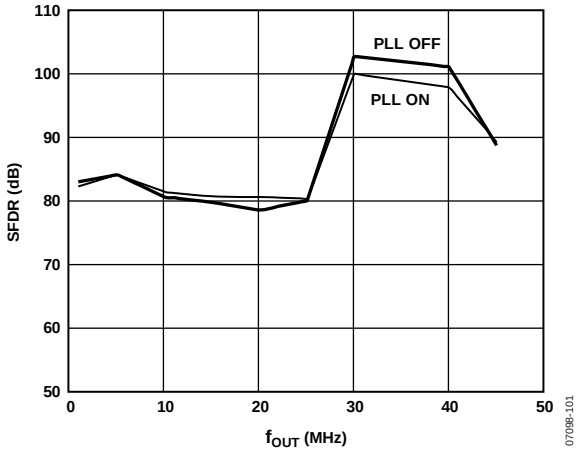


Figure 41. AD9788 In-Band SFDR vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/PLL Off

TERMINOLOGY

Integral Nonlinearity (INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span is called gain error. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
Spurious-free dynamic range is the difference, in decibels, between the peak amplitude of the output signal and the peak amplitude of the largest spurious signal in a given frequency band from the signal. For out-of-band SFDR, the frequency band is 0 to one half the DAC sample rate. For in-band SFDR, the frequency band is 0 to one half the input data rate.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Noise Spectral Density (NSD)
NSD is the noise power at the analog output measured in a 1 Hz bandwidth.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second intermediate frequency (IF). These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

Sinc
Sinc is shorthand for the mathematical function

$$\text{sinc}(x) = \sin(x)/x$$

This function is a useful tool for digital signal processing. The normalized sinc function is used here and is defined as follows:

$$\text{sinc}(x) = \sin(\pi \times x)/(\pi \times x)$$

THEORY OF OPERATION

The AD9785/AD9787/AD9788 devices combine many features that make them very attractive DACs for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface to common quadrature modulators when designing single sideband transmitters. The speed and performance of the AD9785/AD9787/AD9788 allow wider bandwidths and more carriers to be synthesized than in previously available DACs. In addition, these devices include an innovative low power, 32-bit complex NCO that greatly increases the ease of frequency placement.

The AD9785/AD9787/AD9788 offer features that allow simplified synchronization with incoming data and between multiple parts, as well as the capability to phase synchronize NCOs on multiple devices. Auxiliary DACs are also provided on chip for output dc offset compensation (for LO compensation in SSB transmitters) and for gain matching (for image rejection optimization in SSB transmitters). Another innovative feature in the devices is the digitally programmable output phase compensation, which increases the amount of image cancellation capability in SSB (single sideband) transmitters.

SERIAL PORT INTERFACE

The AD9785/AD9787/AD9788 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola® 6905/11 SPI and the Intel® 8051 SSR protocols.

The serial interface allows read/write access to all registers that configure the AD9785/AD9787/AD9788. MSB first and LSB first transfer formats are supported. In addition, the serial interface port can be configured as a single-pin I/O (SDIO), which allows a 3-wire interface, or two unidirectional pins for input/output (SDIO/SDO), which enables a 4-wire interface. One optional pin, $\overline{\text{SPI\_CS}}$ (chip select), allows enabling of multiple devices on a single bus.

With the AD9785/AD9787/AD9788, the instruction byte specifies read/write operation and the register address. Serial operations on the AD9785/AD9787/AD9788 occur only at the register level, not at the byte level, due to the lack of byte address space in the instruction byte.

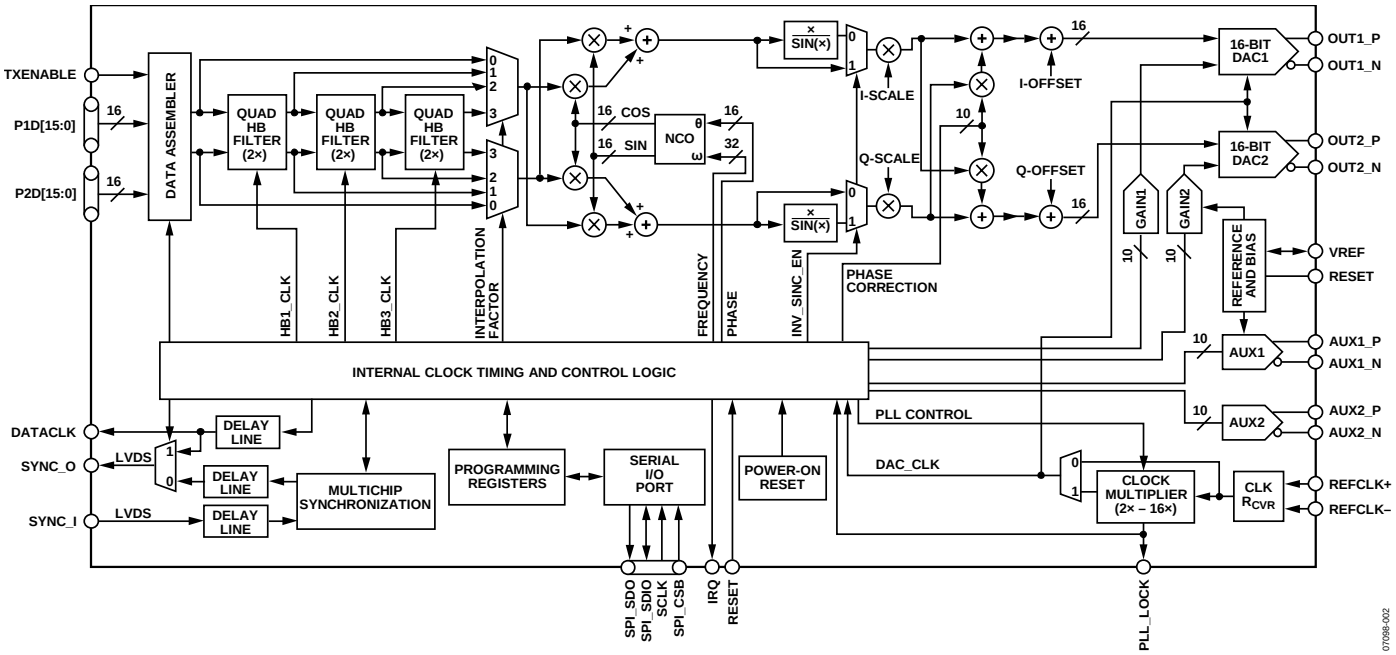


Figure 42. Functional Block Diagram

There are two phases to a communication cycle with the AD9785/AD9787/AD9788. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9785/AD9787/AD9788, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9785/AD9787/AD9788 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The instruction byte defines whether the upcoming data transfer is read or write and the serial address of the register being accessed.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9785/AD9787/AD9788. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9785/AD9787/AD9788 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register being accessed.

For example, when accessing the frequency tuning word (FTW) register, which is four bytes wide, Phase 2 requires that four bytes be transferred. If accessing the amplitude scale factor (ASF) register, which is three bytes wide, Phase 2 requires that three bytes be transferred. After transferring all data bytes per the instruction byte, the communication cycle is completed.

At the completion of any communication cycle, the AD9785/AD9787/AD9788 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input is registered on the rising edge of SCLK. All data is driven out of the AD9785/AD9787/AD9788 on the falling edge of SCLK.

Figure 43 through Figure 46 are useful in understanding the general operation of the AD9785/AD9787/AD9788 serial port.

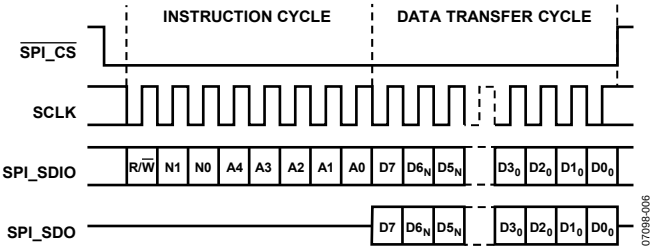


Figure 43. Serial Register Interface Timing, MSB First

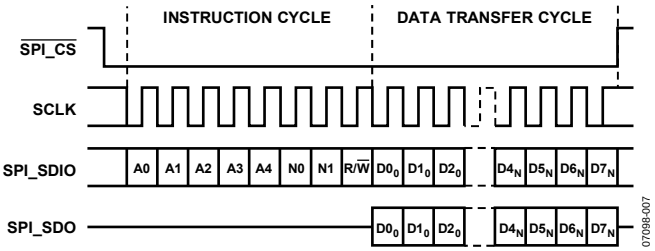


Figure 44. Serial Register Interface Timing, LSB First

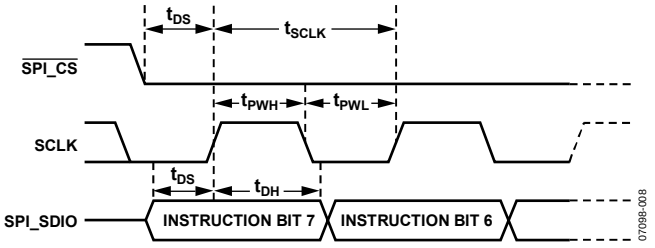


Figure 45. SPI Register Write Timing

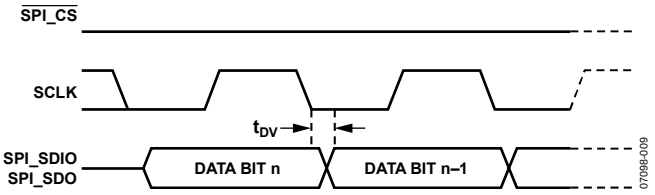


Figure 46. SPI Register Read Timing Instruction Byte

Instruction Byte

The instruction byte contains the following information as shown in the instruction byte bit map.

Instruction Byte Information Bit Map

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/$\overline{W}$	X	X	A4	A3	A2	A1	A0

R/$\overline{W}$—Bit 7 of the instruction byte determines whether a read or write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation.

X, X —Bit 6 and Bit 5 of the instruction byte are don't care. In previous TxDAC devices, such as the AD9779, these bits define the number of registers written to or read from in an SPI read/write operation. In the AD9785/AD9787/AD9788, the register itself now defines how many bytes are written to or read from.

A4, A3, A2, A1, A0—Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0 of the instruction byte determine which register is accessed during the data transfer portion of the communication cycle.

Serial Interface Port Pin Description

SCLK—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9785/AD9787/AD9788 and to run the internal state machines. SCLK maximum frequency is 40 MHz.

$\overline{SPI\_CS}$—Chip Select

Active low input that allows more than one device on the same serial communications line. The SPI_SDO and SPI_SDIO pins go to a high impedance state when this input is high. If driven high during any communication cycle, that cycle is suspended until $\overline{SPI\_CS}$ is reactivated low. Chip select can be tied low in systems that maintain control of SCLK.

SPI_SDIO—Serial Data I/O

Data is always written into the AD9785/AD9787/AD9788 on this pin. However, this pin can be used as a bidirectional data line. Bit 7 of Register 0x00 controls the configuration of this pin. The default is Logic 0, which configures the SPI_SDIO pin for input only (4-wire) operation.

SPI_SDO—Serial Data Output

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9785/AD9787/AD9788 operate in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB Transfers

The AD9785/AD9787/AD9788 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by Bit 6 of the communication (COMM) register. The default value of COMM Register Bit 6 is low (MSB first). When COMM Register Bit 6 is set high, the serial port is in LSB first format. The instruction byte must be written in the format indicated by COMM Register Bit 6. That is, if the device is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

For MSB first operation, the serial port controller generates the most significant byte (of the specified register) address first, followed by the next lesser significant byte addresses until the I/O operation is complete. All data written to or read from the AD9785/AD9787/AD9788 must be in MSB first order.

If the LSB mode is active, the serial port controller generates the least significant byte address first, followed by the next greater significant byte addresses until the I/O operation is complete. All data written to or read from the AD9785/AD9787/AD9788 must be in LSB first order.

SPI Resynchronization Capability

If the SPI port becomes unsynchronized at any time, toggling SCLK for eight or more cycles with $\overline{SPI\_CS}$ held high resets the SPI port state machine. The device is then ready for the next register read or write access.

SPI REGISTER MAP

When reading Table 9, note that the AD9785/AD9787/AD9788 is a 32-bit part and, therefore, the 4th through the 11th columns (beginning with the MSB and ending with the LSB) represent a set of eight bits. Refer to the Bit Range column for the actual bits being described.

Table 9.

Address	Register Name	Bit Range	MSB	MSB – 1	MSB – 2	MSB – 3	MSB – 4	MSB – 5	MSB – 6	LSB	Default
0x00	Comm. (COMM) Register	[7:0]	SPI_SDIO bidirectional (active high, 3-wire)	LSB first	Software reset	Power-down mode	Auto power-down enable	I/O transfer (self-reset)	Automatic I/O transfer enable	Open	0x02
0x01	Digital Control Register	[7:0]	Interpolation Factor [1:0]		Data format	Single-port mode	Real mode	IQ select invert	Q first	Modulator gain control	0x00
		[15:8]	Reserved	Clear phase accumulator	PN code sync enable	Sync mode select	Pulse sync enable	Reserved	Inverse sinc enable	DATACLK output enable	0x31
0x02	Data Sync Control Register	[7:0]	Data Timing Margin [0]	LVDS data clock enable	DATACLK invert	DATACLK delay enable	Data timing mode	Set high	Data sync polarity	Reserved	0x00
		[15:8]	DATACLK Delay [4:0]					Data Timing Margin [3:1]			0x00
0x03	Multichip Sync Control Register	[7:0]	Clock State [3:0]				Sync Timing Margin [3:0]				0x00
		[15:8]	SYNC _O Delay [4:0]					Set high	SYNC_O polarity	Sync loopback enable	0x00
		[23:16]	SYNC_I Delay [4:0]					Sync error check mode	Set low	DATACLK input	0x00
		[31:24]	Correlate Threshold [4:0]					SYNC_I enable	SYNC _O enable	Set low	0x80
0x04	PLL Control Register	[7:0]	PLL Band Select [5:0]						PLL VCO Drive [1:0]		0xCF
		[15:8]	PLL enable	PLL VCO Divisor [1:0]		PLL Loop Divisor [1:0]		PLL Bias [2:0]			0x37
		[23:16]	VCO Control Voltage [2:0]			PLL Loop Bandwidth [4:0]					0x38
0x05	I DAC Control Register	[7:0]	I DAC Gain Adjustment [7:0]								0xF9
		[15:8]	I DAC sleep	I DAC power-down	Reserved				I DAC Gain Adjustment [9:8]		0x01
0x06	Auxiliary DAC 1 Control Register	[7:0]	Auxiliary DAC 1 Data [7:0]								0x00
		[15:8]	Auxiliary DAC 1 sign	Auxiliary DAC 1 current direction	Auxiliary DAC 1 power-down	Reserved			Auxiliary DAC 1 Data [9:8]		0x00
0x07	Q DAC Control Register	[7:0]	Q DAC Gain Adjustment [7:0]								0xF9
		[15:8]	Q DAC sleep	Q DAC power-down	Reserved				Q DAC Gain Adjustment [9:8]		0x01
0x08	Auxiliary DAC 2 Control Register	[7:0]	Auxiliary DAC 2 Data [7:0]								0x00
		[15:8]	Auxiliary DAC 2 sign	Auxiliary DAC 2 current direction	Auxiliary DAC 2 power-down	Reserved			Auxiliary DAC 2 Data [9:8]		0x00
0x09	Interrupt Control Register	[7:0]	Data timing error IRQ	Sync timing error IRQ	Data timing error type	Sync timing error type	PLL lock indicator	Reserved	Data port IRQ enable	Sync port IRQ enable	0x00
		[15:8]	Reserved			Clear lock indicator (self-reset)	Sync lock lost status	Sync lock status	Reserved		0x00
0x0A	Frequency Tuning Word Register	[31:0]	Frequency Tuning Word [31:0]								0x00

Address	Register Name	Bit Range	MSB	MSB – 1	MSB – 2	MSB – 3	MSB – 4	MSB – 5	MSB – 6	LSB	Default
0x0B	Phase Control Register	[15:0]	NCO Phase Offset Word [15:0]								0x00
		[23:16]	Phase Correction Word [7:0]								0x00
		[31:24]	Reserved						Phase Correction Word [9:8]		0x00
0x0C	Amplitude Scale Factor Register	[7:0]	I DAC Amplitude Scale Factor [7:0]								0x80
		[15:8]	Q DAC Amplitude Scale Factor [6:0]							I DAC Amplitude Scale Factor [8]	0x00
		[23:16]	Reserved						Q DAC Amplitude Scale Factor [8:7]		0x01
0x0D	Output Offset Register	[15:0]	I DAC Offset [15:0]								0x00
		[31:16]	Q DAC Offset [15:0]								0x00
0x0E[1]	Version Register	[7:0]	Version ID								
		[15:8]	Reserved								
0x1D[1]	RAM	[31:0]	RAM								
0x1E	Test Register	[23:0]	Test								

[1] Address space between Address 0x0E and Address 0x1D is intentionally left open.

SPI REGISTER DESCRIPTIONS

The communication (COMM) register comprises one byte located at Address 0x00.

Table 10. Communication (COMM) Register

Address	Bit	Name	Description
0x00	[7]	SPI_SDIO Bidirectional	0: Default. Use the SPI_SDIO pin for input data only, 4-wire serial mode. 1: Use SPI_SDIO as a read/write pin, 3-wire serial mode.
	[6]	LSB First	0: Default. MSB first format is active. 1: Serial interface accepts serial data in LSB first format.
	[5]	Software Reset	0: Default. Bit is in the inactive state. 1: In the AD9785/AD9787/AD9788, all programmable bits return to their power-up state except for the COMM register bits, which are unaffected by the software reset. The software reset remains in effect until this bit is set to 0 (inactive state).
	[4]	Power-Down Mode	0: Default. The full chip power-down is not active. 1: The AD9785/AD9787/AD9788 enter a power-down mode in which all functions are powered down. This power-down puts the part into its lowest possible power dissipation state. The part remains in this low power state until the user sets this bit to a Logic 0. The analog circuitry requires 250 ms to become operational.
	[3]	Auto Power-Down Enable	0: Default. Inactive state, automatic power-down feature is not enabled. 1: The device automatically switches into its low power mode whenever TXENABLE is deasserted for a sufficiently long period of time.
	[2]	I/O Transfer (self-reset)	0: Default. Inactive state. 1: The contents of the frequency tuning word memory buffer, phase control memory buffer, amplitude scale factor memory buffer, and the output offset memory buffer are moved to a memory location that affects operation of the device. The one-word memory buffer is employed to simultaneously update the NCO frequency, phase, amplitude, and offset control. Note that this bit automatically clears itself after the I/O transfer occurs. For this reason, unless the reference clock is stopped, it is difficult to read back a Logic 1 on this bit.
	[1]	Automatic I/O Transfer Enable	0: Automatic I/O transfer disabled. The I/O transfer bit (Bit 2) must be set to update the device in the event that changes have been made to Register 0x0A, Register 0x0B, Register 0x0C, or Register 0x0D. This allows the user to change important operating modes of the device all at once, rather than one at a time with individual SPI writes. 1: Default. Automatic I/O transfer enabled. The device updates its operation immediately when SPI writes are completed to Register 0x0A, Register 0x0B, Register 0x0C, or Register 0x0D.

The digital control (DCTL) register comprises two bytes located at Address 0x01.

Table 11. Digital Control (DCTL) Register

Address	Bit	Name	Description
0x01	[15]	Reserved	Reserved for future use.
	[14]	Clear Phase Accumulator	0: Default. The feature that clears the NCO phase accumulator is inactive. The phase accumulator operates as normal. 1: The NCO phase accumulator is held in the reset state until this bit is cleared.
	[13]	PN Code Sync Enable	0: PN code synchronization mode is disabled. 1: PN code synchronization mode is enabled. See the Device Synchronization section for details.
	[12]	Sync Mode Select	0: Selects pulse mode synchronization. 1: Selects PN code synchronization. See the Device Synchronization section for details.
	[11]	Pulse Sync Enable	0: Pulse mode synchronization is disabled. 1: Pulse mode synchronization is enabled. See the Device Synchronization section for details.
	[10]	Reserved	Reserved for future use.
	[9]	Inverse Sinc Enable	0: Default. The inverse sinc filter is bypassed. 1: The inverse sinc filter is enabled and operational.
	[8]	DATACLK Output Enable	0: Data clock pin is disabled. 1: Default. The output data clock pin is active (configured as an output).
	[7:6]	Interpolation Factor [1:0]	Specifies the filter interpolation rate where: 00: 1× interpolation. 01: 2× interpolation. 10: 4× interpolation. 11: 8× interpolation.
	[5]	Data Format	0: Default. The incoming data is expected to be twos complement. 1: The incoming data is expected to be offset binary.
	[4]	Single-Port Mode	0: Default. When the single-port bit is cleared, I/Q data is sampled simultaneously on the P1D and P2D input ports. Specifically, I data is registered from the P1D[15:0] pins and Q data is registered from the P2D[15:0] pins. 1: When the single-port bit is set, I/Q data is sampled in a serial word fashion on the P1D input port. In this mode, the I/Q data is sampled into the part at twice the I/Q sample rate.
	[3]	Real Mode	0: Default. Logic 0 is the inactive state for this bit. 1: When the real mode bit is set, the Q path logic after modulation and phase compensation is disabled.
	[2]	IQ Select Invert	0: Default. When the IQ Select Invert bit is cleared, a Logic 1 on the TXENABLE pin indicates I data, and a Logic 0 on the TXENABLE pin indicates Q data, if the user is employing a continuous timing style on the TXENABLE pin. 1: When the IQ Select Invert bit is set, a Logic 1 on the TXENABLE pin indicates Q data, and a Logic 0 on the TXENABLE pin indicates I data, if the user is employing a continuous timing style on the TXENABLE pin.
	[1]	Q First (data pairing)	0: Default. When the Q first bit is cleared, the I/Q data pairing is nominal, that is, the I data precedes the Q data in the assembly of the I/Q data pair. As such, data input to the device as I0, Q0, I1, Q1… In, Qn is paired as follows: (I0/Q0), (I1/Q1) … (In/Qn). 1: When the Q first bit is set, the I/Q data pairing is altered such that the I data is paired with the previous Q data. As such, data input to the device as I0, Q0, I1, Q1, I2, Q2, I3, Q3 … In, Qn is paired as follows: (I1/Q0), (I2/Q1), (I3/Q2) … (In + 1/Qn).
	[0]	Modulator Gain Control	0: Default. No gain scaling is applied to the NCO input to the internal digital modulator. 1: Gain scaling of 0.5 is applied to the NCO input to the modulator. This can eliminate saturation of the modulator output for some combinations of data inputs and NCO signals.

The data synchronization control register (DSCR) comprises two bytes located at Address 0x02.

Table 12. Data Synchronization Control Register (DSCR)

Address	Bit	Name	Description
0x02	[15:11]	DATACLK Delay [4:0]	Controls the amount of delay applied to the output data clock signal. The minimum delay corresponds to the 00000 state, and the maximum delay corresponds to the 11111 state. The minimum delay is 0.7 ns and the maximum delay is 6.5 ns. The incremental delay is 190 ps and corresponds to an incremental change in the data clock delay bits.
	[10:7]	Data Timing Margin [3:0]	The data timing margin bits control the amount of delay applied to the data and clock signals used for checking setup and hold times, respectively, on the input data ports, with respect to the internal data assembler clock. The minimum delay corresponds to the 0000 state, and the maximum delay corresponds to the 1111 state. The delays are 190 ps.
	[6]	LVDS Data Clock Enable	0: Default. When the LVDS data clock enable bit is cleared, the SYNC_O+ and SYNC_O– LVDS pad cells are driven by the multichip synchronization logic. 1: When the LVDS data clock enable bit is set, the SYNC_O+ and SYNC_O– LVDS pad cells are driven by the signal that drives the CMOS DATACLK output pad.
	[5]	DATACLK Invert	0: Default. When the data clock invert bit is cleared, the DATACLK signal is in phase with the clock that samples the data into the part. 1: When the DATACLK invert bit is set, the DATACLK signal is inverted from the clock that samples the data into the part.
	[4]	DATACLK Delay Enable	0: Default. When the DATACLK delay enable bit is cleared, the data port input synchronization function is effectively inactive and the delay is bypassed. 1: When the DATACLK delay enable bit is set, the data port input synchronization function is active and controlled by the data delay mode bits. The data output clock is routed through the delay cell.
	[3]	Data timing mode	Determines the timing optimization mode. See the Optimizing the Data Input Timing section for details. 0: Manual timing optimization mode. 1: Automatic timing optimization mode.
	[2]	Set High	This bit should always be set high.
	[1]	Data Sync Polarity	0: Default. The digital input data sampling edge is aligned with the falling edge of DCI. 1: The digital input data sampling edge is aligned with the rising edge of DCI. Used only in slave mode (see the MSCR register, Address 0x03, Bit 16).
	[0]	Reserved	Reserved for future use.

The multichip synchronization register (MSCR) comprises four bytes located at Address 0x03.

Table 13. Multichip Synchronization Register (MSCR)

Address	Bit	Name	Description
0x03	[31:27]	Correlate Threshold [4:0]	Sets the threshold for determining if the received synchronization data can be demodulated accurately. A smaller threshold value makes the demodulator more noise immune; however, the system becomes more susceptible to false locks (or demodulation errors).
	[26]	SYNC_I Enable	0: Default. The synchronization receive logic is disabled. 1: The synchronization receive logic is enabled.
	[25]	SYNC_O Enable	0: Default. The output synchronization pulse generation logic is disabled. 1: The output synchronization pulse generation logic is enabled.
	[24]	Set Low	This bit should always be set low.
	[23:19]	SYNC_I Delay [4:0]	This value programs the value of the delay line of the SYNC_I signal. The delay line resolution is 80 ps per step. 00000: nominal delay. 00001: adds 80 ps delay to SYNC_I. 00010: adds 160 ps delay to SYNC_I. … 11111: adds 2480 ps delay to SYNC_I.
	[18]	Sync Error Check Mode	Specifies the synchronization pulse error check mode. 0: Manual error check. 1: Automatic continuous error check.
	[17]	Set Low	This bit should always be set low.
	[16]	DATACLK Input	0: Default. Slave mode is disabled. 1: Slave mode is enabled. Pin 37 functions as an input for the DATACLK signal, called DCI (DATACLK input) in this mode. Depending on the state of Bit 1 in the DSCR register (Address 0x02), the sampling edge (where the data is latched into the AD9785/AD9787/AD9788) can be programmed to be aligned with either the rising or falling edge of DCI. This mode can only be used with 4× or 8× interpolation.
	[15:11]	SYNC_O Delay [4:0]	This value programs the value of the delay line of the SYNC_O signal. The delay of SYNC_O is relative to REFCLK. The delay line resolution is 80 ps per step. 00000: nominal delay. 00001: adds 80 ps delay to SYNC_O. 00010: adds 160 ps delay to SYNC_O. … 11111: adds 2480 ps delay to SYNC_O.
	[10]	Set high	This bit should always be set high.
	[9]	SYNC_O Polarity	0: Default. SYNC_O changes state on the rising edge of DACCLK. 1: SYNC_O is generated on the falling edge of DACCLK.
	[8]	Sync Loopback Enable	0: Default. The AD9785/AD9787/AD9788 are not operating in internal loopback mode. 1: If the SYNC_O enable and Sync loopback enable bits are set, the AD9785/AD9787/AD9788 are operating in a mode in which the internal synchronization pulse of the device is used at the multichip receiver logic and the SYNC_I+ and SYNC_I– input pins are ignored. For proper operation of the loopback synchronization mode, the synchronization driver enable and sync enable bits must be set.
	[7:4]	Clock State [3:0]	This value determines the state of the internal clock generation state machine upon synchronization.
	[3:0]	Sync Timing Margin [3:0]	These bits are the synchronization window delay word. These bits are don't care if the synchronization driver enable bit is cleared.

The PLL control (PLLCTL) register comprises three bytes located at Address 0x04. These bits are routed directly to the periphery of the digital logic. No digital functionality within the main digital block is required.

Table 14. PLL Control (PLLCTL) Register

Address	Bit	Name	Description
0x04	[23:21]	VCO Control Voltage [2:0]	000 to 111, proportional to voltage at VCO, control voltage input (readback only). A value of 011 indicates that the VCO control voltage is centered.
	[20:16]	PLL Loop Bandwidth [4:0]	These bits control the bandwidth of the PLL filter. Increasing the value lowers the loop bandwidth. Set to 01111 for optimal performance.
	[15]	PLL Enable	0: Default. With PLL off, the DAC sample clock is sourced directly by the REFCLK input. 1: With PLL on, the DAC clock is synthesized internally from the REFCLK input via the PLL clock multiplier. See the Clock Multiplication section for details.
	[14:13]	PLL VCO Divisor [1:0]	Sets the value of the VCO output divider, which determines the ratio of the VCO output frequency to the DAC sample clock frequency, f_{VCO}/f_{DACCLK}. 00: $f_{VCO}/f_{DACCLK} = 1$. 01: $f_{VCO}/f_{DACCLK} = 2$. 10: $f_{VCO}/f_{DACCLK} = 4$. 11: $f_{VCO}/f_{DACCLK} = 8$.
	[12:11]	PLL Loop Divisor [1:0]	Sets the value of the DACCLK divider, which determines the ratio of the DAC sample clock frequency to the REFCLK frequency, f_{DACCLK}/f_{REFCLK}. 00: $f_{DACCLK}/f_{REFCLK} = 2$. 01: $f_{DACCLK}/f_{REFCLK} = 4$. 10: $f_{DACCLK}/f_{REFCLK} = 8$. 11: $f_{DACCLK}/f_{REFCLK} = 16$.
	[10:8]	PLL Bias [2:0]	These bits control the VCO bias current. Set to 011 for optimal performance.
	[7:2]	PLL Band Select [5:0]	These bits set the operating frequency of the VCO. For further details, refer to Table 35.
	[1:0]	PLL VCO Drive [1:0]	These bits control the signal strength of the VCO output. Set to 11 for optimal performance.

The I DAC control register comprises two bytes located at Address 0x05. These bits are routed directly to the periphery of the digital logic. No digital functionality within the main digital block is required.

Table 15. I DAC Control Register

Address	Bit	Name	Description
0x05	[15]	I DAC Sleep	0: Default. If the I DAC sleep bit is cleared, the I DAC is active. 1: If the I DAC sleep bit is set, the I DAC is inactive and enters a low power state.
	[14]	I DAC Power-Down	0: Default. If the I DAC power-down bit is cleared, the I DAC is active. 1: If the I DAC power-down bit is set, the I DAC is inactive and enters a low power state.
	[13:10]	Reserved	Reserved for future use.
	[9:0]	I DAC Gain Adjustment	These bits are the I DAC gain adjustment bits.

The Auxiliary DAC 1 control register comprises two bytes located at Address 0x06. These bits are routed directly to the periphery of the digital logic. No digital functionality within the main digital block is required.

Table 16. Auxiliary DAC 1 Control Register

Address	Bit	Name	Description
0x06	[15]	Auxiliary DAC 1 Sign	0: Default. If the Auxiliary DAC 1 sign bit is cleared, the Aux DAC 1 sign is positive. Pin 90 is the active pin. 1: If the Auxiliary DAC 1 sign bit is set, the Aux DAC 1 sign is negative. Pin 89 is the active pin.
	[14]	Auxiliary DAC 1 Current Direction	0: Default. If the Auxiliary DAC 1 current direction bit is cleared, the Aux DAC 1 sources current. 1: If the Auxiliary DAC 1 current direction bit is set, the Aux DAC 1 sinks current.
	[13]	Auxiliary DAC 1 Power-Down	0: Default. If the Auxiliary DAC 1 power-down bit is cleared, the Aux DAC 1 is active. 1: If the Auxiliary DAC 1 power-down bit is set, the Aux DAC 1 is inactive and enters a low power state.
	[12:10]	Reserved	Reserved for future use.
	[9:0]	Auxiliary DAC 1 Data	These bits are the Auxiliary DAC 1 gain adjustment bits.

The Q DAC control register comprises two bytes located at Address 0x07. These bits are routed directly to the periphery of the digital logic. No digital functionality within the main digital block is required.

Table 17. Q DAC Control Register

Address	Bit	Name	Description
0x07	[15]	Q DAC Sleep	0: Default. If the Q DAC sleep bit is cleared, the Q DAC is active. 1: If the Q DAC sleep bit is set, the Q DAC is inactive and enters a low power state.
	[14]	Q DAC Power-Down	0: Default. If the Q DAC power-down bit is cleared, the Q DAC is active. 1: If the Q DAC power-down bit is set, the Q DAC is inactive and enters a low power state.
	[13:10]	Reserved	Reserved for future use.
	[9:0]	Q DAC Gain Adjustment	These bits are the Q DAC gain adjustment bits.

The Auxiliary DAC 2 control register comprises two bytes located at Address 0x08. These bits are routed directly to the periphery of the digital logic. No digital functionality within the main digital block is required.

Table 18. Auxiliary DAC 2 Control Register

Address	Bit	Name	Description
0x08	[15]	Auxiliary DAC 2 Sign	0: Default. If the Auxiliary DAC 2 sign bit is cleared, the Aux DAC 2 sign is positive. Pin 86 is the active pin. 1: If the Auxiliary DAC 2 sign bit is set, the Aux DAC 2 sign is negative. Pin 87 is the active pin.
	[14]	Auxiliary DAC 2 Current Direction	0: Default. If the Auxiliary DAC 2 current direction bit is cleared, the Aux DAC 2 sources current. 1: If the Auxiliary DAC 2 current direction bit is set, the Aux DAC 2 sinks current.
	[13]	Auxiliary DAC 2 Power-Down	0: Default. If the Auxiliary DAC 2 power-down bit is cleared, the Aux DAC 2 is active. 1: If the Auxiliary DAC 2 power-down bit is set, the Aux DAC 2 is inactive and enters a low power state.
	[12:10]	Reserved	Reserved for future use.
	[9:0]	Auxiliary DAC 2 Data	These bits are the Auxiliary DAC 2 gain adjustment bits.

The interrupt control register comprises two bytes located at Address 0x09. Bits [11:10] and Bits [7:3] are read-only bits that indicate the current status of a specific event that may cause an interrupt request (IRQ pin active low). These bits are controlled via the digital logic and are read only via the serial port. Bits [1:0] are the IRQ mask (or enable) bits, which are writable by the user and can also be read back.

Table 19. Interrupt Control Register

Address	Bit	Name	Description
0x09	[15:13]	Reserved	Reserved for future use.
	[12]	Clear Lock Indicator	Writing a 1 to this bit clears the sync lock lost status bit. This bit does not automatically reset itself to 0 when the reset is complete.
	[11]	Sync Lock Lost Status	When high, this bit indicates that the device has lost synchronization. This bit is latched and does not reset automatically after the device regains synchronization. To reset this bit to 0, a 1 must be written to the clear lock indicator bit.
	[10]	Sync Lock Status	When this bit is low, the device is not synchronized. When this bit is high, the device is synchronized.
	[9:8]	Reserved	Reserved for future use.
	[7]	Data Timing Error IRQ	0: Default. No setup or hold time error has been detected via the input data port setup/hold error checking logic. 1: A setup or hold time error has been detected via the input data port setup/hold error checking logic.
	[6]	Sync Timing Error IRQ	0: Default. No setup or hold time error has been detected via the multichip synchronization receive pulse setup/hold error checking logic. 1: A setup or hold time error has been detected via the multichip synchronization receive pulse setup/hold error checking logic.
	[5]	Data Timing Error type	0: Default. A hold error has been detected via the input data port setup/hold error checking logic. This bit is valid only if the data timing error IRQ bit (Bit 7) is set. 1: A setup error has been detected via the input data port setup/hold error checking logic. This bit is valid only if the data timing error IRQ bit (Bit 7) bit is set.
	[4]	Sync Timing Error Type	0: Default. A hold error has been detected via the multichip synchronization receive pulse setup/hold error checking logic. This bit is valid only if the sync timing error IRQ bit (Bit 6) is set. 1: A setup error has been detected via the multichip synchronization receive pulse setup/hold error checking logic. This bit is valid only if the sync timing error IRQ bit (Bit 6) is set.
	[3]	PLL Lock Indicator	0: Default. The PLL clock multiplier is not locked to the input reference clock. 1: The PLL clock multiplier is locked to the input reference clock.
	[2]	Reserved	Reserved for future use.
	[1]	Data Port IRQ Enable	0: Default. The data IRQ bit (and the IRQ pin) are not enabled (masked) for any errors that may be detected via the input data port setup/hold error checking logic. 1: The data IRQ bit (and the IRQ pin) are enabled and go active if a setup or hold error is detected via the input data port setup/hold error checking logic.
	[0]	Sync Port IRQ Enable	0: Default. The sync IRQ bit (and the IRQ pin) are not enabled (masked) for any errors that may be detected via the multichip synchronization receive pulse setup/hold error checking logic. 1: The sync IRQ bit (and the IRQ pin) are enabled and go active if a setup or hold error is detected via the multichip synchronization receive pulse setup/hold error checking logic.

The frequency tuning word (FTW) register comprises four bytes located at Address 0x0A.

Table 20. Frequency Tuning Word (FTW) Register

Address	Bit	Name	Description
0x0A	[31:0]	Frequency Tuning Word [31:0]	These bits make up the frequency tuning word applied to the NCO phase accumulator. See the Numerically Controlled Oscillator section for details.

The phase control register (PCR) comprises four bytes located at Address 0x0B.

Table 21. Phase Control Register (PCR)

Address	Bit	Name	Description
0x0B	[31:26]	Reserved	Reserved for future use.
	[25:16]	Phase Correction Word [9:0]	These bits are the 10-bit phase correction word.
	[15:0]	NCO Phase Offset Word [15:0]	These bits are the 16-bit NCO phase offset word. See the Numerically Controlled Oscillator section for details.

The amplitude scale factor (ASF) register comprises three bytes located at Address 0x0C.

Table 22. Amplitude Scale Factor (ASF) Register

Address	Bit	Name	Description
0x0C	[23:18]	Reserved	Reserved for future use.
	[17:9]	Q DAC Amplitude Scale Factor [8:0]	These bits are the 9-bit Q DAC amplitude scale factor. The bit weighting is MSB = 2^1, LSB = 2^{-7}, which yields a multiplier range of 0 to 3.9921875. Note that by setting the gain to 1.0 (0x080), the gain block is bypassed. This changes the latency of the signal. Therefore, in systems using quadrature signals, either both I and Q scale factors should be bypassed or both should have gains set to a value other than 1.0.
	[8:0]	I DAC Amplitude Scale Factor [8:0]	These bits are the 9-bit I DAC amplitude scale factor. The bit weighting is MSB = 2^1, LSB = 2^{-7}, which yields a multiplier range of 0 to 3.9921875.

The output offset (OOF) register comprises four bytes located at Address 0x0D.

Table 23. Output Offset (OOF) Register

Address	Bit	Name	Description
0x0D	[31:16]	Q DAC Offset [15:0]	These bits are the 16-bit Q DAC offset factor. The LSB bit weight is 2^0.
	[15:0]	I DAC Offset [15:0]	These bits are the 16-bit I DAC offset factor. The LSB bit weight is 2^0.

The version register (VR) comprises two bytes located at Address 0x0E and is read only.

Table 24. Version Register (VR)

Address	Bit	Name	Description
0x0E	[15:8]	Reserved	Reserved for future use.
	[7:0]	Version ID	These bits read back the current version of the product.

INPUT DATA PORTS

The AD9785/AD9787/AD9788 can operate in two data input modes: dual-port mode and single-port mode. In the default dual-port mode (single-port mode = 0), each DAC receives data from a dedicated input port. In single-port mode (single-port mode = 1), both DACs receive data from Port 1. In single-port mode, DAC 1 and DAC 2 data is interleaved and the TXENABLE input is used to steer data to the intended DAC. In dual-port mode, the TXENABLE input is used to power down the digital datapath.

In dual-port mode, the data must be delivered at the input data rate. In single-port mode, data must be delivered at twice the input data rate of each DAC. Because the data inputs function up to a maximum of 300 MSPS, it is only practical to operate with input data rates up to 150 MHz per DAC in single-port mode.

In both dual-port and single-port modes, a data clock output (DATACLK) signal is available as a fixed-time base with which to drive data from an FPGA (field programmable gate array) or from another data source. This output signal operates at the input data rate. The DATACLK pin can operate as either an input or an output.

SINGLE-PORT MODE

In single-port mode, data for both DACs is received on the Port 1 input bus (P1D[15:0]). I and Q data samples are interleaved and are latched on the rising edges of DATACLK. Accompanying the data is the TXENABLE (Pin 39) input signal, which steers incoming data to its respective DAC. When TXENABLE is high, the corresponding data-word is sent to the I DAC and, when TXENABLE is low, the corresponding data is sent to the Q DAC. The timing of the digital interface in interleaved mode is shown in Figure 48.

The Q first bit (Register 0x01, Bit 1) controls the pairing order of the input data. With the Q first bit set to the default of 0, the I/Q pairing sent to the DACs is the two input data-words corresponding to TXENABLE low followed by TXENABLE high.

With the Q first bit set to 1, the I/Q pairing sent to the DACs is the two input data-words corresponding to TXENABLE high followed by TXENABLE low. Note that with Q first set, the I data still corresponds to the TXENABLE high word and the Q data corresponds to the TXENABLE low word and only the pairing order changes.

DUAL-PORT MODE

In dual-port mode, data for each DAC is received on the respective input bus (P1D[15:0] or P2D[15:0]). I and Q data arrive simultaneously and are sampled on the rising edge of an internal sampling clock (SMP_CLK) that is synchronous with DATACLK. In dual-port mode, driving the TXENABLE input low powers down the digital datapath. TXENABLE should be held high during normal data transmission.

INPUT DATA REFERENCED TO DATACLK

The simplest method of interfacing to the AD9785/AD9787/AD9788 is when the input data is referenced to the DATACLK output. The DATACLK output is phase-locked (with some offset) to the internal clock that is used to latch the input data. Therefore, if the setup and hold times of the input data with respect to DATACLK are met, the interface timing latches in the data correctly.

Table 25 shows the setup and hold time requirements for the input data over the operating temperature range of the device. Table 25 also shows the data valid window (DVW). The data valid window is the sum of the setup and hold times of the interface. This is the minimum amount of time valid data must be presented to the device in order to ensure proper sampling.

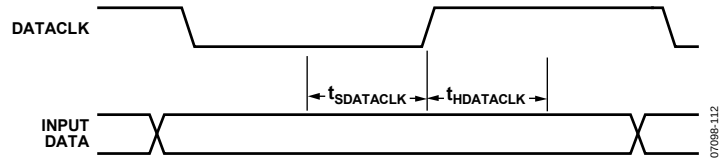


Figure 47. DATACLK Timing

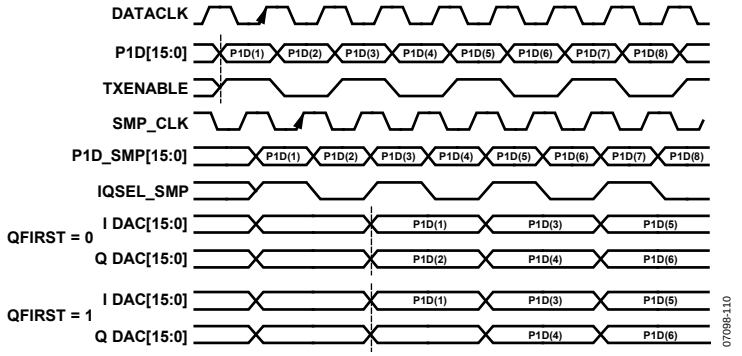


Figure 48. Single-Port (Interleaved) Mode Digital Interface Timing

Table 25. Data Timing Specifications vs. Temperature

Timing Parameter	Temperature	Min t_S (ns)	Min t_H (ns)	Min DVW (ns)
Data with respect to REFCLK	−40°C	−0.25	1.7	1.45
	+25°C	−0.45	2.1	1.65
	+85°C	−0.6	2.4	1.8
	−40°C to +85°C	−0.25	2.4	2.15
Data with respect to DATACLK	−40°C	3.7	−1.5	2.2
	+25°C	4.2	−1.8	2.4
	+85°C	4.6	−2.0	2.6
	−40°C to +85°C	4.6	−1.5	3.1
SYNC_I with respect to REFCLK	−40°C	0.45	−0.1	0.35
	+25°C	0.3	0.1	0.4
	+85°C	0.2	0.25	0.45
	−40°C to +85°C	0.45	0.25	0.7

Setting the Frequency of DATACLK

The DATACLK signal is derived from the internal DAC sample clock, DACCLK. The frequency of DATACLK output depends on several programmable settings. The relationship between the frequency of DACCLK and DATACLK is

$$f_{DATACLK} = \frac{f_{DACCLK}}{IF \times P}$$

where the variables have the values shown in Table 26.

Table 26. DACCLK to DATACLK Divisor Values

		Address	
Variable	**Value**	**Register**	**Bits**
IF	Interpolation factor	0x01	[7:6]
P	0.5 (if single port is enabled) 1 (if dual port is selected)	0x01	[4]

INPUT DATA REFERENCED TO REFCLK

In some systems, it may be more convenient to use the REFCLK input instead of the DATACLK output as the input data timing reference. If the frequency of DACCLK is equal to the frequency of the data input (PLL is bypassed and no interpolation is used), the timing parameter "Data with respect to REFCLK" shown in Table 25 applies directly without further considerations. If the frequency of DACCLK is greater than the frequency of the data input, a divider is used to generate the internal data sampling clock (DCLK_SMP). This divider creates a phase ambiguity between REFCLK and DCLK_SMP, which, in turn, causes a sampling time uncertainty. To establish fixed setup and hold times for the data interface, this phase ambiguity must be eliminated.

To eliminate the phase ambiguity, the SYNC_I input pins (Pin 13 and Pin 14) must be used to synchronize the data to a specific DCLK_SMP phase. The specific steps for accomplishing this are detailed in the Device Synchronization section. The timing relationships between SYNC_I, DACCLK, REFCLK, and the input data are shown in Figure 49 through Figure 51.

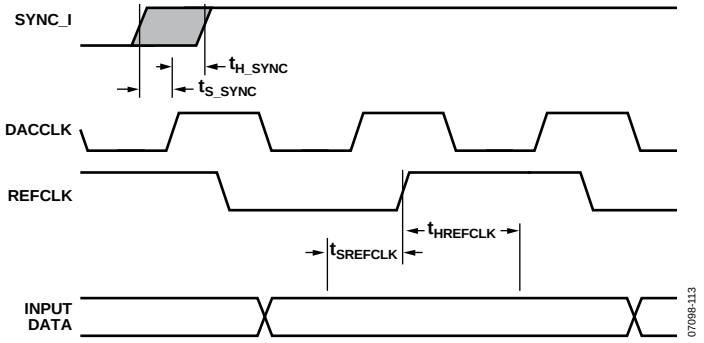


Figure 49. REFCLK 2×

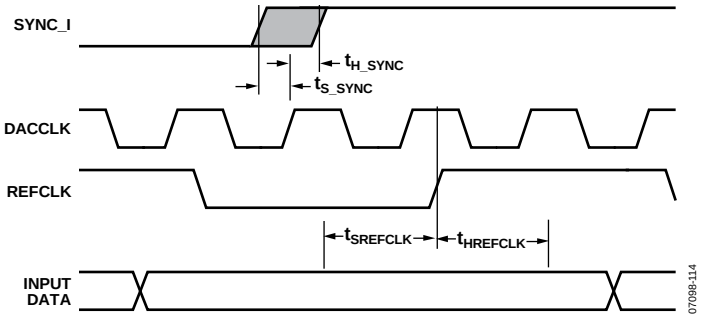


Figure 50. REFCLK 4×

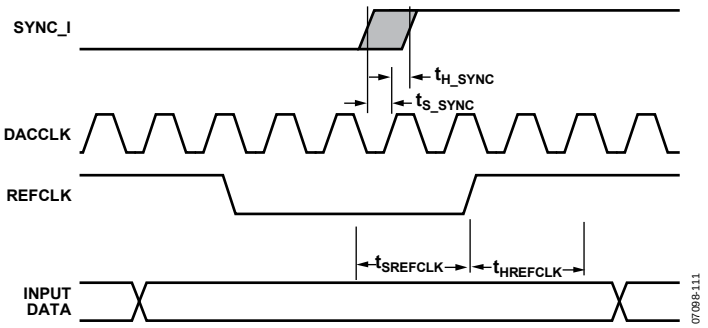


Figure 51. REFCLK 8×

OPTIMIZING THE DATA INPUT TIMING

The AD9785/AD9787/AD9788 have on-chip circuitry that enables the user to optimize the input data timing by adjusting the relationship between the DATACLK output and DCLK_SMP, the internal clock that samples the input data. This optimization is made by a sequence of SPI register read and write operations. The timing optimization can be done under strict control of the user, or the device can be programmed to maintain a configurable timing margin automatically.

Figure 52 shows the circuitry that detects sample timing errors and adjusts the data interface timing. The DCLK_SMP signal is the internal clock used to latch the input data. Ultimately, it is the rising edge of this signal that must be centered in the valid sampling period of the input data. This is accomplished by adjusting the time delay, t_D, which changes the DATACLK timing and, as a result, the arrival time of the input data with respect to DCLK_SMP.

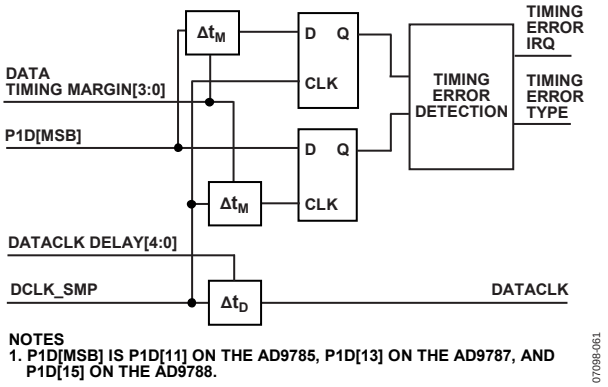


Figure 52. Timing Error Detection and Optimization Circuitry

The error detection circuitry works by creating two sets of sampled data (referred to as the margin test data) in addition to the actual sampled data used in the device datapath. One set of sampled data is latched before the actual data sampling point. The other set of sampled data is latched after the actual data sampling point. If the margin test data matches the actual data, the sampling is considered valid and no error is declared. If there is a mismatch between the actual data and the margin test data, an error is declared.

The Data Timing Margin [3:0] variable (Register 0x02, Bits [10:7]) determines the amount of time before and after the actual data sampling point the margin test data are latched. That is, the Data Timing Margin [3:0] variable determines how much setup and hold margin the interface needs for the data timing error IRQ to remain inactive (to show error-free operation). Therefore, the data timing error IRQ is set whenever the setup and hold margins drop below the Data Timing Margin [3:0] value. This does not necessarily indicate that the data latched into the device is incorrect.

In addition to setting the data timing error IRQ, the data timing error type bit (Register 0x09, Bit 5) is set when an error occurs. The data timing error bit is set low to indicate a hold error and high to indicate a setup error. Figure 53 shows a timing diagram of the data interface and the status of the data timing error type bit.

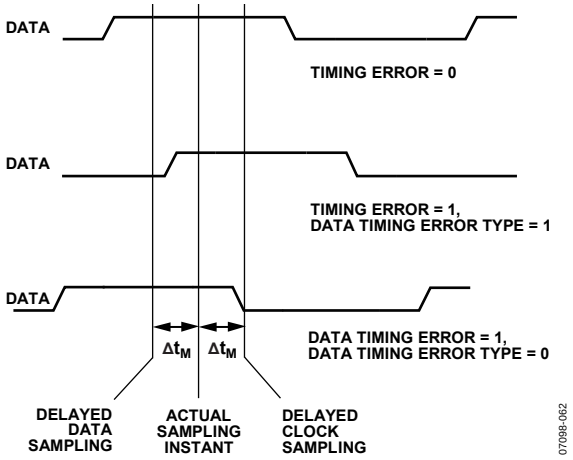


Figure 53. Timing Diagram of Margin Test Data

Automatic Timing Optimization Mode

When the automatic timing optimization mode is enabled (Register 0x02, Bit 3 = 1), the device continuously monitors the timing error IRQ and timing error type bits. The DATACLK Delay [4:0] value (Register 0x02, Bits [4:0]) increases if a setup error is detected and decreases if a hold error is detected. The value of the DATACLK Delay [4:0] setting currently in use can be read back by the user.

Manual Timing Optimization Mode

When the device is operating in manual timing optimization mode (Register 0x02, Bit 3 = 0), the device does not alter the DATACLK Delay [4:0] value that is programmed by the user. By default, the DATACLK delay enable is inactive. This bit must be set high for the DATACLK Delay [4:0] value to be realized.

The delay (in absolute time) when programming the DATACLK delay from 00000 to 11111 varies from about 700 ps to about 6.5 ns. Typical delays per increment over temperature are shown in Table 27.

Table 27. Data Delay Line Typical Delays over Temperature

Delay	−40°C	+25°C	+85°C	Unit
Zero code delay (delay upon enabling delay line)	630	700	740	ps
Average unit delay	175	190	210	ps

In manual mode, the error checking logic is activated and generates an interrupt if a setup/hold violation is detected. One error check operation is performed per device configuration. Any change to the Data Timing Margin [3:0] or DATACLK Delay [4:0] values triggers a new error check operation.

INPUT DATA RAM

The AD9785/AD9787/AD9788 feature on-chip RAM that can be used as an alternative input data source to the input data pins. The input data RAM is loaded through the SPI port. After the input data is stored in memory, the device can be configured to transmit the stored data instead of receiving data through the input data pins. This can be a useful test mode for factory or in-system testing.

The RAM is 64 words long and 32 bits wide. The 16 MSBs drive the I datapath, and the 16 LSBs drive the Q datapath. The RAM configuration is shown in Figure 54.

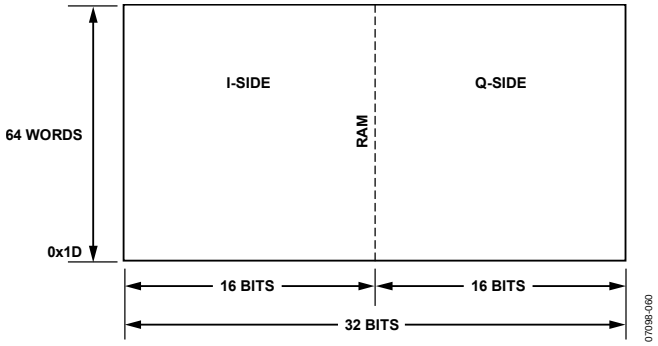


Figure 54. Input Data RAM Configuration

The data can be written to the RAM in either LSB first or MSB first format.

To write to the RAM in MSB first format, complete the following steps:

1. Set Bit 6 of Register 0x00 to 0.
2. Apply an instruction byte of 0xEE followed by the data to be stored.

After the instruction byte (a write to Register 0x1D) is received, the device automatically generates the addresses required to write the RAM, starting at the most significant address. The 32 rising SCLK edges following the instruction byte write the first RAM word. At this time, the internal address generator decrements and the next 32 rising edges of SCLK write the second RAM word. This cycle of decrementing the RAM address and writing 32-bit words continues until the last word is written. After the 64th word is written, the communication cycle is complete.

To write to the RAM in LSB first format, complete the following steps:

1. Set Bit 6 of Register 0x00 to 1.
2. Apply an instruction byte of 0xEE followed by the data to be stored.

All memory elements must be accessed to complete a communication cycle. Note that the RAM is not a dual-port memory element; therefore, if an I/O operation is begun while the RAM is being used to drive data into the signal processing path, the I/O operation has priority.

To begin using the RAM as an internal data generator, set Register 0x1E (test register) to a value of 0x00C000. After these 24 bits are written, the DAC starts to output the waveform stored in memory.

DIGITAL DATAPATH

The AD9785/AD9787/AD9788 digital datapath consists of three 2× half-band interpolation filters, a quadrature modulator, and an inverse sinc filter. A 32-bit NCO provides the sine and cosine carrier signals required for the quadrature modulator.

INTERPOLATION FILTERS

The AD9785/AD9787/AD9788 contain three half-band filters that can be bypassed. This allows the device to operate with 2×, 4×, or 8× interpolation rates, or without interpolation. The interpolation filters have a linear phase response. The coefficients of the low-pass filters are given in Table 28, Table 29, and Table 30. Spectral plots for the filter responses are shown in Figure 55, Figure 56, and Figure 57.

In 2×, 4×, or 8× interpolation mode, the usable bandwidth of the interpolation filter is 80% of the complex input data rate. The usable bandwidth has a pass-band ripple of less than 0.0005 dB and a stop-band attenuation of greater than 85 dB. The center frequency of the interpolation filter is set by the NCO frequency tuning word (Register 0x0A, Bits [31:0]), so baseband input signals are always centered in the interpolation filter pass band.

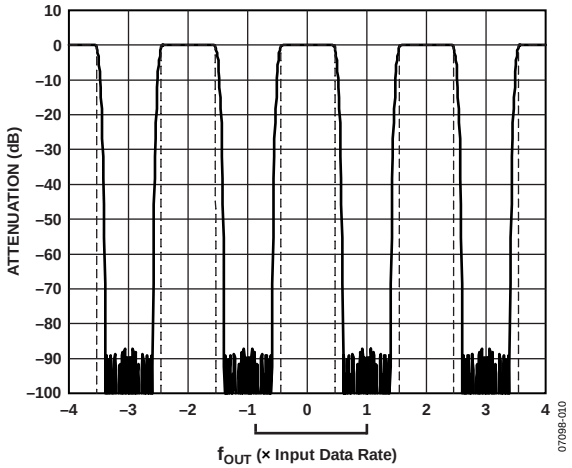


Figure 55. 2× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

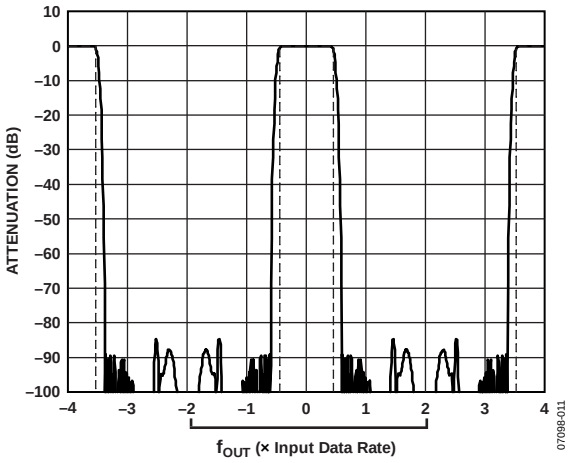


Figure 56. 4× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

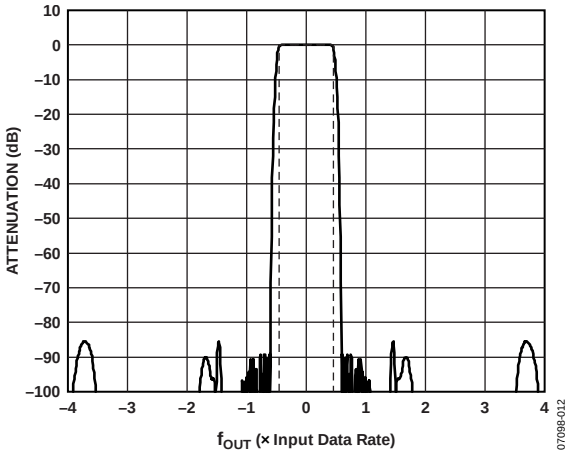


Figure 57. 8× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

Table 28. Half-Band Filter 1

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(55)	−4
H(2)	H(54)	0
H(3)	H(53)	+13
H(4)	H(52)	0
H(5)	H(51)	−34
H(6)	H(50)	0
H(7)	H(49)	+72
H(8)	H(48)	0
H(9)	H(47)	−138
H(10)	H(46)	0
H(11)	H(45)	+245
H(12)	H(44)	0
H(13)	H(43)	−408
H(14)	H(42)	0
H(15)	H(41)	+650
H(16)	H(40)	0
H(17)	H(39)	−1003
H(18)	H(38)	0
H(19)	H(37)	+1521
H(20)	H(36)	0
H(21)	H(35)	−2315
H(22)	H(34)	0
H(23)	H(33)	+3671
H(24)	H(32)	0
H(25)	H(31)	−6642
H(26)	H(30)	0
H(27)	H(29)	+20,755
H(28)		+32,768

Table 29. Half-Band Filter 2

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	−2
H(2)	H(22)	0
H(3)	H(21)	+17
H(4)	H(20)	0
H(5)	H(19)	−75
H(6)	H(18)	0
H(7)	H(17)	+238
H(8)	H(16)	0
H(9)	H(15)	−660
H(10)	H(14)	0
H(11)	H(13)	+2530
H(12)		+4096

Table 30. Half-Band Filter 3

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(15)	−39
H(2)	H(14)	0
H(3)	H(13)	+273
H(4)	H(12)	0
H(5)	H(11)	−1102
H(6)	H(10)	0
H(7)	H(9)	+4964
H(8)		+8192

QUADRATURE MODULATOR

The quadrature modulator is used to mix the carrier signal generated by the NCO with the upsampled I and Q data provided by the user at the 16-bit parallel input port of the device. Figure 58 shows a detailed block diagram of the quadrature modulator.

The NCO provides a quadrature carrier signal with a frequency determined by the 32-bit frequency tuning word (FTW) set in Register 0x0A, Bits [31:0]. The NCO operates at the rate equal to the upsampled I data and Q data. The generated carrier signal is mixed via multipliers with the I data and Q data. The quadrature products are then summed.

Note that the sine output of the NCO contains a mux that allows negating of the data. The mux is controlled with a spectral inversion bit that the user stores in an I/O register (Register 0x01, Bit 10). The default condition is to select negated sine data.

NUMERICALLY CONTROLLED OSCILLATOR

The NCO generates a complex carrier signal to translate the input signal to a new center frequency. A complex carrier signal is a pair of sinusoidal waveforms of the same frequency, offset 90° from each other. The frequency of the complex carrier signal is set via the Frequency Tuning Word [31:0] value in Register 0x0A. The frequency of the complex carrier signal is calculated as follows:

If $\{0 \le FTW \le 2^{31}\}$, use $f_{CENTER} = (FTW)\ (f_{DACCLK})/2^{32}$

If $\{2^{31} < FTW < 2^{32} - 1\}$, use $f_{CENTER} = f_{DACCLK} \times (1 - (FTW/2^{32}))$

A 16-bit phase offset may be added to the output of the phase accumulator via the serial port. This static phase adjustment results in an output signal that is offset by a constant angle relative to the nominal signal. This allows the user to phase align the NCO output with some external signal, if necessary. This can be especially useful when NCOs of multiple AD9785/AD9787/AD9788 devices are programmed for synchronization. The phase offset allows for the adjustment of the output timing between the devices. The static phase adjustment is sourced from the NCO Phase Offset Word [15:0] value located in Register 0x0B.

By default, when an SPI write is completed for the frequency tuning word, phase control, DAC gain scaling, or DAC offset registers (Register 0x0A through Register 0x0D), the operation of the AD9785/AD9787/AD9788 is immediately updated to reflect these changes. However, in many applications it may be more useful to update these registers without changing the device operation until all these functions can be updated at once. With the automatic I/O transfer enable bit set low in the COMM register (Register 0x00, Bit 1), the value of all these functions is stored in a buffer after the initial SPI write. To update all these functions simultaneously, Bit 2 of the COMM register should be set. This bit is self-resetting and thus does not require another reset in a later SPI write.

INVERSE SINC FILTER

The inverse sinc filter is implemented as a nine-tap FIR filter. It is designed to provide greater than ±0.05 dB pass-band ripple up to a frequency of $0.4 \times f_{DACCLK}$. To provide the necessary peaking at the upper end of the pass band, the inverse sinc filter has an intrinsic insertion loss of 3.4 dB. The tap coefficients are given in Table 31.

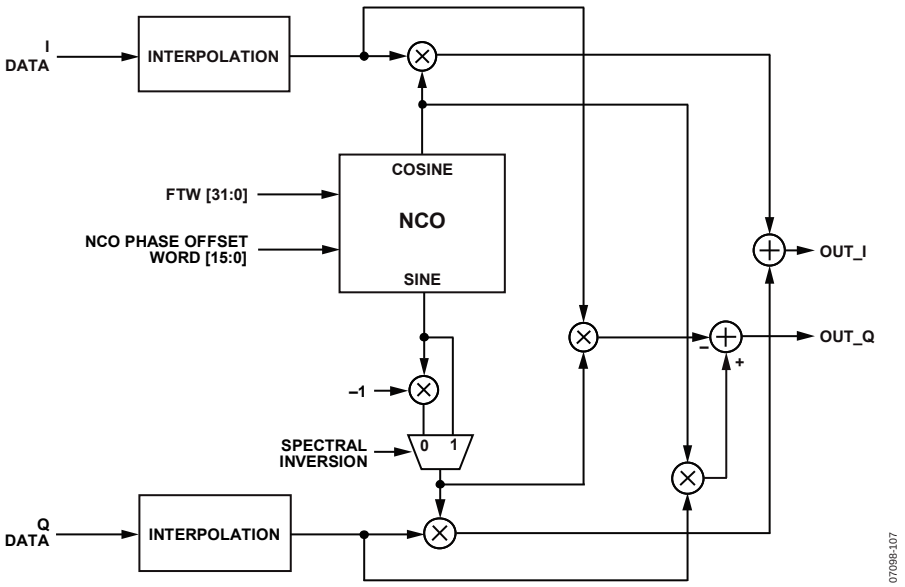


Figure 58. Quadrature Modulator Block Diagram

Table 31. Inverse Sinc Filter

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(9)	+2
H(2)	H(8)	−4
H(3)	H(7)	+10
H(4)	H(6)	−35
H(5)	–	+401

The inverse sinc filter is disabled by default. It can be enabled by setting the inverse sinc enable bit (Bit 9) in Register 0x01.

DIGITAL AMPLITUDE AND OFFSET CONTROL

The gain of the I datapath and the Q datapath can be independently scaled by adjusting the I DAC Amplitude Scale Factor [8:0] or Q DAC Amplitude Scale Factor [8:0] value in Register 0x0C. These values control the input to a digital multiplier. The value of the scale factor ranges from 0 to 3.9921875 and can be calculated as follows:

$$Scale\ Factor\ Value = \frac{Scale\ Factor\ [8:0]}{128}$$

The digital scale factor can be used to compensate for amplitude imbalance between the I and Q channels or to provide equal gain scaling to both channels for output level adjustment. Note that when the gain is set to 1.0 (scale factor = 0x80), the gain block is bypassed. When bypassed, the gain block has a different delay from when it is used. Therefore, to maintain matched latency in each path, both gain blocks should be set to exactly 1.0, or neither path should be set to exactly 1.0. Failing to maintain matched latencies in the I and Q paths creates a phase imbalance in quadrature signals, which results in poor sideband suppression of upconverted signals.

The dc value of the I datapath and the Q datapath can also be independently controlled. This is accomplished by adjusting the I DAC Offset [15:0] and Q DAC Offset [15:0] values in Register 0x0D. These values are added directly to the datapath values. Care should be taken not to overrange the transmitted values.

Figure 59 shows how the DAC offset current varies as a function of the I DAC Offset [15:0] and Q DAC Offset [15:0] values. With the digital inputs fixed at midscale (0x0000, twos complement data format), the figure shows the nominal I_{OUTx_P} and I_{OUTx_N} currents as the DAC offset value is swept from 0 to 65535. Because I_{OUTx_P} and I_{OUTx_N} are complementary current outputs, the sum of I_{OUTx_P} and I_{OUTx_N} is always 20 mA.

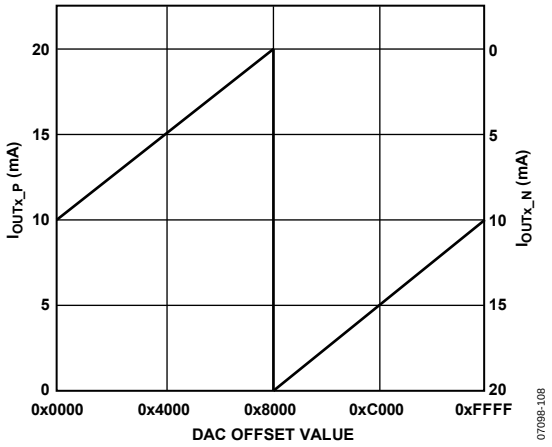


Figure 59. DAC Output Currents vs. DAC Offset Value

The offset currents generated by the DAC offset parameter increase from 0 mA to 10 mA as the offset is swept from 0 to 0x7FFF. The offset currents increase from −10 mA to 0 mA as the offset is swept from 0x8000 to 0xFFFF.

DIGITAL PHASE CORRECTION

The purpose of the phase correction block is to enable compensation of the phase imbalance of the analog quadrature modulator following the DAC. If the quadrature modulator has a phase imbalance, the unwanted sideband appears with significant energy. Adjusting the phase correction word can optimize image rejection in single sideband radios.

Ordinarily the I and Q channels have an angle of precisely 90° between them. The Phase Correction Word [9:0] (Register 0x0B) is used to change the angle between the I and Q channels. When the Phase Correction Word [9:0] is set to 1000000000b, the Q DAC output moves approximately 14° away from the I DAC output, creating an angle of 104° between the channels. When the Phase Correction Word [9:0] is set to 0111111111b, the Q DAC output moves approximately 14° towards the I DAC output, creating an angle of 76° between the channels. Based on these two endpoints, the resolution of the phase compensation register is approximately 28°/1024 or 0.027° per code.

DEVICE SYNCHRONIZATION

System demands may impose two different requirements for synchronization. Some systems require multiple DACs to be synchronized to each other, for example, a system that supports transmit diversity or beamforming, where multiple antennas are used to transmit a correlated signal. In this case, the DAC outputs need to be phase aligned with each other, but there may not be a requirement for the DAC outputs to be aligned with a system-level reference clock. In systems with a time division multiplexing transmit chain, one or more DACs may be required to be synchronized with a system-level reference clock.

Multiple devices are considered synchronized to each other when the state of the clock generation state machines is identical for all parts and the NCO phase accumulator is identical for all parts. Devices are considered synchronized to a system clock when there is a fixed and known relationship between the clock generation state machine and the NCO phase accumulator of the device to a particular clock edge of the system clock. The AD9785/AD9787/AD9788 support two modes of operation, pulse mode and PN code mode, for synchronizing devices under these two conditions.

SYNCHRONIZATION LOGIC OVERVIEW

Figure 60 shows a block diagram of the on-chip synchronization receive logic. There are two different modes of operation for the multichip synchronization feature: pulse mode and pseudorandom noise code (PN code) modulation/demodulation mode. The basic function of these two modes is to initialize the internal clock generation state machine and the NCO phase accumulator upon the application of external signals to the device.

The receive logic responsible for initializing the clock generation state machine generates a single DACCLK cycle-wide initialization pulse that sets the clock generation state machine logic to a known state. In pulse mode, this pulse is generated at every rising edge of the SYNC_I inputs. In PN code mode, the pulse is generated every time the correct code sequence is received on the SYNC_I inputs.

This initialization pulse loads the clock generation state machine with the Clock State [3:0] value (Register 0x03, Bits [7:4]) as its next state. If the initialization pulse from the synchronization logic is generated properly, it is active for one DAC clock cycle, every 32 (or multiple of 32) DAC clock cycles. Because the clock generation state machine has 32 states operating at the DACCLK rate, every initialization pulse received after the first pulse loads the current state (the state to which the state machine is already set), maintaining the proper clock operation of the device.

The Clock State [3:0] value is the state to which the clock generation state machine resets upon initialization. By varying this value, the timing of the internal clocks, with respect to the SYNC_I signal, can be adjusted. Every increment of the Clock State [3:0] value advances the internal clocks by one DACCLK period.

The NCO phase accumulators can be initialized in pulse mode or PN code mode. In pulse mode, a simultaneous strobe signal must be sent to the TXENABLE pin of all devices that is synchronous to the DATACLK signal. This signal resets the phase accumulator of the NCOs across all devices, effectively synchronizing the NCOs.

In PN code mode, the phase information of the master device is sent to the slave devices by the SYNC_I signal. The slave devices decode this phase information and automatically initialize their NCO phase accumulators to match the master device.

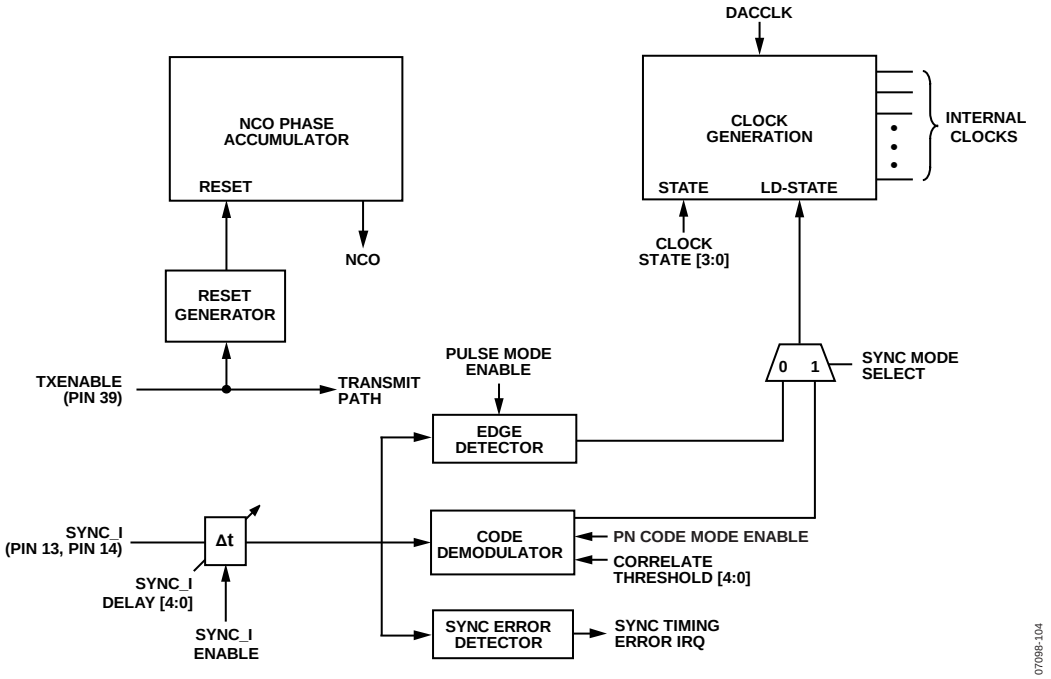


Figure 60. Synchronization Receive Circuitry Block Diagram

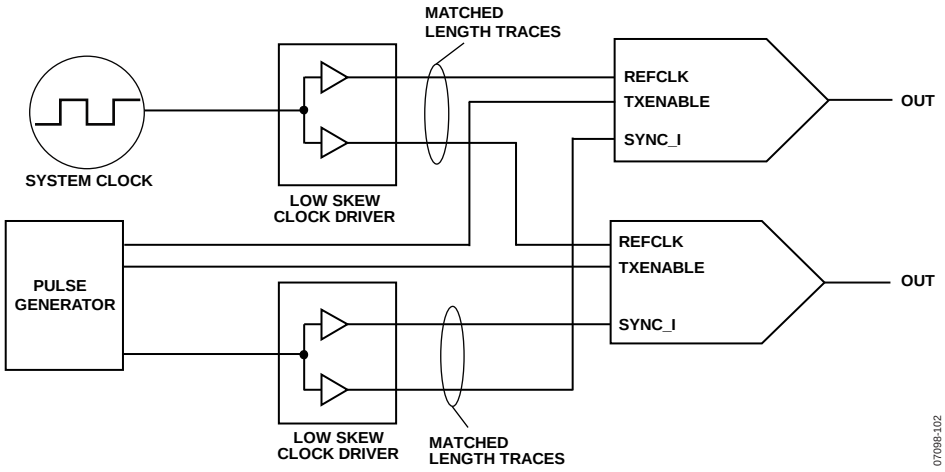


Figure 61. Multichip Synchronization in Pulse Mode

SYNCHRONIZING DEVICES TO A SYSTEM CLOCK

The AD9785/AD9787/AD9788 offer a pulse mode synchronization scheme (see Figure 61) to align the DAC outputs of multiple devices within a system to the same DAC clock edge. The pulse mode synchronization scheme is a two-part operation. First, the internal clocks are synchronized by providing either a one-time pulse or periodic signal to the SYNC_I (SYNC_I+/SYNC_I−) inputs. The SYNC_I signal is sampled by the internal DACCLK sample rate clock.

The SYNC_I input frequency has the following two constraints:

$$f_{SYNC\_IN} \leq f_{DATACLK}$$

$$f_{SYNC\_IN} = \frac{f_{DAC}}{16 \times N}$$

where N is an integer.

When the internal clocks are synchronized, the data sampling clocks between all devices are phase aligned. The next step requires a simultaneous strobe signal to the TXENABLE pin of all devices that is synchronous to the DATACLK signal. This resets the phase accumulator of the NCOs across all devices, effectively synchronizing the NCOs. The strobe signal is sampled by $f_{DATACLK}$ and must meet the same setup and hold times as the input data. Because the TXENABLE pin is an active high logic level pin, the strobe signal should be a low logic level pulse unless the TXENABLE invert bit is set in the SPI.

For this synchronization scheme, all devices are slave devices, while the system clock generation/distribution chip serves as the master. The external LVDS signal should be connected to the SYNC_I inputs of all the slave devices following the constraints. The DAC clock inputs and the SYNC_I inputs must be matched in length across all devices.

It is vital that the SYNC_I signal be distributed between the DACs with low skew. Likewise, the REFCLK signals must be distributed with low skew. Any skew on these signals between the DACs must be accounted for in the timing budget. The SYNC_I signal is sampled at the DACCLK rate, thus the data valid window of the SYNC_I pulse must be presented to all the DACs within the same DACCLK period.

Figure 62 shows the timing of the SYNC_I input with respect to the REFCLK input. Note that although the timing is relative to the REFCLK signal, SYNC_I is sampled at the DACCLK rate. This means that the rising edge of the SYNC_I signal must occur after the hold time of the preceding DACCLK rising edge and not the preceding REFCLK rising edge. Figure 63 shows a timing diagram of the TXENABLE input.

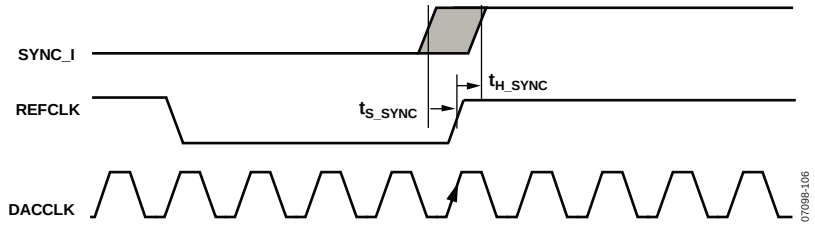


Figure 62. Timing Diagram of SYNC_I with Respect to REFCLK

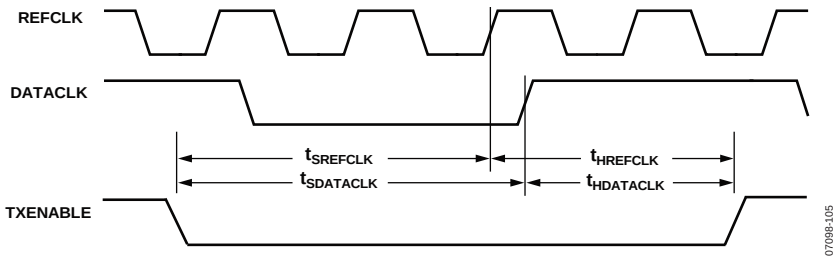


Figure 63. Timing Diagram of TXENABLE vs. DATACLK and REFCLK

Table 32 shows the register settings required to enable the pulse mode synchronization feature.

Table 32. Register Settings for Enabling Pulse Sync Mode

Register	Bit	Parameter	Value
0x01	[13]	PN code sync enable	0
	[12]	Sync mode select	0
	[11]	Pulse sync enable	1
0x03	[26]	SYNC_I enable	1
	[25]	SYNC_O enable	0
	[10]	Set high	0

Synchronization Timing Error Detection

The synchronization logic has error detection circuitry similar to the input data timing. The Sync Timing Margin [3:0] variable (Register 0x03) determines the setup and hold margin that the synchronization interface needs for the SYNC timing error IRQ to remain inactive (show error-free operation). Thus, the SYNC timing error IRQ is set whenever the setup and hold margins drop below the Sync Timing Margin [3:0] value and does not necessarily indicate that the SYNC_I input was latched incorrectly.

When a SYNC timing error IRQ is set, corrective action can restore the timing margin. The device can be configured for manual mode sync error monitoring and error correction.

Follow these steps to monitor SYNC_I setup and hold timing margins in manual mode:

1. Set sync error check mode (Register 0x03, Bit 18) = 0 (manual check mode).
2. Set Sync Timing Margin [3:0] (Register 0x03, Bits [3:0]) = 0000 (timing margin to minimum value).
3. Set SYNC_I Delay [4:0] (Register 0x03, Bits [23:19]) = 00000 (SYNC_I delay line to minimum value).
4. Set sync port IRQ enable (Register 0x09, Bit 0) = 1.
5. Write 1 to sync timing error IRQ (Register 0x09, Bit 6) to clear.
6. Read back sync timing error IRQ and sync timing error type (Register 0x09, Bit 4). If sync timing error IRQ is high, a sampling error has occurred, and sync timing error type indicates whether the sampling error is due to a setup time violation or a hold time violation.
7. Adjust the SYNC_I Delay [4:0] value until the sync timing error IRQ is no longer present.

SYNCHRONIZING MULTIPLE DEVICES TO EACH OTHER

The AD9785/AD9787/AD9788 synchronization engine uses a PN code synchronization scheme to align multiple devices within a system to the same DAC clock edge. The PN code scheme synchronizes all the internal clocks, as well as the phase accumulator of the NCO for all devices. With this scheme, one device functions as the master, and the remainder of the devices are configured as slaves.

The master device generates the PN encoded signal and drives the signal out on the SYNC_O (SYNC_O+/SYNC_O−) output pins. This signal is then sent to the SYNC_I (SYNC_I+/SYNC_I−) inputs of all the slave devices and to itself. The slave devices receive the code from the master and demodulate the signal to produce a synchronization pulse every time a valid code is received. The encoded signal of every device must be sampled on the same DAC clock edge for the devices to be properly synchronized. Therefore, it is extremely important that the REFCLK signals arrive at all the devices with as little skew between them as possible. In addition, the SYNC_I signals must arrive at all the devices with as little skew as possible. At high DACCLK frequencies, this requires using low skew clock distribution devices to deliver the REFCLK and SYNC_I signals and paying careful attention to printed circuit board signal routing to equalize the trace lengths of these signals.

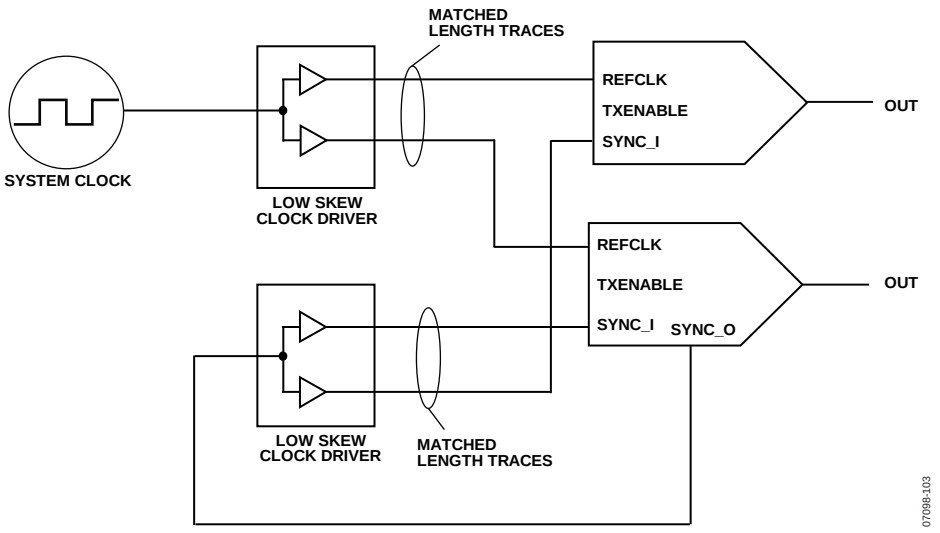


Figure 64. Multichip Synchronization in PN Code Mode

Table 33 lists the register settings required to enable the PN code mode synchronization feature.

Table 33. Register Settings for Enabling PN Code Mode

Register	Bit	Parameter	Value
0x01	[13]	PN code sync enable	1
	[12]	Sync mode select	1
	[11]	Pulse sync enable	0
0x03	[31:27]	Correlate Threshold [4:0]	10000
	[26]	SYNC_I enable	1
	[25]	SYNC_O enable	0 (slave devices) 1 (master device)
	[10]	Set high	1

To verify that the devices have successfully synchronized, read back the sync lock status bit on all devices (Register 0x09, Bit 10). The sync lock status bit should read back as 1 on all devices. Next, read back the sync lock lost status bit on all devices (Register 0x09, Bit 11). The sync lock lost status bit should read back as 0 on all devices. To clear the sync lock lost status bit, set the clear lock indicator bit to 1, followed by a 0 (Register 0x09, Bit 12).

Because the SYNC_O signal generated by the master is spread over many bits, this method of synchronization is very robust. Any individual bits that may become corrupted or somehow misread by the slave device usually have no effect on the synchronization of the device. If the devices do not reliably synchronize, there are several options for correcting the situation. The SYNC_O Delay [4:0] value (Register 0x03, Bits [15:11]) on the master device can be used to adjust the timing in 80 ps steps effective across all devices. In addition, the SYNC_O polarity bit (Register 0x03, Bit 9) on the master device can be set to provide a delay of one half the DACCLK period. The SYNC_I Delay [4:0] bits (Register 0x03, Bits [23:19]) can be used to adjust the timing on a single slave device in 80 ps steps.

The Correlate Threshold [4:0] value (Register 0x03, Bits [31:27]) indicates how closely the code of the received SYNC_I signal is to the expected code. A high threshold requires a closer match of the encoded signal to set the sync lock status bit; a lower value reduces the matching requirements to set the sync lock status bit.

Increasing the Correlate Threshold [4:0] value makes the part more resistant to false synchronization locks but requires a lower bit error rate on the SYNC_I input to maintain locked status. Decreasing the Correlate Threshold [4:0] value makes the part more susceptible to false synchronization locks, but maintains a locked status in the face of a higher bit error rate on the SYNC_I input (that is, it is more noise resistant). The recommended value for Correlate Threshold [4:0] is the default value of 16.

INTERRUPT REQUEST OPERATION

The IRQ pin (Pin 71) acts as an alert that the device has experienced a timing error and that it should be queried (by reading Register 0x09) to determine the exact fault condition. The IRQ pin is an open-drain, active low output. The IRQ pin should be pulled high external to the device. This pin may be tied to the IRQ pins of other devices with open-drain outputs to wire-OR these pins together.

There are two different error flags that can trigger an interrupt request: a data timing error or a sync timing error. By default, when either or both of these error flags are set, the IRQ pin is active low. Either or both of these error flags can be masked to prevent them from activating an interrupt on the IRQ pin.

The error flags are latched and remain active until the flag bits are overwritten.

DRIVING THE REFCLK INPUT

The REFCLK input requires a low jitter differential drive signal. REFCLK is a PMOS input differential pair powered from the 1.8 V supply; therefore, it is important to maintain the specified 400 mV input common-mode voltage. Each input pin can safely swing from 200 mV p-p to 1 V p-p about the 400 mV common-mode voltage. Although these input levels are not directly LVDS-compatible, REFCLK can be driven by an offset ac-coupled LVDS signal, as shown in Figure 65.

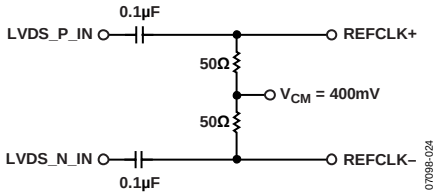


Figure 65. LVDS REFCLK Drive Circuit

If a clean sine clock is available, it can be transformer-coupled to REFCLK, as shown in Figure 66. Use of a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through a CMOS-to-LVDS translator, then ac-coupled.

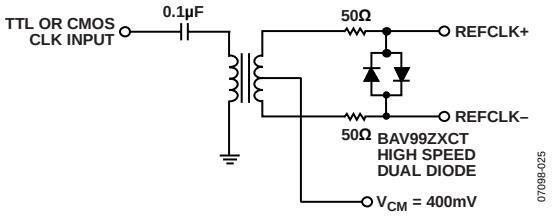


Figure 66. TTL or CMOS REFCLK Drive Circuit

A simple bias network for generating V_{CM} is shown in Figure 67. It is important to use CVDD18 and CGND for the clock bias circuit. Any noise or other signal that is coupled onto the clock is multiplied by the DAC digital input signal and can degrade DAC performance.

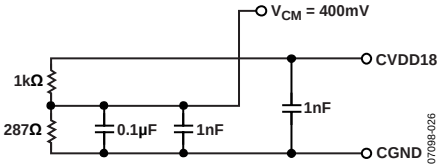


Figure 67. REFCLK V_{CM} Generator Circuit

DAC REFCLK CONFIGURATION

The AD9785/AD9787/AD9788 offer two modes of sourcing the DAC sample clock (DACCLK). The first mode employs an on-chip clock multiplier that accepts a reference clock operating at the lower input frequency, most commonly the data input frequency. The on-chip phase-locked loop (PLL) then multiplies the reference clock up to a higher frequency, which can then be used to generate all the internal clocks required by the DAC.

The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier removes the burden of generating and distributing the high speed DACCLK.

The second mode bypasses the clock multiplier circuitry and allows DACCLK to be directly sourced through the REFCLK pins. This mode enables the user to source a very high quality clock directly to the DAC core. Sourcing the DACCLK directly through the REFCLK pins may be necessary in demanding applications that require the lowest possible DAC output noise at higher output frequencies.

In either case, using the on-chip clock multiplier or sourcing the DACCLK directly through the REFCLK pins, it is necessary that the REFCLK signal have low jitter to maximize the DAC noise performance.

Direct Clocking

When the PLL is disabled (Register 0x04, Bit 15 = 0), the REFCLK input is used directly as the DAC sample clock (DACCLK). The output frequency of the DATACLK output pin is

$$f_{DATACLK} = f_{DACCLK}/(IF \times P)$$

where *IF* is the interpolation factor, set in Register 0x01, Bits [7:6], and *P* = 0.5 if in single-port mode.

Clock Multiplication

When the PLL is enabled (Register 0x04, Bit 15 = 1), the clock multiplication circuit generates the DAC sample clock from the lower rate REFCLK input. The functional diagram of the clock multiplier is shown in Figure 68.

The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}, equal to the REFCLK input signal frequency multiplied by N1 × N2.

$$f_{VCO} = f_{REFCLK} \times (N1 \times N2)$$

The DAC sample clock frequency, f_{DACCLK}, is equal to

$$f_{DACCLK} = f_{REFCLK} \times N2$$

The values of N1 and N2 must be chosen to keep f_{VCO} in the optimal operating range of 1.0 GHz to 2.0 GHz. When the VCO output frequency is known, the correct PLL band select value (Register 0x04, Bits [7:2]) can be chosen.

PLL Bias Settings

There are three bias settings for the PLL circuitry that should be programmed to their nominal values. The PLL values shown in Table 34 are the recommended settings for these parameters.

Table 34. PLL Settings

PLL SPI Control	Address		Optimal Setting
	Register	Bit	
PLL Loop Bandwidth	0x04	[20:16]	01111
PLL VCO Drive	0x04	[1:0]	11
PLL Bias	0x04	[10:8]	011

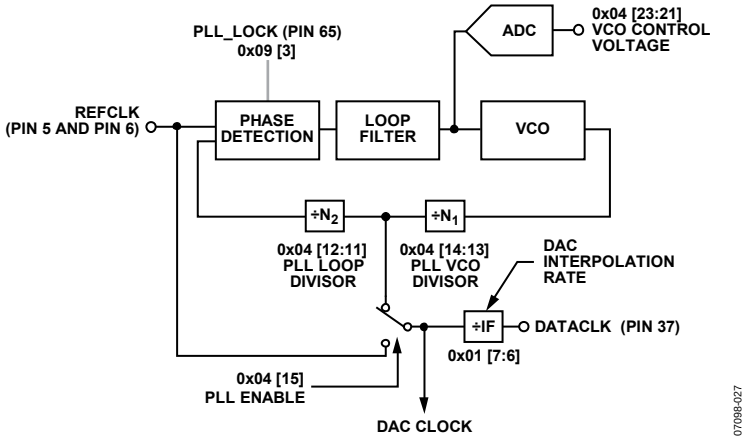


Figure 68. Clock Multiplication Circuit

Table 35. Typical VCO Freq Range vs. PLL Band Select Value

PLL Lock Ranges over Temperature, −40°C to +85°C		
	VCO Frequency Range in MHz[1]	
PLL Band Select	f_{LOW}	f_{HIGH}
111111 (63)	Auto mode	Auto mode
111110 (62)	1975	2026
111101 (61)	1956	2008
111100 (60)	1938	1992
111011 (59)	1923	1977
111010 (58)	1902	1961
111001 (57)	1883	1942
111000 (56)	1870	1931
110111 (55)	1848	1915
110110 (54)	1830	1897
110101 (53)	1822	1885
110100 (52)	1794	1869
110011 (51)	1779	1853
110010 (50)	1774	1840
110001 (49)	1748	1825
110000 (48)	1729	1810
101111 (47)	1730	1794
101110 (46)	1699	1780
101101 (45)	1685	1766
101100 (44)	1684	1748
101011 (43)	1651	1729
101010 (42)	1640	1702
101001 (41)	1604	1681
101000 (40)	1596	1658
100111 (39)	1564	1639
100110 (38)	1555	1606
100101 (37)	1521	1600
100100 (36)	1514	1575
100011 (35)	1480	1553
100010 (34)	1475	1529
100001 (33)	1439	1505
100000 (32)	1435	1489

PLL Lock Ranges over Temperature, −40°C to +85°C		
	VCO Frequency Range in MHz[1]	
PLL Band Select	f_{LOW}	f_{HIGH}
011111 (31)	1402	1468
011110 (30)	1397	1451
011101 (29)	1361	1427
011100 (28)	1356	1412
011011 (27)	1324	1389
011010 (26)	1317	1375
011001 (25)	1287	1352
011000 (24)	1282	1336
010111 (23)	1250	1313
010110 (22)	1245	1299
010101 (21)	1215	1277
010100 (20)	1210	1264
010011 (19)	1182	1242
010010 (18)	1174	1231
010001 (17)	1149	1210
010000 (16)	1141	1198
001111 (15)	1115	1178
001110 (14)	1109	1166
001101 (13)	1086	1145
001100 (12)	1078	1135
001011 (11)	1055	1106
001010 (10)	1047	1103
001001 (9)	1026	1067
001000 (8)	1019	1072
000111 (7)	998	1049
000110 (6)	991	1041
000101 (5)	976	1026
000100 (4)	963	1011
000011 (3)	950	996
000010 (2)	935	981
000001 (1)	922	966
000000 (0)	911	951

[1] The lock ranges in this table are typical values. Actual lock ranges will vary from device to device.

Configuring the PLL Band Select Value

The PLL VCO has a valid operating range from approximately 1.0 GHz to 2.0 GHz covered in 63 overlapping frequency bands as shown in Table 35. For any desired VCO output frequency, there are multiple valid PLL band select values. Note that the data shown in Table 35 is for a typical device. Device-to-device variations can shift the actual VCO output frequency range by 30 MHz to 40 MHz. Also, the VCO output frequency varies as a function of temperature. Therefore, it is required that the optimal PLL band select value be determined for each individual device at the particular operating temperature.

The device has an automatic PLL band select feature on chip. When enabled, the device determines the optimal PLL band setting for the device at the given temperature. This setting holds for a ±60°C temperature swing in ambient temperature. If the device operates in an environment that experiences a larger temperature swing, an offset should be applied to the automatically selected PLL band. The following procedure outlines a method for setting the PLL band select value for a device operating at a particular temperature that holds for a change in ambient temperature over the total −40°C to +85°C operating range of the device without further user intervention. (Note that REFCLK must be applied to the device during this procedure.)

Configuring PLL Band Select with Temperature Sensing

The values of N1 (Register 0x04, Bits [14:13]) and N2 (Register 0x04, Bits [12:11]) should be programmed along with the PLL settings shown in Table 34.

1. Set the PLL Band Select [5:0] value (Register 0x04, Bits [7:2]) to 63 to enable PLL auto mode.
2. Wait for the PLL_LOCK pin or the PLL lock indicator (Register 0x09, Bit 3) to go high. This should occur within 5 ms.
3. Read back the 6-bit PLL band select value (Register 0x04, Bits [7:2]).
4. Based on the temperature when the PLL auto mode is enabled, set the PLL band indicated in Table 36 or Table 37 by rewriting the readback values into the PLL Band Select [5:0] parameter (Register 0x04, Bits [7:2]).

Table 36. Setting Optimal PLL Band for Lower Range (0 to 31) Bands

System Start-Up Temperature	Set PLL Band to
−40°C to −10°C	Readback Band + 2
−10°C to +15°C	Readback Band + 1
15°C to 55°C	Readback Band
55°C to 85°C	Readback Band − 1

Table 37. Setting Optimal PLL Band for Higher Range (32 to 62) Bands

System Start-Up Temperature	Set PLL Band to
−40°C to −30°C	Readback Band + 3
−30°C to −10°C	Readback Band + 2
−10°C to +15°C	Readback Band + 1
15°C to 55°C	Readback Band
55°C to 85°C	Readback Band − 1

Known Temperature Calibration with Memory

The procedure in the Configuring PLL Band Select with Temperature Sensing section requires temperature sensing upon start-up or reset of the device to choose the optimal PLL band select value to hold over the entire operating temperature range. If temperature sensing is not available in the system, another option is to use the automatic PLL band select to determine the optimal setting for the device when the device is in a factory environment where the temperature is known. The optimal band can then be stored in nonvolatile memory. Whenever the system is powered up or restarted, the optimal value can be loaded back into the device.

ANALOG OUTPUTS

Full-scale current on the I DAC and Q DAC can be set from 8.66 mA to 31.66 mA. Initially, the 1.2 V band gap reference is used to set up a current in an external resistor connected to I120 (Pin 75). A simplified block diagram of the reference circuitry is shown in Figure 69.

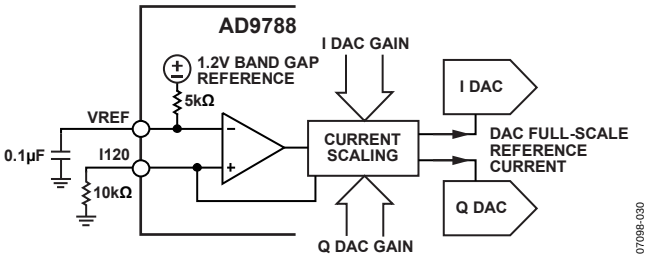


Figure 69. Full-Scale Current Generation Circuitry

The recommended value for the external resistor is 10 kΩ, which sets up an $I_{REFERENCE}$ in the resistor of 120 µA, which in turn provides a DAC output full-scale current of 20 mA. Because the gain error is a linear function of this resistor, a high precision resistor improves gain matching to the internal matching specification of the devices. Internal current mirrors provide a current-gain scaling, where DAC gain is a 10-bit word in the SPI port register (Register 0x05 and Register 0x07). The default value for the DAC gain registers gives an I_{FS} of approximately 20 mA, where I_{FS} for either I DAC or Q DAC is equal to

$$\frac{1.2\ \text{V}}{R} \times \left(\frac{27}{12} + \left(\frac{6}{1024} \times DAC\ gain \right) \right) \times 32$$

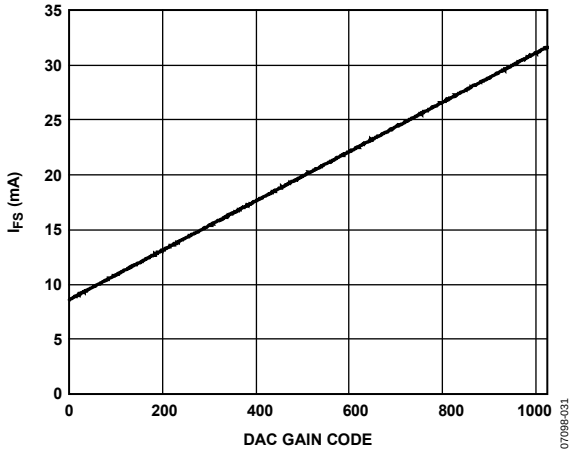


Figure 70. DAC Full-Scale Current vs. DAC Gain Code

DIGITAL AMPLITUDE SCALING

Gain scaling of the analog DAC output can be achieved by changing the values in Register 0x05 and Register 0x07. However, if this is done, the output common-mode voltage at the analog output also decreases proportionally. This poses a problem when the AD9785/AD9787/AD9788 are dc-coupled to a quadrature modulator. Typical quadrature modulators have tight restrictions on input common-mode variation.

The AD9785/AD9787/AD9788 use a digital gain scaling block to get around this problem. Because the gain scaling is done in the digital processing of the AD9785/AD9787/AD9788, there is no effect on the output full-scale current. This digital gain scaling is done in such a way that the midscale value of the signal is unaffected; the swing of the signal around midscale is the value that is adjusted with the register settings. Digital gain scaling is done using the amplitude scale factor (ASF) register (Register 0x0C).

Auxiliary DAC Operation

Two auxiliary DACs are provided on the AD9785/AD9787/AD9788. The full-scale output current on these DACs is derived from the 1.2 V band gap reference and external resistor. The gain scale from the reference amplifier current, $I_{REFERENCE}$, to the auxiliary DAC reference current is 16.67 with the auxiliary DAC gain set to full scale (10-bit values, Register 0x06, Bits [9:0] and Register 0x08, Bits [9:0]). This gives a full-scale current of approximately 2 mA for Auxiliary DAC 1 and Auxiliary DAC 2.

The auxiliary DAC outputs are not differential. Only one side of the auxiliary DAC (P or N) is active at one time. The inactive side goes into a high impedance state (100 kΩ). In addition, the P or N output can act as a current source or a current sink. Control of the P and N sides for both auxiliary DACs is via Register 0x06 and Register 0x08, Bits [15:14]. When sourcing current, the output compliance voltage is 0 V to 1.6 V. When sinking current, the output compliance voltage is 0.8 V to 1.6 V.

There are two output signals on each auxiliary DAC. One signal is designated P, the other N. The sign bit in each auxiliary DAC control register (Bit 15) controls whether the P side or the N side of the auxiliary DAC is turned on. Only one side of the auxiliary DAC is active at a time. The auxiliary DAC structure is shown in Figure 71.

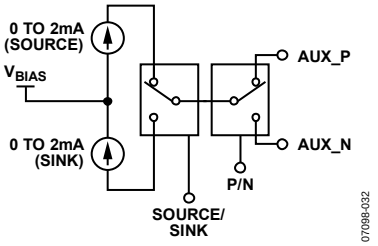


Figure 71. Auxiliary DAC Structure

The magnitude of the auxiliary DAC 1 current is controlled by the auxiliary DAC 1 control register (Register 0x06), and the magnitude of the auxiliary DAC 2 current is controlled by the auxiliary DAC 2 control register (Register 0x08). These auxiliary DACs have the ability to source or sink current. This selection is programmable via Bit 14 in either auxiliary DAC control register.

The choice of sinking or sourcing should be made at circuit design time. There is no advantage to switching between sourcing and sinking current after the circuit is in place.

The auxiliary DACs can be used for local oscillator (LO) cancellation when the DAC output is followed by a quadrature modulator. This LO feedthrough is caused by the input referred dc offset voltage of the quadrature modulator (and the DAC output offset voltage mismatch) and can degrade system performance. Typical DAC-to-quadrature modulator interfaces are shown in Figure 72 and Figure 73. Often, the input common-mode voltage for the modulator is much higher than the output compliance range of the DAC, so that ac coupling or a dc level shift is necessary. If the required common-mode input voltage on the quadrature modulator matches that of the DAC, then the dc blocking capacitors in Figure 72 can be removed.

A low-pass or band-pass passive filter is recommended when spurious signals from the DAC (distortion and DAC images) at the quadrature modulator inputs can affect system performance. Placing the filter at the location shown in Figure 72 and Figure 73 allows easy design of the filter, as the source and load impedances can easily be designed close to 50 Ω.

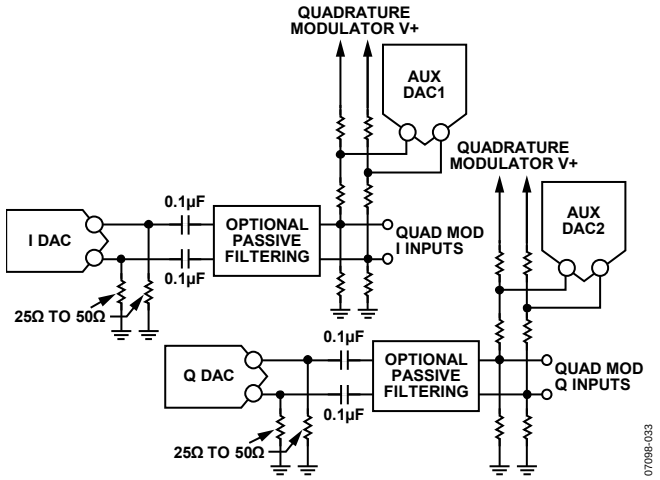


Figure 72. Typical Use of Auxiliary DACs AC Coupling to Quadrature Modulator

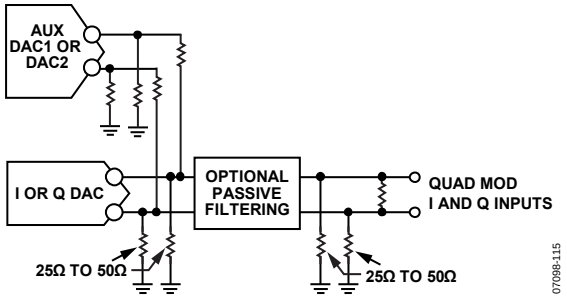


Figure 73. Typical Use of Auxiliary DACs DC Coupling to Quadrature Modulator with DC Shift

POWER DISSIPATION

Figure 74 through Figure 78 detail the power dissipation of the AD9785/AD9787/AD9788 under a variety of operating conditions. All of the graphs are taken with data being supplied to both the I and Q channels. The power consumption of the device does not vary significantly with changes in the modulation mode or analog output frequency. Graphs of the total power dissipation are shown along with the power dissipation of the DVDD18, DVDD33, and CVDD18 supplies.

The power dissipation of the AVDD33 supply rail is independent of the digital operating mode and sample rate. The current drawn from the AVDD33 supply rail is typically 51 mA (182 mW) when the full-scale current of the I and Q DACs is set to the nominal value of 20 mA. Changing the full-scale current directly impacts the supply current drawn from the AVDD33 rail. For example, if the full-scale current of the I DAC and the Q DAC is changed to 10 mA each, the AVDD33 supply current drops to 31 mA.

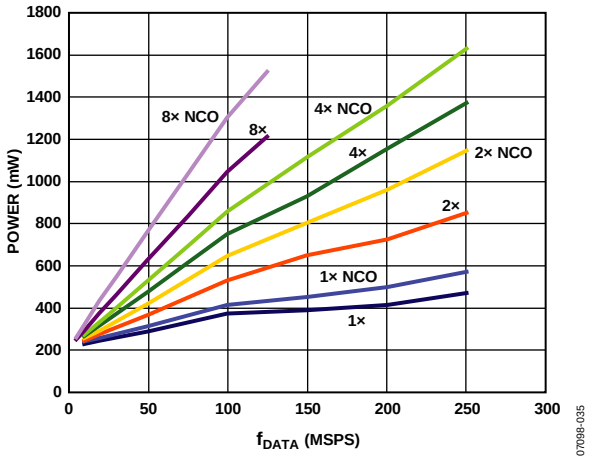


Figure 74. Power Dissipation, I and Q Data, Dual DAC Mode

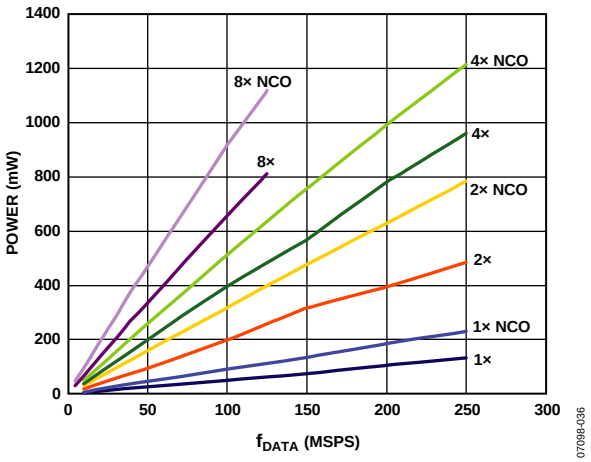


Figure 75. Power Dissipation, Digital 1.8 V Supply, I and Q Data, Dual DAC Mode

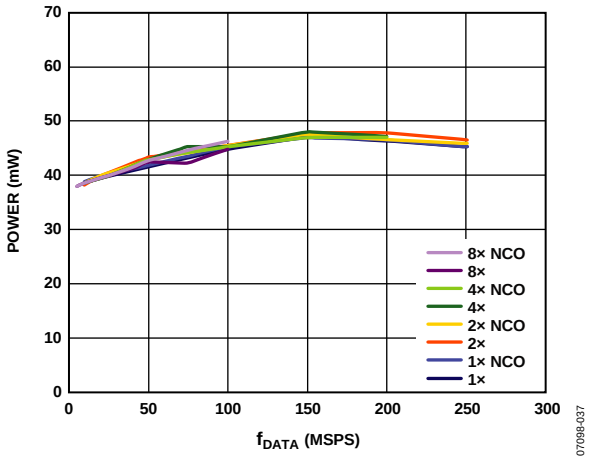


Figure 76. Power Dissipation, Digital 3.3 V Supply, I and Q Data, Dual DAC Mode

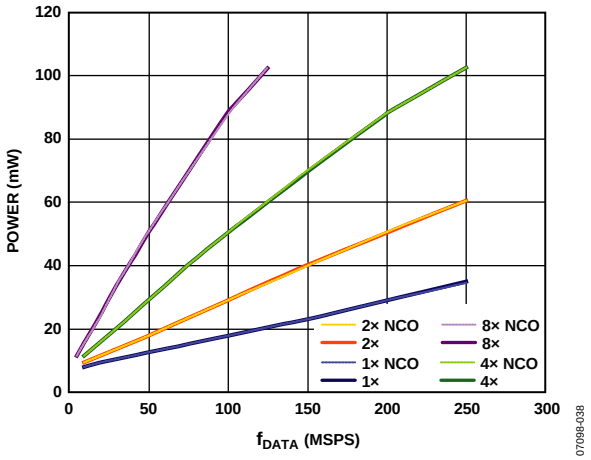


Figure 77. Power Dissipation, Clock 1.8 V Supply, I and Q Data, Dual DAC Mode

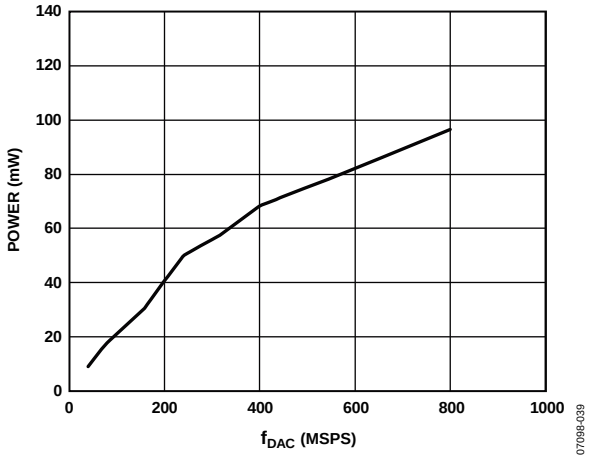


Figure 78. Digital 1.8 V Supply, Power Dissipation of Inverse Sinc Filter

AD9785/AD9787/AD9788 EVALUATION BOARDS

The remainder of this data sheet describes the evaluation boards for testing the AD9785, AD9787, and AD9788 devices.

OUTPUT CONFIGURATION

Each evaluation board contains an Analog Devices ADL5372 quadrature modulator. The AD9785/AD9787/AD9788 devices and the ADL5372 provide an easy-to-interface DAC/modulator combination that can be easily characterized on the evaluation board.

Solderable jumpers can be configured to evaluate the single-ended or differential outputs of the AD9785/AD9787/AD9788.

The factory default jumper configuration is as follows:

- Jumpers JP2, JP3, JP4, and JP8 are unsoldered.
- Jumpers JP14, JP15, JP16, and JP17 are soldered.

To evaluate the ADL5372 on the evaluation board, reverse the jumper positions as follows:

- Jumpers JP2, JP3, JP4, and JP8 are soldered.
- Jumpers JP14, JP15, JP16, and JP17 are unsoldered.

Note that the ADL5372 also requires its own separate 5 V and GND connection on the evaluation board.

DIGITAL PICTURE OF EVALUATION BOARD

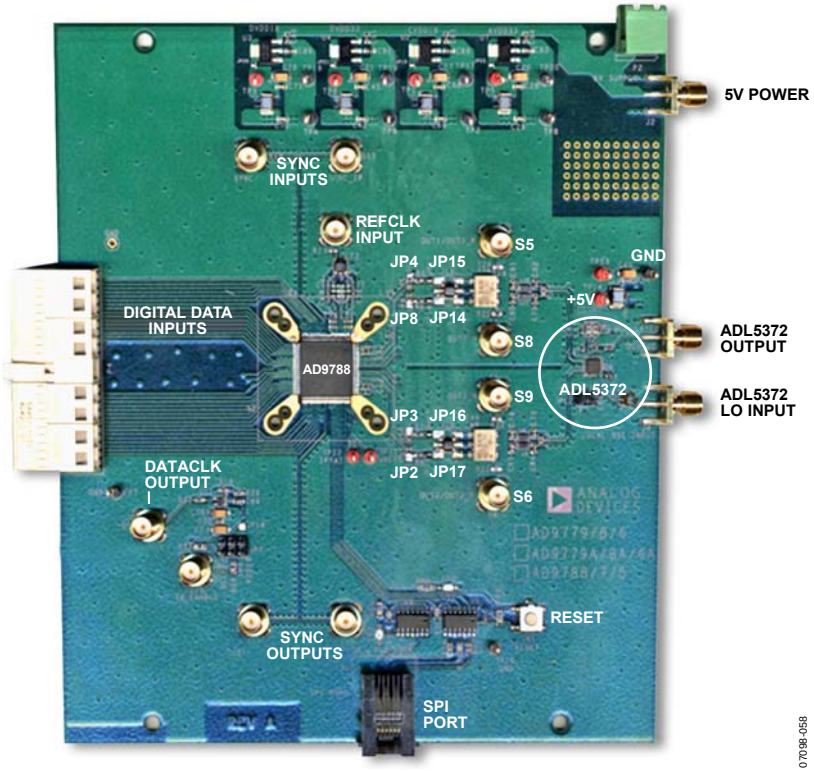


Figure 79. Evaluation Board

EVALUATION BOARD SOFTWARE

A GUI .exe file for Microsoft® Windows® is included on the CD that ships with the evaluation board. This file allows the user to easily program all the functions on the AD9785/AD9787/AD9788.

Figure 80 shows this user interface. The most important features for configuring the AD9785/AD9787/AD9788 are called out in the figure.

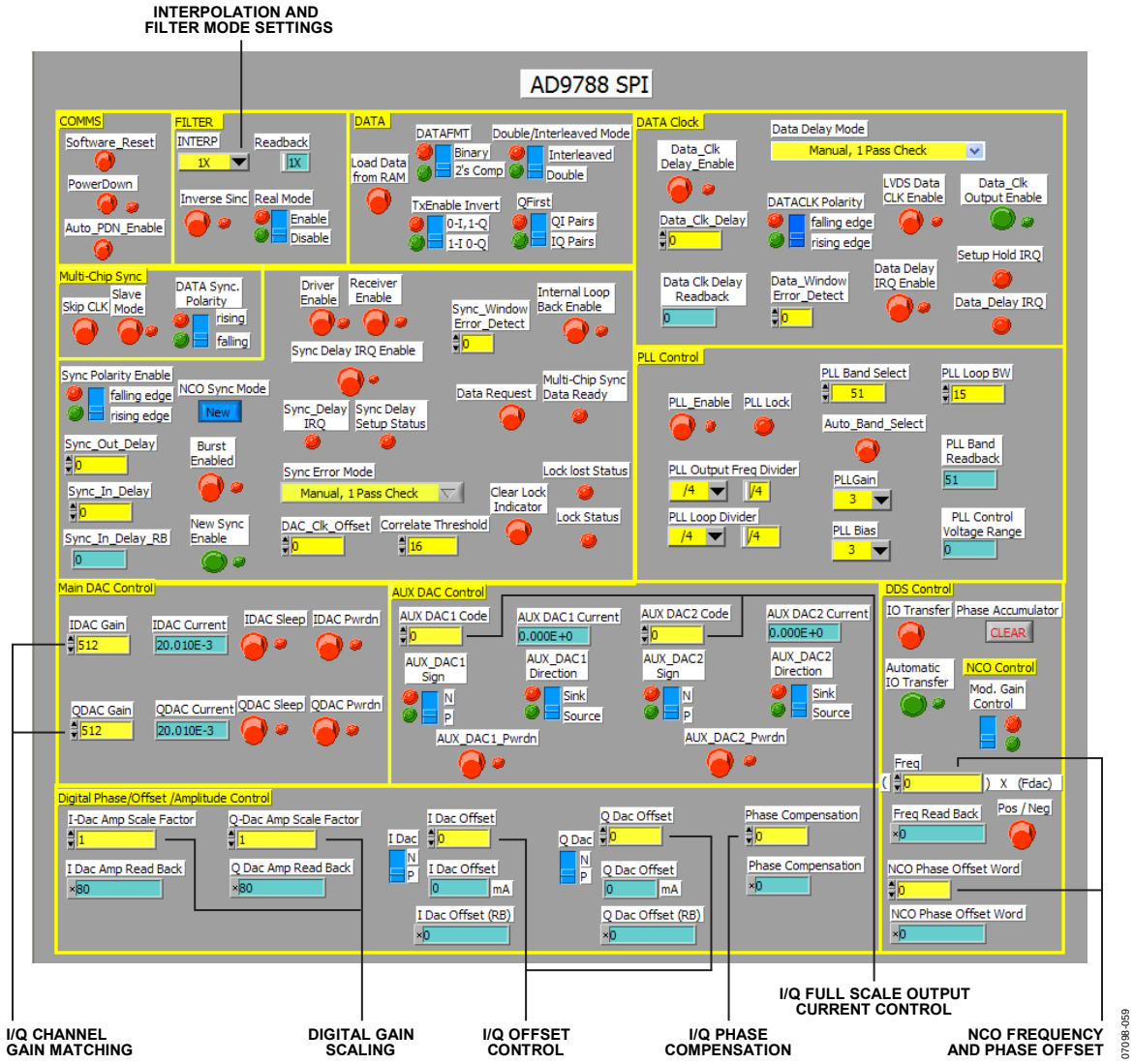


Figure 80. AD9788 User Interface

EVALUATION BOARD SCHEMATICS

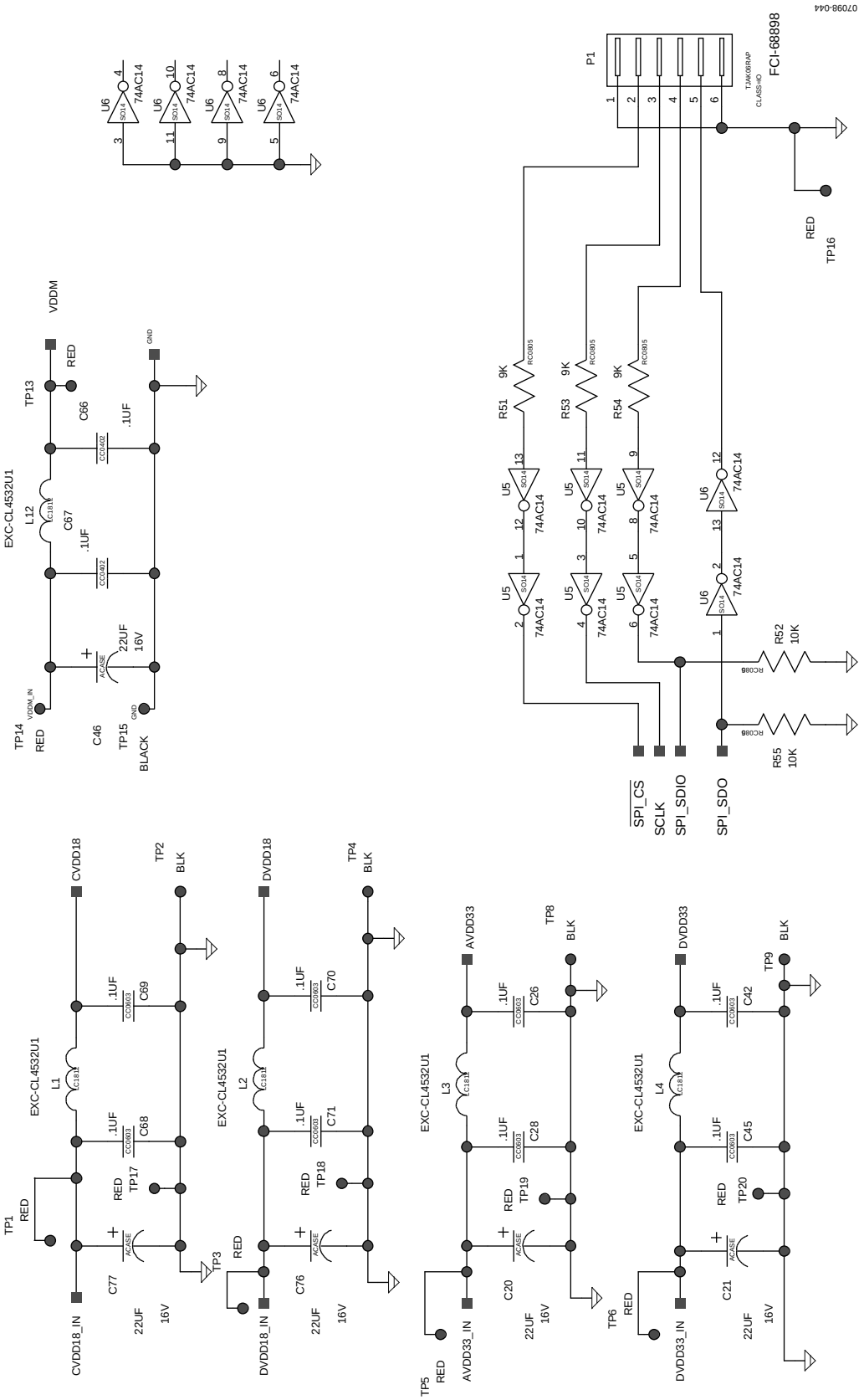


Figure 81. Evaluation Board, Power Supply and Decoupling

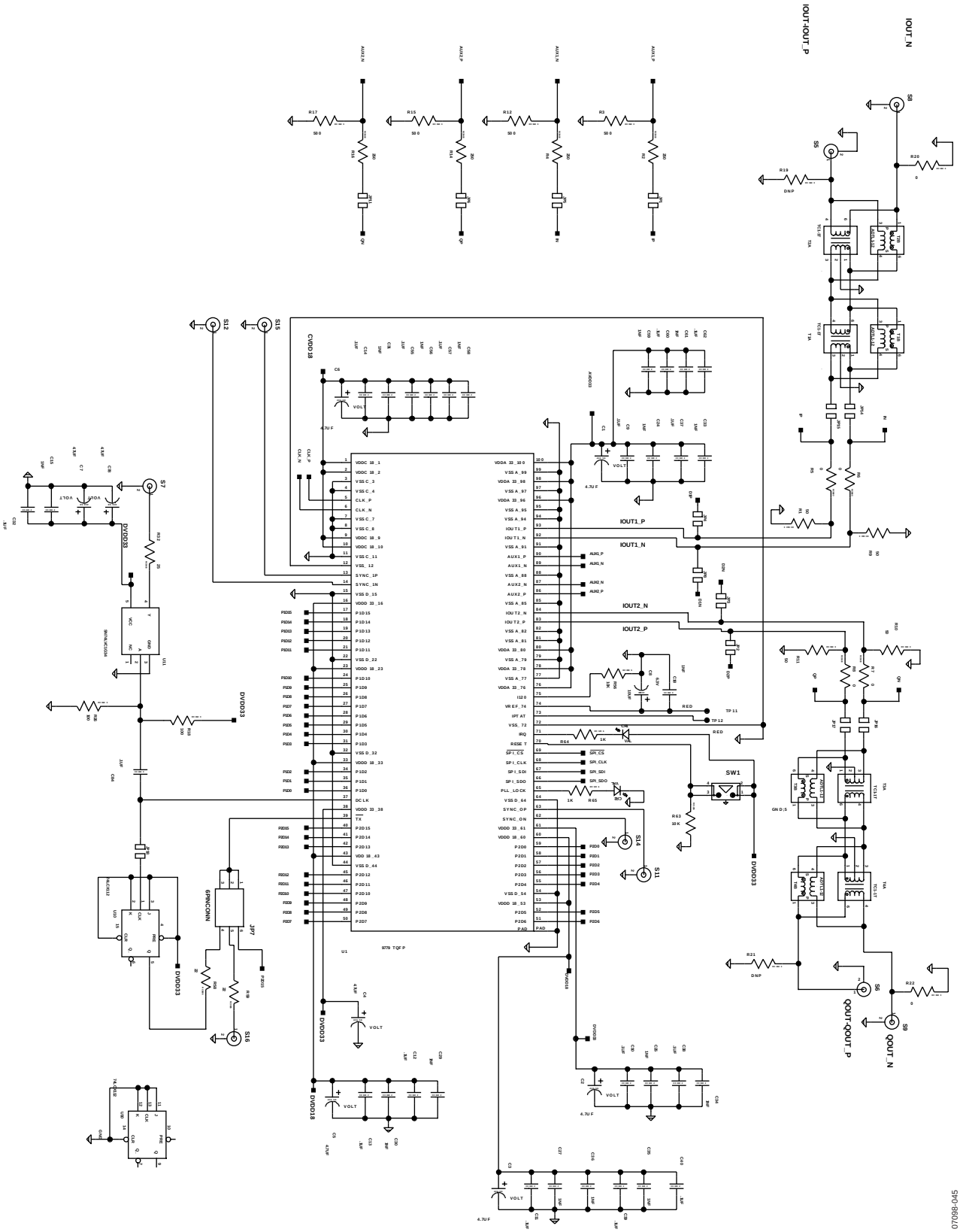


Figure 82. Evaluation Board, Analog and Digital Interfaces to TxDAC

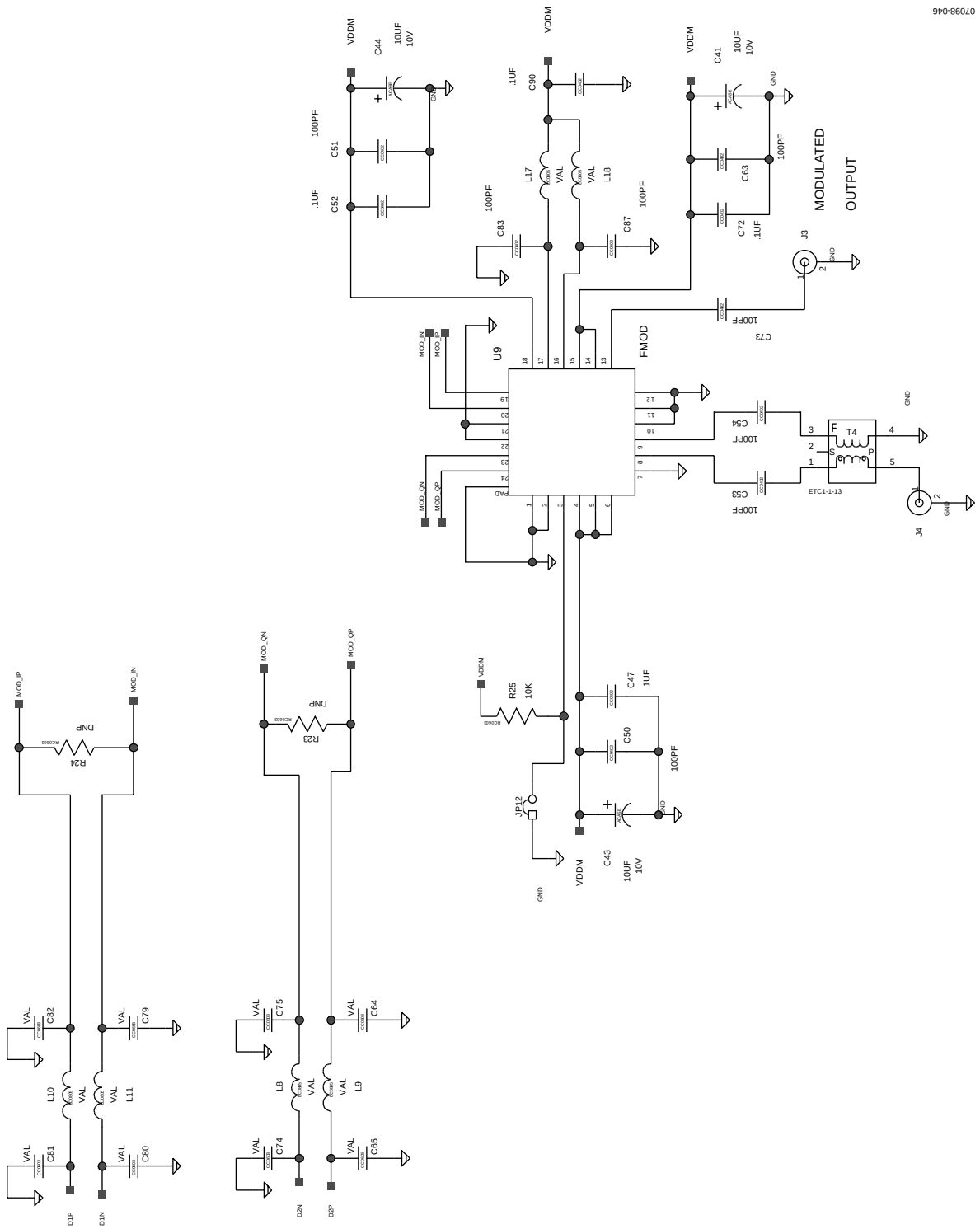


Figure 83. Evaluation Board, ADL5372 (FMOD2) Quadrature Modulator

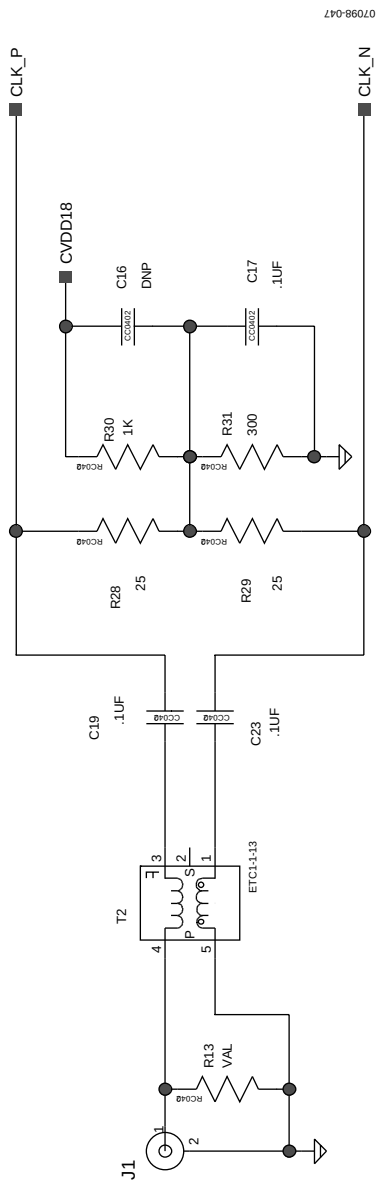


Figure 84. Evaluation Board, TxDAC Clock Interface

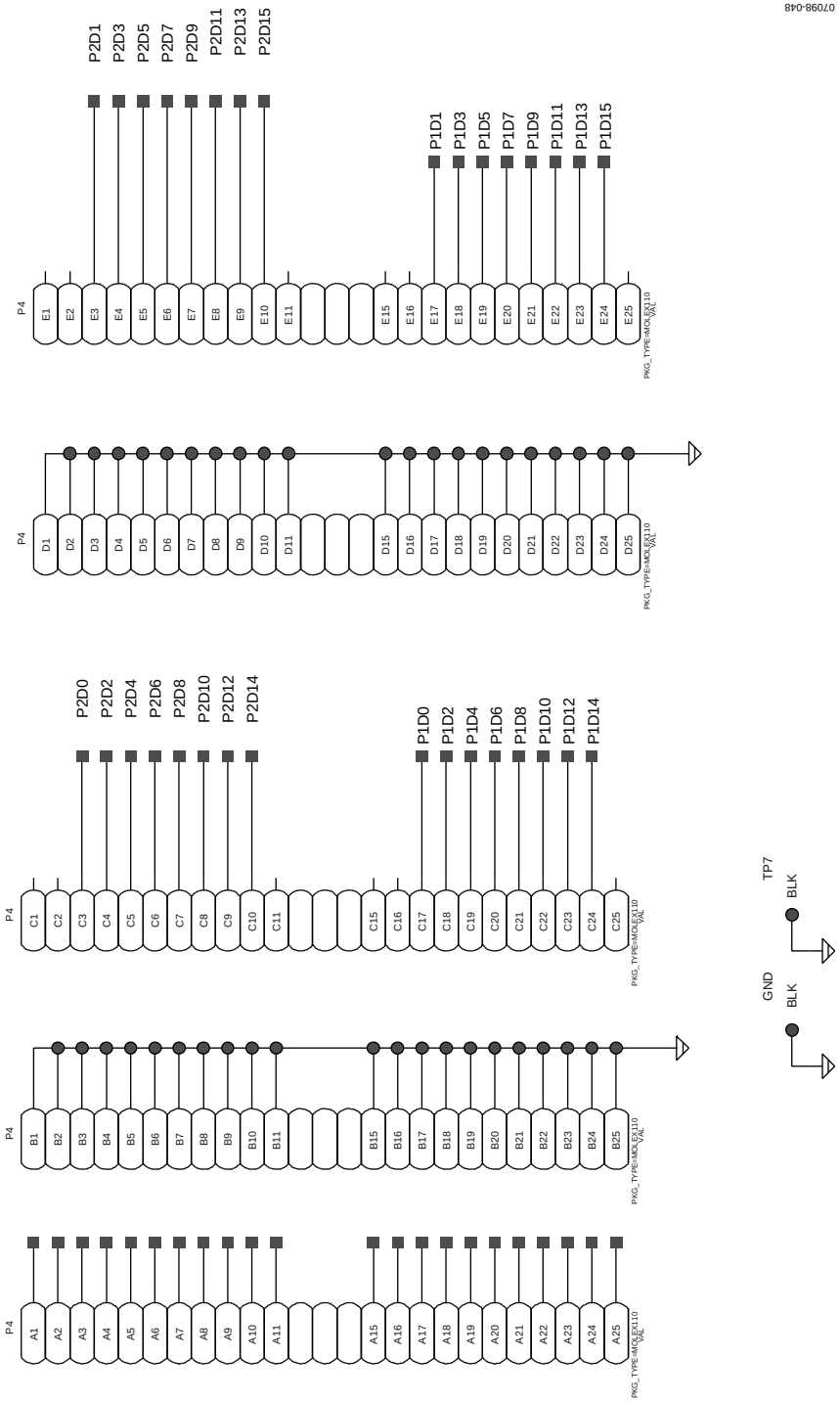


Figure 85. Evaluation Board, Digital Input Data Lines

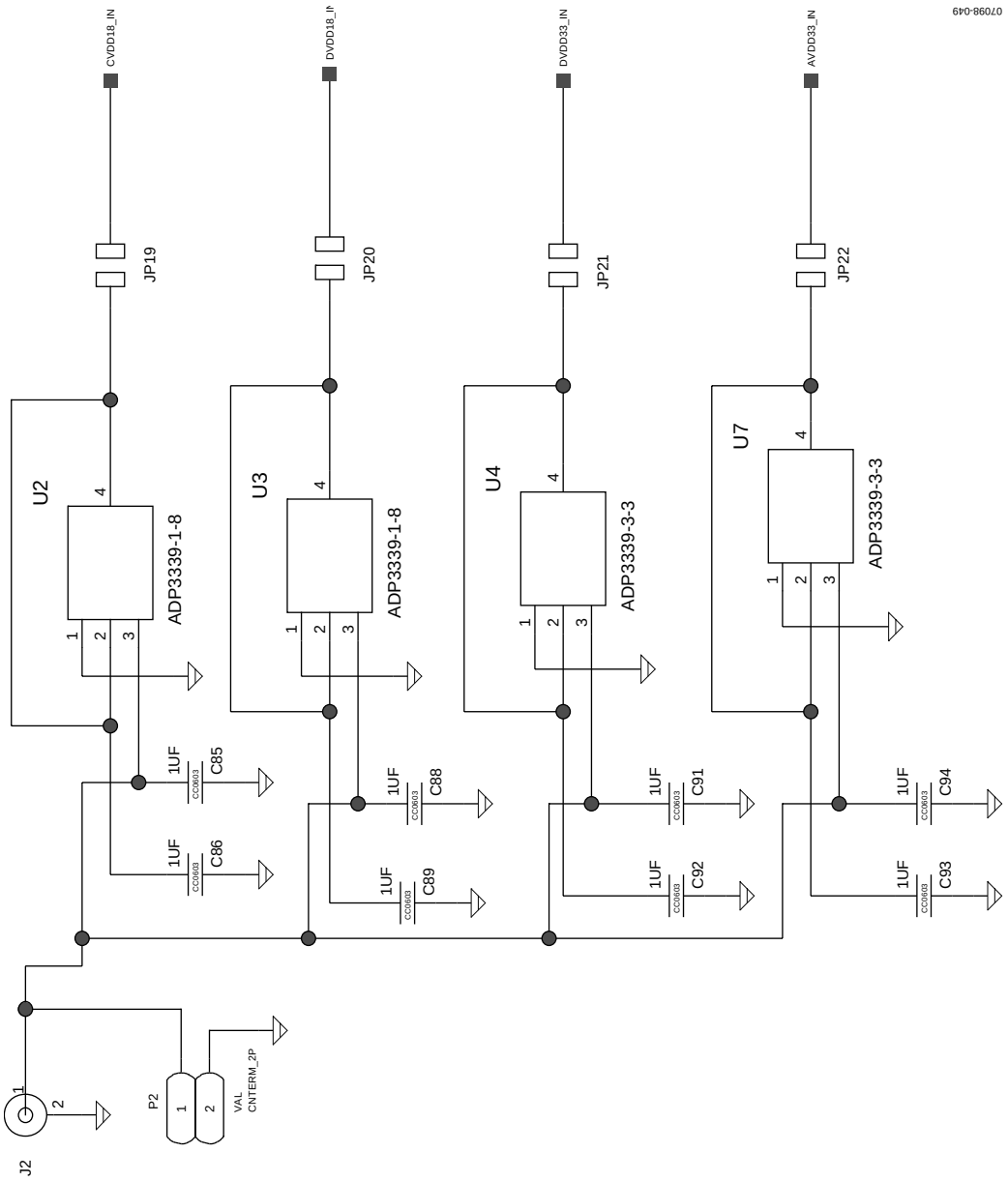
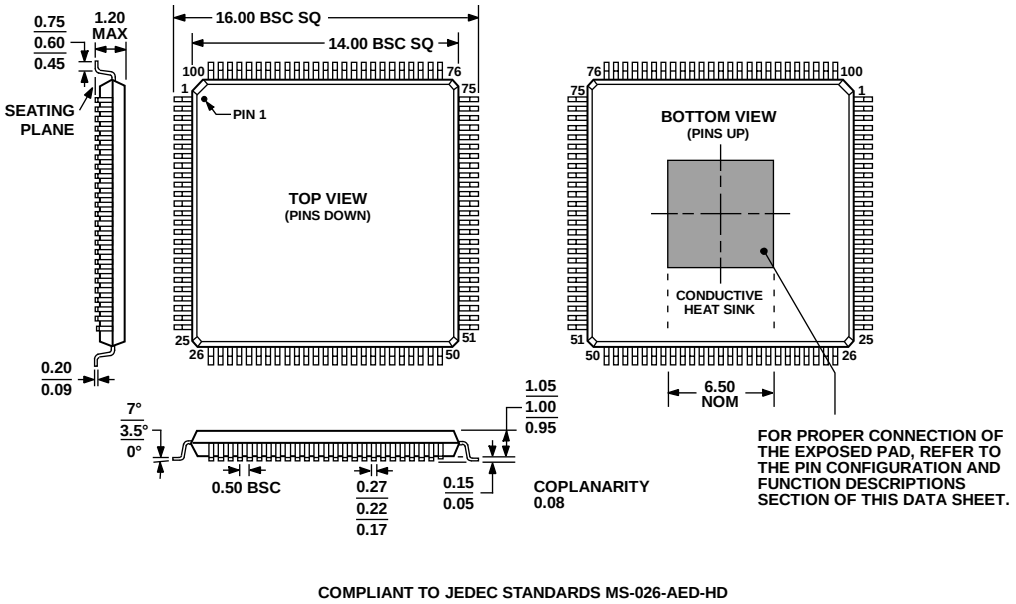


Figure 86. Evaluation Board, On-Board Power Supply

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

Figure 87. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9785BSVZ	−40°C to +85°C	100-Lead TQFP_EP	SV-100-1
AD9785BSVZRL	−40°C to +85°C	100-Lead TQFP_EP	SV-100-1
AD9787BSVZ	−40°C to +85°C	100-Lead TQFP_EP	SV-100-1
AD9787BSVZRL	−40°C to +85°C	100-Lead TQFP_EP	SV-100-1
AD9788BSVZ	−40°C to +85°C	100-Lead TQFP_EP	SV-100-1
AD9788BSVZRL	−40°C to +85°C	100-Lead TQFP_EP	SV-100-1
AD9785-DPG2-EBZ		Evaluation Board	
AD9787-DPG2-EBZ		Evaluation Board	
AD9788-DPG2-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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