

N-channel 650 V, 0.024 Ω typ., 88 A, MDmesh™ V Power MOSFET in a ISOTOP™ package

Datasheet - production data

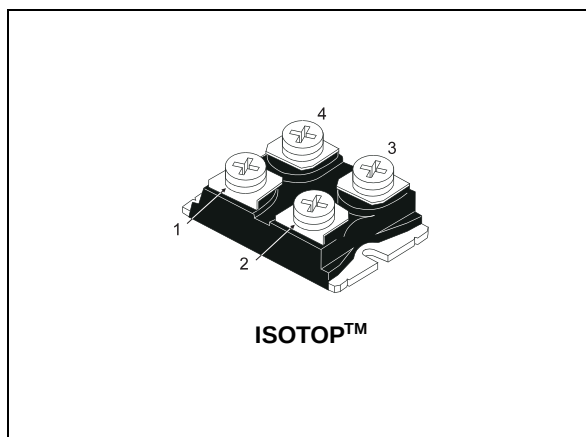
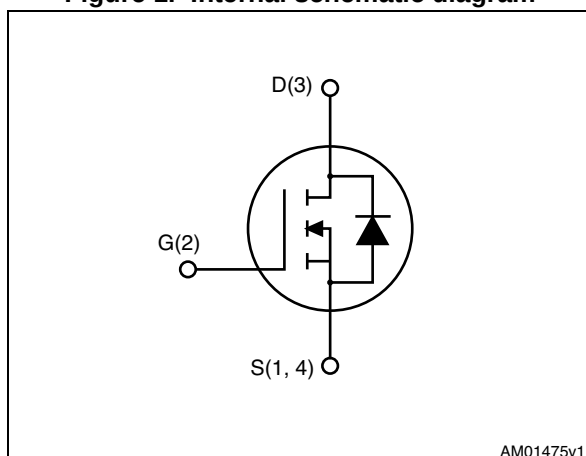


Figure 1. Internal schematic diagram



Features

Order code	$V_{DS} @ T_{jmax}$	$R_{DS(on)}$ max	I_D
STE88N65M5	710 V	0.029 Ω	88 A

- Very low $R_{DS(on)}$
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STE88N65M5	88N65M5	ISOTOP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	88	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	55.7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	352	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	494	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	15	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	2000	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 88\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DD} = 400\text{ V}$, $V_{DS(\text{peak})} < V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.253	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	30	$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$			1	μA
		$V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}$, $I_D = 42\text{ A}$		0.024	0.029	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	8825	-	pF
C_{oss}	Output capacitance		-	223	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	778	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	202	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.79	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 42\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	204	-	nC
Q_{gs}	Gate-source charge		-	51	-	nC
Q_{gd}	Gate-drain charge		-	84	-	nC

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 56\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17) (see Figure 20)	-	141	-	ns
$t_{r(v)}$	Voltage rise time		-	16	-	ns
$t_{f(i)}$	Current fall time		-	29	-	ns
$t_{c(off)}$	Crossing time		-	56	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		88	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		352	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 88\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 84\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 17)	-	544		ns
Q_{rr}	Reverse recovery charge		-	14		μC
I_{RRM}	Reverse recovery current		-	50		A
t_{rr}	Reverse recovery time	$I_{SD} = 84\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	660		ns
Q_{rr}	Reverse recovery charge		-	20		μC
I_{RRM}	Reverse recovery current		-	60		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

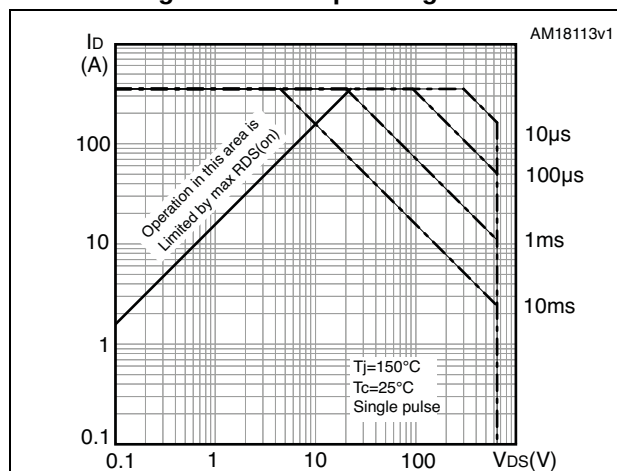


Figure 3. Thermal impedance

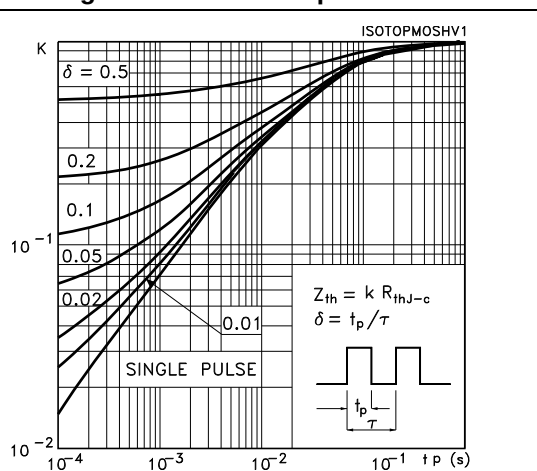


Figure 4. Output characteristics

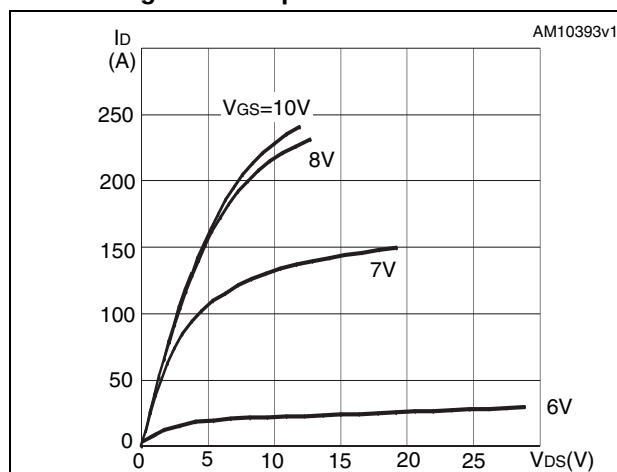


Figure 5. Transfer characteristics

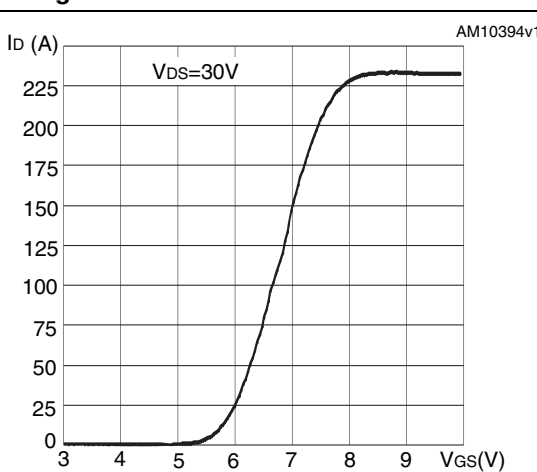
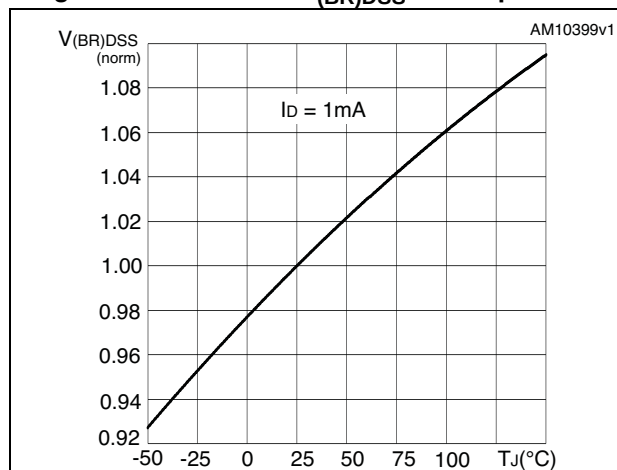
Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

Figure 7. Static drain-source on-resistance

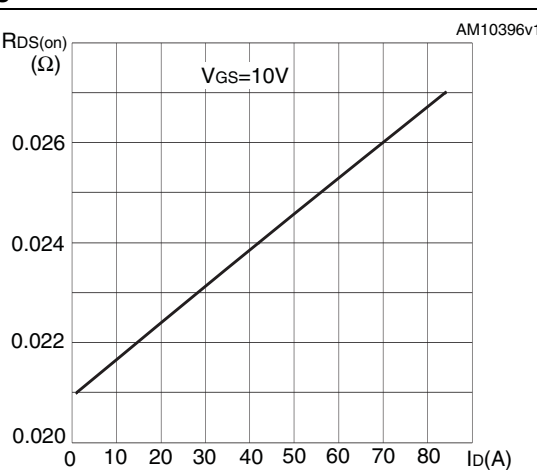


Figure 8. Gate charge vs gate-source voltage

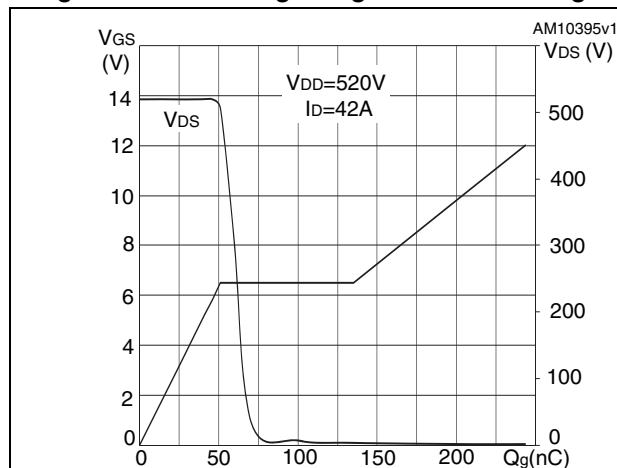


Figure 9. Capacitance variations

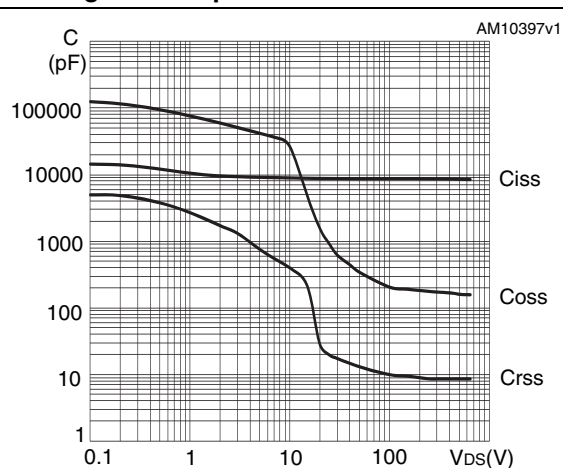


Figure 10. Normalized gate threshold voltage vs temperature

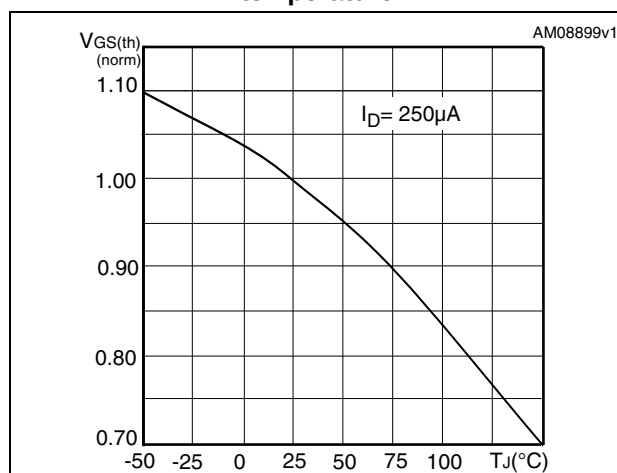


Figure 11. Normalized on-resistance vs temperature

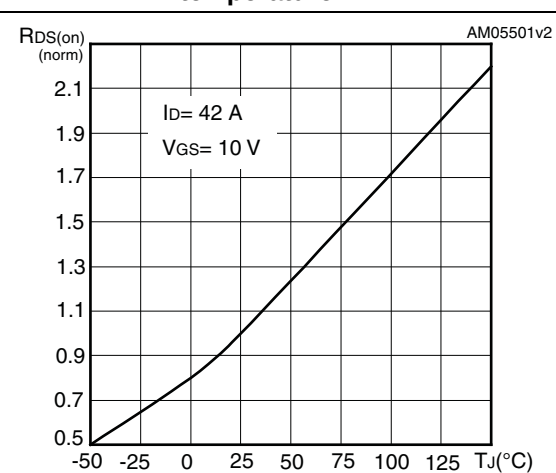


Figure 12. Source-drain diode forward characteristics

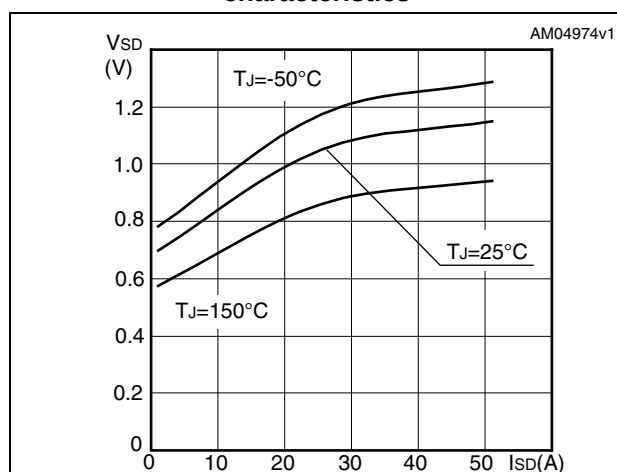


Figure 13. Output capacitance stored energy

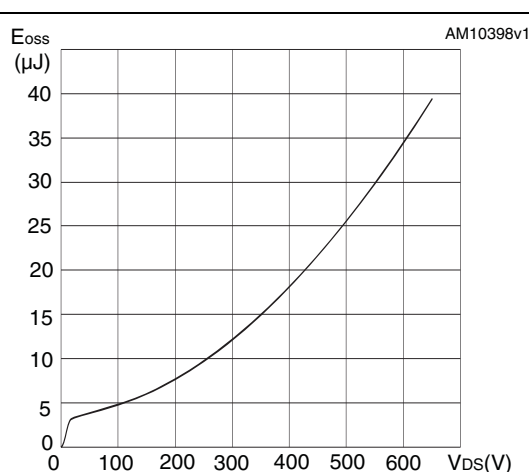
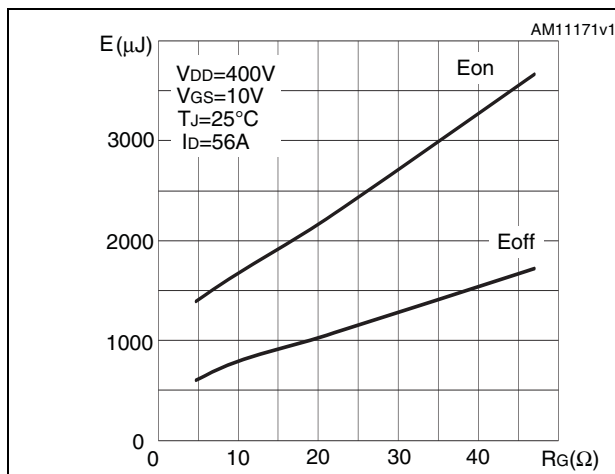


Figure 14. Switching losses vs gate resistance ⁽¹⁾



1. E_{on} including reverse recovery of a SiC diode.

4 Package mechanical data

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Figure 21. ISOTOP drawing

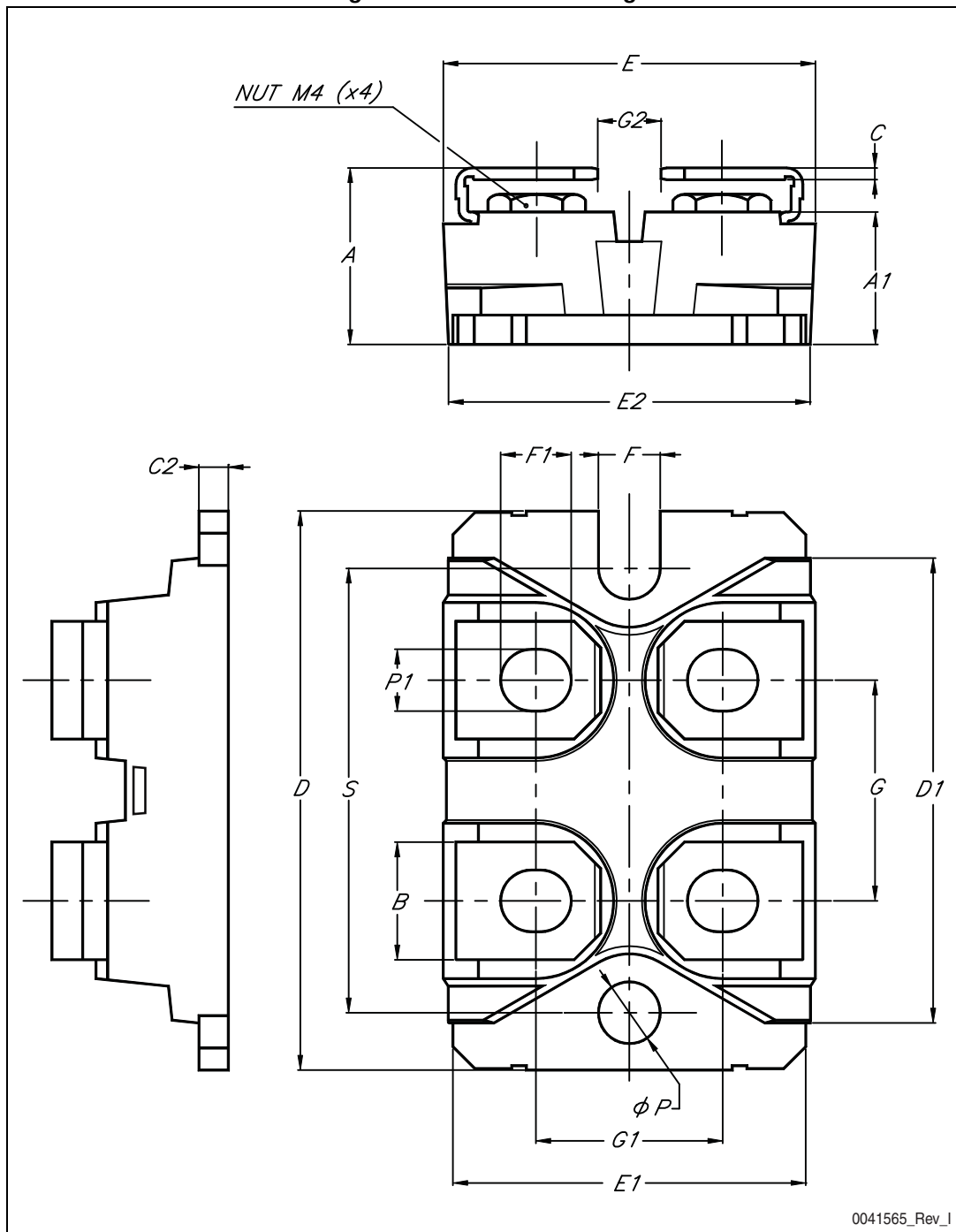


Table 8. ISOTOP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	11.80		12.20
A1	8.90		9.10
B	7.80		8.20
C	0.75		0.85
C2	1.95		2.05
D	37.80		38.20
D1	31.50		31.70
E	25.15		25.50
E1	23.85		24.15
E2		24.80	
G	14.90		15.10
G1	12.60		12.80
G2	3.50		4.30
F	4.10		4.30
F1	4.60		5
φP	4		4.30
P1	4		4.40
S	30.10		30.30

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Feb-2014	1	Initial release.

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