



The Infinite Bandwidth Company™

# MIC58P01

## 8-Bit Parallel-Input Protected Latched Driver

### Final Information

### General Description

The MIC58P01 parallel-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Similar to the MIC5801, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and overcurrent shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC58P01 has open-collector outputs capable of sinking 500 mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers may be paralleled for higher load current capability.

With a 5V logic supply, the MIC58P01 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors.

Each of these eight outputs has an independent overcurrent shutdown of 500mA. Upon current shutdown, the affected channel will turn OFF until  $V_{DD}$  is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2μs will not activate current shutdown. Temperatures above 165°C will shut down all outputs. The UVLO circuit disables the outputs at low  $V_{DD}$ ; hysteresis of 0.5V is provided.

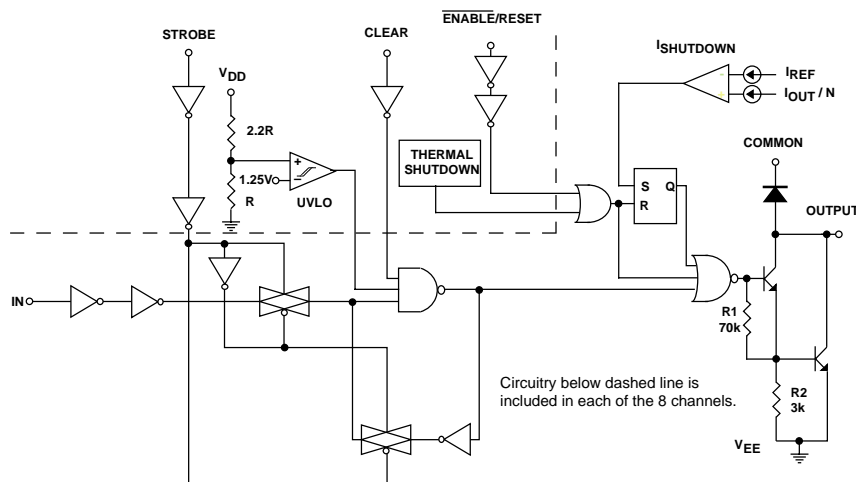
### Features

- 4.4MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Per-Output Overcurrent Shutdown (500mA typical)
- Under Voltage Lockout
- Thermal Shutdown
- Output Transient Protection Diodes
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

### Ordering Information

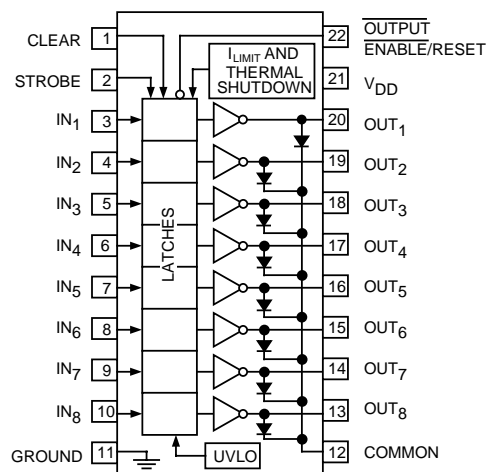
| Part Number | Temperature Range | Package            |
|-------------|-------------------|--------------------|
| MIC58P01BN  | -40°C to +85°C    | 22-Pin Plastic DIP |
| MIC58P01BV  | -40°C to +85°C    | 28-Pin PLCC        |
| MIC58P01BWM | -40°C to +85°C    | 24-Pin Wide SOIC   |

### Functional Diagram

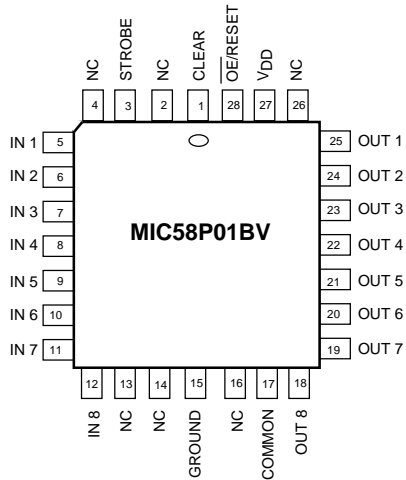


### Pin Configuration

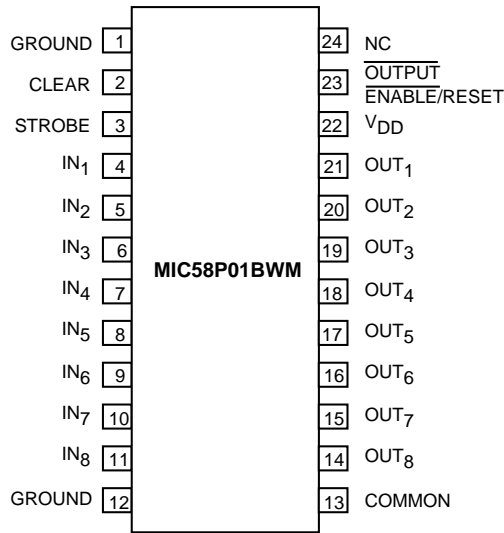
(DIP)



### Pin Configuration, Continued



**MIC58P01BV, 28-Pin PLCC**



**MIC58P01BWM, 24-Pin SOIC**  
(not pin compatible with MIC5801BWM)

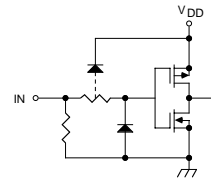
### Absolute Maximum Ratings: (Note 1)

at +25°C Free-Air Temperature

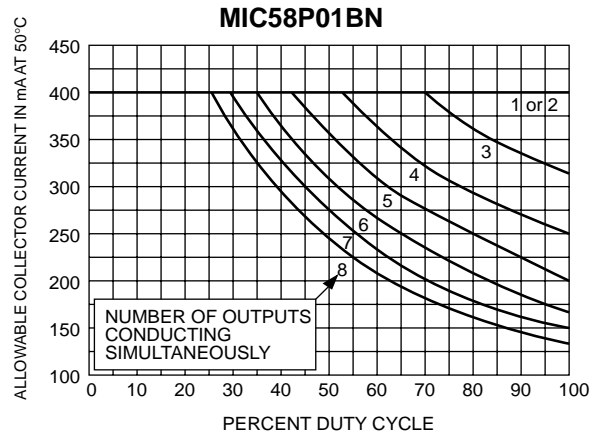
|                                    |                          |
|------------------------------------|--------------------------|
| Output Voltage, $V_{CE}$           | 80V                      |
| Supply Voltage, $V_{DD}$           | 15V                      |
| Input Voltage Range, $V_{IN}$      | -0.3V to $V_{DD} + 0.3V$ |
| Package Power Dissipation:         |                          |
| MIC58P01BN                         | 2.25W                    |
| Derate above $T_A = +25^\circ C$   | 22.5mW/°C                |
| MIC58P01BV                         | 1.6W                     |
| Derate above $T_A = +25^\circ C$   | 16mW/°C                  |
| MIC58P01BWM                        | 1.4W                     |
| Derate above $T_A = +25^\circ C$   | 14mW/°C                  |
| Operating Temperature Range, $T_A$ | -55°C to +85°C           |
| Storage Temperature Range, $T_S$   | -65°C to +125°C          |

Note 1: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

### Typical Input



### Allowable Output Current As A Function of Duty Cycle



### Pin Description

| Pin (DIP) | Name                | Description   |
|-----------|---------------------|---|
| 1         | CLEAR               | Resets all Latches and turns all outputs OFF (open).  |
| 2         | STROBE              | Input Strobe Pin. Loads output latches when High.   |
| 3-10      | INPUT               | Parallel Inputs, 1 through 8  |
| 11        | GROUND              | Logic and Output Ground pin.  |
| 12        | COMMON              | Transient suppression diode common cathode pin.   |
| 13-20     | OUTPUT              | Parallel Outputs, 8 through 1.  |
| 21        | $V_{DD}$            | Logic Supply voltage.   |
| 22        | OUTPUT ENABLE/RESET | When Low, Outputs are active. When High, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE input. |

**Electrical Characteristics (Note 3):** at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$  (unless otherwise noted)

| Characteristic                       | Symbol   | Test Conditions                                   | Limits |      |      | Units            |
|--------------------------------------|--|---|--------|------|------|------------------|
|                                      |  |   | Min.   | Typ. | Max. |                  |
| Output Leakage Current               | $I_{CEX}$  | $V_{CE} = 80\text{V}$ , $T_A = +25^\circ\text{C}$ |        |      | 50   | $\mu\text{A}$    |
|                                      |  | $V_{CE} = 80\text{V}$ , $T_A = +70^\circ\text{C}$ |        |      | 100  |                  |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$                                      | $I_C = 100\text{mA}$                              |        | 0.9  | 1.1  | V                |
|                                      |  | $I_C = 200\text{mA}$                              |        | 1.1  | 1.3  |                  |
|                                      |  | $I_C = 350\text{mA}$                              |        | 1.3  | 1.6  |                  |
| Input Voltage                        | $V_{IN(0)}$  |   |        |      | 1.0  | V                |
|                                      | $V_{IN(1)}$  | $V_{DD} = 12\text{V}$                             | 10.5   |      |      |                  |
|                                      |  | $V_{DD} = 10\text{V}$                             | 8.5    |      |      |                  |
| Input Resistance                     | $R_{IN}$   | $V_{DD} = 12\text{V}$                             | 50     | 200  |      | $\text{k}\Omega$ |
|                                      |  | $V_{DD} = 10\text{V}$                             | 50     | 300  |      |                  |
|                                      |  | $V_{DD} = 5.0\text{V}$                            | 50     | 600  |      |                  |
| Supply Current                       | $I_{DD(ON)}$<br>(One output active)                | $V_{DD} = 12\text{V}$ , Outputs Open              |        | 3.3  | 4.5  | mA               |
|                                      |  | $V_{DD} = 10\text{V}$ , Outputs Open              |        | 3.1  | 4.5  |                  |
|                                      |  | $V_{DD} = 5.0\text{V}$ , Outputs Open             |        | 2.4  | 3.6  |                  |
|                                      | $I_{DD(ON)}$<br>(All outputs active)               | $V_{DD} = 12\text{V}$ , Outputs Open              |        | 6.4  | 10.0 | mA               |
|                                      |  | $V_{DD} = 10\text{V}$ , Outputs Open              |        | 6.0  | 9.0  |                  |
|                                      |  | $V_{DD} = 5.0\text{V}$ , Outputs Open             |        | 4.7  | 7.5  |                  |
| $I_{DD(OFF)}$<br>(Total)             | $V_{DD} = 12\text{V}$ , Outputs Open, Inputs = 0V  |   | 3.0    | 4.5  | mA   |                  |
|                                      | $V_{DD} = 5.0\text{V}$ , Outputs Open, Inputs = 0V |   | 2.2    | 3.6  |      |                  |
| Clamp Diode Leakage Current          | $I_R$  | $V_R = 80\text{V}$ , $T_A = +25^\circ\text{C}$    |        |      | 50   | $\mu\text{A}$    |
|                                      |  | $V_R = 80\text{V}$ , $T_A = +70^\circ\text{C}$    |        |      | 100  |                  |
| Overcurrent Threshold                | $I_{LIM}$  | Per Output  |        | 500  |      | mA               |
| Start-Up Voltage                     | $V_{SU}$   | Note 2.   | 3.5    | 4.0  | 4.5  | V                |
| Minimum Operating $V_{DD}$           | $V_{DD\text{ MIN}}$                                |   | 3.0    | 3.5  | 4.0  | V                |
| Clamp Diode Forward Voltage          | $V_F$  | $I_F = 350\text{mA}$                              |        | 1.7  | 2.0  | V                |
| Thermal Shutdown                     |  |   |        | 165  |      | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis          |  |   |        | 10   |      | $^\circ\text{C}$ |

**NOTE 1:** Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

**NOTE 2:** Under-Voltage Lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.

**NOTE 3:** Specification for packaged product only.

**Truth Table**

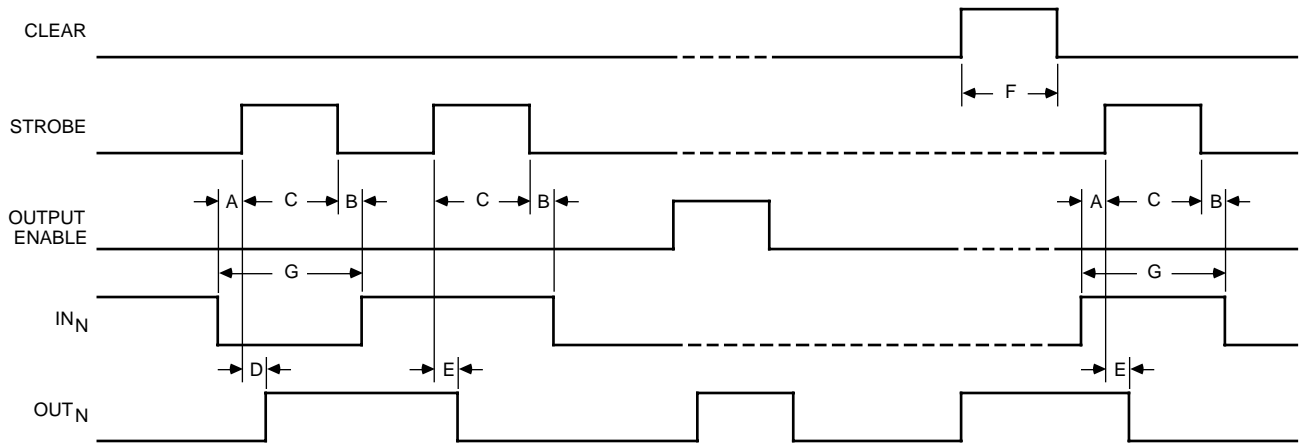
| $IN_N$ | Strobe | Clear | $\overline{\text{Output Enable}}$ | $OUT_N$ |     |
|--------|--------|-------|-----------------------------------|---------|-----|
|        |        |       |                                   | t-1     | t   |
| 0      | 1      | 0     | 0                                 | X       | OFF |
| 1      | 1      | 0     | 0                                 | X       | ON  |
| X      | X      | 1     | X                                 | X       | OFF |
| X      | X      | X     | 1                                 | X       | OFF |
| X      | 0      | 0     | 0                                 | ON      | ON  |
| X      | 0      | 0     | 0                                 | OFF     | OFF |

X = Irrelevant

t-1 = previous output state

t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the Data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current shutdown is activated, the OUTPUT ENABLE must be pulsed high to restore operation. Over temperature faults are not latched and require no reset pulse.

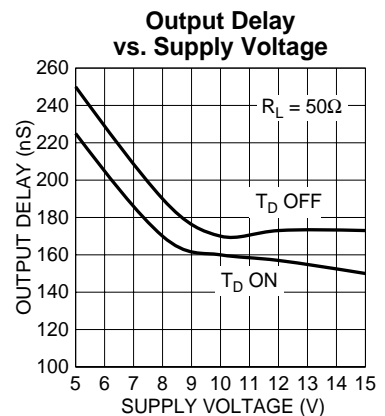
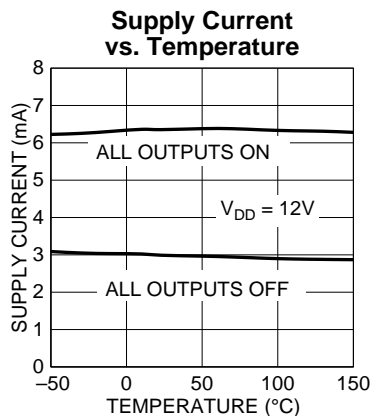
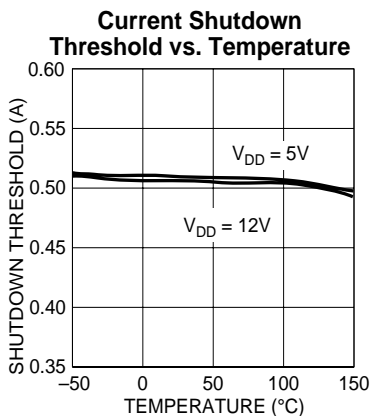
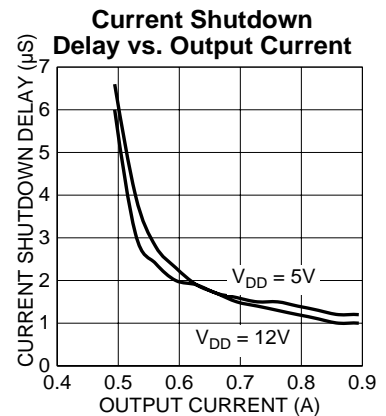
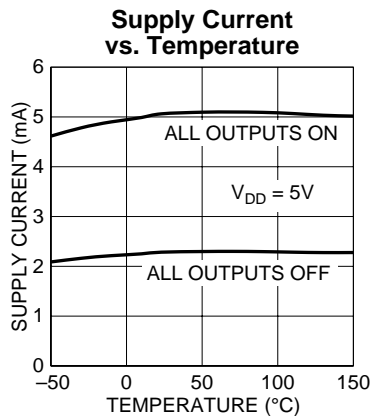
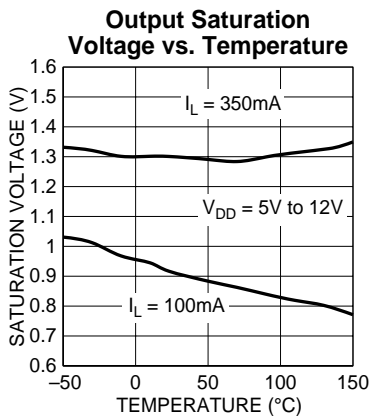


### Timing Conditions

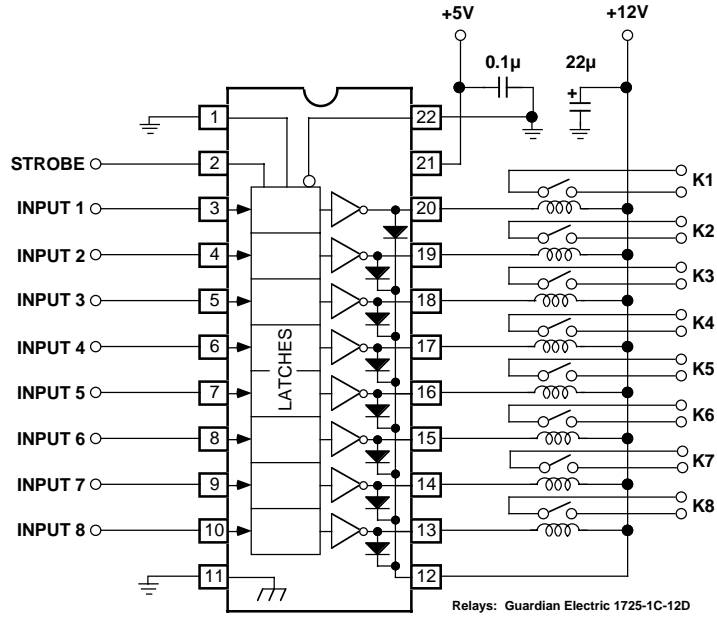
( $T_A = +25^\circ\text{C}$ , Logic Levels are  $V_{DD}$  and Ground,  $V_{DD} = 5\text{V}$ )

- A. Minimum data active time before strobe enabled (data set-up time) ..... 50ns
- B. Minimum data active time after strobe disabled (data hold time) ..... 50ns
- C. Minimum strobe pulse width ..... 125 ns
- D. Typical time between strobe activation and output on to off transition ..... 500ns
- E. Typical time between strobe activation and output off to on transition ..... 500ns
- F. Minimum clear pulse width ..... 300ns
- G. Minimum data pulse width ..... 225 ns

### Typical Characteristic Curves

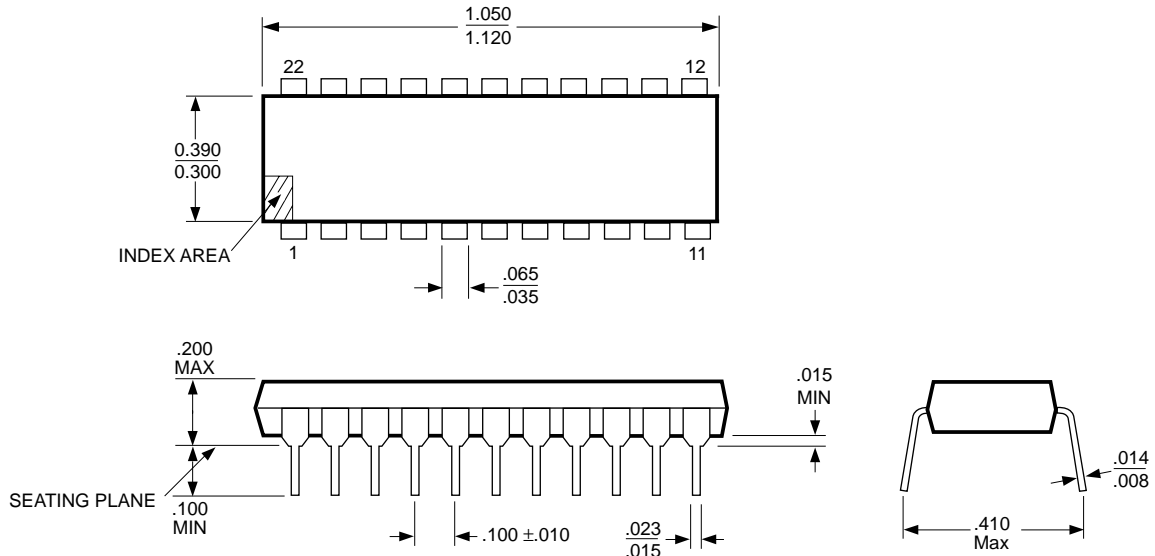


# Typical Application

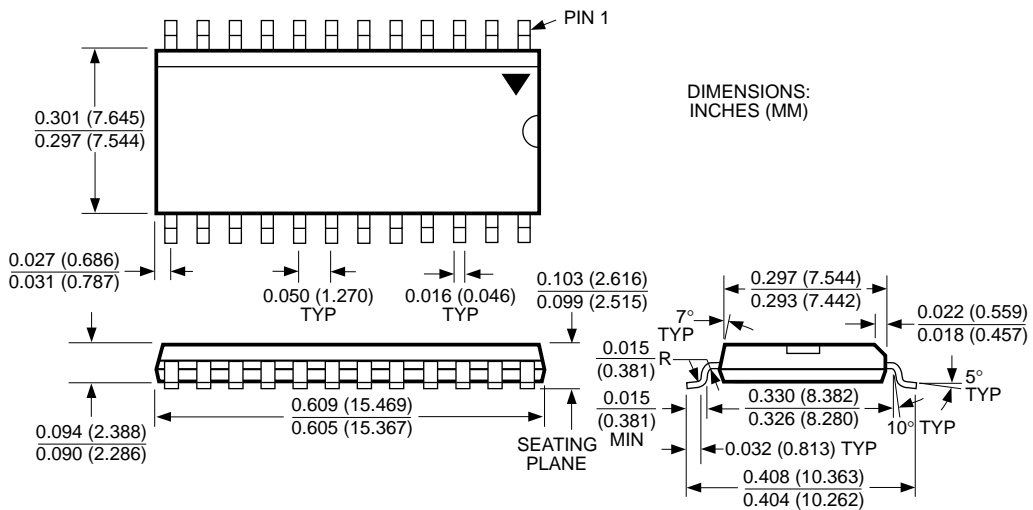


MIC58P01 Protected Relay Driver

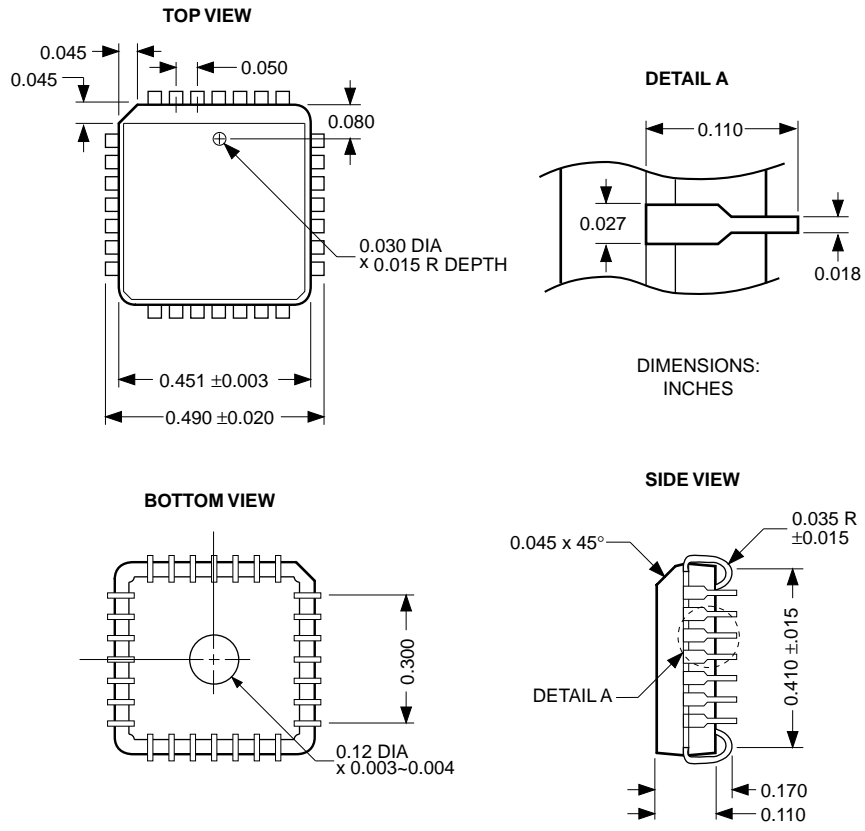
Package Information



22-Pin Plastic DIP (N)



24-Pin Wide SOP (WM)



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