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January 2016

FDMD8240LET40

Dual N-Channel Power Trench® MOSFET

40 V, 103 A, 2.6 mΩ

Features

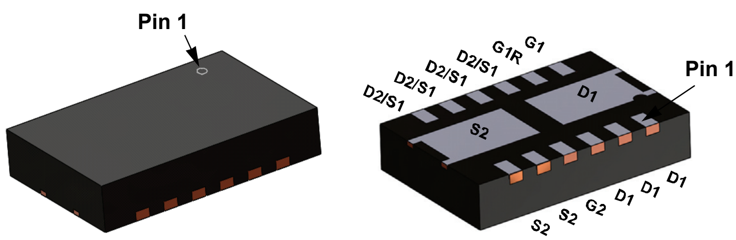
- Extended T_J Rating to 175 °C
- Max $r_{DS(on)}$ = 2.6 mΩ at V_{GS} = 10 V, I_D = 23 A
- Max $r_{DS(on)}$ = 3.95 mΩ at V_{GS} = 4.5 V, I_D = 19 A
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- Termination is Lead-free and RoHS Compliant

General Description

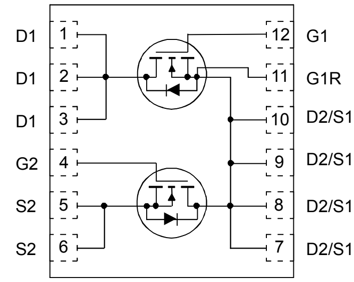
This device includes two 40V N-Channel MOSFETs in a dual Power (3.3 mm X 5 mm) package. HS source and LS Drain are internally connected for half/full bridge, low source inductance package, low $r_{DS(on)}$/Qg FOM silicon.

Applications

- Synchronous Buck : Primary Switch of Half / Full Bridge Converter for Telecom
- Motor Bridge : Primary Switch of Half / Full bridge Converter for BLDC Motor
- MV POL : Synchronous Buck Switch



Power 3.3 x 5



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter				Ratings	Units
V_{DS}	Drain to Source Voltage				40	V
V_{GS}	Gate to Source Voltage				±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		(Note 5)	103	A
	-Continuous	T_C = 100 °C		(Note 5)	73	
	-Continuous	T_A = 25 °C		(Note 1a)	24	
	-Pulsed			(Note 4)	489	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	216	mJ
P_D	Power Dissipation	T_C = 25 °C			50	W
	Power Dissipation	T_A = 25 °C		(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8240LT	FDMD8240LET40	Power 3.3 x 5	13 ”	12 mm	3000 units

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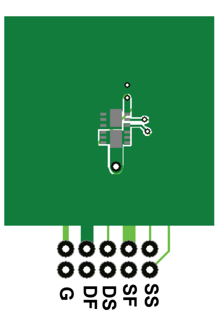
Electrical Characteristics T_J = 25 °C unless otherwise noted.

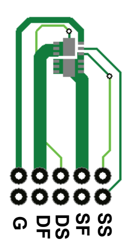
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 23 A		2.0	2.6	mΩ
		V_{GS} = 4.5 V, I_D = 19 A		3.2	3.95	
		V_{GS} = 10 V, I_D = 23 A, T_J = 150 °C		3.3	4.3	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 23 A		107		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V f = 1 MHz		3020	4230	pF
C_{oss}	Output Capacitance			876	1230	pF
C_{rss}	Reverse Transfer Capacitance			33	52	pF
R_g	Gate Resistance		0.1	2.8	6	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20 V, I_D = 23 A V_{GS} = 10 V, R_{GEN} = 6 Ω		12	22	ns
t_r	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			36	58	ns
t_f	Fall Time			9	18	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 20 V, I_D = 23 A		40	56	nC
	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 20 V, I_D = 23 A		21	30	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V, I_D = 23 A		9		nC
Q_{gd}	Gate to Drain "Miller" Charge	V_{DD} = 20 V, I_D = 23 A		5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 23 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 1.6 A (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 23 A, di/dt = 100 A/μs		41	65	ns
Q_{rr}	Reverse Recovery Charge			21	32	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 130 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 216 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 12 A, V_{DD} = 40 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 37 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted.

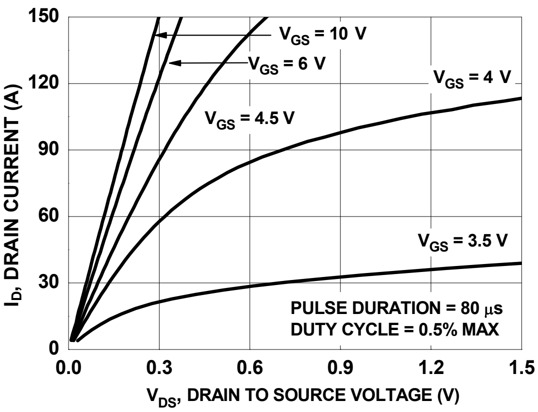


Figure 1. On-Region Characteristics

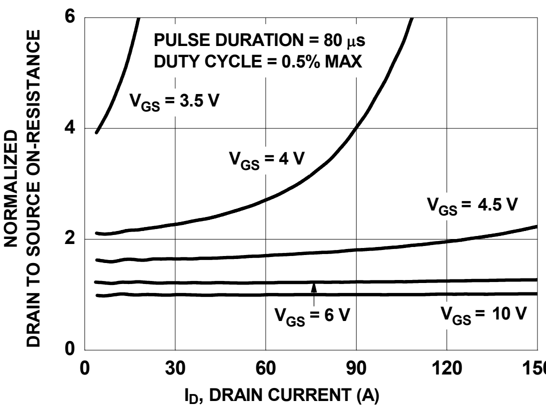


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

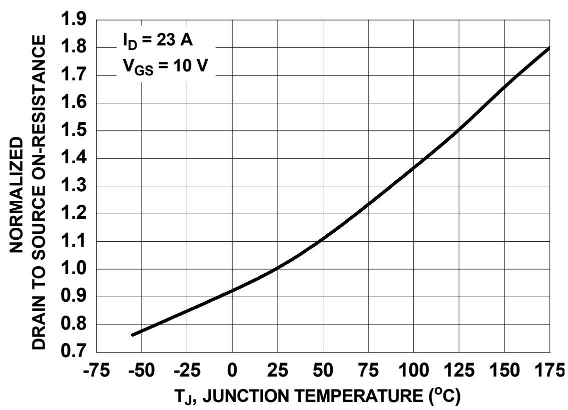


Figure 3. Normalized On Resistance vs. Junction Temperature

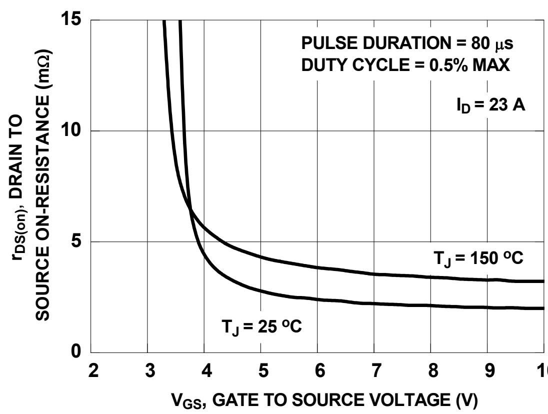


Figure 4. On Resistance vs. Gate to Source Voltage

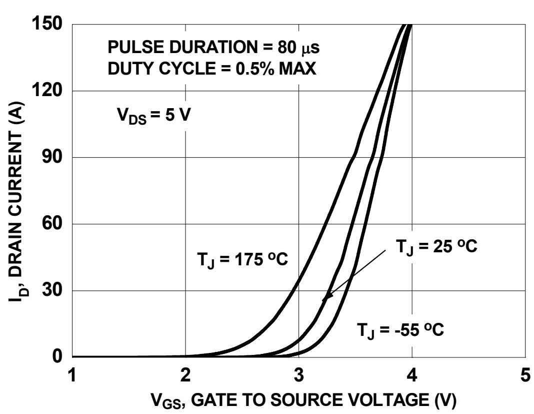


Figure 5. Transfer Characteristics

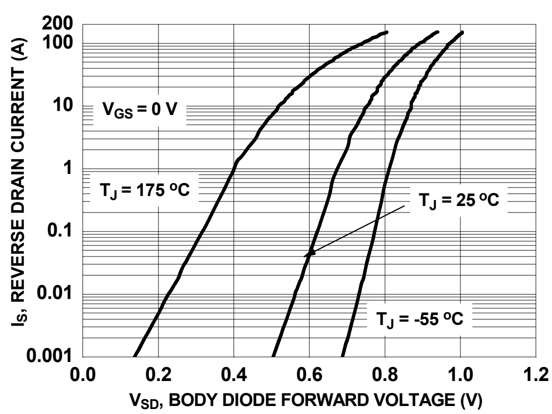


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted.

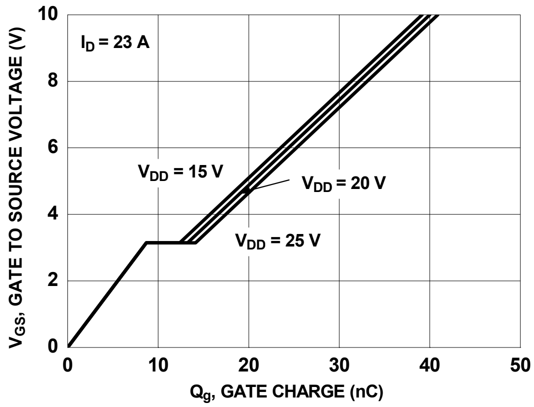


Figure 7. Gate Charge Characteristics

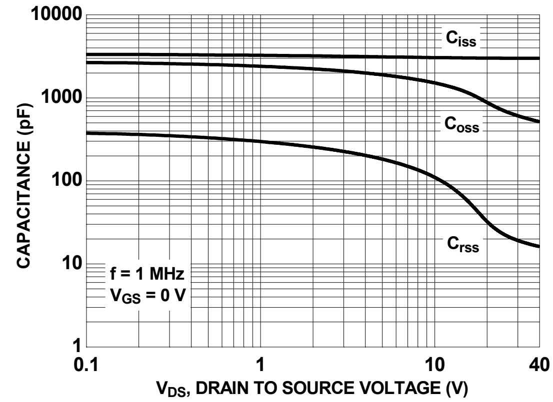


Figure 8. Capacitance vs. Drain to Source Voltage

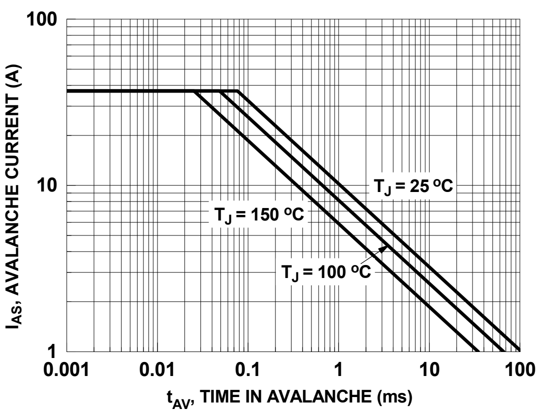


Figure 9. Unclamped Inductive Switching Capability

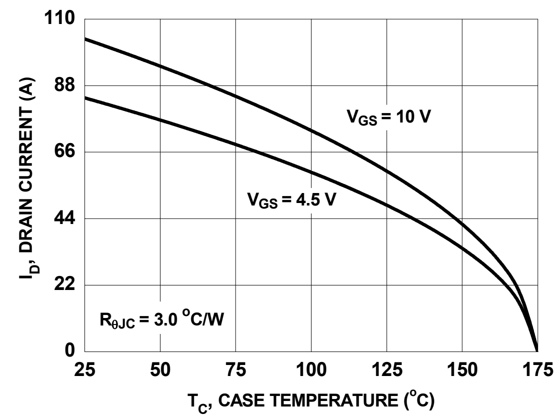


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

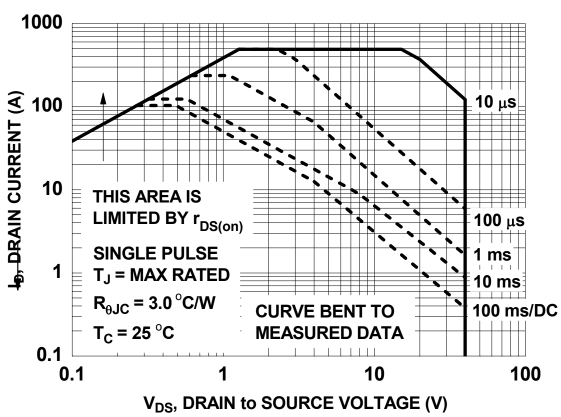


Figure 11. Forward Bias Safe Operating Area

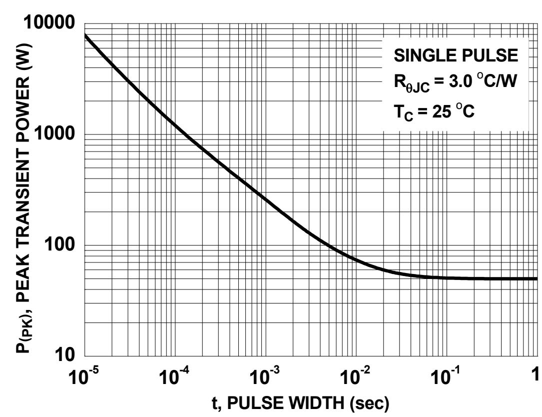


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted.

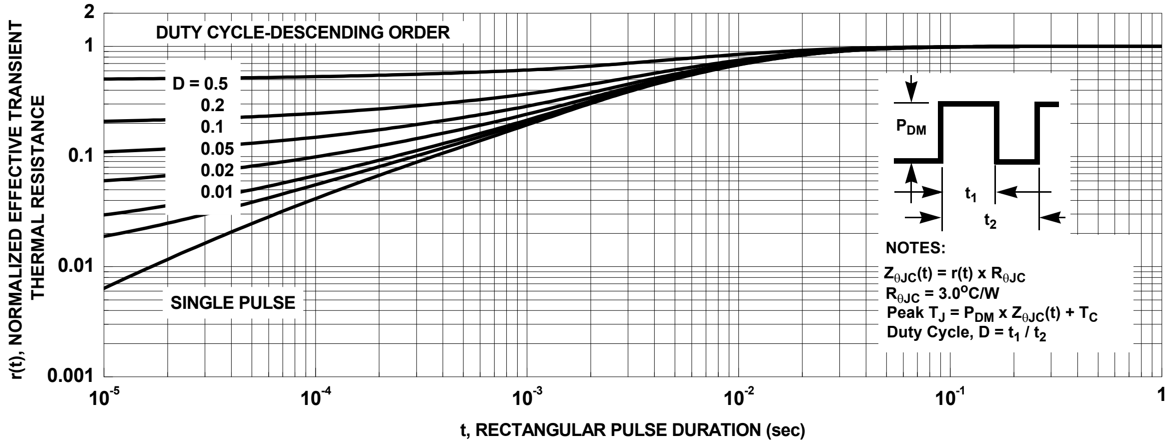
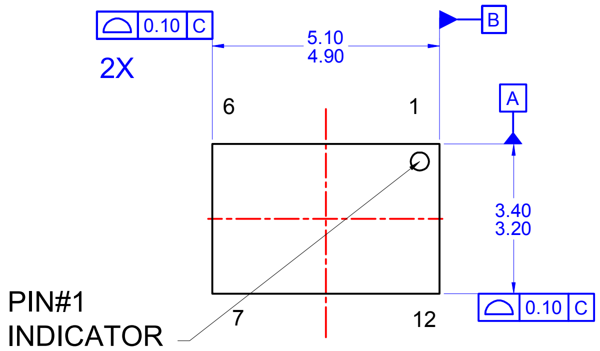
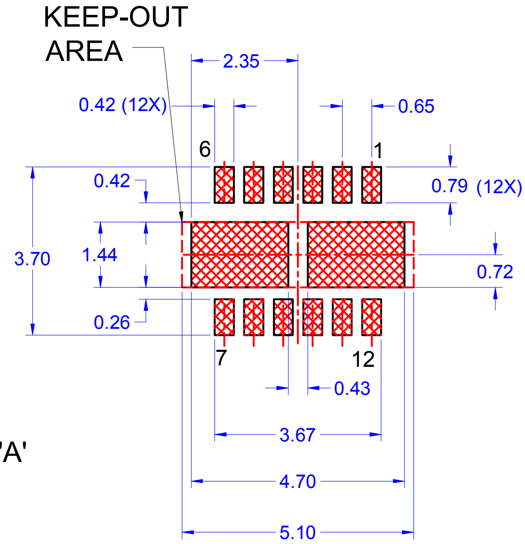


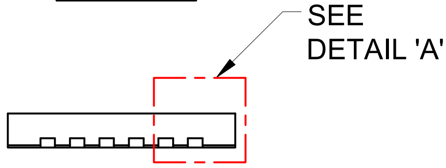
Figure 13. Junction-to-Case Transient Thermal Response Curve



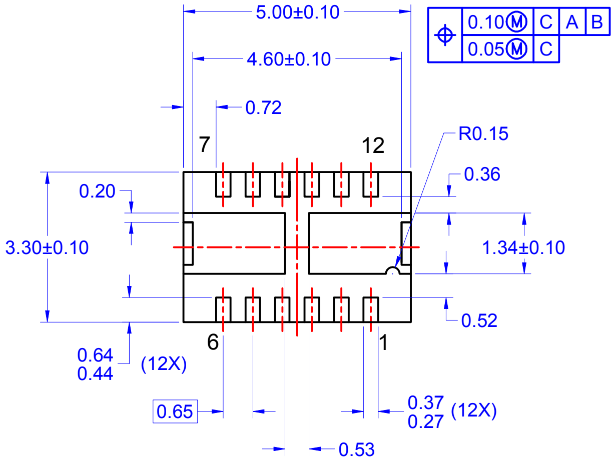
TOP VIEW



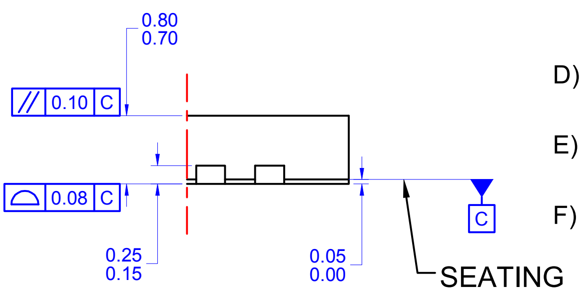
LAND PATTERN
RECOMMENDATION



FRONT VIEW



BOTTOM VIEW



DETAIL 'A'

SCALE: 2:1

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