PCA9527

3-channel bidirectional bus extender for HDMI, I²C-bus and SMBus

Rev. 01 — 29 June 2009 Product data sheet

1. General description

The PCA9527 is a 3-channel bidirectional open-drain bus buffer for Display Data Control (DDC) clock, data and Consumer Electronic Control (CEC) for HDMI application. The device has two power supply pins to allow voltage level shift from 2.7 V to 5 V, and a rise time accelerator on port A of each DDC clock and data for driving longer cable (up to 18 meters or 1400 pF reliably without violating the bus rise time). The 5 V tolerant CEC channel is internally connected to $V_{CC(B)}$ and has no rise time accelerator. The CEC channel can be used as an interrupt or reset.

While retaining all the operating modes and features of the I²C-bus system during the level shift, it also permits extension of the I²C-bus by providing bidirectional buffering for data (SDA), clock (SCL), and CEC. Using the PCA9527 enables the system designer to isolate bus capacitance to meet HDMI DDC version 1.3 distance specification. The SDAx and SCLx pins are overvoltage tolerant and are high-impedance when the PCA9527 is unpowered. The port B drivers (SDAB, SCLB, CECB) with static level offset behave much like the drivers on the PCA9515 device, while the SDAA and SCLA drivers integrate the rise time accelerator, sink more current and eliminate the static offset voltage. The CECA driver has the same current and static offset voltage features as the SDAA and SCLA, but it does not have the rise time accelerator and is powered and referenced to $V_{CC(B)}$. This results in a LOW on the port B translating into a nearly 0 V LOW on port A, providing zero offset. The static level offset design of the port B I/O drivers prevent them from being connected to another device that has rise time accelerator including the PCA9507 (port B), PCA9510, PCA9511, PCA9512, PCA9513, PCA9514, PCA9515, PCA9516A, PCA9517 (port B), or PCA9518A. Port A of two or more PCA9527s can be connected together, however, to allow a star topography with port A on the common bus, and port A can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PCA9527s can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider. Rise time accelerators on the SDAA and SCLA pins are turned on when input threshold is above $0.3V_{CC(A)}$. The PCA9527 SDA and SCL drivers are not enabled unless $V_{CC(A)}$ and $V_{CC(B)}$ are above 2.7 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle. The output pull-down on the port B internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring.

2. Features

- 3-channel, bidirectional buffer isolates capacitance allowing 1400 pF on port A and 400 pF on port B
- Exceeds 18 meters (above the maximum distance for HDMI DDC)
- Rise time accelerator and normal I/O on port A (no accelerator for CEC)
- Static level offset on port B
- Voltage level translation from 2.7 V to 5.5 V
- CEC is 5 V tolerant, powered by $V_{CC(B)}$
- Upgrade replacement over PCA9507 and PCA9517A for cable application
- I²C-bus, SMBus and DDC-bus compatible
- Active HIGH buffer enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins
- Port A operating supply voltage range of 2.7 V to 5.5 V
- Port B operating supply voltage range of 2.7 V to 3.6 V
- 5 V tolerant I²C-bus and enable pins
- 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater)
- ESD protection exceeds 8000 V HBM per JESD22-A114, 500 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offered: TSSOP10

3. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9527DP	9527	TSSOP10[1]	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1

[1] Also known as MSOP10.

4. Functional diagram

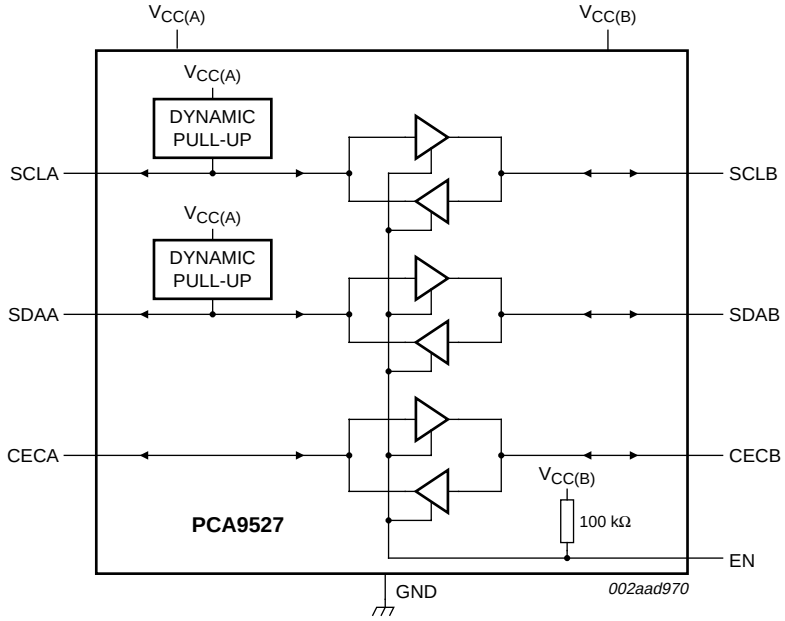


Fig 1. Functional diagram of PCA9527

5. Pinning information

5.1 Pinning

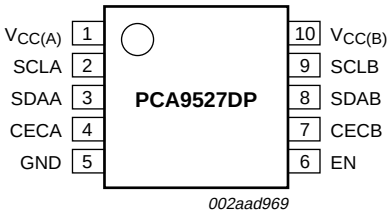


Fig 2. Pin configuration for TSSOP10

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	port A supply voltage (2.7 V to 5.5 V)
SCLA	2	serial clock port A bus with rise time accelerator for DDC line or cable, 5 V tolerant
SDAA	3	serial data port A bus with rise time accelerator for DDC line or cable, 5 V tolerant
CECA	4	serial data with normal I/O powered by $V_{CC(B)}$, 5 V tolerant

Table 2. Pin description *...continued*

Symbol	Pin	Description
GND	5	supply ground (0 V)
EN	6	active HIGH buffer enable input
CECB	7	serial data with static level offset, powered by $V_{CC(B)}$, 5 V tolerant
SDAB	8	serial data port B bus with static level offset, 5 V tolerant
SCLB	9	serial clock port B bus with static level offset, 5 V tolerant
$V_{CC(B)}$	10	port B supply voltage (2.7 V to 3.6 V)

6. Functional description

Refer to Figure 1 “Functional diagram of PCA9527”.

The PCA9527 consists of 3 channels of bidirectional open-drain I/Os specifically designed to support up-translation/down-translation between low voltages (as low as 2.7 V) and a 3.3 V or 5 V I²C-bus and SMBus. The device contains a rise time accelerator, specifically on port A of the SCLA and SDAA that enables the device to drive a long cable or a heavier capacitive load for DDC, I²C-bus and SMBus applications. With dual supply rails, the device translates from voltage ranges 2.7 V to 5.5 V down to a voltage as low as 2.7 V without degradation of system performance. Unlike the SDAA and SCLA, the CECA is powered by the $V_{CC(B)}$ and does not have a rise time accelerator, but is similar in that its port A has normal I/O and port B static level offset. All I/Os are overvoltage tolerant to 5.5 V even when the device is un-powered ($V_{CC(B)}$ and/or $V_{CC(A)}$ = 0 V).

The PCA9527 includes a power-up circuit that keeps the SDA and SCL output drivers turned off until $V_{CC(A)}$ and $V_{CC(B)}$ rise above 2.7 V. The CECA output drivers are turned OFF until $V_{CC(B)}$ rises above 2.7 V. $V_{CC(A)}$ and $V_{CC(B)}$ can be applied in any sequence at power-up.

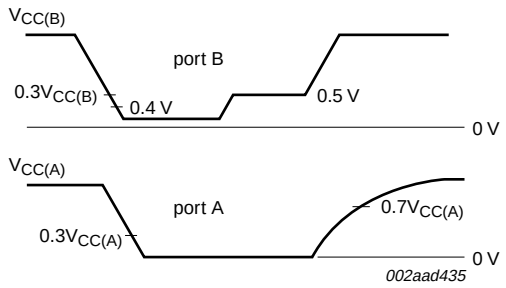


Fig 3. Port A and port B I/O levels

When port B falls first and goes below $0.3V_{CC(B)}$ the port A driver is turned on and port A pulls down to 0 V. As port A falls below $0.3V_{CC(A)}$ the port B pulls down to about 0.5 V. The external port B driver must drive the port B to a LOW that is ≤ 0.4 V or else it is not possible to know who is driving the port A LOW. The PCA9527 direction control assumes that port A is controlling the part unless port B falls below 0.4 V. When the port B voltage is ≤ 0.4 V the port A driver of the PCA9527 is on and holds port A down to nearly 0 V. As the port B voltage rises because the external driver turns off, the port B voltage rises up to ~0.5 V because port A is LOW; once port B rises to ~0.5 V the port A pull-down driver turns off. Then port A rises with a rise time determined by the RC of port A when it

crosses the port A threshold ~0.3$V_{CC(A)}$ the port B driver is turned off and the rising edge accelerator is turned on, which causes a faster rising edge until it reaches the turn-off point for the rising edge accelerator ~0.7$V_{CC(A)}$. Then it continues to rise at the slower rate determined by the RC of port A. When the port B driver turns off, port B rises with the RC of port B.

$V_{CC(A)}$ powers the 0.3$V_{CC(A)}$ reference for SCLA and SDAA as well as the port A power good detect circuit. $V_{CC(B)}$ powers the rest of the chip including the port B I/Os, the CEC I/Os, and the support functions. Figure 3 illustrates the threshold and I/O levels for port A and port B.

6.1 Enable

The EN pin is active HIGH with an internal ~100 kΩ pull-up to $V_{CC(B)}$ and allows the user to select when the buffer is active. The enable pin puts the PCA9527 in a power-down state when it is disabled, so that there is a recovery delay and a lower power-down power. This can be used to isolate the line when the HDMI DDC transmitter or receiver is not ready, or from a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled. The enable pin should only change state when the global bus and the buffer port are in an idle state to prevent system failures.

6.2 Rise time accelerators

PCA9527 has rise time accelerators on port A of SCL and SDA only; the CECA pin does not have a rise time accelerator. During port A positive bus transitions a current source is switched on to quickly slew the SDAA and SCLA lines HIGH once the input level of 0.3$V_{CC(A)}$ is exceeded for the PCA9527 and turns off as the 0.7$V_{CC(A)}$ voltage is approached.

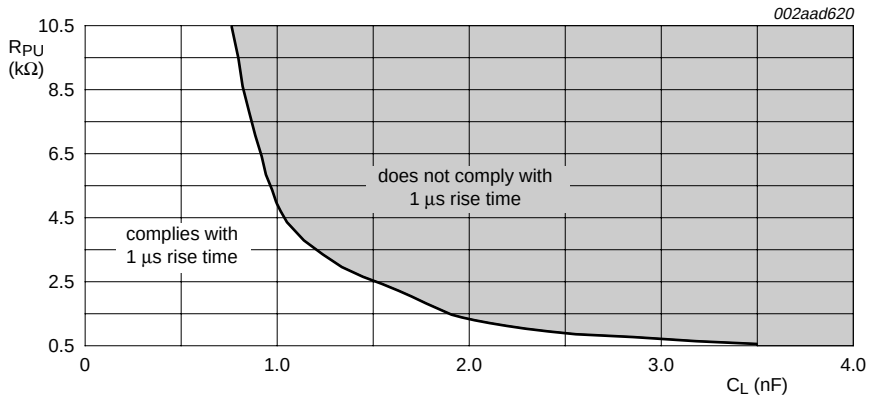
6.3 Resistor pull-up value selection

6.3.1 Port A (SDAA and SCLA)

SDAA and SCLA are open-drain I/O that have rise time accelerators and strong pull-down. When the inputs transition above 0.3$V_{CC(A)}$, the rise time accelerator activates and boosts the pull-up current during rising edge to meet the I²C-bus rise time specification when the device drives a long cable or heavier capacitance load. The strong pull-down enables the output to drive to nearly zero voltage for logic LOW. The selection for pull-up resistors are defined in the HDMI DDC specification shown in Table 3. For HDMI transmitter applications like digital video player, recorder, or set-top box, the pull-up resistor is in the range of 1.5 kΩ to 2 kΩ. For HDMI receiver applications like in LCD TV or video card, the pull-up resistor is 47 kΩ on the SCLA line, and there is no pull-up on the SDAA line. Please refer to Table 3, Figure 6 and Figure 7 for more details. Figure 4 shows the port A pull-up resistor values (in kΩ) versus capacitance load (in nF) for 5 V supply voltage complied with 1 µs rise time per I²C-bus Standard-mode specification. The graph contrasts a shaded and unshaded region. Any resistor value chosen within the unshaded region would comply with 1 µs rise time, while any value chosen in the shaded region would not.

Table 3. HDMI DDC pull-up resistors specification

Pin	Where	Minimum	Maximum
SDAA	at the source (DVD/STB)	1.5 kΩ	2.0 kΩ
	at the sink (LCD TV)	-	-
SCLA	at the source (DVD/STB)	1.5 kΩ	2.0 kΩ
	at the sink (LCD TV)	47 kΩ ± 10 %	



rise time = 1 µs; $V_{CC(A)}$ = 5 V

Fig 4. SDAA/SCLA line pull-up resistor versus load capacitance

6.3.2 Port A (CECA)

CECA does not have a rise time accelerator, but has a standard open-drain I/O. In addition to incurring no offset voltage, it has edge rate control and a lower capacitance than those of standard discrete MOSFET, and isolates the input/output capacitance. It is designed for a lower speed channel for consumer electronic control (less than 10 kHz) or general purpose interrupt or reset over long cable.

CECA does not have internal pull-up. The pull-up resistor is calculated using standard I²C-bus pull-up resistor formula, as shown in Section 6.3.3 “Port B (SDAB, SCLB, CECB)”.

6.3.3 Port B (SDAB, SCLB, CECB)

SDAB and SCLB are standard I²C-bus with static level offset that has no rise time accelerator. The static level offset produces an output LOW of 0.5 V (typical) at 6 mA. As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels. The size of these pull-up resistors depends on the system requirement, and should meet the current sinking capability of the device that drives the buffer, as well as that of the buffer. The minimum and maximum pull-up resistors are determined and the pull-up resistor's value is chosen to be within the minimum and maximum range.

Using Equation 1, calculate the minimum pull-up resistor value:

$$R_{PU(min)} = \frac{V_{pu(max)} - 0.4\ V}{I_{OL(max)}} \quad (1)$$

Where:

$R_{PU(min)}$ is the minimum pull-up resistor value for the open-drain SCLB and SDAB.

$V_{pu(max)}$ is the maximum supply rail of the pull-up resistor and should not exceed 5.5 V.

0.4 V is the maximum V_{OL} of the device that drives the buffer on logic LOW.

$I_{OL(max)}$ at V_{OL} = 0.4 V is the maximum sink current of the device that drives the buffer on logic LOW.

The maximum pull-up resistor should also be sized such that the RC time constant meets the standard I²C-bus rise time, which is 1 µs for Standard-mode (100 kHz) or 300 ns for Fast-mode (400 kHz). DDC bus complies with the I²C-bus Standard-mode and operates below 100 kHz, and maximum rise time is 1 µs using a simplified RC equation.

Using Equation 2, calculate the maximum pull-up resistor value:

$$R_{PU(max)} \times C_{L(max)} = 1.2 \times t_r \quad (2)$$

Where:

$R_{PU(max)}$ is the maximum allowable pull-up resistor on the SCLB and SDAB in order to meet the I²C-bus rise time specification.

$C_{L(max)}$ is the maximum allowable capacitance load (include the capacitance of driver, the line, and the buffer) in order to meet the rise time specification.

t_r is the rise time specified as 1 µs (for bus speed 100 kHz or lower) and 300 ns (for bus speed 400 kHz or lower).

The chosen pull-up resistor R_{PU} is: $R_{PU(min)} \leq R_{PU} \leq R_{PU(max)}$.

7. Application design-in information

A typical application is shown in Figure 5. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. HDMI DDC applications for DVD/R and LCD TV are shown in Figure 6 and Figure 7, respectively. In these applications the HDMI transmitter or receiver is 3.3 V, while the DDC line is 5 V, PCA9527 behaves like a voltage level shift, a buffer and long cable bus extender to ensure signal integrity for accessing the EDID on the DDC line.

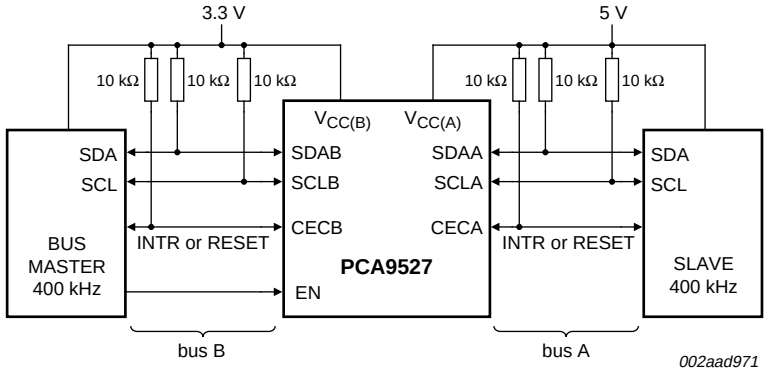


Fig 5. Typical application

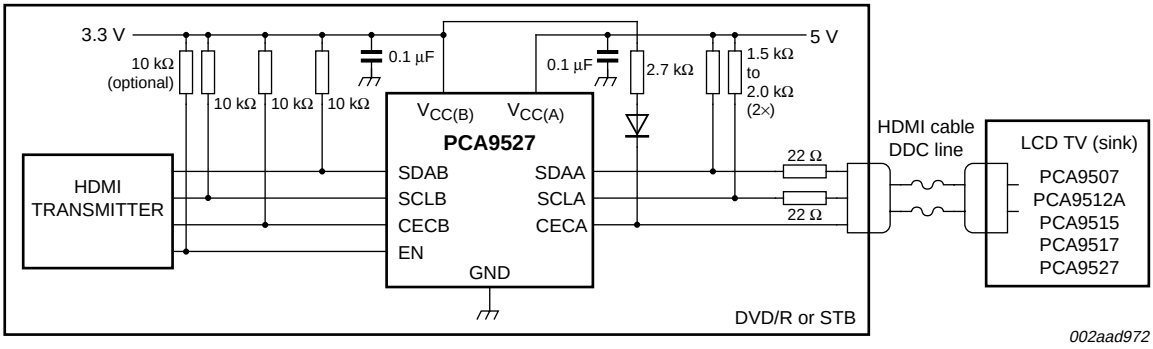


Fig 6. Source or DVD/R, STB application

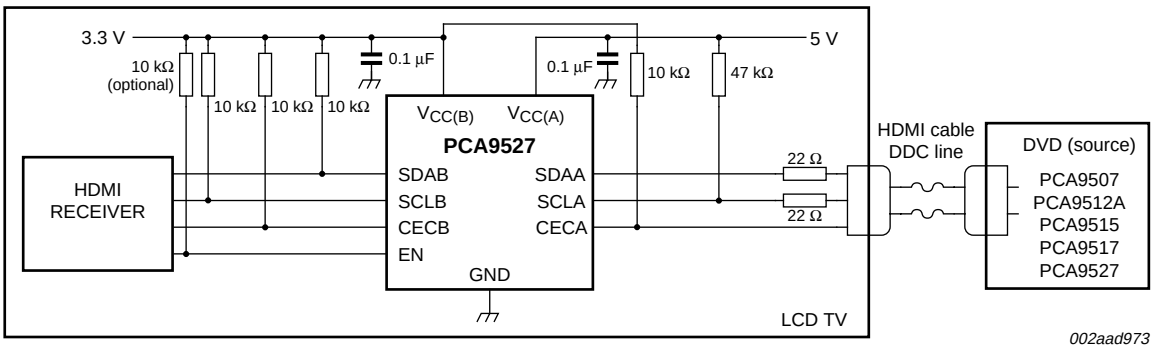


Fig 7. Sink or LCD TV application

According to Figure 5, when port A of the PCA9527 is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9527 falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 11 and Figure 12.

If the bus master in Figure 5 were to write to the slave through the PCA9527, waveforms shown in Figure 11 would be observed on the A bus. This looks like a normal I²C-bus transmission except that the HIGH level may be as low as 2.7 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

The master drives the B bus to ground or lets it float to $V_{CC(B)}$ as it sends data to the slave at the falling edge of the 8th clock, master releases SDAB on the B bus and slave pulls SDAA on the A bus to ground, causing the PCA9527 to pull SDAB on the B bus to 0.5 V. At the falling edge of the 9th clock, the master again drives the B bus and slave releases the A bus.

Multiple PCA9527 port A sides can be connected in a star configuration (Figure 8), allowing all nodes to communicate with each other.

Multiple PCA9527s can be connected in series (Figure 9) as long as port A is connected to port B. I²C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

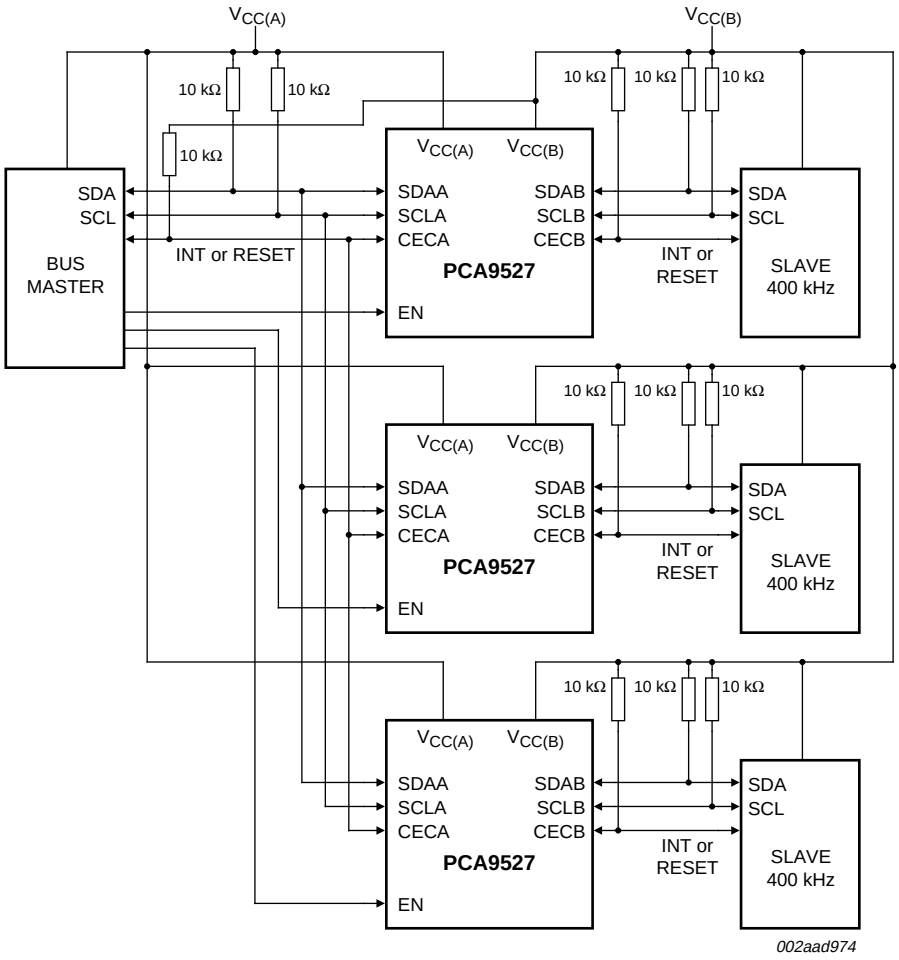


Fig 8. Typical star application

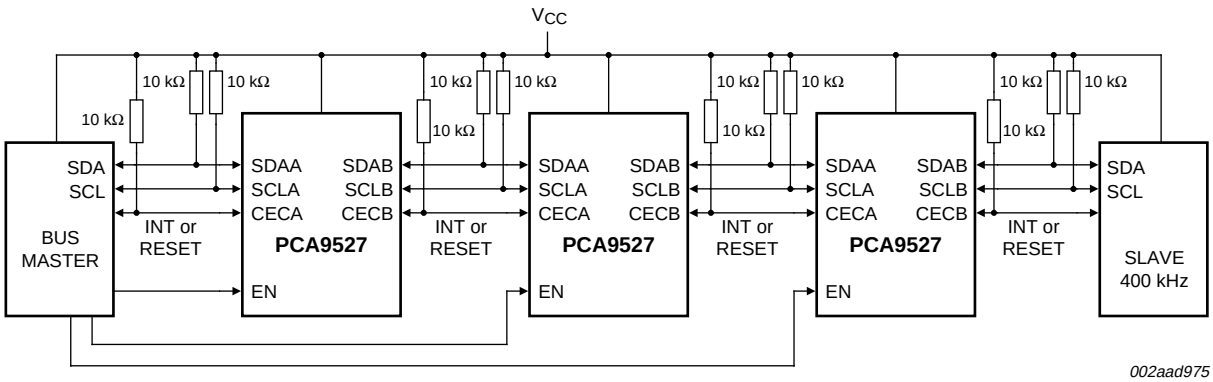


Fig 9. Typical series application

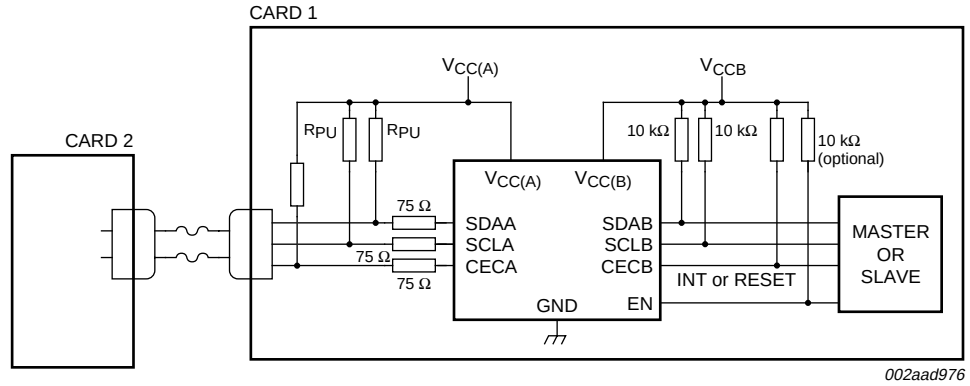


Fig 10. Typical application of PCA9527 driving a short cable

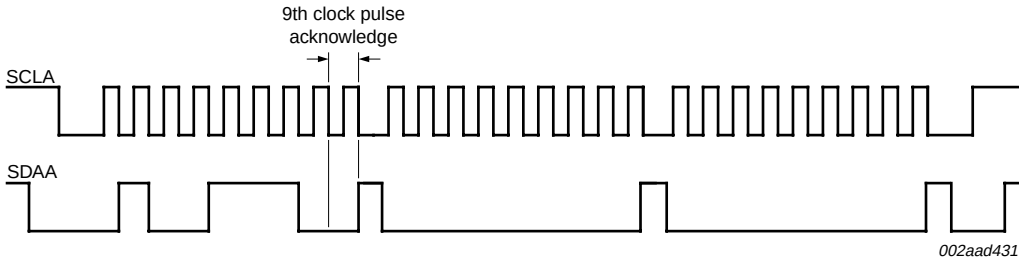


Fig 11. Bus A (2.7 V to 5.5 V bus) waveform

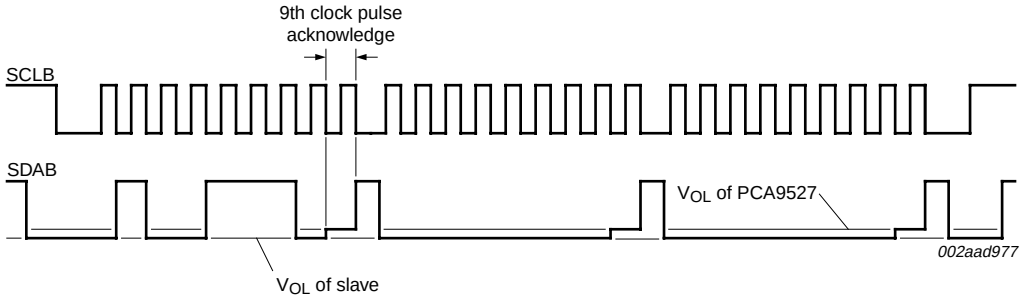


Fig 12. Bus B (2.7 V to 5.5 V) waveform

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(B)}$	supply voltage port B		–0.5	+7	V
$V_{CC(A)}$	supply voltage port A		–0.5	+7	V
$V_{I/O}$	voltage on an input/output pin	port B; port A; EN	–0.5	+7	V
$I_{I/O}$	input/output current	port A; port B	-	50	mA
I_{SS}	ground supply current		-	100	mA
P_{tot}	total power dissipation		-	100	mW
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature	operating in free air	–40	+85	°C
T_j	junction temperature		-	+125	°C

9. Static characteristics

Table 5. Static characteristics

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
$V_{CC(B)}$	supply voltage port B			2.7	-	3.6	V
$V_{CC(A)}$	supply voltage port A		[1]	2.7	-	5.5	V
I_{stb}	standby current	inputs ≥ V_{CC} or GND on pin $V_{CC(A)}$; EN = 0 V		-	40	60	µA
$I_{CCH(A)}$	port A HIGH-level supply current			-	0.5	0.8	mA
$I_{CCL(A)}$	port A LOW-level supply current	A port channels LOW; $V_{CC(B)}$ = 3.6 V; $V_{CC(A)}$ = 5.5 V; B port open		-	1.1	1.7	mA
I_{stb}	standby current	inputs ≥ V_{CC} or GND on pin $V_{CC(B)}$; EN = 0 V		-	40	60	µA
$I_{CCH(B)}$	port B HIGH-level supply current	all inputs HIGH; $V_{CC(B)}$ = 3.6 V; SDAA = SCLA = $V_{CC(A)}$; SDAB, SCLB, CECn, EN = $V_{CC(B)}$					
		$V_{CC(A)}$ = 5 V		-	0.8	1.2	mA
		$V_{CC(A)}$ = 0 V		-	0.5	0.7	mA
$I_{CCL(B)}$	port B LOW-level supply current	B port channels LOW; $V_{CC(B)}$ = 3.6 V; A port open					
		$V_{CC(A)}$ = 5 V		-	1.4	2.2	mA
		$V_{CC(A)}$ = 0 V		-	0.7	1.1	mA
$I_{CC(B)c}$	contention port B supply current	$V_{CC(B)}$ = 3.6 V; SDAB = SCLB = 0.2 V		-	1.4	2.2	mA

Table 5. Static characteristics *…continued*

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input and output SDAB, SCLB and CECB							
V_{IH}	HIGH-level input voltage			$0.7V_{CC(B)}$	-	5.5	V
V_{IL}	LOW-level input voltage		[2]	−0.5	-	$+0.3V_{CC(B)}$	V
V_{ILc}	contention LOW-level input voltage			−0.5	0.4	-	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_I = 5.5 V		-	-	±1	µA
I_{IL}	LOW-level input current	V_I = 0.2 V		-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA or 6 mA		0.47	0.52	0.6	V
V_{OL}−V_{ILc}	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design		-	-	70	mV
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		-	6	8	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		-	6	8	pF
Input and output SDAA, SCLA							
V_{IH}	HIGH-level input voltage			$0.7V_{CC(A)}$	-	5.5	V
V_{IL}	LOW-level input voltage		[3]	−0.5	-	$+0.3V_{CC(A)}$	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_{CC} = V_I = 5.5 V		-	-	±1	µA
I_{IL}	LOW-level input current	V_I = 0.2 V		-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	0.1	0.2	V
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		-	6	8	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		-	6	8	pF
$I_{trt(pu)}$	transient boosted pull-up current	SCLA, SDAA only; $V_{CC(A)}$ = 4.5 V; slew rate = 1.25 V/µs		-	6	-	mA
Input and output CECA							
V_{IH}	HIGH-level input voltage			$0.7V_{CC(B)}$	-	5.5	V
V_{IL}	LOW-level input voltage		[3]	−0.5	-	$+0.3V_{CC(B)}$	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_{CC} = V_I = 5.5 V		-	-	±1	µA
I_{IL}	LOW-level input current	V_I = 0.2 V		-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	0.1	0.2	V
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		-	6	8	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		-	6	8	pF
Enable							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{CC(B)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{CC(B)}$	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V, EN pin only; V_{CC} = 3.6 V		-	−10	−30	µA
I_{LI}	input leakage current	V_I = V_{CC}		−1	-	+1	µA
C_i	input capacitance	V_I = 3.0 V or 0 V		-	2	5	pF

[1] LOW-level supply voltage.

[2] V_{IL} specification is for the first LOW level seen by the SDAB/SCLB/CECB lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAB/SCLB/CECB lines to retain a valid LOW level the static level must be less than V_{ILc}.

[3] V_{IL} for port A with envelope noise must be below $0.3V_{CC(A)}$ for stable performance.

10. Dynamic characteristics

Table 6. Dynamic characteristics

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.[1][2]

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	port B to port A; Figure 15	[4]	70	115	350	ns
t_{PHL}	HIGH to LOW propagation delay	port B to port A; Figure 13		40	75	180	ns
t_{TLH}	LOW to HIGH output transition time	port A; Figure 13		20	155	280	ns
t_{THL}	HIGH to LOW output transition time	port A; Figure 13		20	60	100	ns
t_{PLH}	LOW to HIGH propagation delay	port A to port B; Figure 14	[5]	125	175	310	ns
t_{PHL}	HIGH to LOW propagation delay	port A to port B; Figure 14	[5]	130	220	330	ns
t_{TLH}	LOW to HIGH output transition time	port B; Figure 14		80	130	260	ns
t_{THL}	HIGH to LOW output transition time	port B; Figure 14		20	45	100	ns
t_{PLH}	LOW to HIGH propagation delay	CECA; Figure 16		40	110	250	ns
t_{PHL}	HIGH to LOW propagation delay	CECA; Figure 16		40	80	180	ns
t_{TLH}	LOW to HIGH output transition time	CECA; Figure 16		80	150	260	ns
t_{THL}	HIGH to LOW output transition time	CECA; Figure 16		20	60	100	ns
t_{su}	set-up time	EN HIGH before START condition	[6]	200	-	-	µs
t_h	hold time	EN HIGH after STOP condition	[6]	200	-	-	ns
$t_{rec(pd-act)}$	recovery time from power-down to active	$V_{CC(A)}$ power-down to active; EN HIGH and $V_{CC(B)}$ on; $V_{CC(A)}$ ramping up	[7]	200	-	-	µs
		$V_{CC(B)}$ power-down to active; EN HIGH and $V_{CC(A)}$ on; $V_{CC(B)}$ ramping up	[8]	200	-	-	µs

[1] Times are specified with loads of 1.35 kΩ pull-up resistance and 57 pF load capacitance on port B, and 450 Ω pull-up resistance and 57 pF load capacitance on port A. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

[2] Pull-up voltages are $V_{CC(A)}$ on port A and $V_{CC(B)}$ on port B.

[3] Typical values were measured with $V_{CC(A)}$ = 3.3 V at T_{amb} = 25 °C, unless otherwise noted.

[4] The t_{PLH} delay data from port B to port A is measured at 0.5 V on port B to $0.3V_{CC(A)}$ on port A.

[5] The proportional delay data from port A to port B is measured at $0.3V_{CC(A)}$ on port A to $0.3V_{CC(B)}$ on port B.

[6] The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

[7] If the $V_{CC(A)}$ ramp up is fast, then the $t_{rec(pd-act)}$ time must be allowed before the inputs are switched. If the supply ramp up is slow, the channels may be connected even before the final supply voltage is reached.

[8] If the $V_{CC(B)}$ ramp up is fast, then the $t_{rec(pd-act)}$ time must be allowed before the inputs are switched. If the supply ramp up is slow, the channels may be connected even before the final supply voltage is reached.

10.1 AC waveforms

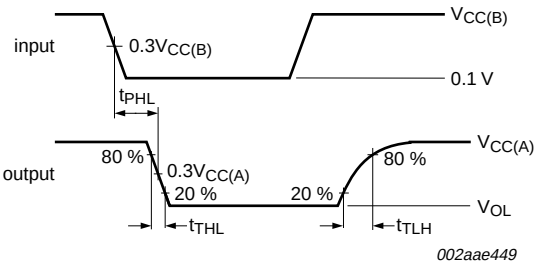


Fig 13. t_{PHL} propagation delay and transition times; SCLB/SDAB to SCLA/SDAA

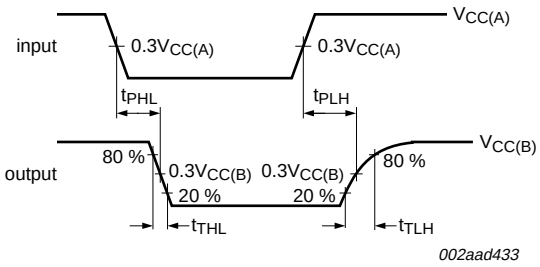
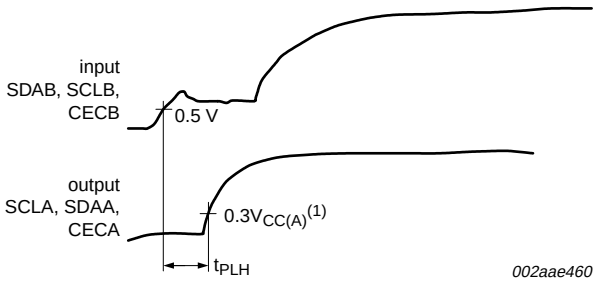


Fig 14. Propagation delay and transition times; SCLA/SDAA to SCLB/SDAB



(1) CECA output has $0.3V_{CC(B)}$ reference.

Fig 15. t_{PLH} propagation delay; B inputs to A inputs

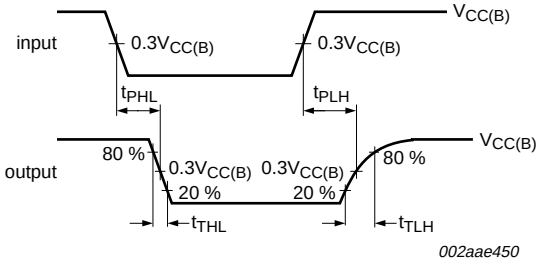
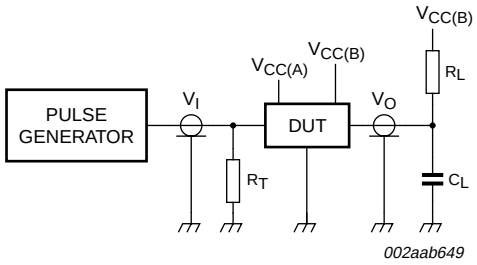


Fig 16. Propagation delay and transition times; CEC in to CEC out

11. Test information



R_L = load resistor; 1.35 kΩ on port B (2.7 V to 5 V) and 1.5 kΩ on port A (5.0 V).

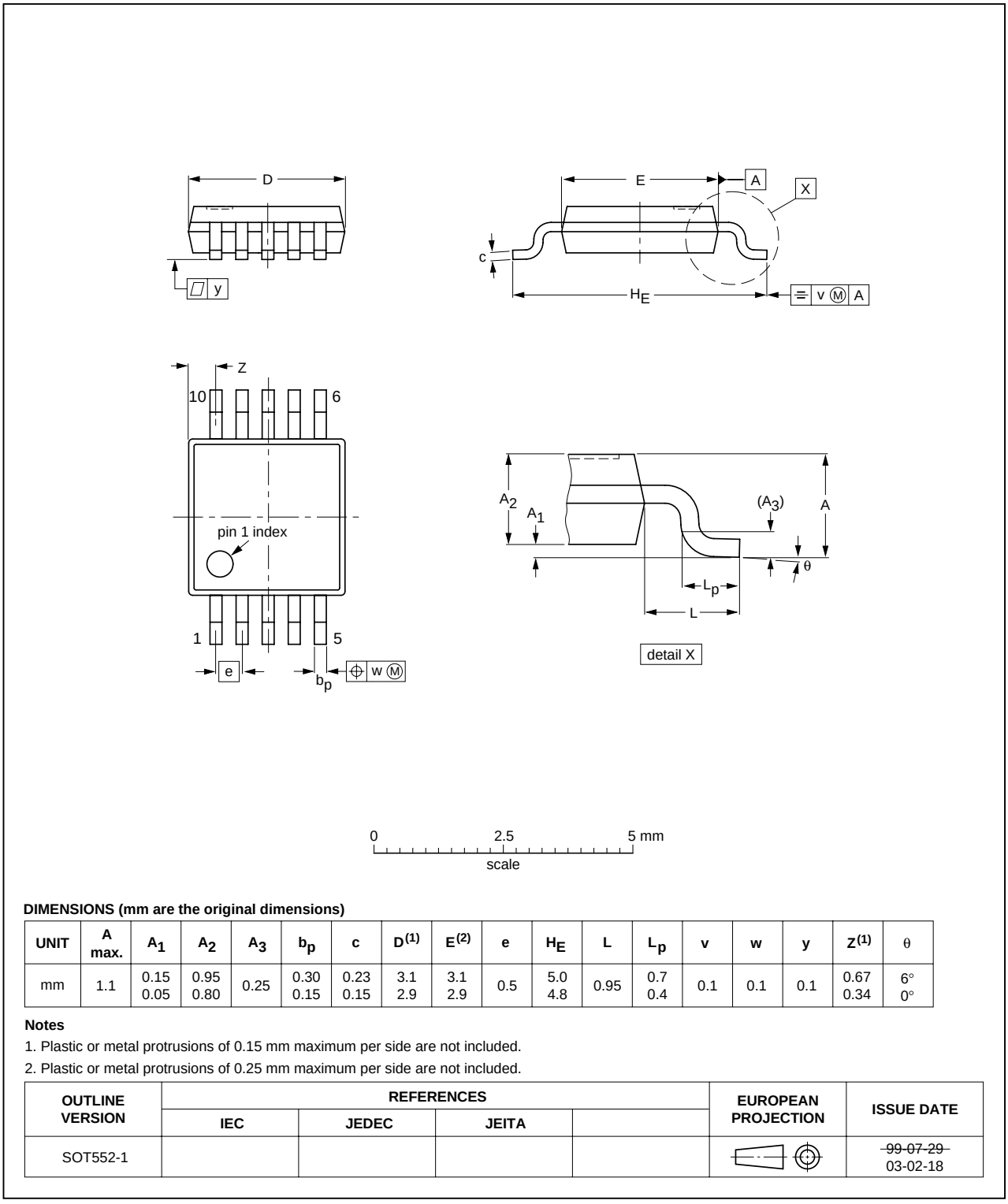
C_L = load capacitance includes jig and probe capacitance; 57 pF.

R_T = termination resistance should be equal to Z_o of pulse generators.

Fig 17. Test circuit for open-drain outputs

12. Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm **SOT552-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT552-1						~~99-07-29~~ 03-02-18

Fig 18. Package outline SOT552-1 (TSSOP10)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020C)

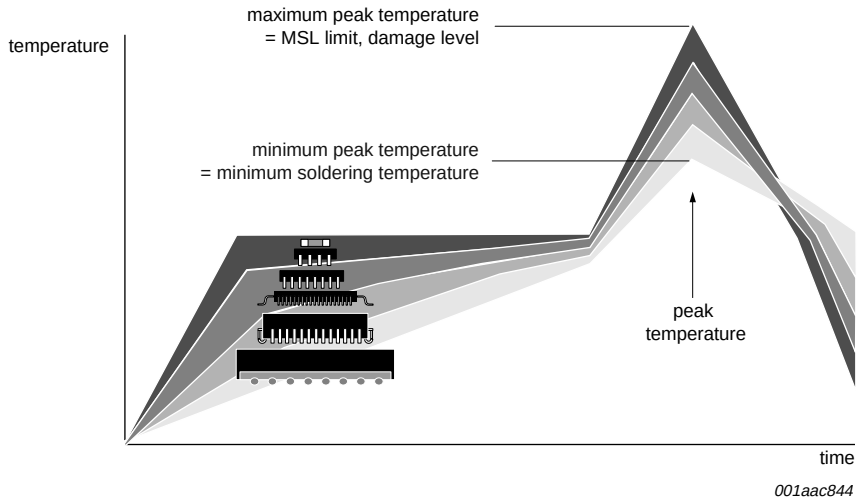
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CEC	Consumer Electronic Control
CMOS	Complementary Metal-Oxide Semiconductor
DDC	Display Data Channel
DVD	Digital Video Disc
DUT	Device Under Test
EDID	Extended Display Identification Data
ESD	ElectroStatic Discharge
HBM	Human Body Model
HDMI	High-Definition Multimedia Interface
I²C-bus	Inter Integrated Circuit bus
I/O	Input/Output
LCD	Liquid Crystal Display
MM	Machine Model
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
RC	Resistor-Capacitor network
SMBus	System Management Bus
STB	Set-Top Box

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9527_1	20090629	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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