1.2 A, 20 V, 700 kHz/1.4 MHz, Nonsynchronous Step-Down Regulator

Data Sheet

ADP2300/ADP2301

FEATURES

- 1.2 A maximum load current
- ±2% output accuracy over temperature range
- Wide input voltage range: 3.0 V to 20 V
- 700 kHz (ADP2300) or 1.4 MHz (ADP2301) switching frequency options
- High efficiency up to 91%
- Current-mode control architecture
- Output voltage from 0.8 V to 0.85 × V_{IN}
- Automatic PFM/PWM mode switching
- Precision enable pin with hysteresis
- Integrated high-side MOSFET
- Integrated bootstrap diode
- Internal compensation and soft start
- Minimum external components
- Undervoltage lockout (UVLO)
- Overcurrent protection (OCP) and thermal shutdown (TSD)
- Available in ultrasmall, 6-lead TSOT package
- Supported by ADIsimPower™ design tool

APPLICATIONS

- LDO replacement for digital load applications
- Intermediate power rail conversion
- Communications and networking
- Industrial and instrumentation
- Healthcare and medical
- Consumer

TYPICAL APPLICATIONS CIRCUIT

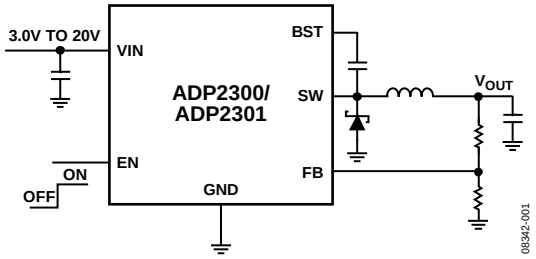

Figure 1.

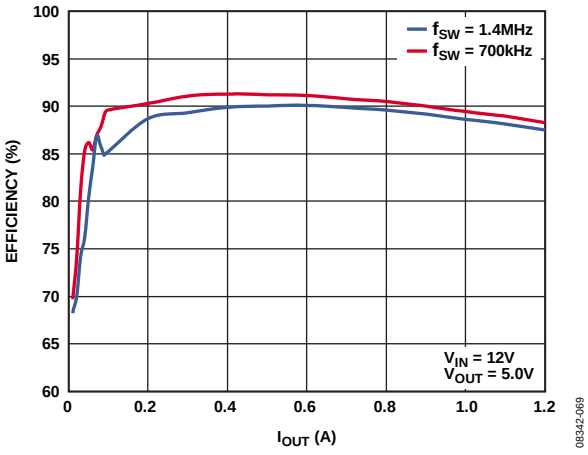

Figure 2. Efficiency vs. Output Current

GENERAL DESCRIPTION

The ADP2300/ADP2301 are compact, constant-frequency, current-mode, step-down dc-to-dc regulators with integrated power MOSFET. The ADP2300/ADP2301 devices run from input voltages of 3.0 V to 20 V, making them suitable for a wide range of applications. A precise, low voltage internal reference makes these devices ideal for generating a regulated output voltage as low as 0.8 V, with ±2% accuracy, for up to 1.2 A load current.

There are two frequency options: the ADP2300 runs at 700 kHz, and the ADP2301 runs at 1.4 MHz. These options allow users to make decisions based on the trade-off between efficiency and total solution size. Current-mode control provides fast and stable line and load transient performance. The ADP2300/ADP2301 devices include internal soft start to prevent inrush current at power-up. Other key safety features include short-circuit protection, thermal shutdown (TSD), and input undervoltage lockout (UVLO). The precision enable pin threshold voltage allows the ADP2300/ADP2301 to be easily sequenced from other input/output supplies. It can also be used as a programmable UVLO input by using a resistive divider.

The ADP2300/ADP2301 are available in a 6-lead TSOT package and are rated for the −40°C to +125°C junction temperature range.

Rev. C
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REVISION HISTORY

11/12—Rev. B to Rev. C

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6/12—Rev. A to Rev. B

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6/10—Rev. 0 to Rev. A

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2/10—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.3 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN						
Voltage Range	V_{IN}		3		20	V
Supply Current	I_{VIN}	No switching, V_{IN} = 12 V		640	800	µA
Shutdown Current	I_{SHDN}	V_{EN} = 0 V, V_{IN} = 12 V		18	35	µA
Undervoltage Lockout Threshold	UVLO	V_{IN} rising		2.80	2.95	V
		V_{IN} falling	2.15	2.40		V
FB						
Regulation Voltage	V_{FB}	T_J = 0°C to +125°C	0.788	0.800	0.812	V
		T_J = −40°C to +125°C	0.784	0.800	0.816	V
Bias Current	I_{FB}			0.01	0.1	µA
SW						
On Resistance[1]		$V_{BST} - V_{SW}$ = 5 V, I_{SW} = 150 mA		440	700	mΩ
Peak Current Limit[2]		$V_{BST} - V_{SW}$ = 5 V, V_{IN} = 12 V	1.5	1.9	2.5	A
Minimum On Time				100	135	ns
Minimum Off Time		ADP2300		145	190	ns
		ADP2301		70	120	ns
OSCILLATOR FREQUENCY		ADP2300	0.5	0.7	0.9	MHz
		ADP2301	1.0	1.4	1.75	MHz
SOFT START TIME		ADP2300		1460		µs
		ADP2301		730		µs
EN						
Input Threshold	V_{EN}		1.13	1.2	1.27	V
Input Hysteresis				100		mV
Pull-Down Current				1.2		µA
BOOTSTRAP VOLTAGE	V_{BOOT}	No switching, V_{IN} = 12 V		5.0		V
THERMAL SHUTDOWN						
Threshold				140		°C
Hysteresis				15		°C

[1] Pin-to-pin measurements.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN	−0.3 V to +28 V
SW	−1.0 V to +28 V
BST to SW	−0.6 V to +6 V
BST	−0.3 V to +28 V
FB	−0.3 V to +3.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to GND.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}	Unit
6-Lead TSOT	186.02	66.34	°C/W

[1] θ_{JA} and θ_{JC} are measured using natural convection on a JEDEC 4-layer board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

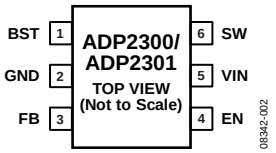

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST	Boost Supply for the High-Side MOSFET Driver. A 0.1 µF capacitor is connected between the SW and BST pins to form a floating supply to drive the gate of the MOSFET switch above the V_{IN} supply voltage.
2	GND	Ground. Connect this pin to the ground plane.
3	FB	Feedback Voltage Sense Input. Connect this pin to a resistive divider from V_{OUT}. Set the voltage to 0.8 V for a desired V_{OUT}.
4	EN	Output Enable. Pull this pin high to enable the output. Pull this pin low to disable the output. This pin can also be used as a programmable UVLO input. This pin has a 1.2 µA pull-down current to GND.
5	VIN	Power Input. Connect to the input power source with a ceramic bypass capacitor to GND directly from this pin.
6	SW	Switch Node Output. Connect an inductor to V_{OUT} and a catch diode to GND from this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3 V, T_A = 25°C, V_{EN} = V_{IN}, unless otherwise noted.

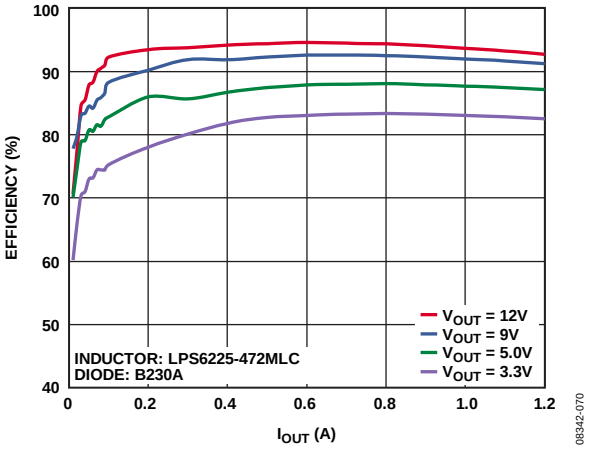

Figure 4. Efficiency Curve, V_{IN} = 18 V, f_{SW} = 1.4 MHz

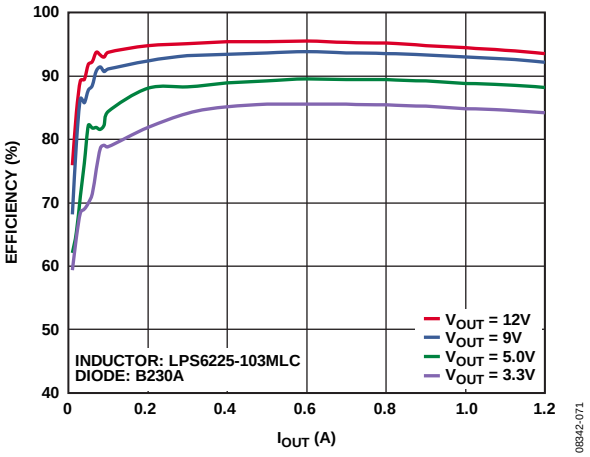

Figure 5. Efficiency Curve, V_{IN} = 18 V, f_{SW} = 700 kHz

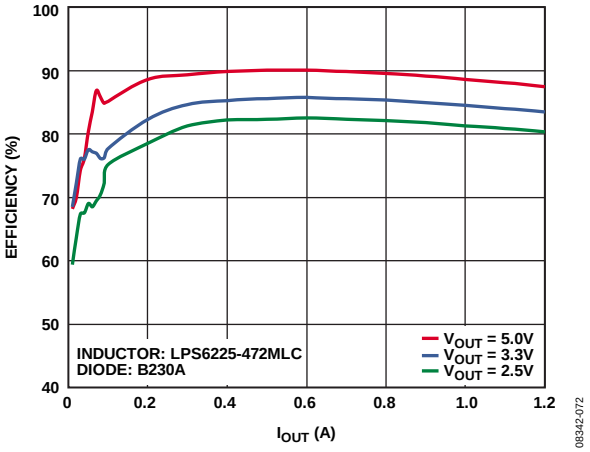

Figure 6. Efficiency Curve, V_{IN} = 12 V, f_{SW} = 1.4 MHz

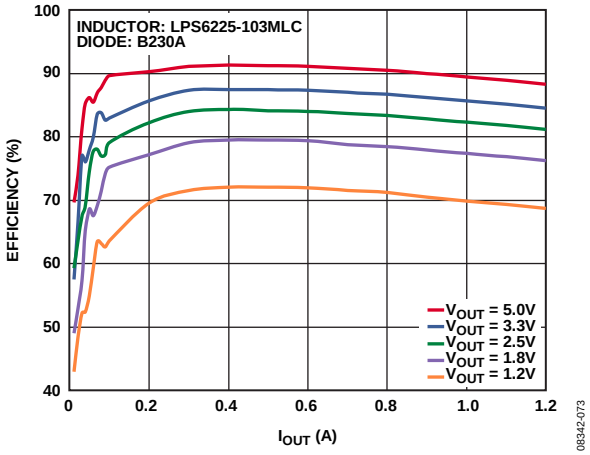

Figure 7. Efficiency Curve, V_{IN} = 12 V, f_{SW} = 700 kHz

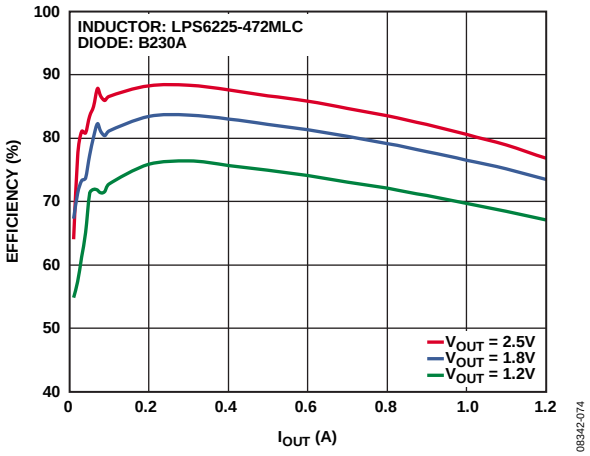

Figure 8. Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 1.4 MHz

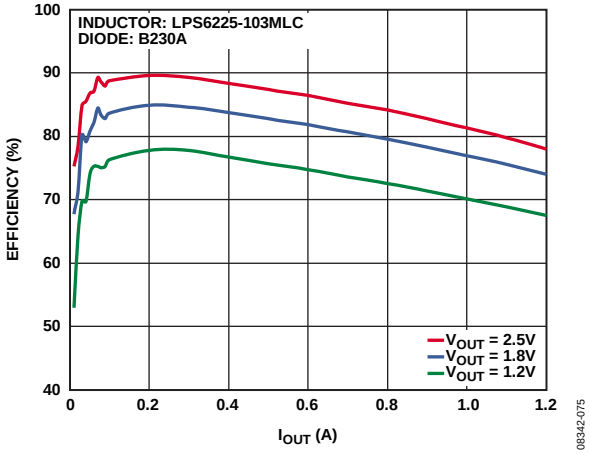

Figure 9. Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 700 kHz

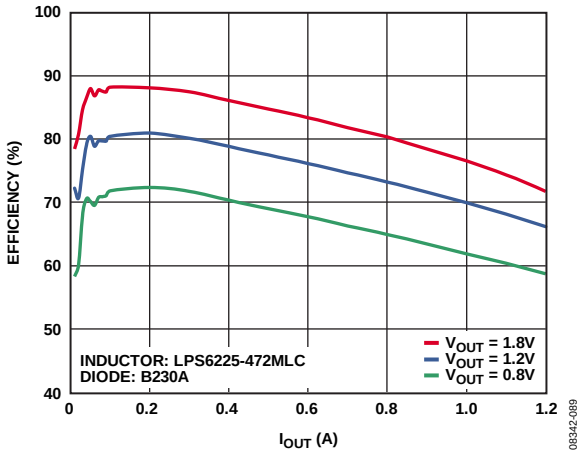

Figure 10. Efficiency Curve, V_{IN} = 3.3 V with External 5.0 V Bootstrap Bias Voltage, f_{SW} = 1.4 MHz

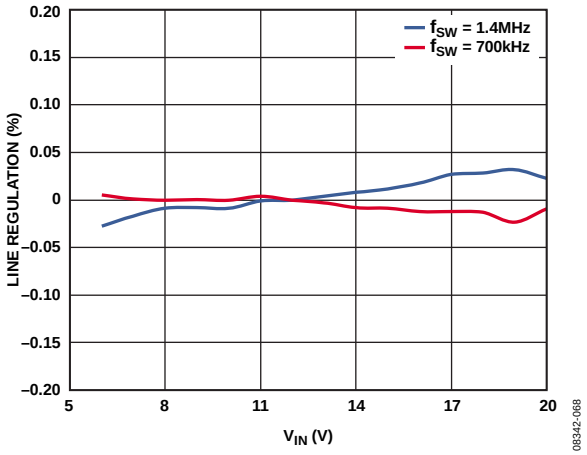

Figure 13. Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

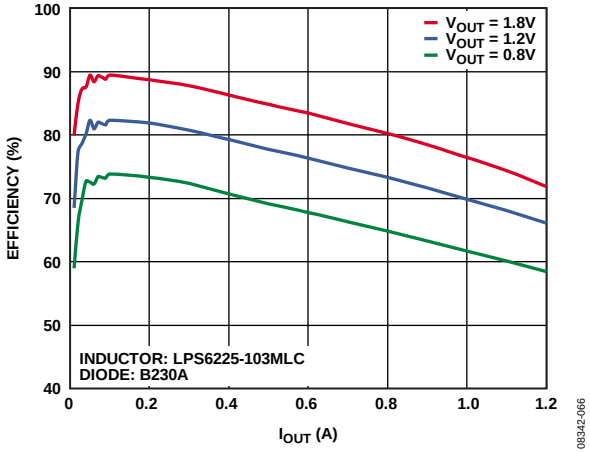

Figure 11. Efficiency Curve, V_{IN} = 3.3 V with External 5.0 V Bootstrap Bias Voltage, f_{SW} = 700 kHz

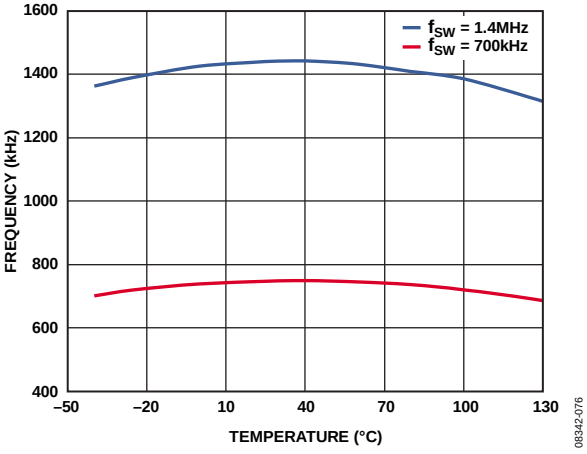

Figure 14. Frequency vs. Temperature

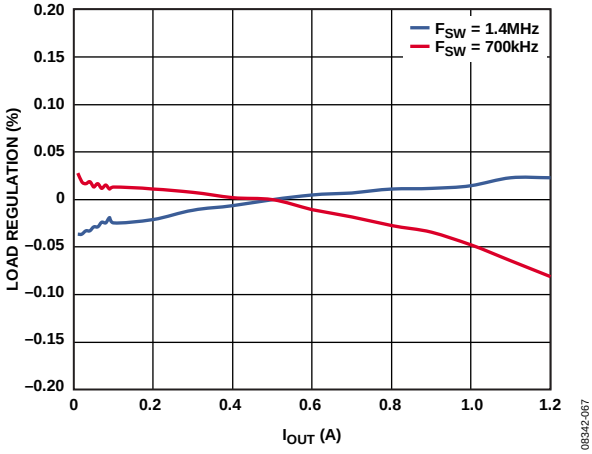

Figure 12. Load Regulation, V_{OUT} = 3.3 V, V_{IN} = 12 V

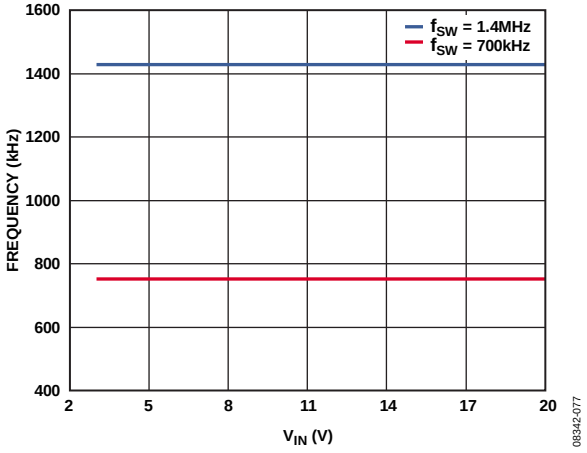

Figure 15. Frequency vs. V_{IN}

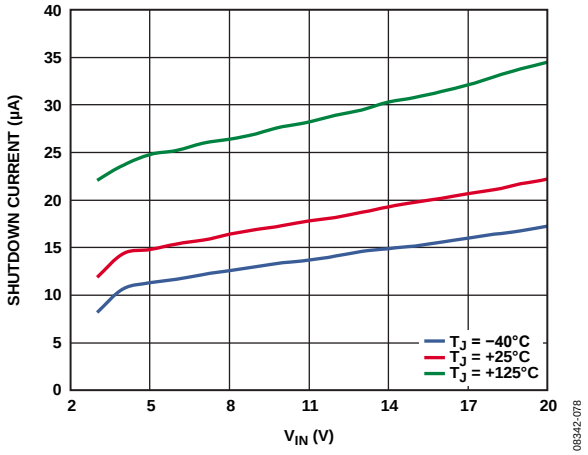

Figure 16. Shutdown Current vs. V_{IN}

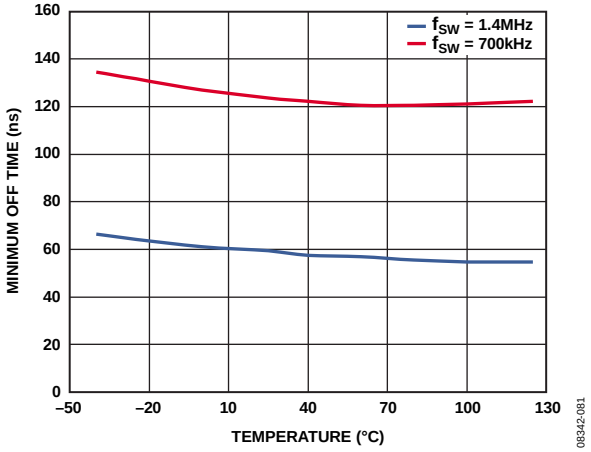

Figure 19. Minimum Off Time vs. Temperature

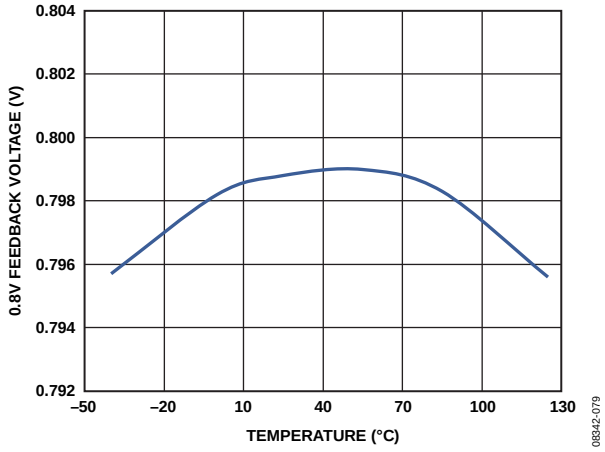

Figure 17. 0.8 V Feedback Voltage vs. Temperature

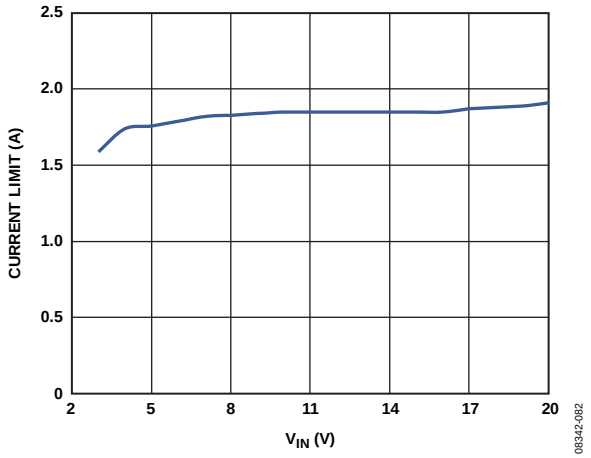

Figure 20. Current-Limit Threshold vs. V_{IN}, $V_{BST} - V_{SW} = 5.0$ V

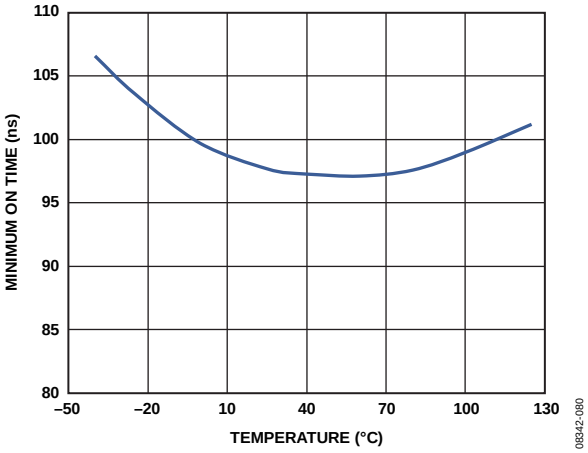

Figure 18. Minimum On Time vs. Temperature

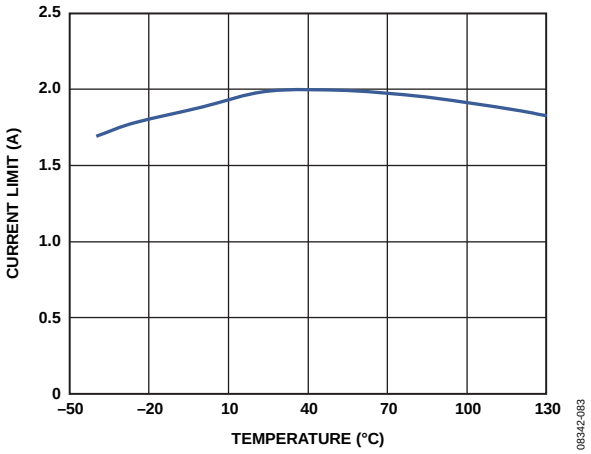

Figure 21. Current-Limit Threshold vs. Temperature

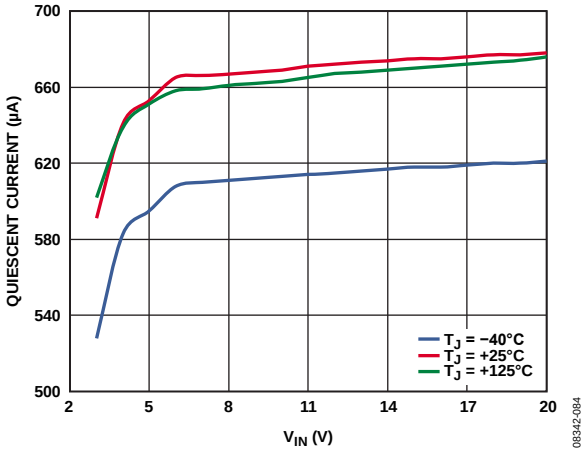

Figure 22. Quiescent Current vs. V_{IN}

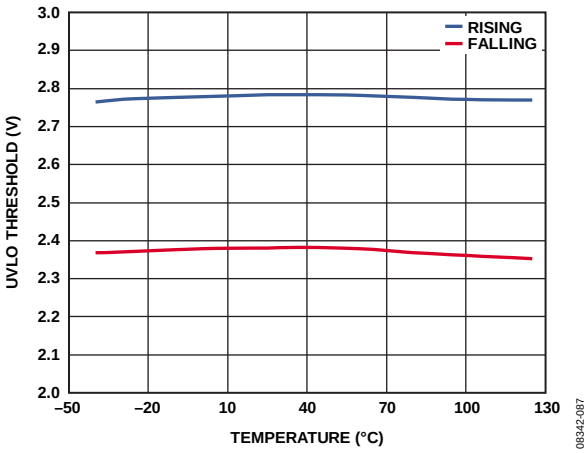

Figure 25. UVLO Threshold vs. Temperature

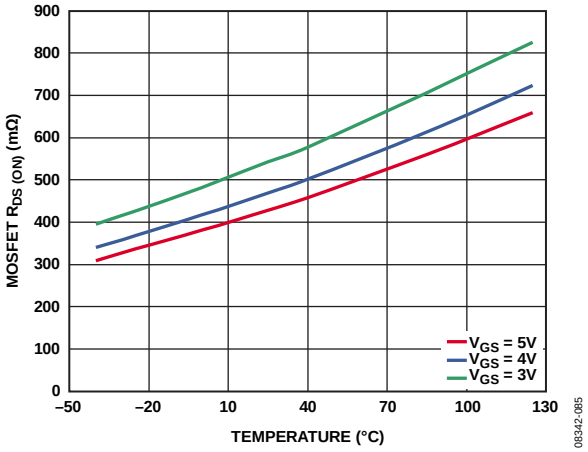

Figure 23. MOSFET $R_{DS(ON)}$ vs. Temperature (Pin-to-Pin Measurements)

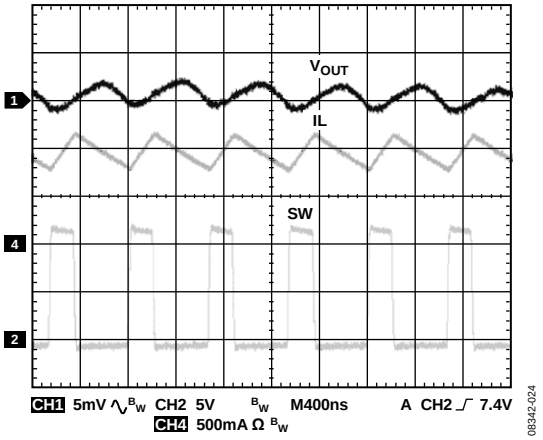

Figure 26. Steady State at Heavy Load, f_{SW} = 1.4 MHz, I_{OUT} = 1 A

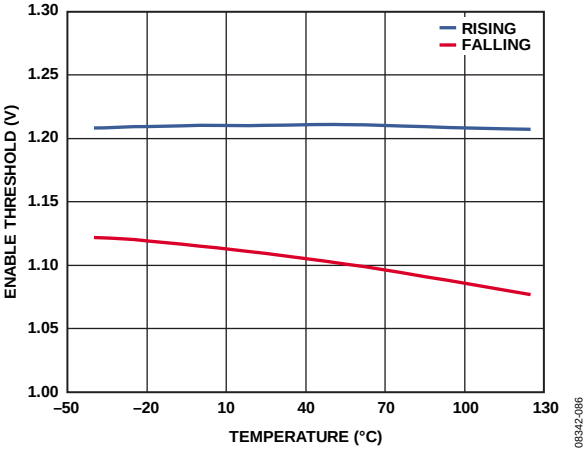

Figure 24. Enable Threshold vs. Temperature

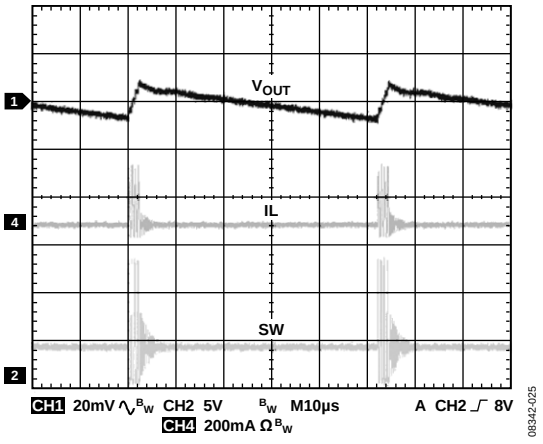

Figure 27. Steady State at Light Load, f_{SW} = 1.4 MHz, I_{OUT} = 40 mA

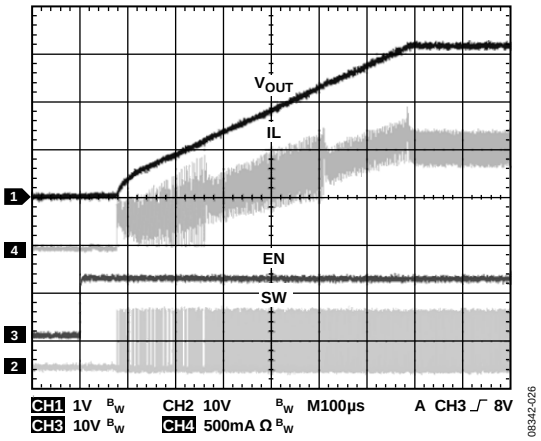

Figure 28. Soft Start with 1 A Resistance Load, f_{SW} = 1.4 MHz

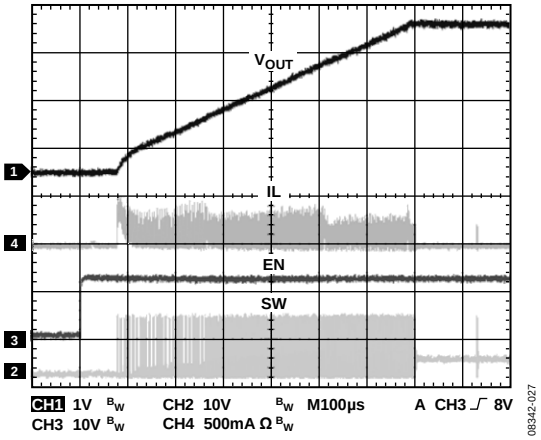

Figure 29. Soft Start with No Load, f_{SW} = 1.4 MHz

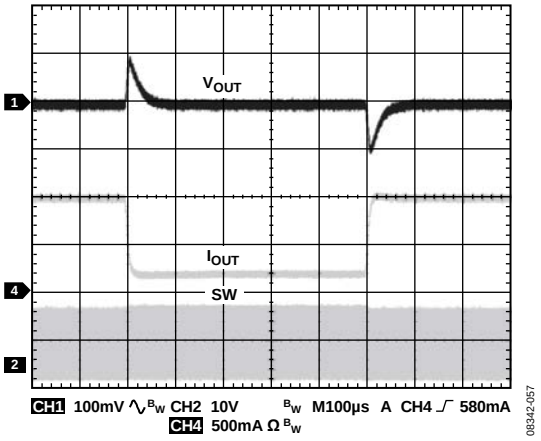

Figure 30. ADP2301 Load Transient, 0.2 A to 1.0 A, V_{OUT} = 5.0 V, V_{IN} = 12 V (f_{SW} = 1.4 MHz, L = 4.7 µH, C_{OUT} = 10 µF)

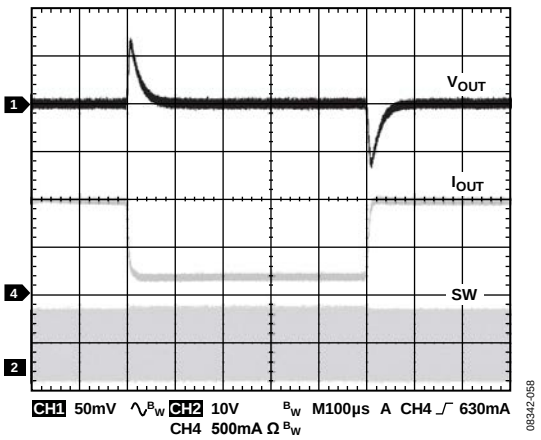

Figure 31. ADP2301 Load Transient, 0.2 A to 1.0 A, V_{OUT} = 3.3 V, V_{IN} = 12 V (f_{SW} = 1.4 MHz, L = 4.7 µH, C_{OUT} = 22 µF)

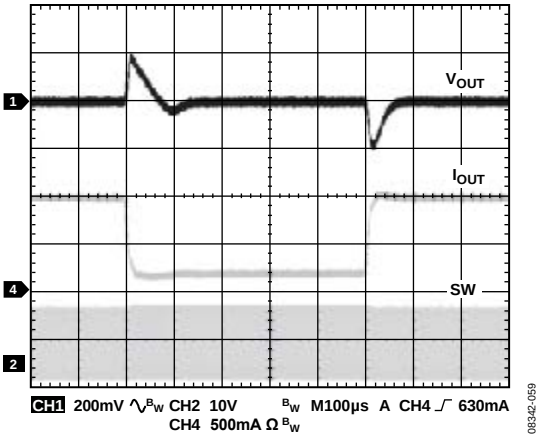

Figure 32. ADP2300 Load Transient, 0.2 A to 1.0 A, V_{OUT} = 5.0 V, V_{IN} = 12 V (f_{SW} = 700 kHz, L = 10 µH, C_{OUT} = 22 µF)

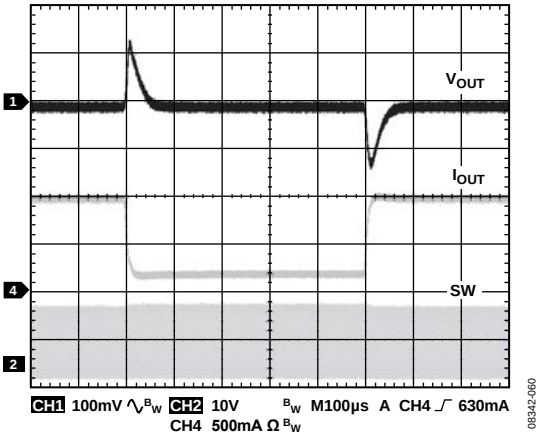

Figure 33. ADP2300 Load Transient, 0.2 A to 1.0 A, V_{OUT} = 3.3 V, V_{IN} = 12 V (f_{SW} = 700 kHz, L = 10 µH, C_{OUT} = 22 µF)

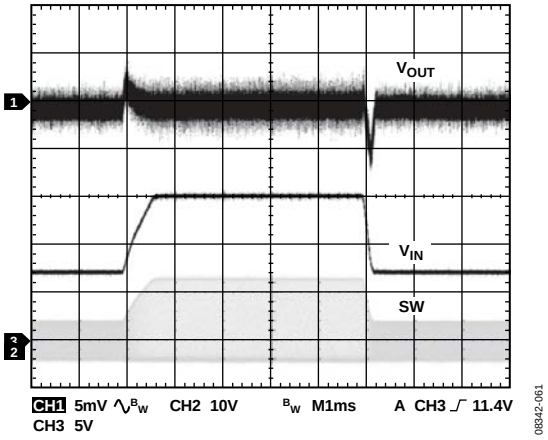

Figure 34. ADP2301 Line Transient,
7 V to 15 V, V_{OUT} = 3.3 V, I_{OUT} = 1.2 A, f_{SW} = 1.4 MHz

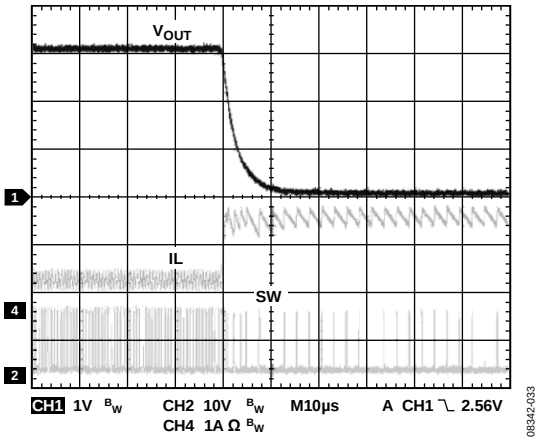

Figure 35. ADP2301 Short-Circuit Entry, V_{OUT} = 3.3 V
(f_{SW} = 1.4 MHz)

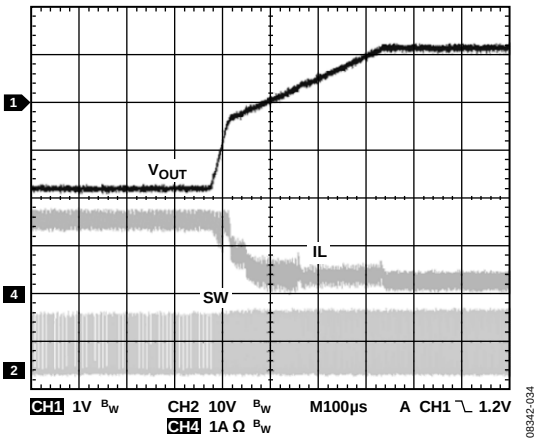

Figure 36. ADP2301 Short-Circuit Recovery, V_{OUT} = 3.3 V
(f_{SW} = 1.4 MHz)

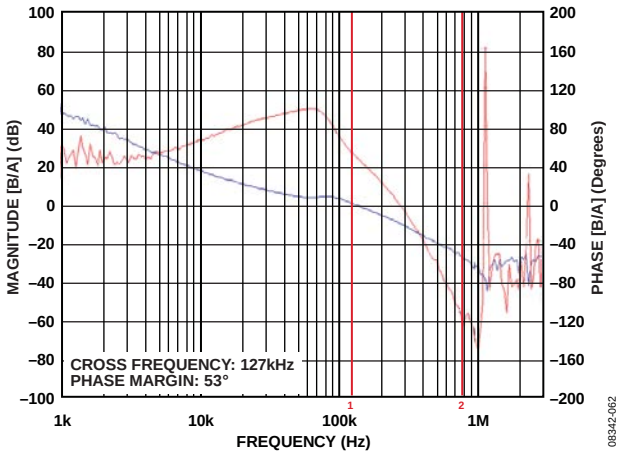

Figure 37. ADP2301 Bode Plot, V_{OUT} = 5.0 V, V_{IN} = 12 V
(f_{SW} = 1.4 MHz, L = 4.7 µH, C_{OUT} = 10 µF)

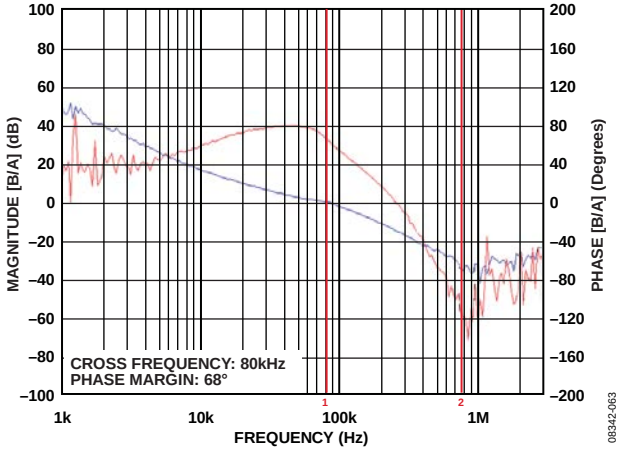

Figure 38. ADP2301 Bode Plot, V_{OUT} = 3.3 V, V_{IN} = 12 V
(f_{SW} = 1.4 MHz, L = 4.7 µH, C_{OUT} = 22 µF)

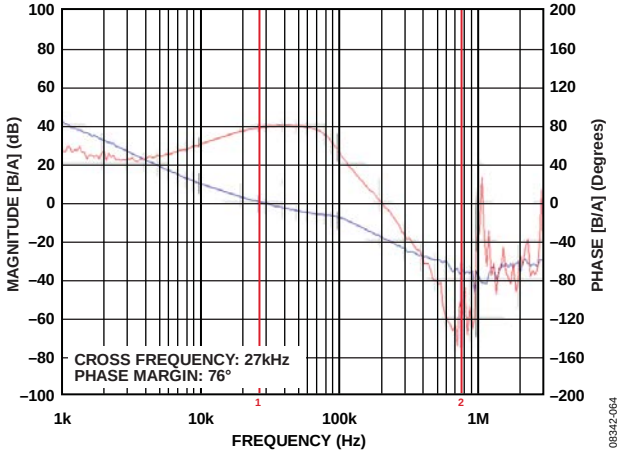

Figure 39. ADP2300 Bode Plot, V_{OUT} = 5.0 V, V_{IN} = 12 V
(f_{SW} = 700 kHz, L = 10 µH, C_{OUT} = 22 µF)

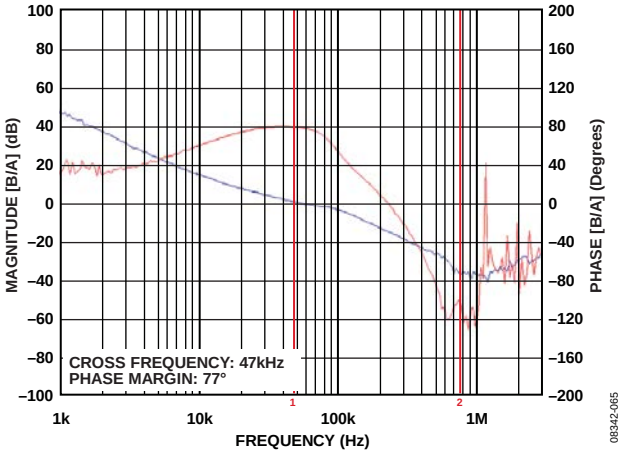

Figure 40. ADP2300 Bode Plot, V_{OUT} = 3.3 V, V_{IN} = 12 V (f_{SW} = 700 kHz, L = 10 µH, C_{OUT} = 22 µF)

FUNCTIONAL BLOCK DIAGRAM

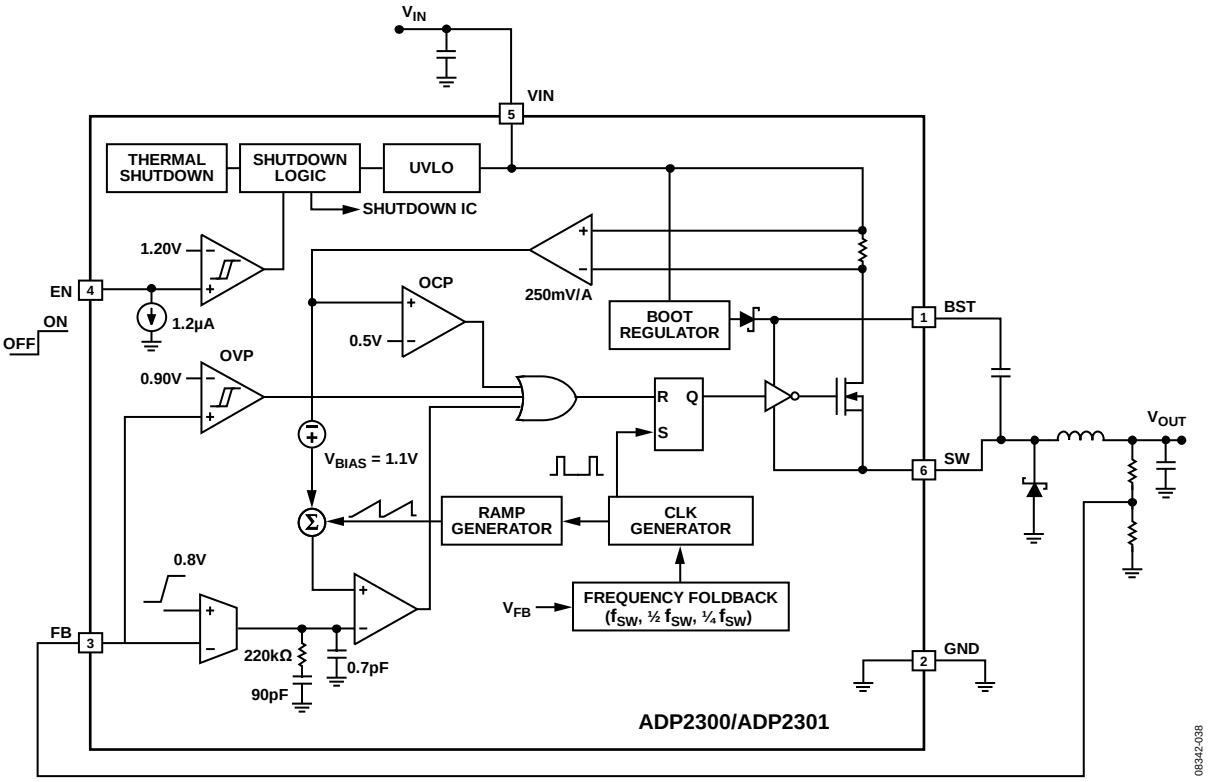

Figure 41. ADP2300/ADP2301 Functional Block Diagram

THEORY OF OPERATION

The ADP2300/ADP2301 are nonsynchronous, step-down dc-to-dc regulators, each with an integrated high-side power MOSFET. A high switching frequency and ultrasmall, 6-lead TSOT package allow small step-down dc-to-dc regulator solutions.

The ADP2300/ADP2301 can operate with an input voltage from 3.0 V to 20 V while regulating an output voltage down to 0.8 V.

The ADP2300/ADP2301 are available in two fixed-frequency options: 700 kHz (ADP2300) and 1.4 MHz (ADP2301).

BASIC OPERATION

The ADP2300/ADP2301 use the fixed-frequency, peak current-mode PWM control architecture at medium to high loads, but shift to a pulse-skip mode control scheme at light loads to reduce the switching power losses and improve efficiency. When the devices operate in fixed-frequency PWM mode, output regulation is achieved by controlling the duty cycle of the integrated MOSFET. When the devices operate in pulse-skip mode at light loads, the output voltage is controlled in a hysteretic manner with higher output ripple. In this mode of operation, the regulator periodically stops switching for a few cycles, thus keeping the conversion losses minimal to improve efficiency.

PWM MODE

In PWM mode, the ADP2300/ADP2301 operate at a fixed frequency, set by an internal oscillator. At the start of each oscillator cycle, the MOSFET switch is turned on, sending a positive voltage across the inductor. The inductor current increases until the current-sense signal crosses the peak inductor current threshold that turns off the MOSFET switch; this threshold is set by the error amplifier output. During the MOSFET off time, the inductor current declines through the external diode until the next oscillator clock pulse starts a new cycle. The ADP2300/ADP2301 regulate the output voltage by adjusting the peak inductor current threshold.

POWER SAVING MODE

To achieve higher efficiency, the ADP2300/ADP2301 smoothly transition to the pulse-skip mode when the output load decreases below the pulse-skip current threshold. When the output voltage dips below regulation, the ADP2300/ADP2301 enter PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET switch is turned off, and the output capacitor supplies all the output current.

Since the pulse-skip mode comparator monitors the internal compensation node, which represents the peak inductor current information, the average pulse-skip load current threshold depends on the input voltage (V_{IN}), the output voltage (V_{OUT}), the inductor, and the output capacitor.

Because the output voltage occasionally dips below regulation and then recovers, the output voltage ripple in the power saving mode is larger than the ripple in the PWM mode of operation.

BOOTSTRAP CIRCUITRY

The ADP2300/ADP2301 each have an integrated boot regulator, which requires that a 0.1 µF ceramic capacitor (X5R or X7R) be placed between the BST and SW pins to provide the gate drive voltage for the high-side MOSFET. There must be at least a 1.2 V difference between the BST and SW pins to turn on the high-side MOSFET. This voltage should not exceed 5.5 V in case the BST pin is supplied with an external voltage source through a diode.

The ADP2300/ADP2301 generate a typical 5.0 V bootstrap voltage for a gate drive circuit by differentially sensing and regulating the voltage between the BST and SW pins. A diode integrated on the chip blocks the reverse voltage between the VIN and BST pins when the MOSFET switch is turned on.

PRECISION ENABLE

The ADP2300/ADP2301 feature a precision enable circuit that has a 1.2 V reference voltage with 100 mV hysteresis. When the voltage at the EN pin is greater than 1.2 V, the part is enabled. If the EN voltage falls below 1.1 V, the chip is disabled. The precision enable threshold voltage allows the ADP2300/ADP2301 to be easily sequenced from other input/output supplies. It can also be used as programmable UVLO input by using a resistive divider. An internal 1.2 µA pull-down current prevents errors if the EN pin is floating.

INTEGRATED SOFT START

The ADP2300/ADP2301 include internal soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time is typically fixed at 1460 µs for the ADP2300 and at 730 µs for the ADP2301.

CURRENT LIMIT

The ADP2300/ADP2301 include current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET switch. The positive current limit on the power switch limits the amount of current that can flow from the input to the output.

SHORT-CIRCUIT PROTECTION

The ADP2300/ADP2301 include frequency foldback to prevent output current runaway when there is a hard short on the output. The switching frequency is reduced when the voltage at the FB pin drops below a certain value, which allows more time for the inductor current to decline, but increases the ripple current while regulating the peak current. This results in a reduction in average output current and prevents output current runaway. The correlation between the switching frequency and the FB pin voltage is shown in Table 5.

Table 5. Correlation Between the Switching Frequency and the FB Pin Voltage

FB Pin Voltage	Switching Frequency
$V_{FB} \geq 0.6$ V	f_{SW}
0.6 V > V_{FB} > 0.2 V	½ f_{SW}
$V_{FB} \leq 0.2$ V	¼ f_{SW}

When a hard short ($V_{FB} \leq 0.2$ V) is removed, a soft start cycle is initiated to regulate the output back to its level during normal operation, which helps to limit the inrush current and prevent possible overshoot on the output voltage.

UNDERVOLTAGE LOCKOUT (UVLO)

The ADP2300/ADP2301 have fixed, internally set undervoltage lockout circuitry. If the input voltage drops below 2.4 V, the ADP2300/ADP2301 shut down and the MOSFET switch turns off. After the voltage rises again above 2.8 V, the soft start period is initiated, and the part is enabled.

THERMAL SHUTDOWN

If the ADP2300/ADP2301 junction temperature rises above 140°C, the thermal shutdown circuit disables the chip. Extreme junction temperature can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that when thermal shutdown occurs, the ADP2300/ADP2301 do not return to operation until the on-chip temperature drops below 125°C. After the devices recover from thermal shutdown, a soft start is initiated.

CONTROL LOOP

The ADP2300/ADP2301 are internally compensated to minimize external component count and cost. In addition, the built-in slope compensation helps to prevent subharmonic oscillations when the ADP2300/ADP2301 operate at a duty cycle greater than or close to 50%.

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP2300/ADP2301 are supported by the ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can request an unpopulated board through the tool.

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage of the ADP2300/ADP2301 is externally set by a resistive voltage divider from the output voltage to the FB pin, as shown in Figure 42. Suggested resistor values for the typical output voltage setting are listed in Table 6. The equation for the output voltage setting is

$$V_{OUT} = 0.800\ \text{V} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where:
V_{OUT} is the output voltage.
R_{FB1} is the feedback resistor from V_{OUT} to FB.
R_{FB2} is the feedback resistor from FB to GND.

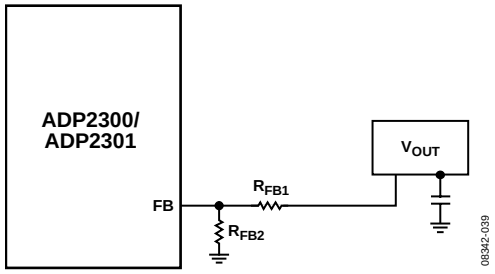

Figure 42. Programming the Output Voltage Using a Resistive Voltage Divider

Table 6. Suggested Values for Resistive Voltage Divider

V_{OUT} (V)	R_{FB1} (kΩ), ±1%	R_{FB2} (kΩ), ±1%
1.2	4.99	10
1.8	12.7	10.2
2.5	21.5	10.2
3.3	31.6	10.2
5.0	52.3	10

VOLTAGE CONVERSION LIMITATIONS

There are both lower and upper output voltage limitations for a given input voltage due to the minimum on time, the minimum off time, and the bootstrap dropout voltage.

The lower limit of the output voltage is constrained by the finite, controllable minimum on time, which can be as high as 135 ns for the worst case. By considering the variation of both the switching frequency and the input voltage, the equation for the lower limit of the output voltage is

$$V_{OUT(\min)} = t_{MIN\text{-}ON} \times f_{SW(\max)} \times (V_{IN(\max)} + V_D) - V_D$$

where:
$V_{IN(max)}$ is the maximum input voltage.
$f_{SW(max)}$ is the maximum switching frequency for the worst case.
$t_{MIN\text{-}ON}$ is the minimum controllable on time.
V_D is the diode forward drop.

The upper limit of the output voltage is constrained by the minimum controllable off time, which can be as high as 120 ns in the ADP2301 for the worst case. By considering the variation of both the switching frequency and the input voltage, the equation for the upper limit of the output voltage is

$$V_{OUT(\max)} = (1 - t_{MIN\text{-}OFF} \times f_{SW(\max)}) \times (V_{IN(\min)} + V_D) - V_D$$

where:
$V_{IN(min)}$ is the minimum input voltage.
$f_{SW(max)}$ is the maximum switching frequency for the worst case.
V_D is the diode forward drop.
$t_{MIN\text{-}OFF}$ is the minimum controllable off time.

In addition, the bootstrap circuit limits the minimum input voltage for the desired output due to internal dropout voltage. To attain stable operation at light loads and ensure proper startup for the prebias condition, the ADP2300/ADP2301 require the voltage difference between the input voltage and the regulated output voltage (or between the input voltage and the prebias voltage) to be greater than 2.1 V for the worst case. If the voltage difference is smaller, the bootstrap circuit relies on some minimum load current to charge the boost capacitor for startup. Figure 43 shows the typical required minimum input voltage vs. load current for the 3.3 V output voltage.

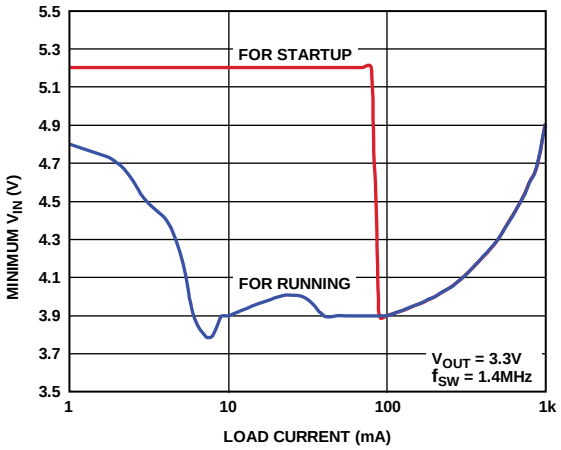

Figure 43. Minimum Input Voltage vs. Load Current

Based on three conversion limitations (the minimum on time, the minimum off time, and the bootstrap dropout voltage), Figure 44 shows the voltage conversion limitations.

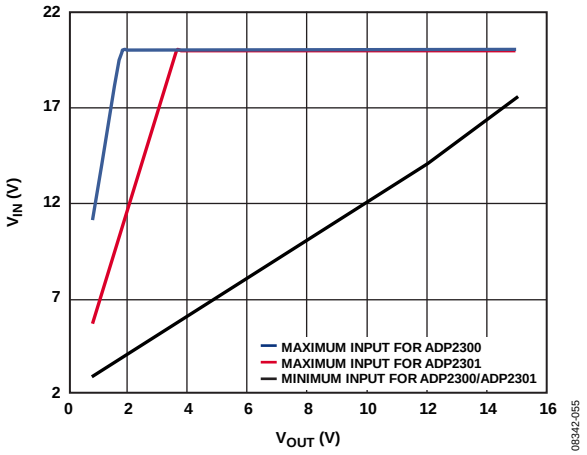

Figure 44. Voltage Conversion Limitations

LOW INPUT VOLTAGE CONSIDERATIONS

For low input voltage between 3 V and 5 V, the internal boot regulator cannot provide enough 5.0 V bootstrap voltage due to the internal dropout voltage. As a result, the increased MOSFET $R_{DS(ON)}$ reduces the available load current. To prevent this, add an external small-signal Schottky diode from a 5.0 V external bootstrap bias voltage. Because the absolute maximum rating between the BST and SW pins is 6.0 V, the bias voltage should be less than 5.5 V. Figure 45 shows the application diagram for the external bootstrap circuit.

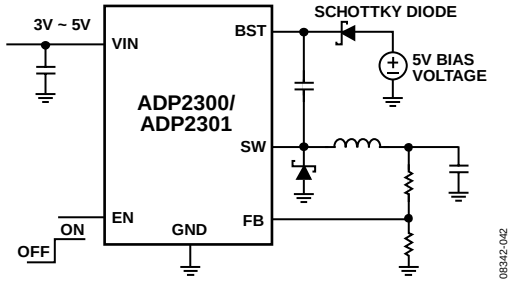

Figure 45. External Bootstrap Circuit for Low Input Voltage Application

PROGRAMMING THE PRECISION ENABLE

Generally, the EN pin can be easily tied to the VIN pin so that the device automatically starts up when the input power is applied. However, the precision enable feature allows the ADP2300/ ADP2301 to be used as a programmable UVLO by connecting a resistive voltage divider to V_{IN}, as shown in Figure 46. This configuration prevents the start-up problems that can occur when V_{IN} ramps up slowly in soft start with a relatively high load current.

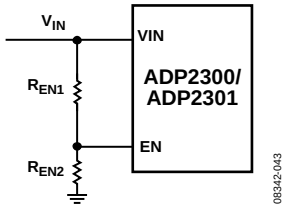

Figure 46. Precision Enable Used as a Programmable UVLO

The precision enable feature also allows the ADP2300/ADP2301 to be sequenced precisely by using a resistive voltage divider with another dc-to-dc output supply, as shown in Figure 47.

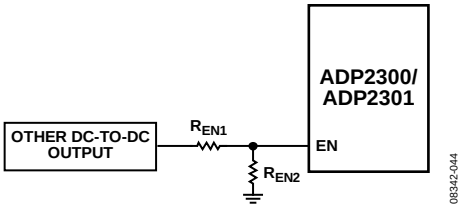

Figure 47. Precision Enable Used as a Sequencing Control from Another DC-to-DC Output

With a 1.2 µA pull-down current on the EN pin, the equation for the start-up voltage in Figure 46 and Figure 47 is

$$V_{STARTUP} = \left(\frac{1.2\ \text{V}}{R_{EN2}} + 1.2\ \mu\text{A} \right) \times R_{EN1} + 1.2\ \text{V}$$

where:

$V_{STARTUP}$ is the start-up voltage to enable the chip.
R_{EN1} is the resistor from the dc source to EN.
R_{EN2} is the resistor from EN to GND.

INDUCTOR

The high switching frequency of the ADP2300/ADP2301 allows the use of small inductors. For best performance, use inductor values between 2 µH and 10 µH for ADP2301, and use inductor values between 2 µH and 22 µH for ADP2300.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$\Delta I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{L \times f_{sw}} \times \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D} \right)$$

where:
f_{SW} is the switching frequency.
L is the inductor value.
V_D is the diode forward drop.
V_{IN} is the input voltage.
V_{OUT} is the output voltage.

Inductors of smaller values are usually smaller in size and less expensive, but increase the ripple current and the output voltage ripple. As a guideline, the inductor peak-to-peak current ripple should typically be set to 30% of the maximum load current for optimal transient response and efficiency. Therefore, the inductor value is calculated using the following equation:

$$L = \frac{\left(V_{IN} - V_{OUT}\right)}{0.3 \times I_{LOAD(\max)} \times f_{sw}} \times \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D} \right)$$

where $I_{LOAD(max)}$ is the maximum load current.

The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(\max)} + \frac{\Delta I_{RIPPLE}}{2}$$

The minimum current rating of the inductor must be greater than the inductor peak current. For ferrite core inductors with a quick saturation characteristic, the inductor saturation current rating should be higher than the switch current-limit threshold to prevent the inductor from reaching its saturation point. Be sure to validate the worst-case condition, in which there is a shorted output, over the intended temperature range.

Inductor conduction losses are caused by the flow of current through the inductor, which is associated with the internal dc resistance (DCR). Larger sized inductors have smaller DCR and, therefore, may reduce inductor conduction losses. However, inductor core losses are also related to the core material and the ac flux swing, which are affected by the peak-to-peak inductor ripple current. Because the ADP2300/ADP2301 are high switching frequency regulators, shielded ferrite core materials are recommended for their low core losses and low EMI. Some recommended inductors are shown in Table 7.

Table 7. Recommended Inductors

Vendor	Value (µH)	Part No.	DCR (mΩ)	I_{SAT} (A)	Dimensions L × W × H (mm)
Coilcraft	4.7	LPS6225-472MLC	65	3.1	6.0 × 6.0 × 2.4
	6.8	LPS6225-682MLC	95	2.7	6.0 × 6.0 × 2.4
	10	LPS6225-103MLC	105	2.1	6.0 × 6.0 × 2.4
Sumida	4.7	CDRH5D28RHPNP-4R7N	43	3.7	6.2 × 6.2 × 3.0
	4.7	CDRH5D16NP-4R7N	64	2.15	5.8 × 5.8 × 1.8
	6.8	CDRH5D28RHPNP-6R8N	61	3.1	6.2 × 6.2 × 3.0
	6.8	CDRH5D16NP-6R8N	84	1.8	5.8 × 5.8 × 1.8
	10	CDRH5D28RHPNP-100M	93	2.45	6.2 × 6.2 × 3.0
Cooper Bussmann	4.7	SD53-4R7-R	39	2.1	5.2 × 5.2 × 3.0
	6.8	SD53-6R8-R	59	1.85	5.2 × 5.2 × 3.0
	10	DR73-100-R	65	2.47	7.6 × 7.6 × 3.5
Toko	4.7	B1077AS-4R7N	34	2.6	7.6 × 7.6 × 4.0
	6.8	B1077AS-6R8N	40	2.3	7.6 × 7.6 × 4.0
	10	B1077AS-100M	58	1.8	7.6 × 7.6 × 4.0
TDK	4.7	VLC5045T-4R7M	34	3.3	5.0 × 5.0 × 4.5
	6.8	VLC5045T-6R8M	46	2.7	5.0 × 5.0 × 4.5
	10	VLC5045T-100M	66	2.1	5.0 × 5.0 × 4.5

CATCH DIODE

The catch diode conducts the inductor current during the off time of the internal MOSFET. The average current of the diode in normal operation is, therefore, dependent on the duty cycle of the regulator as well as the output load current.

$$I_{DIODE(AVG)} = \left(1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}\right) \times I_{LOAD(\max)}$$

where V_D is the diode forward drop.

The only reason to select a diode with a higher current rating than necessary in normal operation is for the worst-case condition, in which there is a shorted output. In this case, the diode current increases up to the typical peak current-limit threshold. Be sure to consult the diode data sheet to ensure that the diode can operate well within the thermal and electrical limits.

The reverse breakdown voltage rating of the diode must be higher than the highest input voltage and allow an appropriate margin for the ringing that may be present on the SW node. A Schottky diode is recommended for best efficiency because it has a low forward voltage drop and fast switching speed. Table 8 provides a list of recommended Schottky diodes.

Table 8. Recommended Schottky Diodes

Vendor	Part No.	V_{RRM} (V)	I_{AVG} (A)
ON Semiconductor	MBRS230LT3	30	2
	MBRS240LT3	40	2
Diodes Inc.	B230A	30	2
	B240A	40	2
Vishay	SL23	30	2
	SS24	40	2

INPUT CAPACITOR

The input capacitor must be able to support the maximum input operating voltage and the maximum rms input current. The maximum rms input current flowing through the input capacitor is $I_{LOAD(max)}/2$. Select an input capacitor capable of withstanding the rms input current for an application's maximum load current using the following equation:

$$I_{IN(RMS)} = I_{LOAD(\max)} \times \sqrt{D \times (1 - D)}$$

where D is the duty cycle and is equal to

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

The recommended input capacitor is ceramic with X5R or X7R dielectrics due to its low ESR and small temperature coefficients. A capacitance of 10 µF should be adequate for most applications. To minimize supply noise, place the input capacitor as close to the VIN pin of the ADP2300/ADP2301 as possible.

OUTPUT CAPACITOR

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the regulator. The ADP2300/ADP2301 are designed to operate with small ceramic capacitors that have low equivalent series resistance (ESR) and equivalent series inductance (ESL) and are, therefore, easily able to meet stringent output voltage ripple specifications.

When the regulator operates in forced continuous conduction mode, the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor.

$$\Delta V_{RIPPLE} = \Delta I_{RIPPLE} \times \left(\frac{1}{8 \times f_{sw} \times C_{OUT}} + ESR_{C_{OUT}}\right)$$

Capacitors with lower ESR are preferable to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}$$

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. X5R or X7R dielectrics are recommended for best performance, due to their low ESR and small temperature coefficients. Y5V and Z5U dielectrics are not recommended because of their poor temperature and dc bias characteristics.

In general, most applications using the ADP2301 (1.4 MHz switching frequency) require a minimum output capacitor value of 10 µF, whereas most applications using the ADP2300 (700 kHz switching frequency) require a minimum output capacitor value of 20 µF. Some recommended output capacitors for $V_{OUT} \leq 5.0$ V are listed in Table 9.

Table 9. Recommended Capacitors for $V_{OUT} \leq 5.0$ V

Vendor	Value	Part No.	Dimensions L × W × H (mm)
Murata	10 µF, 6.3 V	GRM31MR60J106KE19	3.2 × 1.6 × 1.15
	22 µF, 6.3 V	GRM31CR60J226KE19	3.2 × 1.6 × 1.6
TDK	10 µF, 6.3 V	C3216X5R0J106K	3.2 × 1.6 × 1.6
	22 µF, 6.3 V	C3216X5R0J226M	3.2 × 1.6 × 0.85

THERMAL CONSIDERATIONS

The ADP2300/ADP2301 store the value of the inductor current only during the on time of the internal MOSFET. Therefore, a small amount of power is dissipated inside the ADP2300/ADP2301 package, which reduces thermal constraints.

However, when the application is operating under maximum load with high ambient temperature and high duty cycle, the heat dissipated within the package may cause the junction temperature of the die to exceed the maximum junction temperature of 125°C. If the junction temperature exceeds 140°C, the regulator goes into thermal shutdown and recovers when the junction temperature drops below 125°C.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as indicated in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
T_R is the rise in temperature of the package.
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package.
P_D is the power dissipation in the package.

DESIGN EXAMPLE

This section provides the procedures to select the external components, based on the example specifications listed in Table 10. The schematic for this design example is shown in Figure 48.

Table 10. Step-Down DC-to-DC Regulator Requirements

Parameter	Specification	Additional Requirements
Input Voltage, V_{IN}	12.0 V ± 10%	None
Output Voltage, V_{OUT}	3.3 V, 1.2 A, 1% V_{OUT} ripple at CCM mode	None
Programmable UVLO Voltage	V_{IN} start-up voltage approximately 7.8 V	None

SWITCHING FREQUENCY SELECTION

Select the switching frequency—700 kHz (ADP2300) or 1.4 MHz (ADP2301)—using the conversion limitation curve shown in Figure 44 to assess the conversion limitations (the minimum on time, the minimum off time, and the bootstrap dropout voltage).

For example, in Figure 44 V_{IN} = 12 V ± 10% is within the conversion limitation for both the 700 kHz and 1.4 MHz switching frequencies for an output voltage of 3.3 V, but choosing the 1.4 MHz switching frequency provides the smallest sized solution. If higher efficiency is required, choose the 700 kHz option; however, the PCB footprint area of the regulator will be larger because of the bigger inductor and output capacitors.

CATCH DIODE SELECTION

Select the catch diode. A Schottky diode is recommended for best efficiency because it has a low forward voltage drop and faster switching speed. The average current of the catch diode in normal operation, with a typical Schottky diode forward voltage, can be calculated using the following equation:

$$I_{DIODE(AVG)} = \left(1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}\right) \times I_{LOAD(\max)}$$

where:
V_{OUT} = 3.3 V.
V_{IN} = 12 V.
$I_{LOAD(max)}$ = 1.2 A.
V_D = 0.4 V.

Therefore, $I_{DIODE(AVG)}$ = 0.85 A.

However, for the worst-case condition, in which there is a shorted output, the diode current would be increased to 2 A typical, determined by the peak switch current limit (see Table 1). In this case, selecting a B230A, 2.0 A/30 V surface-mount Schottky diode would result in more reliable operation.

INDUCTOR SELECTION

Select the inductor by using the following equation:

$$L = \frac{(V_{IN} - V_{OUT})}{0.3 \times I_{LOAD(\max)} \times f_{sw}} \times \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

where:
V_{OUT} = 3.3 V.
V_{IN} = 12 V.
$I_{LOAD(max)}$ = 1.2 A.
V_D = 0.4 V.
f_{SW} = 1.4 MHz.

This results in L = 5.15 µH. The closest standard value is 4.7 µH; therefore, ΔI_{RIPPLE} = 0.394 A.

The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(\max)} + \frac{\Delta I_{RIPPLE}}{2}$$

where:
$I_{LOAD(max)}$ = 1.2 A.
ΔI_{RIPPLE} = 0.394 A.

Therefore, the calculated peak current for the inductor is 1.397 A. However, to protect the inductor from reaching its saturation point in the current-limit condition, the inductor should be rated for at least a 2.0 A saturation current for reliable operation.

OUTPUT CAPACITOR SELECTION

Select the output capacitor based on the output voltage ripple requirement, according to the following equation:

$$\Delta V_{RIPPLE} = \Delta I_{RIPPLE} \times \left(\frac{1}{8 \times f_{sw} \times C_{OUT}} + ESR_{C_{OUT}}\right)$$

where:
ΔI_{RIPPLE} = 0.394 A.
f_{SW} = 1.4 MHz.
ΔV_{RIPPLE} = 33 mV.

If the ESR of the ceramic capacitor is 3 mΩ, then C_{OUT} = 1.2 µF.

Because the output capacitor is one of the two external components that control the loop stability, most applications using the ADP2301 (1.4 MHz switching frequency) require a minimum 10 µF capacitance to ensure stability. According to the recommended external components in Table 11, choose 22 µF with a 6.3 V voltage rating for this example.

RESISTIVE VOLTAGE DIVIDER SELECTION

To select the appropriate resistive voltage divider, first calculate the output feedback resistive voltage divider, and then calculate the resistive voltage divider for the programmable V_{IN} start-up voltage.

The output feedback resistive voltage divider is

$$V_{OUT} = 0.800\ \text{V} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

For the 3.3 V output voltage, choose R_{FB1} = 31.6 kΩ and R_{FB2} = 10.2 kΩ as the feedback resistive voltage divider, according to the recommended values in Table 11.

The resistive voltage divider for the programmable V_{IN} start-up voltage is

$$V_{STARTUP} = \left(\frac{1.2\ \text{V}}{R_{EN2}} + 1.2\ \mu\text{A}\right) \times R_{EN1} + 1.2\ \text{V}$$

If $V_{STARTUP}$ = 7.8 V, choose R_{EN2} = 10.2 kΩ, and then calculate R_{EN1}, which in this case is 56 kΩ.

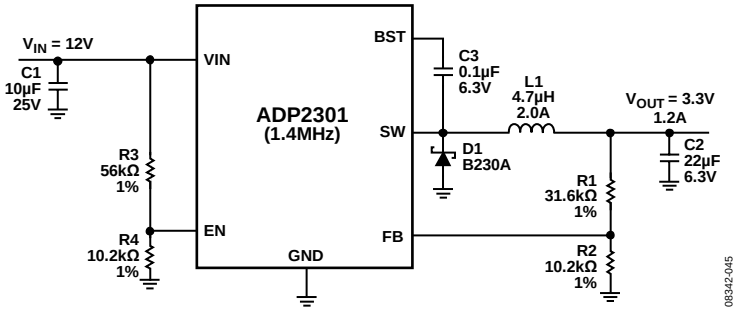

Figure 48. Schematic for the Design Example

Table 11. Recommended External Components for Typical Applications at 1.2 A Output Load

Part Number	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	L (µH)	C_{OUT} (µF)	R_{FB1} (kΩ), ±1%	R_{FB2} (kΩ), ±1%
ADP2300 (700 kHz)	18	3.3	1.2	10	22	31.6	10.2
	18	5.0	1.2	15	22	52.3	10
	12	1.2	1.2	6.8	2 × 22	4.99	10
	12	1.8	1.2	6.8	2 × 22	12.7	10.2
	12	2.5	1.2	10	22	21.5	10.2
	12	3.3	1.2	10	22	31.6	10.2
	12	5.0	1.2	10	22	52.3	10
	9	3.3	1.2	10	22	31.6	10.2
	9	5.0	1.2	10	22	52.3	10
	5	1.8	1.2	4.7	2 × 22	12.7	10.2
	5	2.5	1.2	4.7	22	21.5	10.2
ADP2301 (1.4 MHz)	18	3.3	1.2	4.7	22	31.6	10.2
	18	5.0	1.2	6.8	10	52.3	10
	12	2.5	1.2	4.7	22	21.5	10.2
	12	3.3	1.2	4.7	22	31.6	10.2
	12	5.0	1.2	4.7	10	52.3	10
	9	3.3	1.2	4.7	22	31.6	10.2
	9	5.0	1.2	4.7	10	52.3	10
	5	1.8	1.2	2.2	2 × 22	12.7	10.2
	5	2.5	1.2	2.2	22	21.5	10.2

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential to obtain the best performance from the ADP2300/ADP2301. Poor layout can affect the regulation and stability, as well as the electromagnetic interface (EMI) and electromagnetic compatibility (EMC) performance. A PCB layout example is shown in Figure 50. Refer to the following guidelines for a good PCB layout:

- Place the input capacitor, inductor, catch diode, output capacitor, and bootstrap capacitor close to the IC using short traces.
- Ensure that the high current loop traces are as short and wide as possible. The high current path is shown in Figure 49.
- Maximize the size of ground metal on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Minimize the length of the FB trace connecting the top of the feedback resistive voltage divider to the output. In addition, keep these traces away from the high current traces and the switch node to avoid noise pickup.

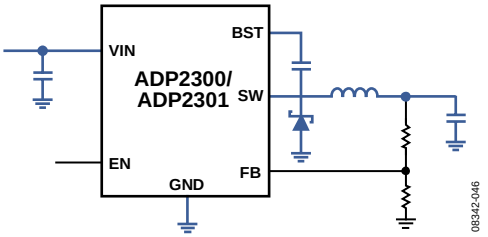

Figure 49. Typical Application Circuit with High Current Traces Shown in Blue

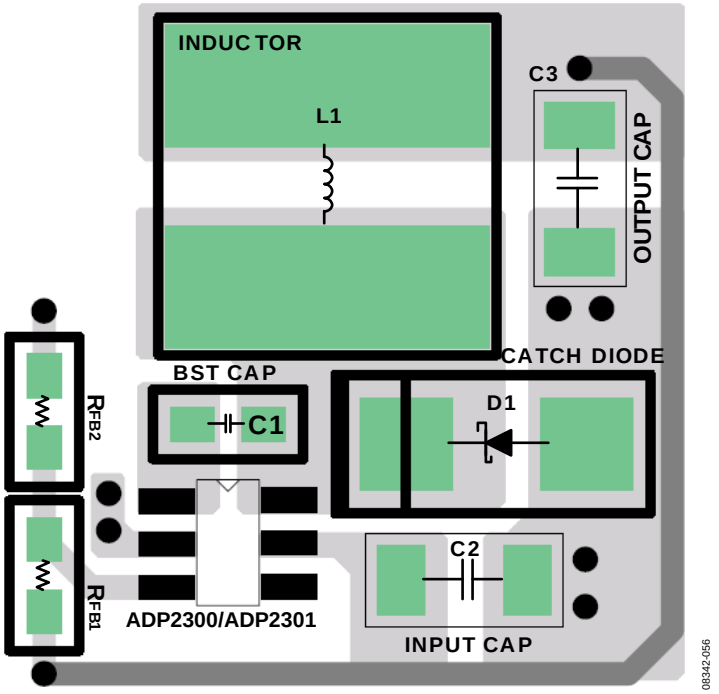

Figure 50. Recommended PCB Layout for the ADP2300/ADP2301

TYPICAL APPLICATION CIRCUITS

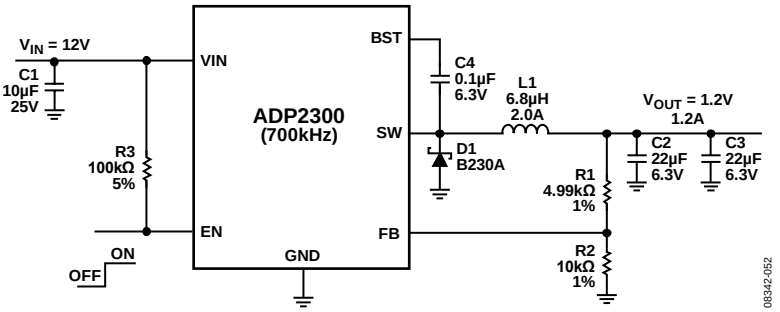

Figure 51. ADP2300—700 kHz Typical Application, V_{IN} = 12 V, V_{OUT} = 1.2 V/1.2 A with External Enabling

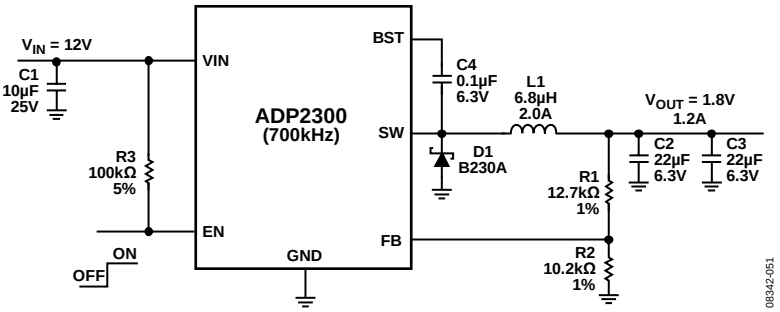

Figure 52. ADP2300—700 kHz Typical Application, V_{IN} = 12 V, V_{OUT} = 1.8 V/1.2 A with External Enabling

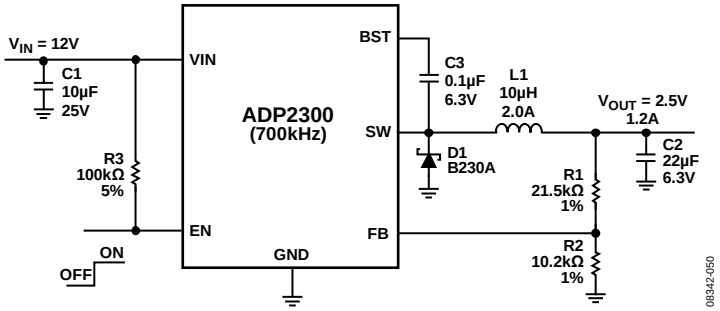

Figure 53. ADP2300—700 kHz Typical Application, V_{IN} = 12 V, V_{OUT} = 2.5 V/1.2 A with External Enabling

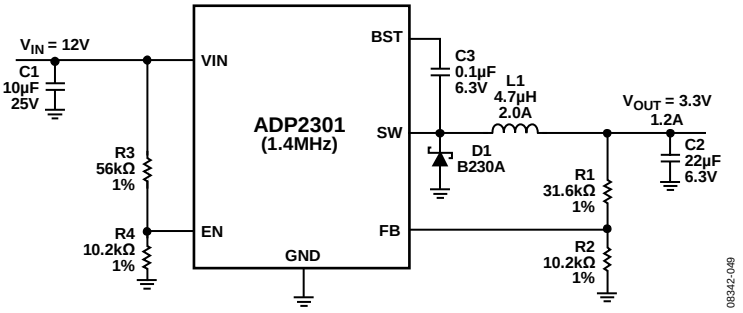

Figure 54. ADP2301—1.4 MHz Typical Application, V_{IN} = 12 V, V_{OUT} = 3.3 V/1.2 A (with Programmable 7.8 V Start-Up Input Voltage)

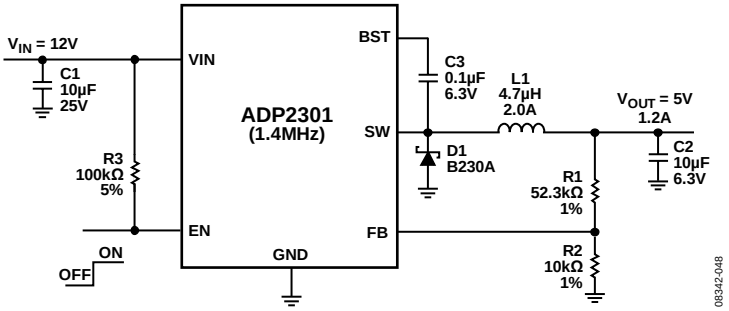

Figure 55. ADP2301—1.4 MHz Typical Application, V_{IN} = 12 V, V_{OUT} = 5.0 V/1.2 A with External Enabling

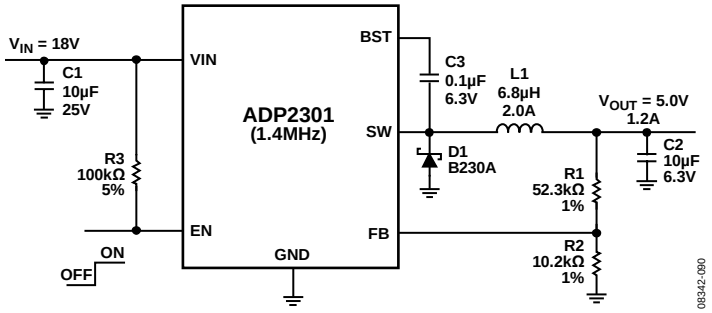

Figure 56. ADP2301—1.4 MHz Typical Application, V_{IN} = 18 V, V_{OUT} = 5.0 V/1.2 A with External Enabling

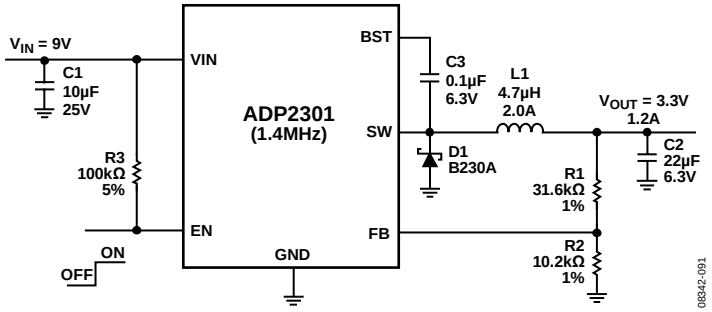

Figure 57. ADP2301—1.4 MHz Typical Application, V_{IN} = 9 V, V_{OUT} = 3.3 V/1.2 A with External Enabling

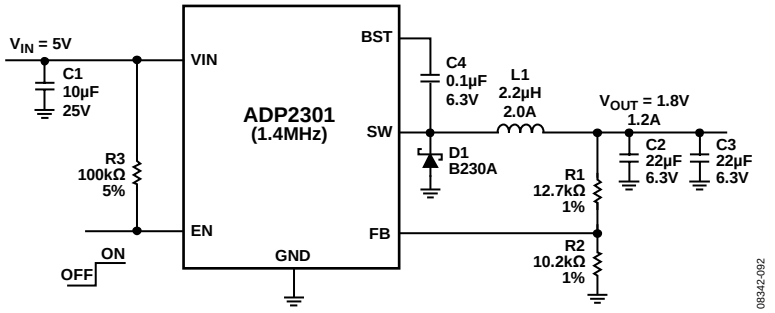

Figure 58. ADP2301—1.4 MHz Typical Application, V_{IN} = 5 V, V_{OUT} = 1.8 V/1.2 A with External Enabling

OUTLINE DIMENSIONS

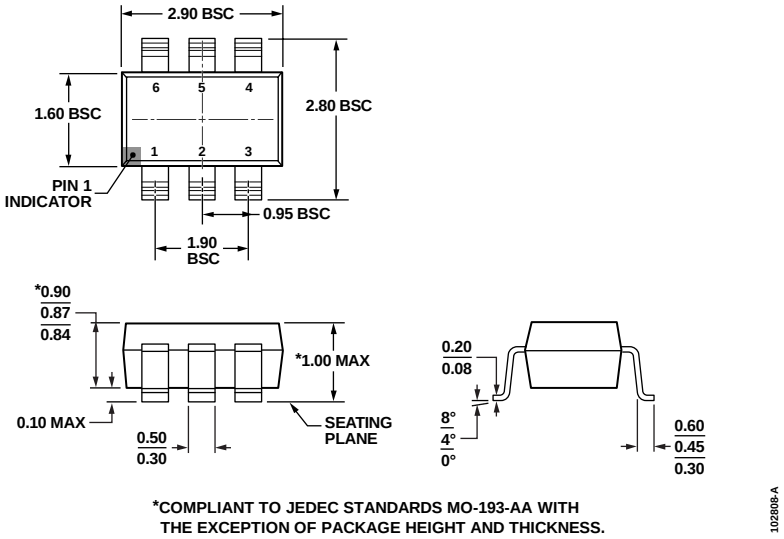

Figure 59. 6-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Switching Frequency	Temperature Range	Package Description	Package Option	Branding
ADP2300AUJZ-R2	700 kHz	−40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	L87
ADP2300AUJZ-R7	700 kHz	−40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	L87
ADP2300-EVALZ			Evaluation Board		
ADP2301AUJZ-R2	1.4 MHz	−40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	L86
ADP2301AUJZ-R7	1.4 MHz	−40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	L86
ADP2301-EVALZ			Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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D08342-0-11/12(C)

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