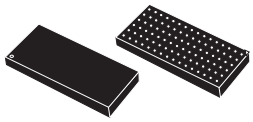
74ACT32701

16-BIT D-TYPE LATCH PULS 16-BIT BUS BUFFER WITH 3-STATE OUTPUTS (NON INVERTED)

PRELIMINARY DATA

- HIGH SPEED: t_{PD} = 4.8ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 8µA(MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX.)
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 24mA (MIN) at V_{CC} = 4.5V
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 4.5V to 5.5V
- FUNCTION COMPATIBLE WITH SERIES 16373 AND 16245 (244)
- IMPROVED LATCH-UP IMMUNITY
- IMPROVED ESD IMMUNITY



LFBGA96
(Top and Bottom view)

ORDER CODES

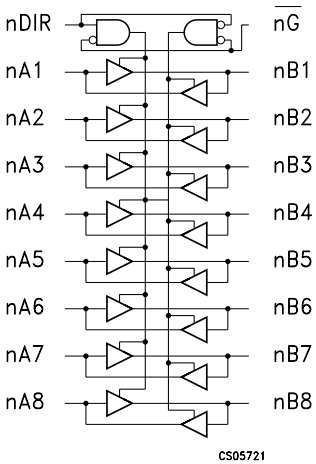
PACKAGE	TRAY	T & R
LFBGA96	74ACT32701LB	74ACT32701LBR

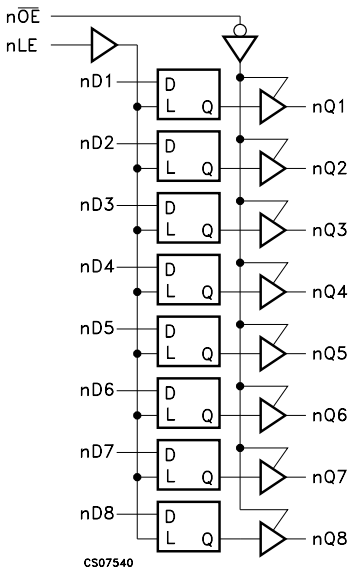
DESCRIPTION

The 74ACT16244 is a low voltage CMOS 16-BIT D-TYPE LATCH and 16 BIT BUS TRANSCEIVER with 3-STATE output non inverting fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.
Both functions can be used as 16 bit or dual octal devices, so the 16 bit transceiver can be used ad 8 bit bus buffer plus 8 bit transceiver, or only 16 bit buffer in select direction.

This device can be used to integrate in one chip the internal logic component required to STV0701 to work ad P.O.D. interface in Digital TV application. It is ideal for low power and high speed 4.5 to 5.5. applications.
All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

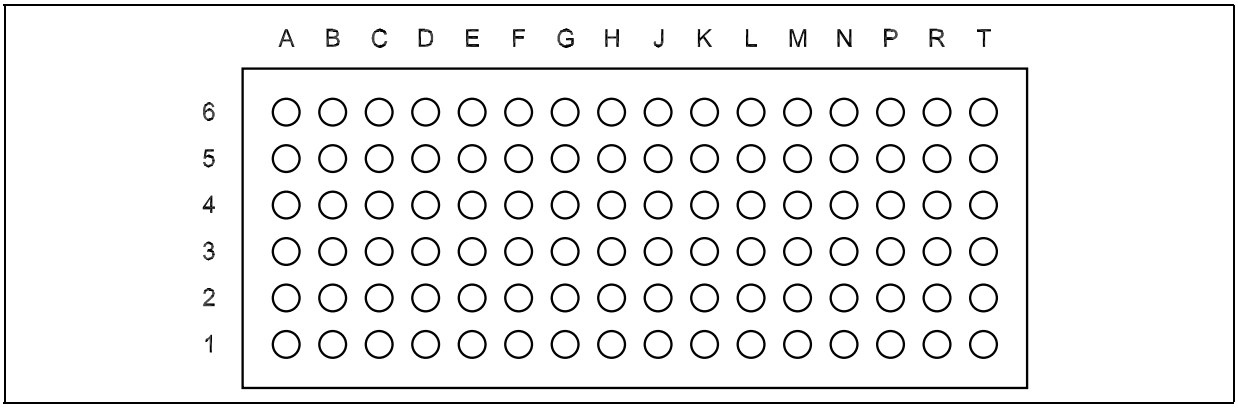
LOGIC DIAGRAM





This is preliminary information on a new product now in development are or undergoing evaluation. Details subject to change without notice.

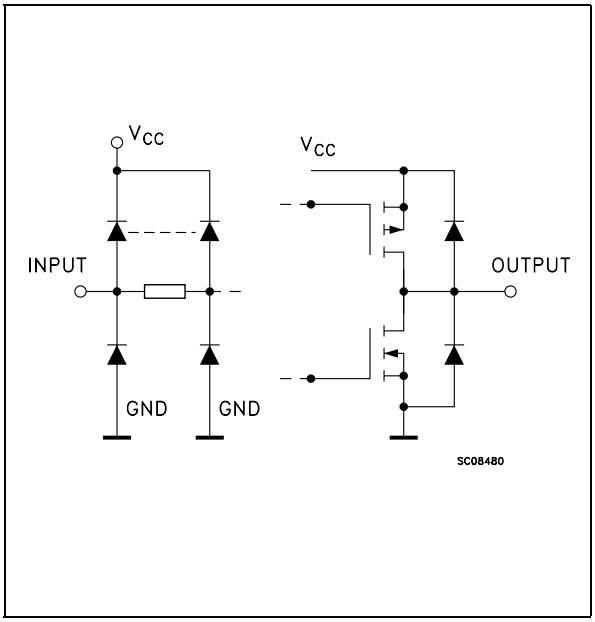
PIN CONNECTION (Top view)



TERMINAL ASSIGNMENT

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3A2	3A4	3A6	3A8	4A2	4A4	4A6	4A7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3A1	3A3	3A5	3A7	4A1	4A3	4A5	4A8
4	1LE	GND	V_{CC}	GND	GND	V_{CC}	GND	2LE	$3\overline{G}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{G}$
3	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$2\overline{OE}$	3DIR	GND	V_{CC}	GND	GND	V_{CC}	GND	4DIR
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2B8	3B1	3B3	3B5	3B7	4B1	4B3	4B5	4B8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2B7	3B2	3B4	3B6	3B8	4B2	4B4	4B6	4B7

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE (each 8bit section of 16bit Latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

TRUTH TABLE (each 8bit section of 16bit Transceiver)

INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to 85	°C
dt/dv	Input Rise and Fall Time V_{CC} = 4.5 to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5	V_O = 0.1 V or V_{CC}-0.1V	2.0			2.0		V
		5.5		2.0			2.0		
V_{IL}	Low Level Input Voltage	4.5	V_O = 0.1 V or V_{CC}-0.1V			0.8		0.8	
		5.5				0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	I_O=-50 µA	4.4	4.49		4.4		V
		5.5	I_O=-50 µA	5.4	5.49		5.4		
		4.5	I_O=-24 mA	3.86			3.76		
		5.5	I_O=-24 mA	4.86			4.76		
V_{OL}	Low Level Output Voltage	4.5	I_O=50 µA		0.001	0.1		0.1	V
		5.5	I_O=50 µA		0.001	0.1		0.1	
		4.5	I_O=24 mA			0.36		0.44	
		5.5	I_O=24 mA			0.36		0.44	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND			± 0.1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	5.5	V_I = V_{IH} or V_{IIL} V_O = V_{CC} or GND			± 0.5		± 5	µA
I_{CCT}	Max I_{CC}/Input	5.5	V_I = V_{CC} - 2.1V		0.9			1	mA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			8		80	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	5.5	V_{OLD} = 1.65 V max					75	mA
I_{OHD}			V_{OHD} = 3.85 V min.					-75	mA

1) Maximum test duration 2ms, one output loaded at time
2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time	5.0(*)		2.0	3.3	5.0	2.0	6.0	ns
t_{PHL}				3.0	4.8	6.5	3.0	8.0	
t_{PZL}	Output Enable Time	5.0(*)		4.0	6.5	8.7	4.0	9.7	ns
t_{PZH}				3.0	5.5	7.7	3.0	8.8	
t_{PLZ}	Output Disable Time	5.0(*)		4.0	6.0	8.0	4.0	9.2	ns
t_{PHZ}				3.0	4.6	6.4	3.0	7.3	

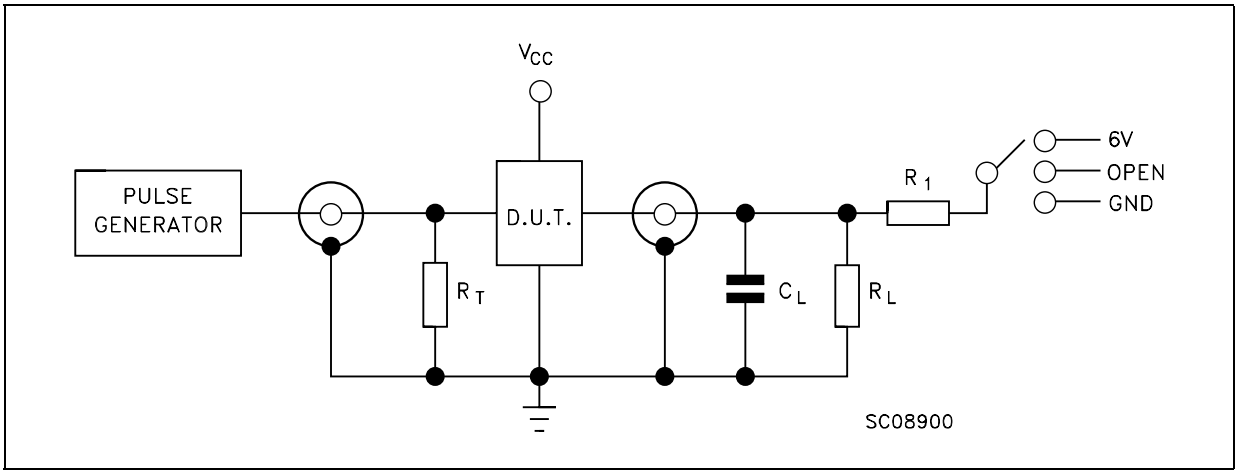
(*) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			3.6				pF
C_{OUT}	Output Capacitance	5.0			11				pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	f_{IN} = 10MHz		42				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)

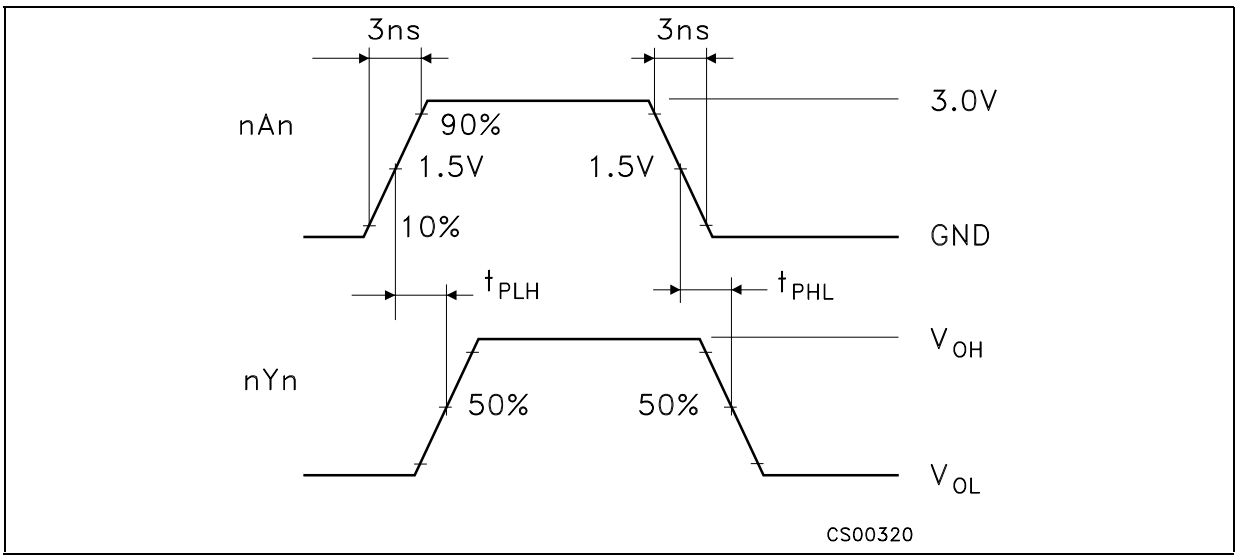
TEST CIRCUIT



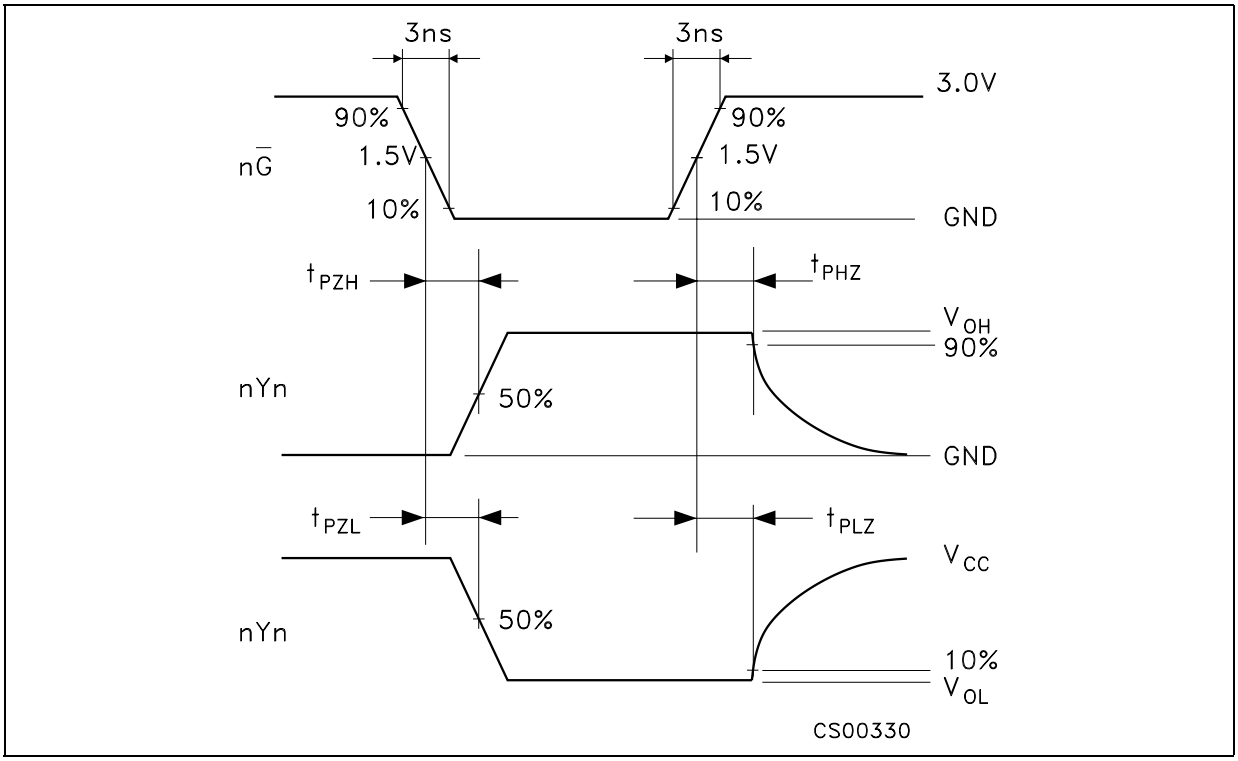
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$2V_{CC}$
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

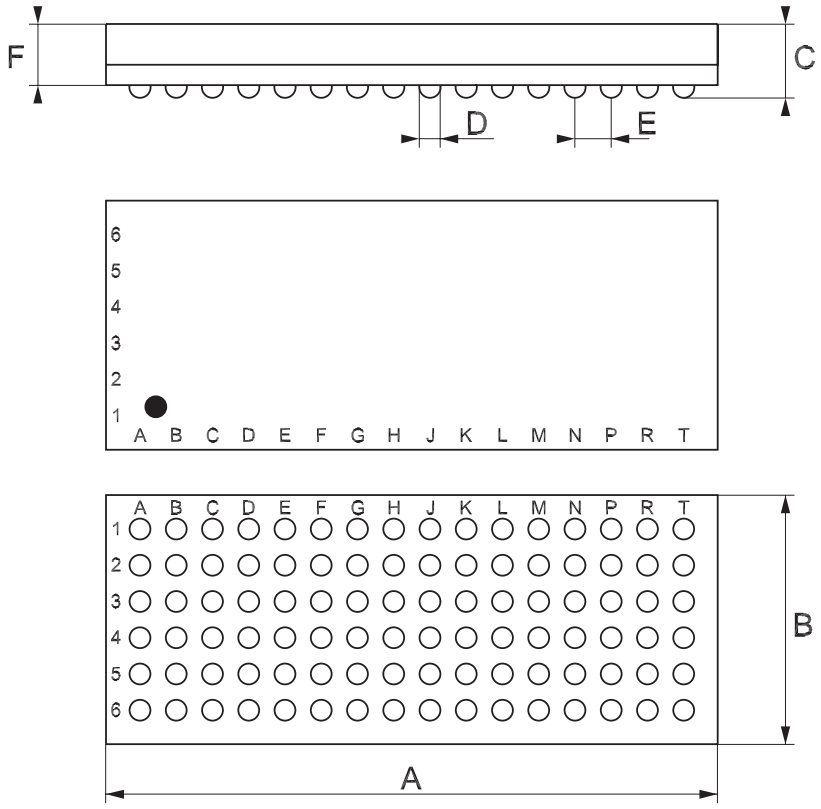


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



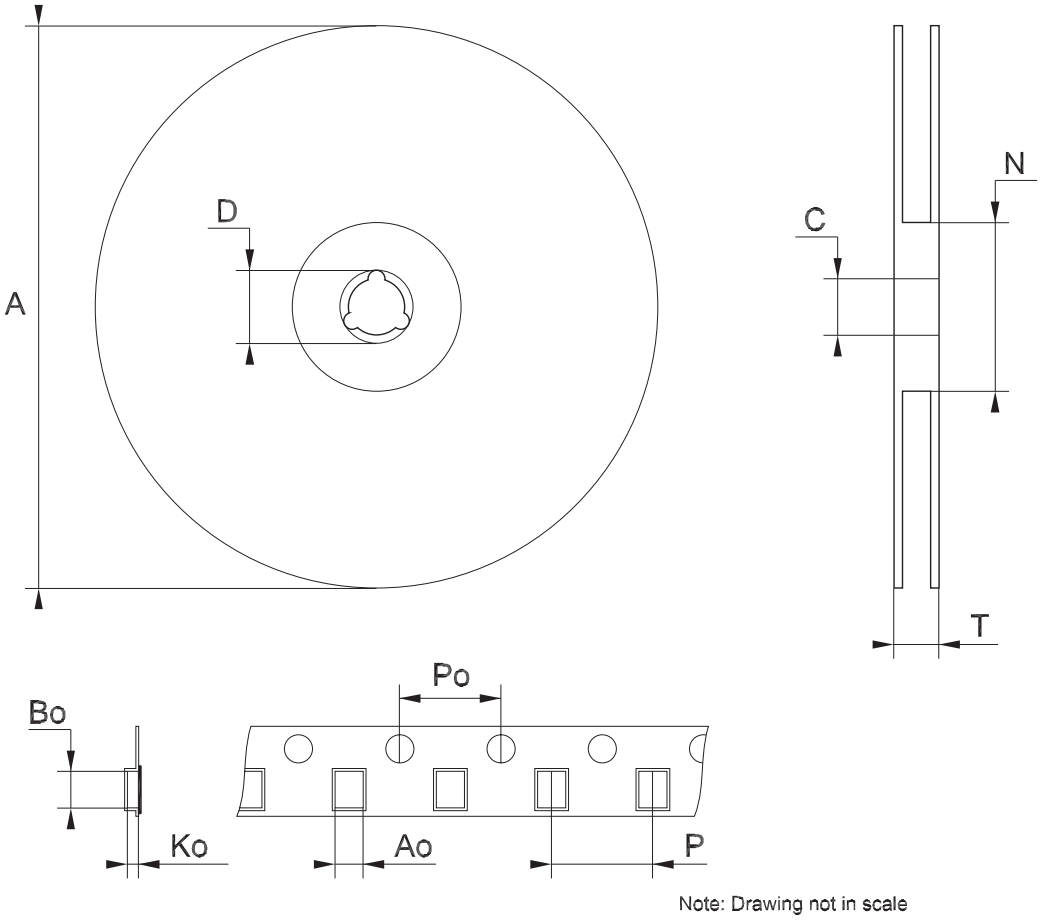
LFBGA96 MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	13.40		13.60	527.5		535.4
B	5.40		5.60	212.6		220.5
C			1.6			63.0
D		0.5			19.7	
E		0.8			31.5	
F	0.85			33.5		



Tape & Reel LFBGA96 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.196
Ao	5.8		6.0	0.228		0.236
Bo	13.8		14.0	0.543		0.551
Ko	2.1		2.3	0.083		0.091
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

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