FAIRCHILD SEMICONDUCTOR™

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# DM74AS280
# 9-Bit Parity Generator/Checker

## General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

The DM74AS280 can be used to upgrade the performance of most systems utilizing the ’180 parity generator/checker. Although the DM74AS280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and no internal connection at pin 3. This permits the DM74AS280 to be substituted for the ’180 in existing designs to produce identical function even if DM74AS280s are mixed with existing ’180s.

## Features

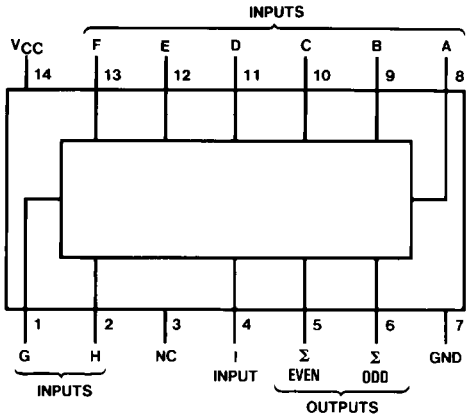
- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for N-bits
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and $V_{CC}$ range

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74AS280M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74AS280N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

## Connection Diagram




## Function Table

| Number of Inputs (A thru I) that are HIGH | Outputs | |
|---|---|---|
| | ∑Even | ∑Odd |
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

L = LOW State
H = HIGH State

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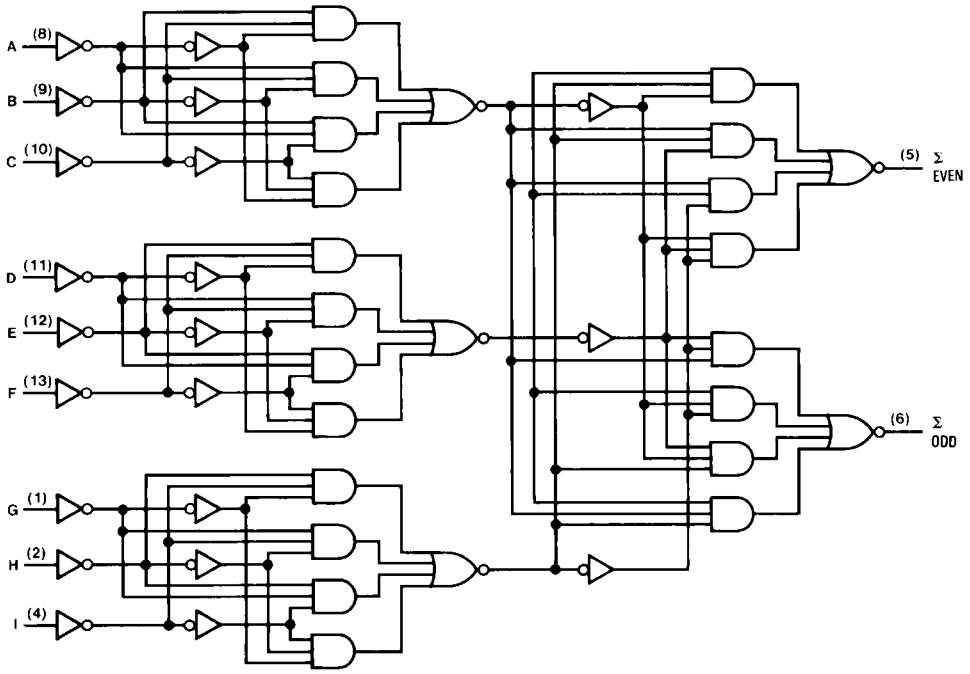
## Logic Diagram



## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Typical $\theta_{JA}$ | |
| N Package | 77.0°C/W |
| M Package | 108.0°C/W |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | HIGH Level Input Voltage | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | −2 | mA |
| $I_{OL}$ | LOW Level Output Current | | | 20 | mA |
| $T_A$ | Free-Air Operating Temperature | 0 | | 70 | °C |

## Electrical Characteristics

Over recommended free-air temperature range. All typical values are measured at $V_{CC}$ = 5V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IK}$ | Input Clamp Voltage | $V_{CC}$ = 4.5V, $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −2 mA, $V_{CC}$ = 4.5V to 5.5V | $V_{CC}$ − 2 | | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = 4.5V, $I_{OL}$ = Max | | 0.35 | 0.5 | V |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = 5.5V, $V_{IH}$ = 7V | | | 0.1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = 5.5V, $V_{IH}$ = 2.7V | | | 20 | μA |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = 5.5V, $V_{IL}$ = 0.4V | | | −0.5 | mA |
| $I_O$ | Output Drive Current | $V_{CC}$ = 5.5V, $V_O$ = 2.25V | −30 | | −112 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5.5V | | 25 | 40 | mA |

## Switching Characteristics

over recommended operating free air temperature range

| Symbol | Parameter | Conditions | From | To | Min | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, LOW-to-HIGH Level Output | $V_{CC}$ = 4.5V to 5.5V, $C_L$ = 50 pF, $R_L$ = 500Ω | Data | ∑Even | 3 | 12 | ns |
| $t_{PHL}$ | Propagation Delay Time, HIGH-to-LOW Level Output | | | | 3 | 11 | ns |
| $t_{PLH}$ | Propagation Delay Time, LOW-to-HIGH Level Output | | Data | ∑Odd | 3 | 12 | ns |
| $t_{PHL}$ | Propagation Delay Time, HIGH-to-LOW Level Output | | | | 3 | 11.5 | ns |

## Typical Applications

Three DM74AS280s can be used to implement a 25-line parity generator/checker.

As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (AS86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.

Longer word lengths can be implemented by cascading DM74AS280s. As shown in Figure 2, parity can be generated for word lengths up to 81 bits.

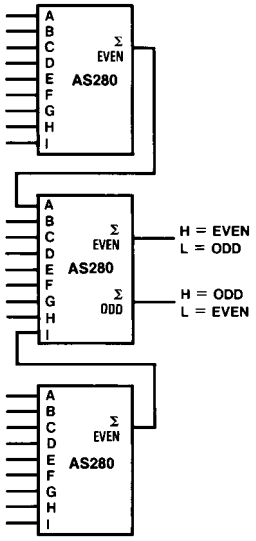



**FIGURE 1. 25-Line Parity/Generator Checker**

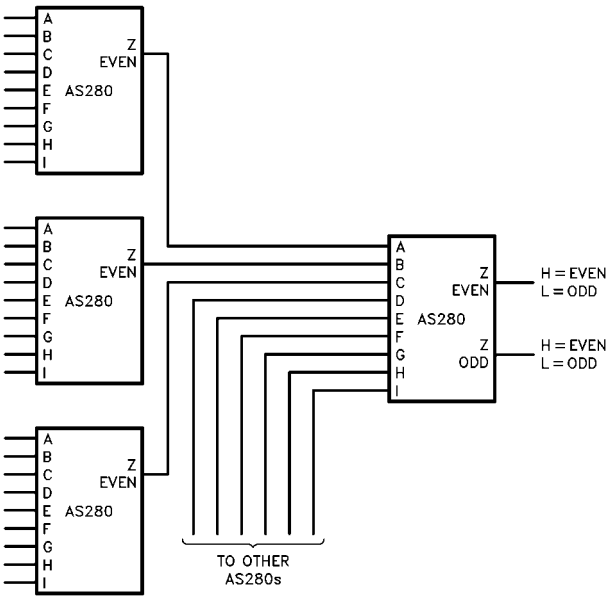
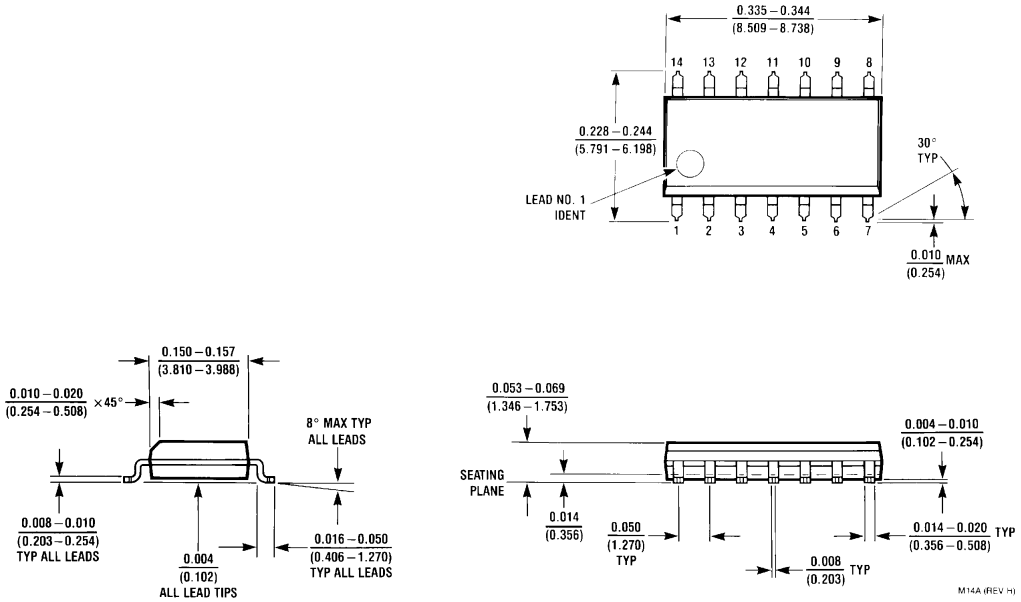


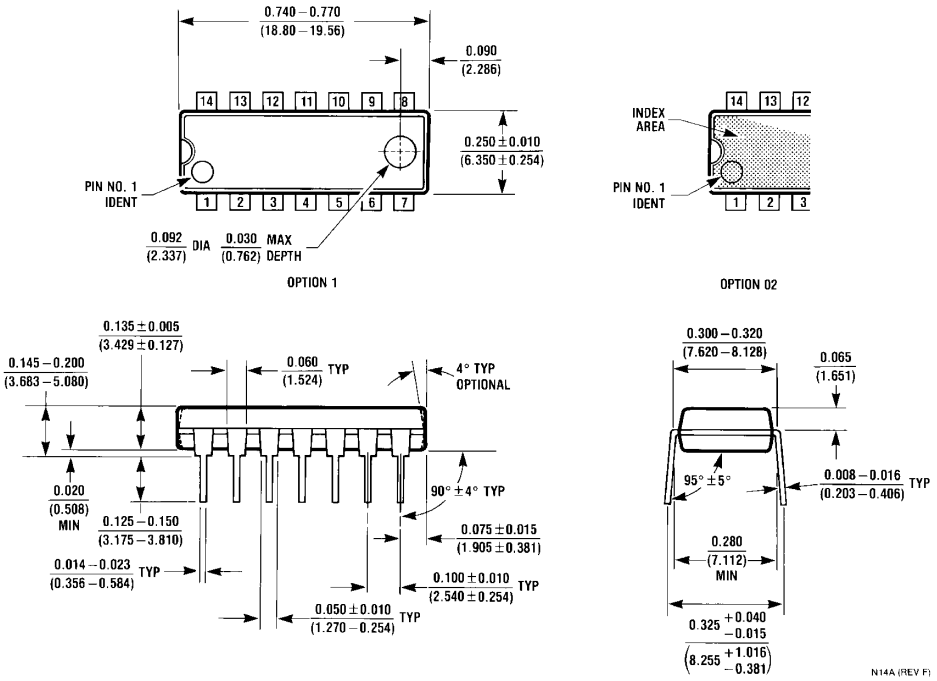

**FIGURE 2. 81-Line Parity/Generator Checker**

## Physical Dimensions inches (millimeters) unless otherwise noted




**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow**
**Package Number M14A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N14A**

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