

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
- 20	0.078 at V _{GS} = - 4.5 V	- 1.4	12.1 nC
	0.098 at V _{GS} = - 2.5 V	- 1	
	0.130 at V _{GS} = - 1.8 V	- 1	
	0.188 at V _{GS} = - 1.5 V	- 0.3	

FEATURES

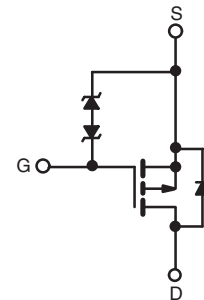
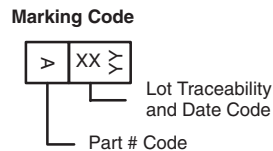
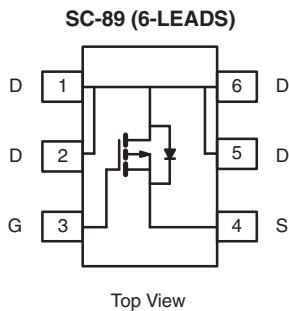
- TrenchFET[®] Power MOSFET
- Typical ESD Performance 2500 V
- 100 % R_g Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch for Portable Devices
- Power Management



Ordering Information: Si1077X-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _A = 25 °C	- 1.75 ^{b, c}
		T _A = 70 °C	- 1.4 ^{b, c}
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 8	A
Continuous Source-Drain Diode Current	I _S	- 0.28 ^{b, c}	W
Maximum Power Dissipation	P _D	T _A = 25 °C	
		T _A = 70 °C	0.21 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, b}	R _{thJA}	t ≤ 5 s	300	375	°C/W
		Steady State	360	450	

Notes:

- Maximum under steady state conditions is 450 °C/W.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.

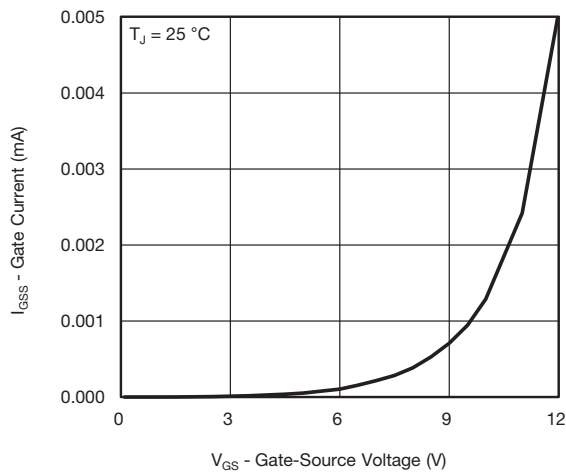
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 11		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 0.4		- 1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 10	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 1	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			- 1	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\text{ V}, V_{GS} = -4.5\text{ V}$	- 8			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -1.8\text{ A}$		0.065	0.078	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		0.081	0.098	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.100	0.130	
		$V_{GS} = -1.5\text{ V}, I_D = -0.3\text{ A}$		0.125	0.188	
Forward Transconductance	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -1.8\text{ A}$		10		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		965		μF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			101		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -8\text{ V}, I_D = -1.75\text{ A}$		20.7	31.1	nC
				12.1	18.2	
Gate-Source Charge	Q_{gs}	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1.75\text{ A}$		1.85		
Gate-Drain Charge	Q_{gd}			2.21		
Gate Resistance	R_g		$f = 1\text{ MHz}$	3.6	18	36
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 7.1\text{ }\Omega$ $I_D \cong -1.4\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		24	36	ns
Rise Time	t_r			17	26	
Turn-Off Delay Time	$t_{d(off)}$			95	145	
Fall Time	t_f			28	42	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 7.1\text{ }\Omega$ $I_D = -1.4\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$		5	10	ns
Rise Time	t_r			8	16	
Turn-Off Delay Time	$t_{d(off)}$			115	173	
Fall Time	t_f			26	39	
Drain-Source Body Diode Characteristics						
Pulse Diode Forward Current ^a	I_{SM}				- 8	A
Body Diode Voltage	V_{SD}	$I_S = -1.4\text{ A}$		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -1.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		16	24	ns
Body Diode Reverse Recovery Charge	Q_{rr}			7	14	nC
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			7		

Notes:

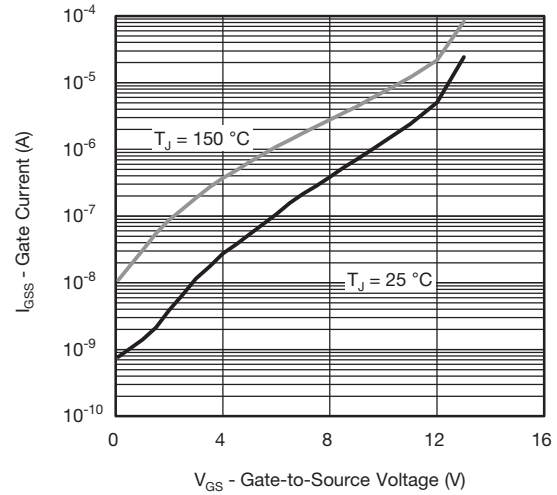
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

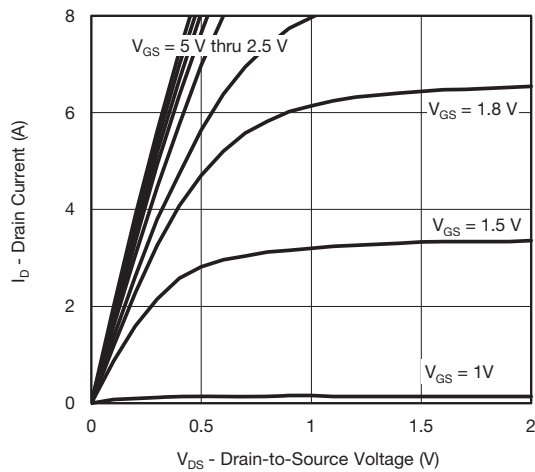
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



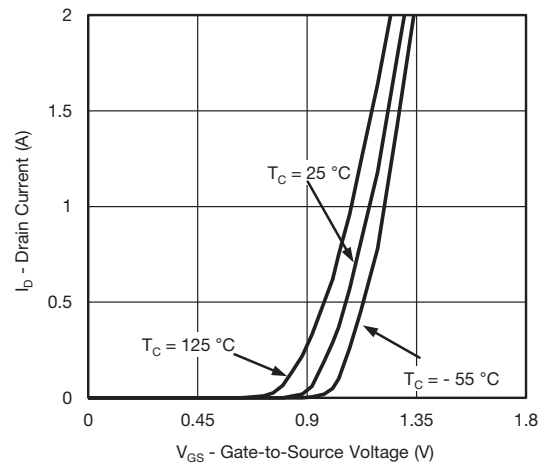
Gate Current vs. Gate-Source Voltage



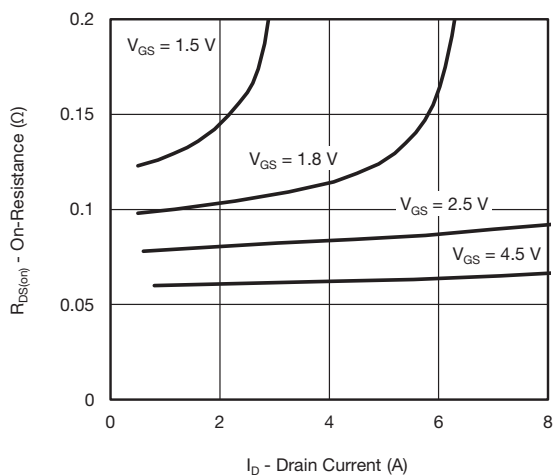
Gate Current vs. Gate-to-Source Voltage



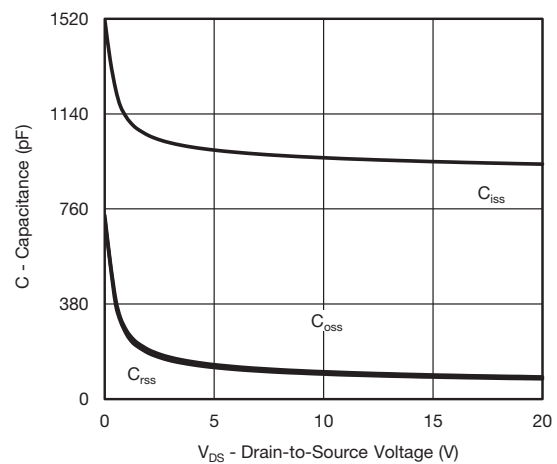
Output Characteristics



Transfer Characteristics Curves vs. Temperature

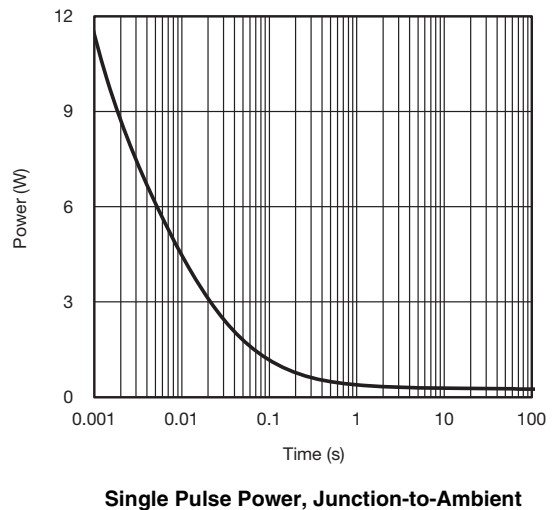
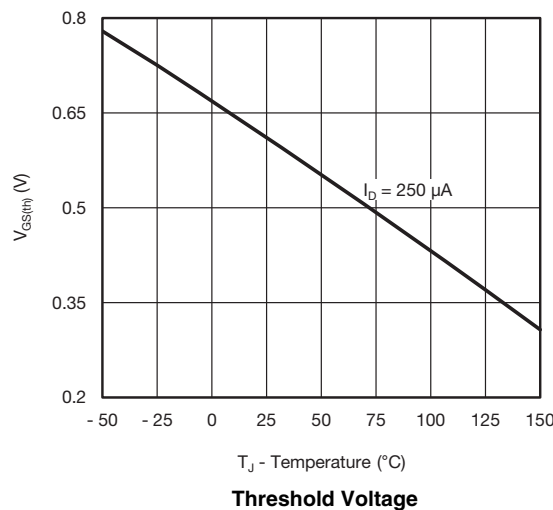
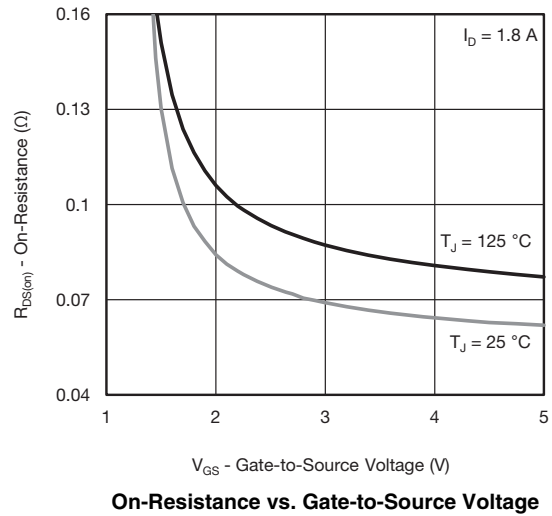
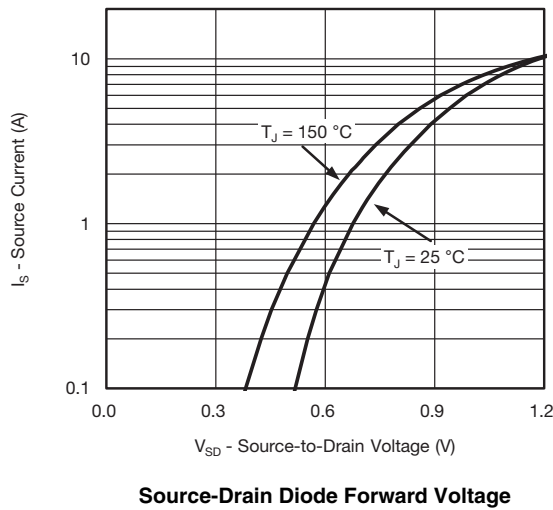
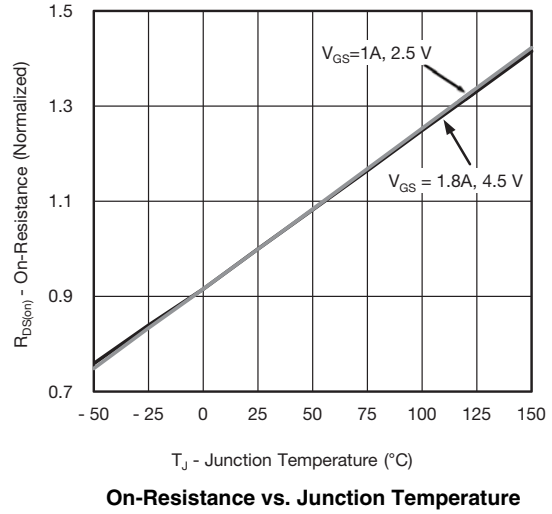
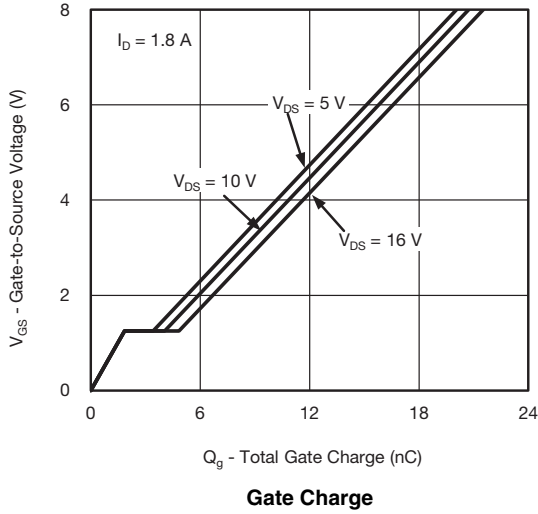


On-Resistance vs. Drain Current

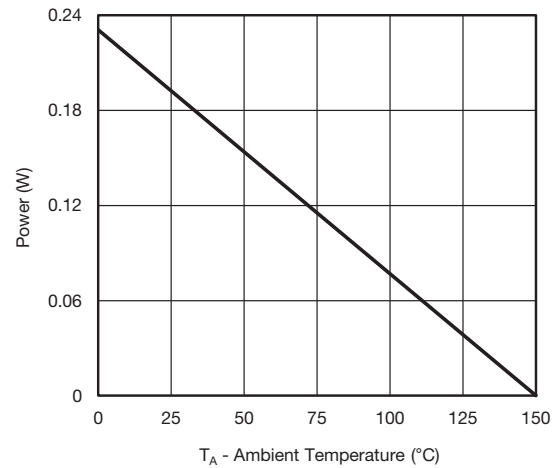
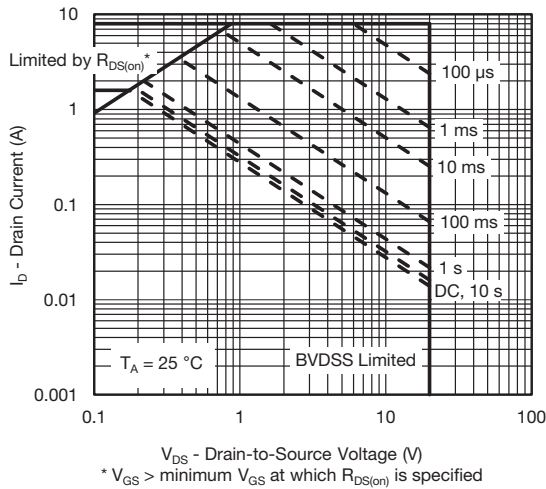


Capacitance

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

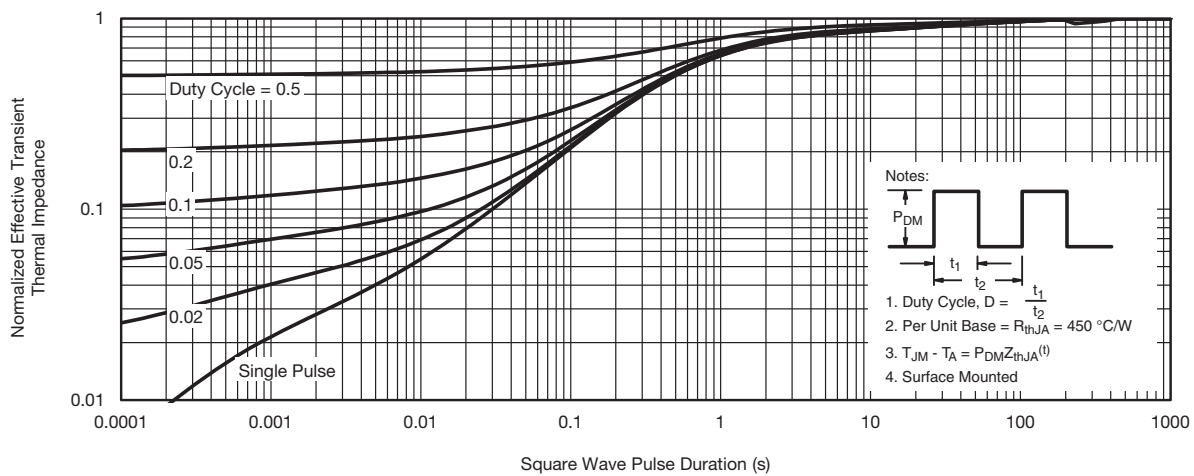


TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient

Power Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63254.

SC-89 6-Leads (SOT-563F)



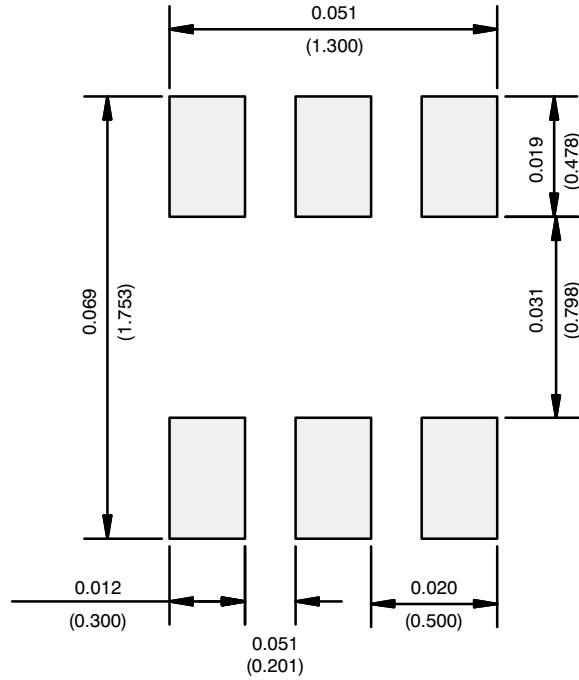
Notes

1. Dimensions in millimeters.
- ⚠ Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- ⚠ Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- ⚠ Datums A, B and D to be determined 0.10 mm from the lead tip.
- ⚠ Terminal numbers are shown for reference only.
- ⚠ These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30

C14-0439-Rev. C, 11-Aug-14
DWG: 5880

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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JONHON

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А