



SY58609U

4.25Gbps Precision, CML 2:1 MUX with Internal Termination and Fail Safe Input

General Description

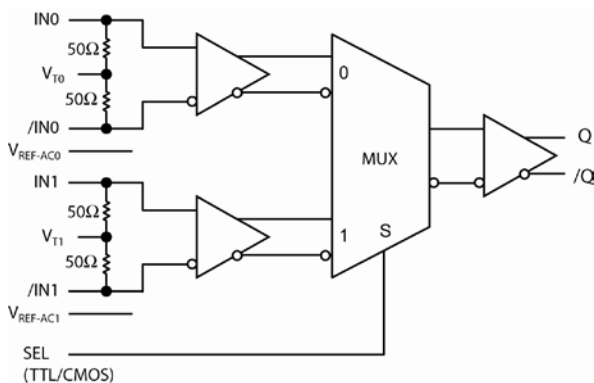
The SY58609U is a 2.5/3.3V, high-speed, fully differential CML 2:1 MUX capable of processing clock signals up to 2.5GHz and data patterns up to 4.25Gbps. The SY58609U is optimized to provide a buffered output of the selected input with less than 20ps of skew and less than 10ps_{pp} total jitter.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled) as small as 100mV (200mV_{pp}) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated reference voltage (V_{REF-AC}) is provided to bias the V_T pin. The outputs are 400mV CML, with extremely fast rise/fall times guaranteed to be less than 90ps.

The SY58609U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require LVPECL or LVDS outputs, consider Micrel's SY58610U and SY58611U, 2:1 MUX with 800mV and 325mV output swings, respectively. The SY58609U is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Precision Edge®

Features

- Precision 400mV CML 2:1 MUX
- Guaranteed AC performance over temperature and voltage:
 - DC-to > 4.25Gbps throughput
 - <370ps propagation delay (IN-to-Q)
 - <90ps rise/fall times
- Fail Safe Input
 - Prevents outputs from oscillating when input is invalid
- Unique, patented MUX input isolation design minimizes adjacent channel crosstalk
- Ultra-low jitter design
 - <1ps_{RMS} cycle-to-cycle jitter
 - <10ps_{PP} total jitter
 - <1ps_{RMS} random jitter
 - <10ps_{PP} deterministic jitter
- High-speed CML outputs
- 2.5V ±5% or 3.3V ±10% power supply operation
- Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

Applications

- Data Distribution: OC-48, OC-48+FEC, XAUI
- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access

Precision Edge is a registered trademark of Micrel, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • <http://www.micrel.com>

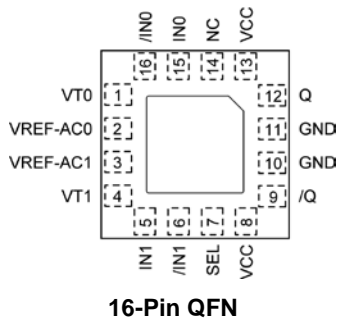
Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|-----------------------------|--------------|-----------------|--------------------------------------|----------------|
| SY58609UMG | QFN-16 | Industrial | 609U with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY58609UMGTR ⁽²⁾ | QFN-16 | Industrial | 609U with Pb-Free bar-line indicator | NiPdAu Pb-Free |

Notes:

- Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
- Tape and Reel.

Pin Configuration



Truth Table

| SEL | Output |
|-----|--------------|
| 0 | IN0 Selected |
| 1 | IN1 Selected |

Pin Description

| Pin Number | Pin Name | Pin Function |
|----------------|------------------------|---|
| 1, 4 | VT0, VT1 | Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" subsection. |
| 2, 3 | VREF-AC0, VREF-AC1 | Reference Voltage: These outputs bias to $V_{CC}-1.2\text{V}$. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with $0.01\mu\text{F}$ low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is $\pm 0.5\text{mA}$. See "Input Interface Applications" subsection. |
| 5, 6 15, 16 | IN1, /IN1 IN0, /IN0 | Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept DC-Coupled differential signals as small as 100mV (200mVpp). Each pin of the pairs internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typical 30mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. See "Input Interface Applications" subsection. |
| 7 | SEL | Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a $25\text{k}\Omega$ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$. |
| 8, 13 | VCC | Positive Power Supply: Bypass with $0.1\mu\text{F}/0.01\mu\text{F}$ low ESR capacitors as close to the VCC pins as possible. |
| 9, 12 | /Q, Q | CML Differential Output Pair: Differential buffered output copy of the selected input signal. The output swing is typically 400mV . Normally terminate with 100Ω across Q and /Q. Unused output pair may be left floating with no impact on jitter. See "CML Output Termination" subsection. |
| 10, 11 | GND | Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pins. |
| 14 | NC | No connect. |

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC}) -0.5V to +4.0V
 Input Voltage (V_{IN}) -0.5V to V_{CC}
 CML Output Voltage (V_{OUT}) $V_{CC}-1.0V$ to $V_{CC}+0.5V$
 Current (V_T)
 Source or sink on V_T pin $\pm 100mA$
 Input Current
 Source or sink Current on (I_N , $/I_N$) $\pm 50mA$
 Current (V_{REF})
 Source or sink current on V_{REF-AC} ⁽⁴⁾ $\pm 0.5mA$
 Maximum operating Junction Temperature 125°C
 Lead Temperature (soldering, 20sec.) 260°C
 Storage Temperature (T_s) -65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC}) +2.375V to +3.60V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽³⁾
 QFN
 Still-air (θ_{JA}) 60°C/W
 Junction-to-board (ψ_{JB}) 33°C/W

DC Electrical Characteristics⁽⁵⁾

$T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|---|------------------------|--------------|------------|--------------|----------|
| V_{CC} | Power Supply Voltage Range | | 2.375 3.0 | 2.5 3.3 | 2.625 3.6 | V |
| I_{CC} | Power Supply Current | No load, max. V_{CC} | | 50 | 60 | mA |
| R_{DIFF_IN} | Differential Input Resistance (IN-to- $/I_N$) | | 90 | 100 | 110 | Ω |
| V_{IH} | Input HIGH Voltage (IN, $/I_N$) | IN, $/I_N$, Note 7 | $V_{CC}-1.6$ | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (IN, $/I_N$) | IN, $/I_N$ | 0.2 | | $V_{IH}-0.1$ | V |
| V_{IN} | Input Voltage Swing (IN, $/I_N$) | see Figure 3a, Note 6 | 0.1 | | 1.0 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing ($ I_N - /I_N $) | see Figure 3b | 0.2 | | | V |
| V_{IN_FSI} | Input Voltage Threshold that Triggers FSI | | | 30 | 100 | mV |
| V_{REF-AC} | AC Reference Voltage | | $V_{CC}-1.3$ | | $V_{CC}-1.0$ | V |
| V_{T_IN} | Voltage from Input to V_T | | | | 1.28 | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. $V_{IN}(max)$ is specified when V_T is floating.
7. $V_{IH}(min)$ not lower than 1.2V.

CML Outputs DC Electrical Characteristics⁽⁷⁾

$V_{CC} = +2.5V \pm 5\%$ or $+3.3V \pm 10\%$, $R_L = 100\Omega$ across the outputs; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|-----------------------------------|------------------------------|----------------|----------------|----------|----------|
| V_{OH} | Output HIGH Voltage | $R_L = 50\Omega$ to V_{CC} | $V_{CC}-0.020$ | $V_{CC}-0.010$ | V_{CC} | V |
| V_{OUT} | Output Voltage Swing | See Figure 3a | 325 | 400 | | mV |
| V_{DIFF_OUT} | Differential Output Voltage Swing | See Figure 3b | 650 | 800 | | mV |
| R_{OUT} | Output Source Impedance | | 45 | 50 | 55 | Ω |

LVTTL/CMOS DC Electrical Characteristics⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|--------------------|-----------|------|-----|-----|---------|
| V_{IH} | Input HIGH Voltage | | 2.0 | | | V |
| V_{IL} | Input LOW Voltage | | | | 0.8 | V |
| I_{IH} | Input HIGH Current | | -125 | | 30 | μA |
| I_{IL} | Input LOW Current | | -300 | | | μA |

Notes:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics⁽⁸⁾

$V_{CC} = +2.5V \pm 5\%$ or $+3.3V \pm 10\%$, $R_L = 100\Omega$ across the outputs; Input $t_R/t_F \leq 300ps$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------|-------------------------------------|-------------------------|------|-----|-----|-------------------|
| f_{MAX} | Maximum Frequency | NRZ Data | 4.25 | | | Gbps |
| | | $V_{OUT} > 200mV$ Clock | 2.5 | 3 | | GHz |
| t_{PD} | Propagation Delay IN-to-Q | $V_{IN}: 100mV-200mV$ | 180 | 330 | 450 | ps |
| | | $V_{IN}: >200mV$ | 140 | 270 | 370 | ps |
| | SEL-to-Q | | 150 | | 450 | ps |
| t_{Skew} | Input-to-Input Skew | Note 9, 10 | | 5 | 20 | ps |
| | Part-to-Part Skew | Note 11 | | | 150 | ps |
| t_{Jitter} | Data Random Jitter | Note 12 | | | 1 | ps _{RMS} |
| | Deterministic Jitter | Note 13 | | | 10 | ps _{PP} |
| | Clock Cycle-to-Cycle Jitter | Note 14 | | | 1 | ps _{RMS} |
| | Total Jitter | Note 15 | | | 10 | ps _{PP} |
| t_R, t_F | Output Rise/Fall Times (20% to 80%) | At full output swing. | 35 | 50 | 90 | ps |
| | Duty Cycle | Differential I/O | 47 | | 53 | % |

Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Input-to-Input skew is the time difference between the two inputs and one output, under identical input transitions.
9. Input-to-Input Skew is included in IN-to-Q propagation delay.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature, same transition edge, and no skew at the edges at the respective inputs.
12. Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.
13. Deterministic jitter is measured at 2.5Gbps with both K28.5 and $2^{23}-1$ PRBS pattern.
14. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
15. Total jitter definition: with an ideal clock input frequency of $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Functional Description

Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below 100mV_{PK} (200mV_{PP}), typically 30mV_{PK} . Maximum frequency of the SY58609U is limited by the FSI function.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, the FSI function will eliminate a metastable condition and guarantee a stable output. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to "Typical Characteristics" for detailed information.

Timing Diagrams

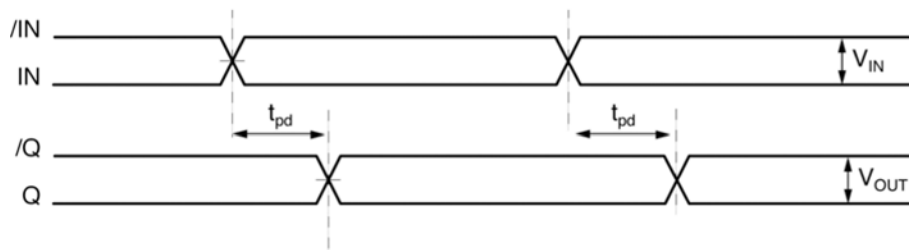


Figure 1a. Propagation Delay

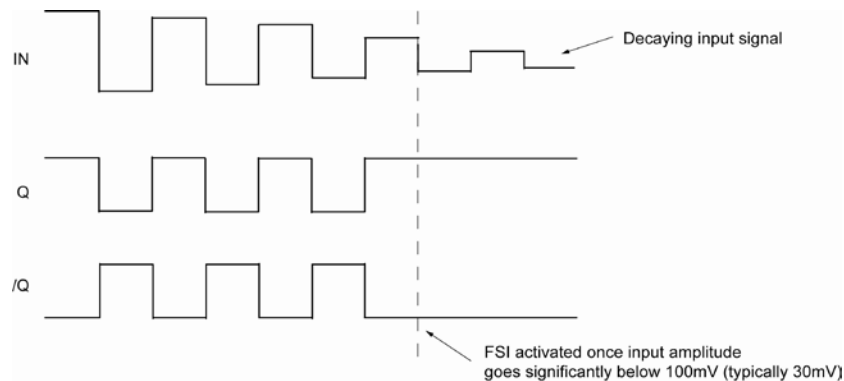


Figure 1b. Fail Safe Feature

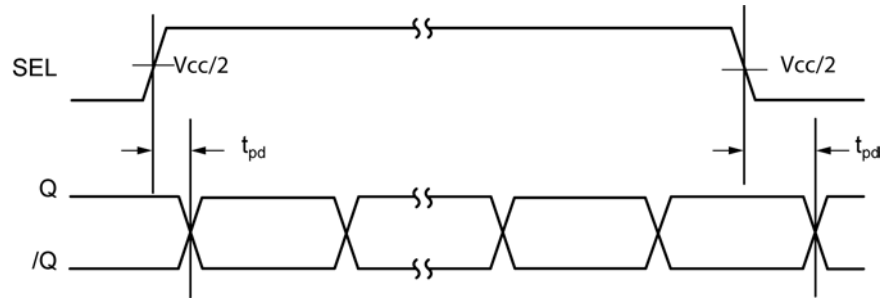
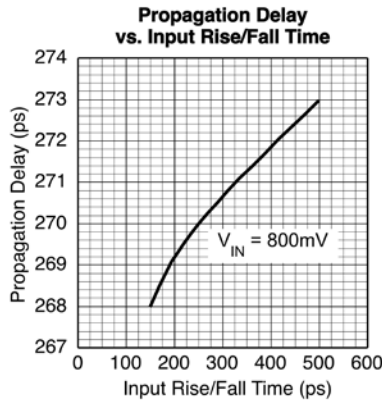
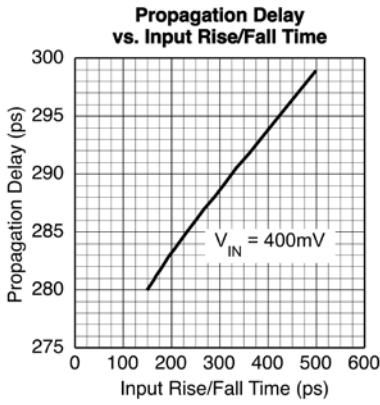
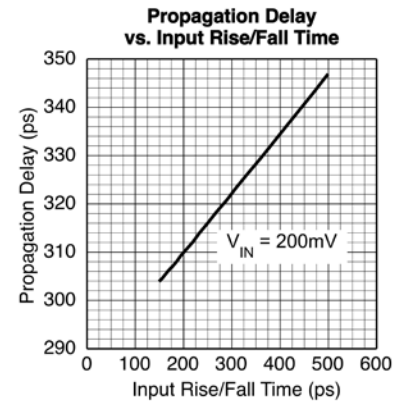
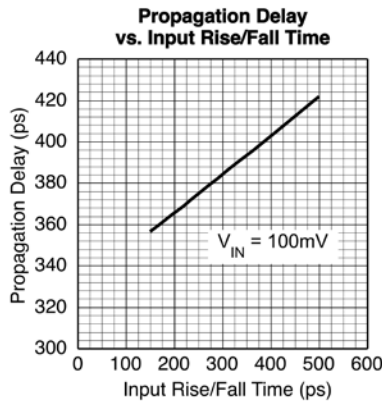
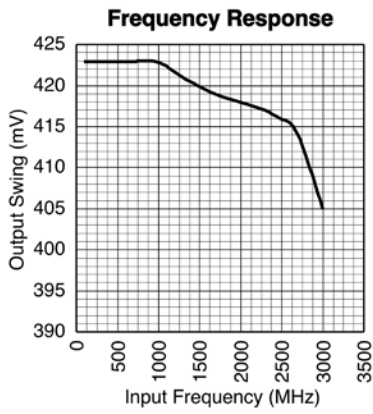


Figure 1c. SEL-to-Q Delay

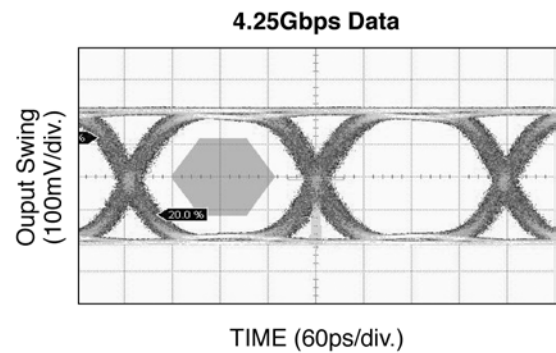
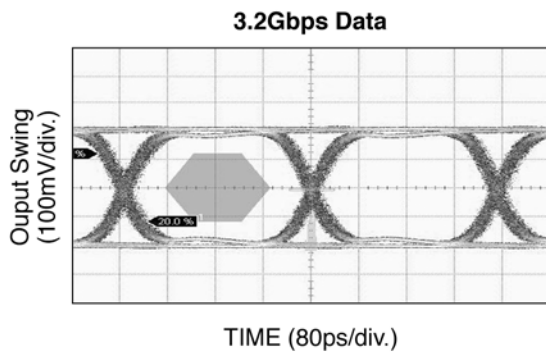
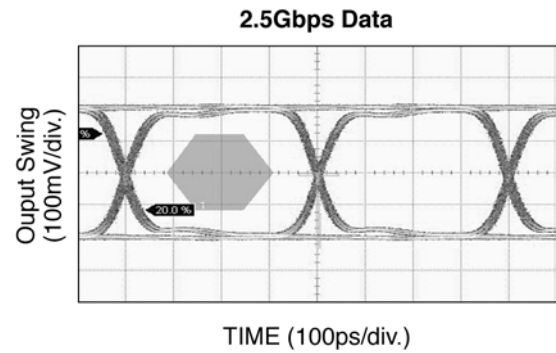
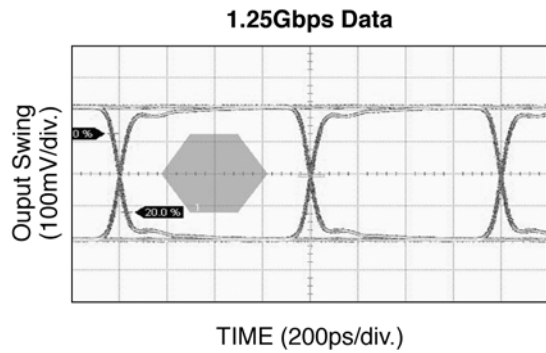
Typical Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 100mV$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



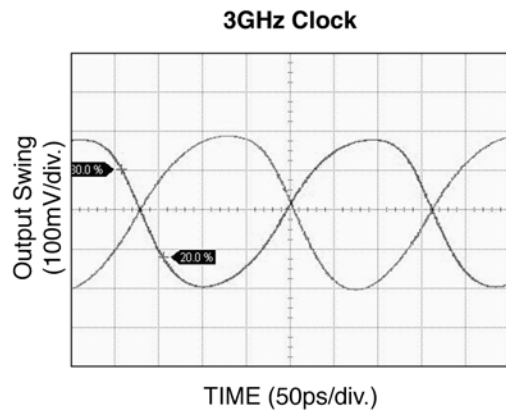
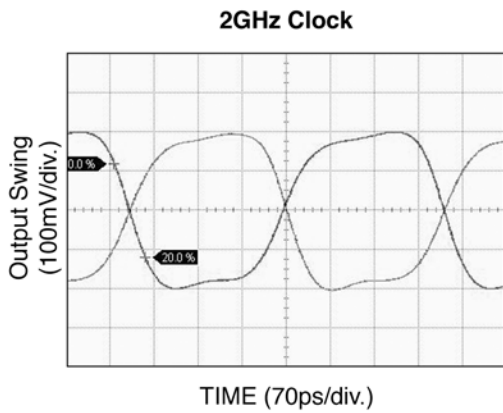
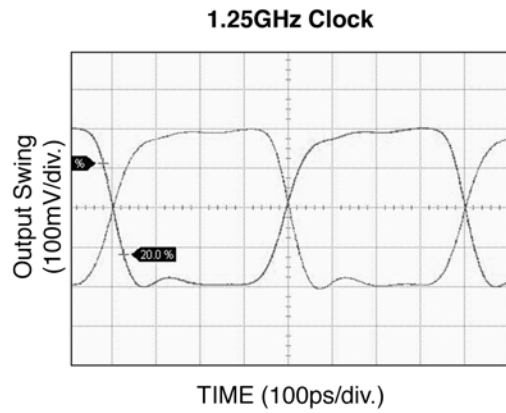
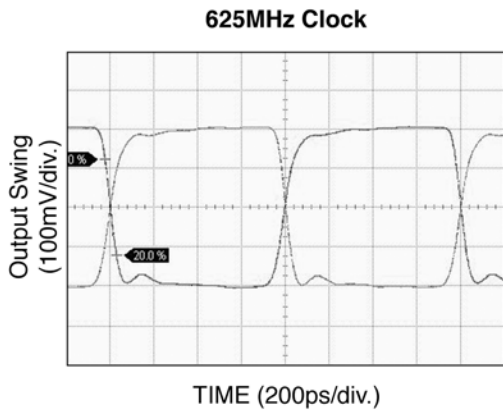
Functional Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 325mV$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



Functional Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 325mV$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



Input and Output Stage

Single-Ended and Differential Swings

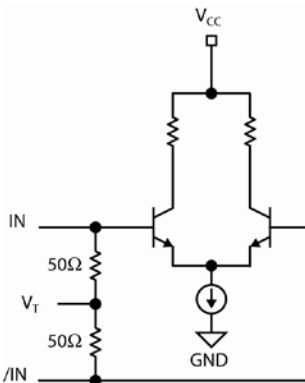


Figure 2a. Simplified Differential Input Buffer

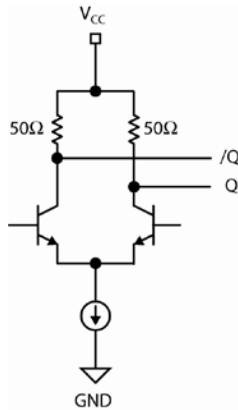


Figure 2b. Simplified CML Output Buffer



Figure 3a. Single-Ended Voltage Swing

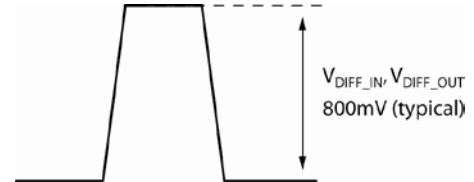


Figure 3b. Differential Voltage Swing

Input Interface Applications

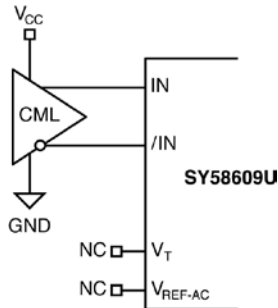


Figure 4a. CML Interface (DC-Coupled)

Option: May connect V_T to V_{CC}

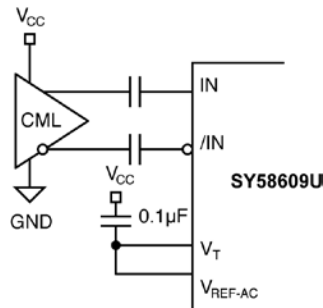


Figure 4b. CML Interface (AC-Coupled)

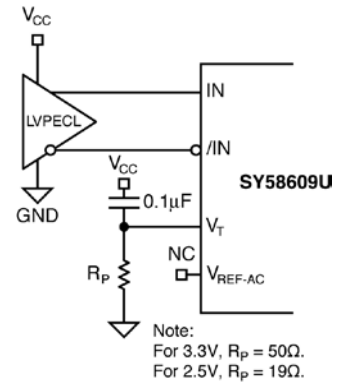


Figure 4c. LVPECL Interface (DC-Coupled)

Note:
For 3.3V, $R_p = 50\Omega$.
For 2.5V, $R_p = 19\Omega$.

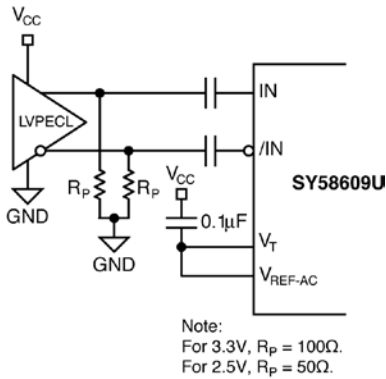


Figure 4d. LVPECL Interface (AC-Coupled)

Note:
For 3.3V, $R_p = 100\Omega$.
For 2.5V, $R_p = 50\Omega$.

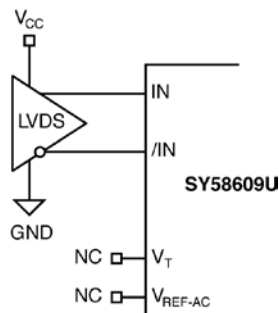


Figure 4e. LVDS Interface

CML Output Termination

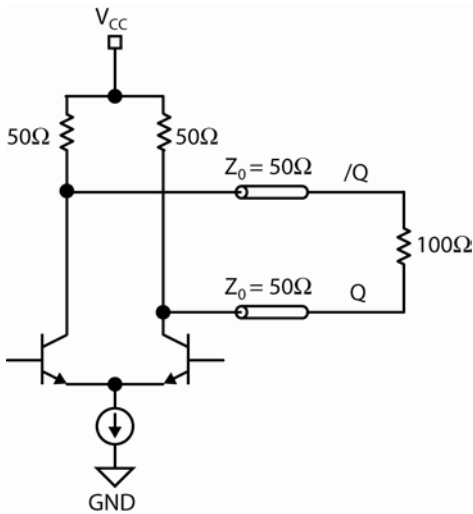


Figure 5a. CML DC-Coupled Termination

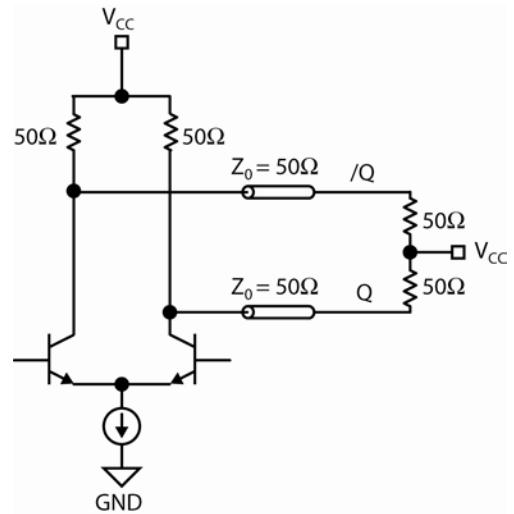


Figure 5b. CML DC-Coupled Termination

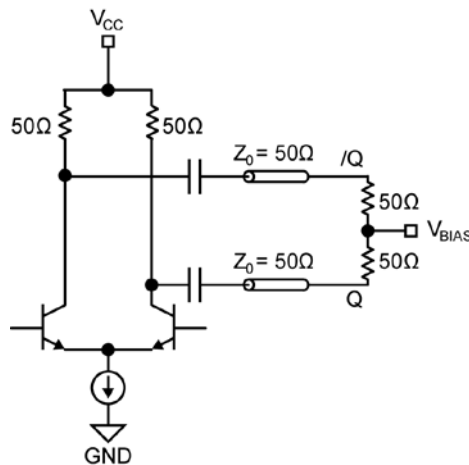
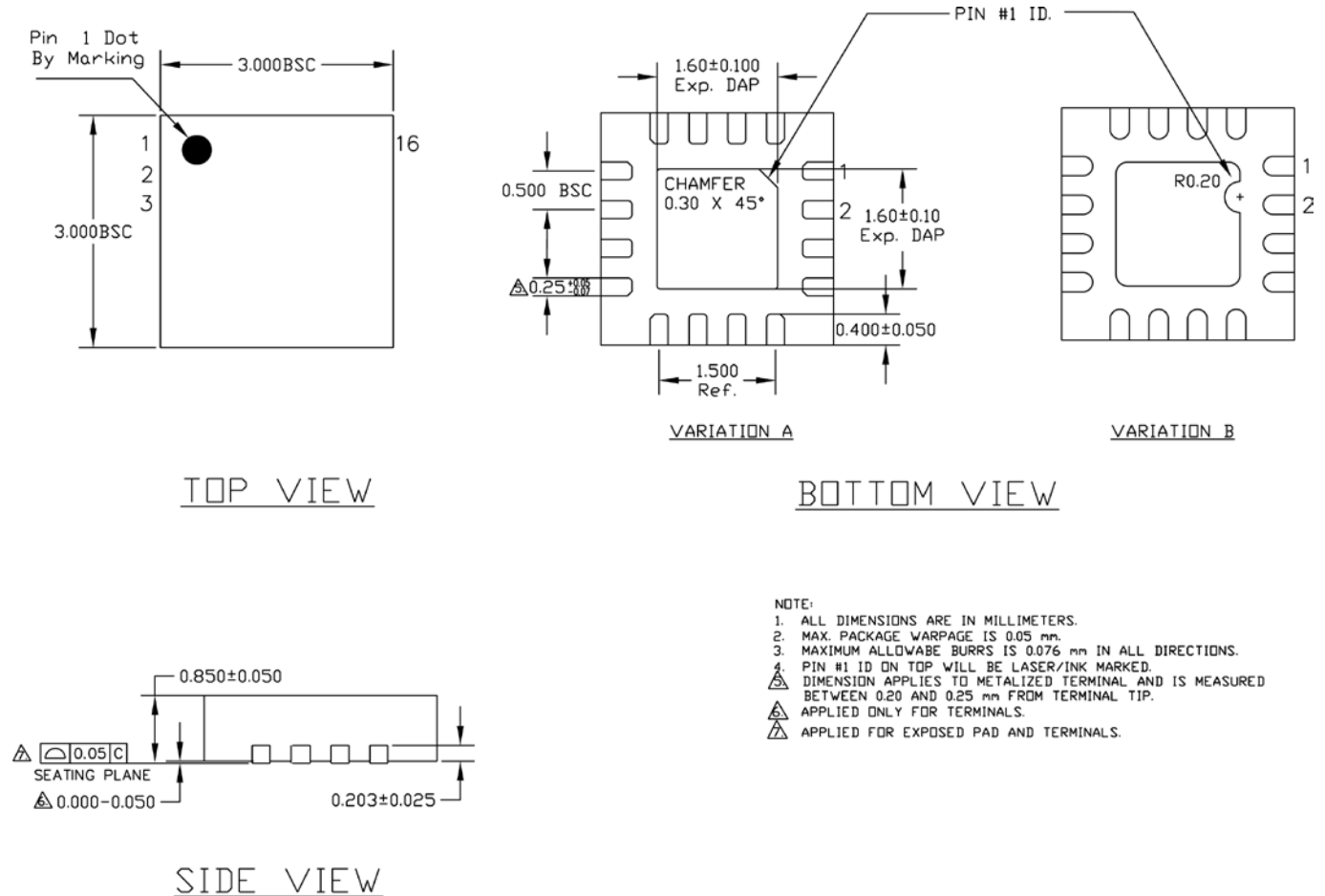


Figure 5c. CML AC-Coupled Termination

Related Product and Support Documents

| Part Number | Function | Datasheet Link |
|---------------|---|---|
| SY58610U | 3.2Gbps Precision, LVPECL 2:1 MUX with Internal Termination and Fail Safe Input | http://www.micrel.com/_PDF/HBW/sy58610u.pdf |
| SY58611U | 3.2Gbps Precision, LVDS 2:1 MUX with Internal Termination and Fail Safe Input | http://www.micrel.com/_PDF/HBW/sy58611u.pdf |
| HBW Solutions | New Products and Termination Application Notes | http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml |

Package Information



16-Pin (3mm x 3mm) QFN

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2006 Micrel, Incorporated.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А