

S7G2 Microcontroller Group

Datasheet

Renesas Synergy™ Platform

Synergy Microcontrollers

S7 Series

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Leading performance 240-MHz Arm® Cortex®-M4 core, up to 4-MB code flash memory, 640-KB SRAM, Graphics LCD Controller, 2D Drawing Engine, Capacitive Touch Sensing Unit, Ethernet MAC Controller with IEEE 1588 PTP, USB 2.0 High-Speed, USB 2.0 Full-Speed, SDHI, Quad SPI, security and safety features, and advanced analog.

Features

■ Arm Cortex-M4 Core with Floating Point Unit (FPU)

- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 240 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and Arm® Memory Protection Unit (MPU)

■ Memory

- Up to 4-MB code flash memory (80 MHz zero wait states)
- 64-KB data flash memory (125,000 erase/write cycles)
- Up to 640-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

■ Connectivity

- Ethernet MAC Controller (ETHERC) × 2
- Ethernet DMA Controller (EDMAC)
- Ethernet PTP Controller (EPTPC)
- USB 2.0 High-Speed Module (USBHS)
 - On-chip transceiver
 - USB battery charge version 1.2 supported
- USB 2.0 Full-Speed Module (USBFS)
 - On-chip transceiver
- Serial Communications Interface (SCI) with FIFO × 10
- Serial Peripheral Interface (SPI) × 2
- I²C Bus Interface (IIC) × 3
- CAN module (CAN) × 2
- Serial Sound Interface (SSI) × 2
- SD/MMC Host Interface (SDHI) × 2
- Quad Serial Peripheral Interface (QSPI)
- IrDA interface
- Sampling Rate Converter (SRC)
- External memory space
 - 8-bit or 16-bit bus space is selectable per area
 - SDRAM support

■ Analog

- 12-Bit A/D Converter (ADC12) with 3 sample-and-hold circuits each, x2
- 12-Bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Programmable Gain Amplifier (PGA) × 6
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 32-Bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-Bit Enhanced (GPT32E) × 4
- General PWM Timer 32-Bit (GPT32) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety

- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management

- Low power modes
- Switching regulator
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption

- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256/MD5
- GHASH
- RSA/DSA/ECC
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)

- Graphics LCD Controller (GLCDC)
- JPEG Codec
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSUS)
- Parallel Data Capture Unit (PDC)

■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General-Purpose I/O Ports

- Up to 172 input/output pins
 - Up to 9 CMOS input
 - Up to 163 CMOS input/output
 - Up to 22 input/output 5 V tolerant
 - Up to 24 high current (20 mA)

■ Operating Voltage

- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages

- Ta = -40°C to +85°C
 - 224-pin BGA (13 mm × 13 mm, 0.8 mm pitch)
 - 176-pin BGA (13 mm × 13 mm, 0.8 mm pitch)
 - 145-pin LGA (7 mm × 7 mm, 0.5 mm pitch)
- Ta = -40°C to +105°C
 - 176-pin LQFP (24 mm × 24 mm, 0.5 mm pitch)
 - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
 - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm[®]-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex[®]-M4 core running up to 240 MHz with the following features:

- Up to 4-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 Arm core

| Feature | Functional description |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Arm Cortex-M4 core | <ul style="list-style-type: none"> • Maximum operating frequency: up to 240 MHz • Arm Cortex-M4 core: <ul style="list-style-type: none"> - Revision: r0p1-01rel0 - Armv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008 • Arm Memory Protection Unit (Arm MPU): <ul style="list-style-type: none"> - Armv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: <ul style="list-style-type: none"> - Driven by SYSTICCLK (LOCO) or ICLK. |

Table 1.2 Memory

| Feature | Functional description |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Code flash memory | Maximum 4 MB of code flash memory. See section 55, Flash Memory in User's Manual. |
| Data flash memory | 64 KB of data flash memory. See section 55, Flash Memory in User's Manual. |
| Option-setting memory | The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual. |
| Memory Mirror Function (MMF) | The Memory Mirror Function (MMF) can be configured to mirror the wanted application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual. |
| SRAM | On-chip high-speed SRAM providing either parity-bit or Double-bit Error Detection (DED). The first 32 KB of SRAM0 is subject to DED. Parity check is performed for other areas. See section 53, SRAM in User's Manual. |
| Standby SRAM | On-chip SRAM that can retain data in Deep Software Standby mode. See section 54, Standby SRAM in User's Manual. |

Table 1.3 System (1 of 2)

| Feature | Functional description |
|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operating modes | Two operating modes: - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes in User's Manual. |
| Resets | 14 resets: <ul style="list-style-type: none"> • RES pin reset • Power-on reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • Independent watchdog timer reset • Watchdog timer reset • Deep Software Standby reset • SRAM parity error reset • SRAM DED error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual. |
| Low Voltage Detection (LVD) | The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual. |
| Clocks | <ul style="list-style-type: none"> • Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • IDWT-dedicated on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual. |
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual. |
| Interrupt Controller Unit (ICU) | The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual. |
| Key interrupt function (KINT) | A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual. |
| Low power modes | Power consumption can be reduced in multiple ways, including by setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual. |
| Battery backup function | A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function in User's Manual. |
| Register write protection | The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual. |
| Memory Protection Unit (MPU) | Three Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual. |

Table 1.3 System (2 of 2)

| Feature | Functional description |
|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Watchdog Timer (WDT) | The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual. |
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT) in User's Manual. |

Table 1.4 Event link

| Feature | Functional description |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual. |

Table 1.5 Direct memory access

| Feature | Functional description |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual. |
| DMA Controller (DMAC) | An 8-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual. |

Table 1.6 External bus interface

| Feature | Functional description |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External buses | <ul style="list-style-type: none"> CS area (EXBIU): Connected to the external devices (external memory interface) SDRAM area (EXBIU): Connected to the SDRAM (external memory interface) QSPI area (EXBIUT2): Connected to the QSPI (external device interface). |

Table 1.7 Timers (1 of 2)

| Feature | Functional description |
|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| General PWM Timer (GPT) | The General PWM Timer (GPT) is a 32-bit timer with 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual. |
| Port Output Enable for GPT (POEG) | Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual. |
| Asynchronous General-Purpose Timer (AGT) | The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Asynchronous General-Purpose Timer (AGT) in User's Manual. |

Table 1.7 Timers (2 of 2)

| Feature | Functional description |
|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Realtime Clock (RTC) | The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual. |

Table 1.8 Communication interfaces (1 of 2)

| Feature | Functional description |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Serial Communications Interface (SCI) | The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 34, Serial Communications Interface (SCI) in User's Manual. |
| IrDA Interface (IrDA) | The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 35, IrDA Interface in User's Manual. |
| I ² C bus Interface (IIC) | The 3-channel I ² C bus interface (IIC) conforms with and provides a subset of the NXP I ² C (Inter-Integrated Circuit) bus interface functions. See section 36, I ² C Bus Interface (IIC) in User's Manual. |
| Serial Peripheral Interface (SPI) | Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 38, Serial Peripheral Interface (SPI) in User's Manual. |
| Serial Sound Interface (SSI) | The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting PCM audio data over a serial bus with the MCU. The SSI supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSI includes 8-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 41, Serial Sound Interface (SSI) in User's Manual. |
| Quad Serial Peripheral Interface (QSPI) | The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 39, Quad Serial Peripheral Interface (QSPI) in User's Manual. |
| Controller Area Network (CAN) module | The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 37, Controller Area Network (CAN) Module in User's Manual. |
| USB 2.0 Full-Speed (USBFS) module | The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 32, USB 2.0 Full-Speed Module (USBFS) in User's Manual. |

Table 1.8 Communication interfaces (2 of 2)

| Feature | Functional description |
|------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| USB 2.0 High-Speed (USBHS) module | The USB 2.0 High-Speed (USBHS) module can operate as a host controller or a device controller. As a host controller, the USBHS supports high-speed transfer, full-speed transfer, and low-speed transfer as defined in Universal Serial Bus Specification 2.0. As a device controller, the USBHS supports high-speed transfer and full-speed transfer as defined in Universal Serial Bus Specification 2.0. The USBHS has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USBHS has FIFO buffers for data transfer, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or your system for communication. See section 33, USB 2.0 High-Speed Module (USBHS) in User's Manual. |
| Ethernet MAC with IEEE 1588 PTP (ETHERC) | Two-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. Each ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. To handle timing and synchronization between devices, an on-chip Precision Time Protocol (PTP) module for the Ethernet PTP Controller (EPTPC) applies the PTP defined in the IEEE 1588-2008 version 2.0 standard. The EPTPC is composed of: <ul style="list-style-type: none"> • Synchronization Frame Processing units (SYNFP0 and SYNFP1) • A Packet Relation Controller unit (PRC-TC) • A Statistical Time Correction Algorithm unit (STCA). Use the EPTPC in combination with the on-chip Ethernet MAC Controller (ETHERC) and the DMA Controller for the PTP Ethernet Controller (PTPEDMAC). See section 29, Ethernet MAC Controller (ETHERC) in User's Manual. |
| SD/MMC Host Interface (SDHI) | The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1-bit and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 43, SD/MMC Host Interface (SDHI) in User's Manual. |

Table 1.9 Analog

| Feature | Functional description |
|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12-bit A/D Converter (ADC12) | Up to two successive approximation 12-bit A/D Converters (ADC12) are provided. In unit 0, up to 13 analog input channels are selectable. In unit 1, up to 12 analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit, 10-bit, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 47, 12-Bit A/D Converter (ADC12) in User's Manual. |
| 12-bit D/A Converter (DAC12) | A 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 48, 12-Bit D/A Converter (DAC12) in User's Manual. |
| Temperature sensor (TSN) | The on-chip Temperature Sensor (TSN) can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 49, Temperature Sensor (TSN) in User's Manual. |
| High-Speed Analog Comparator (ACMPHS) | The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 50, High-Speed Analog Comparator (ACMPHS) in User's Manual. |

Table 1.10 Human machine interfaces

| Feature | Functional description |
|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Capacitive Touch Sensing Unit (CTSU) | The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by the software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrodes. See section 51, Capacitive Touch Sensing Unit (CTSU) in User's Manual. |

Table 1.11 Graphics

| Feature | Functional description |
|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Graphics LCD Controller (GLCDC) | The Graphics LCD Controller (GLCDC) provides multiple functions and supports various data formats and panels. Key GLCDC features include: <ul style="list-style-type: none"> • GPX bus master function for accessing graphics data • Superimposition of three planes (single color background plane, graphic 1 plane, and graphic 2 plane) • Support for many types of 32-bit or 16-bit per pixel graphics data and 8-bit, 4-bit, or 1-bit LUT data format • Digital interface signal output supporting a video image size of WVGA or greater. See section 58, Graphics LCD Controller (GLCDC) in User's Manual. |
| 2D Drawing Engine (DRW) | The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or antialiased. Rasterization is executed at one pixel per clock on the bounding box of the object from left to right and top to bottom. The DRW can also raster from bottom to top to optimize the performance in certain cases. In addition, optimization methods are available to avoid rasterization of many empty pixels of the bounding box. The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object. If a pixel is inside the object, it is selected for rendering. If it is outside, it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for antialiasing. Every pixel that is selected for rendering can be textured. The resulting aRGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The aRGB quadruples can then be blended with one of the multiple blend modes of the DRW. The DRW provides two inputs (texture read and framebuffer read), and one output (framebuffer write). The internal color format is always aRGB (8888). The color formats from the inputs are converted to the internal format on read and a conversion back is made on write. See section 56, 2D Drawing Engine (DRW) in User's Manual. |
| JPEG Codec (JPEG) | The JPEG Codec (JPEG) incorporates a JPEG codec that conforms to the JPEG baseline compression and decompression standard. This provides high-speed compression of image data and high-speed decoding of JPEG data. See section 57, JPEG Codec in User's Manual. |
| Parallel Data Capture (PDC) unit | One Parallel Data Capture (PDC) unit is provided for communicating with external I/O devices, including image sensors, and transferring parallel data such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). See section 44, Parallel Data Capture Unit (PDC) in User's Manual. |

Table 1.12 Data processing (1 of 2)

| Feature | Functional description |
|------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 40, Cyclic Redundancy Check (CRC) Calculator in User's Manual. |

Table 1.12 Data processing (2 of 2)

| Feature | Functional description |
|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data Operation Circuit (DOC) | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 52, Data Operation Circuit (DOC) in User's Manual. |
| Sampling Rate Converter (SRC) | The Sampling Rate Converter (SRC) converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. See section 42, Sampling Rate Converter (SRC) in User's Manual. |

Table 1.13 Security

| Feature | Functional description |
|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Secure Crypto Engine 7 (SCE7) | <ul style="list-style-type: none"> • Security algorithms: <ul style="list-style-type: none"> - Symmetric algorithms: AES, 3DES, and ARC4 - Asymmetric algorithms: RSA, DSA, and ECC. • Other support features: <ul style="list-style-type: none"> - TRNG (True Random Number Generator) - Hash-value generation: SHA1, SHA224, SHA256, GHASH, and MD5 - 128-bit unique ID. |

1.2 Block Diagram

Figure 1.1 shows the block diagram of the MCU superset, some individual devices within the group have a subset of the features.

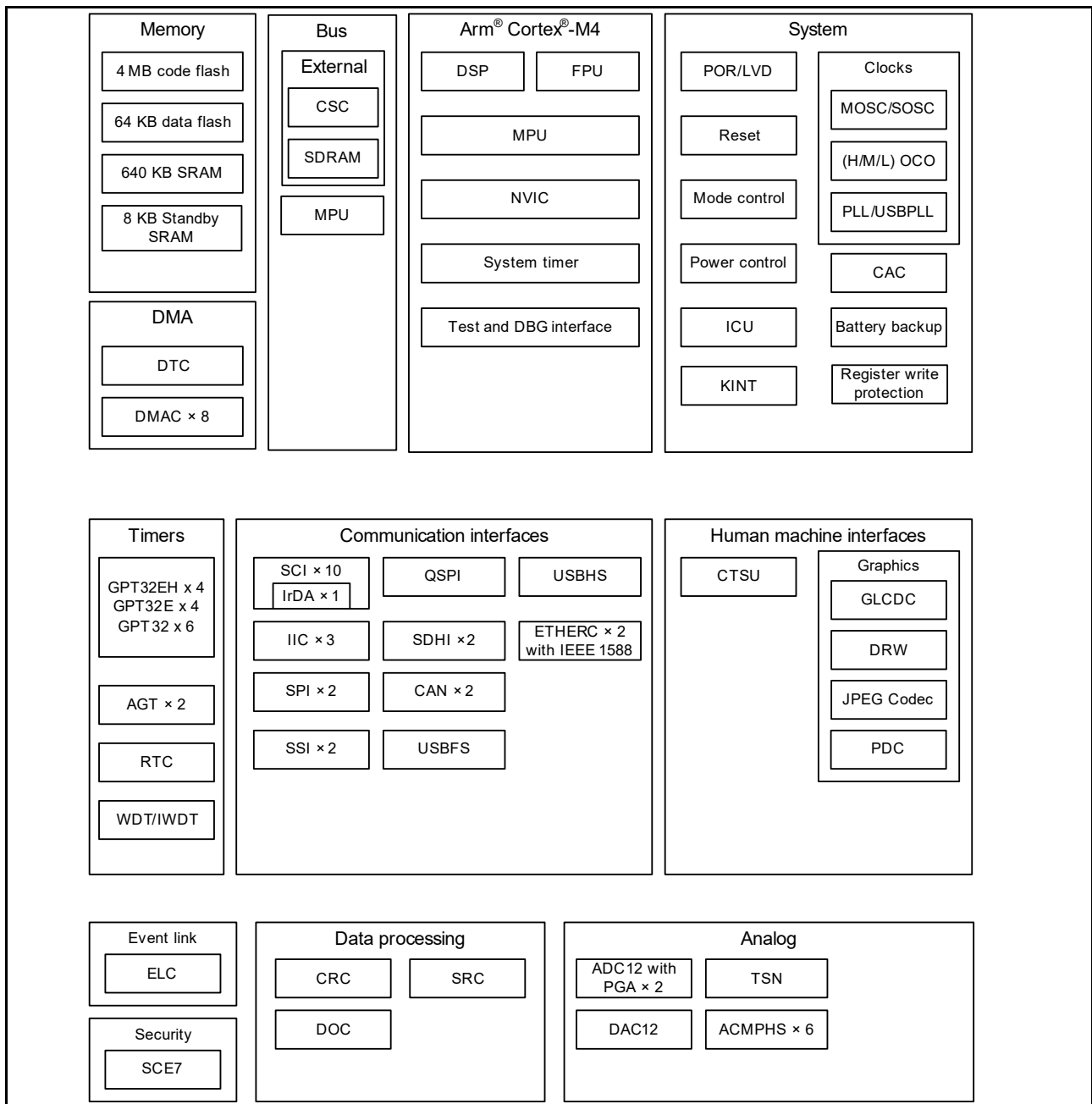


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows product part number information, including memory capacity and package type. Table 1.14 shows a list of products.

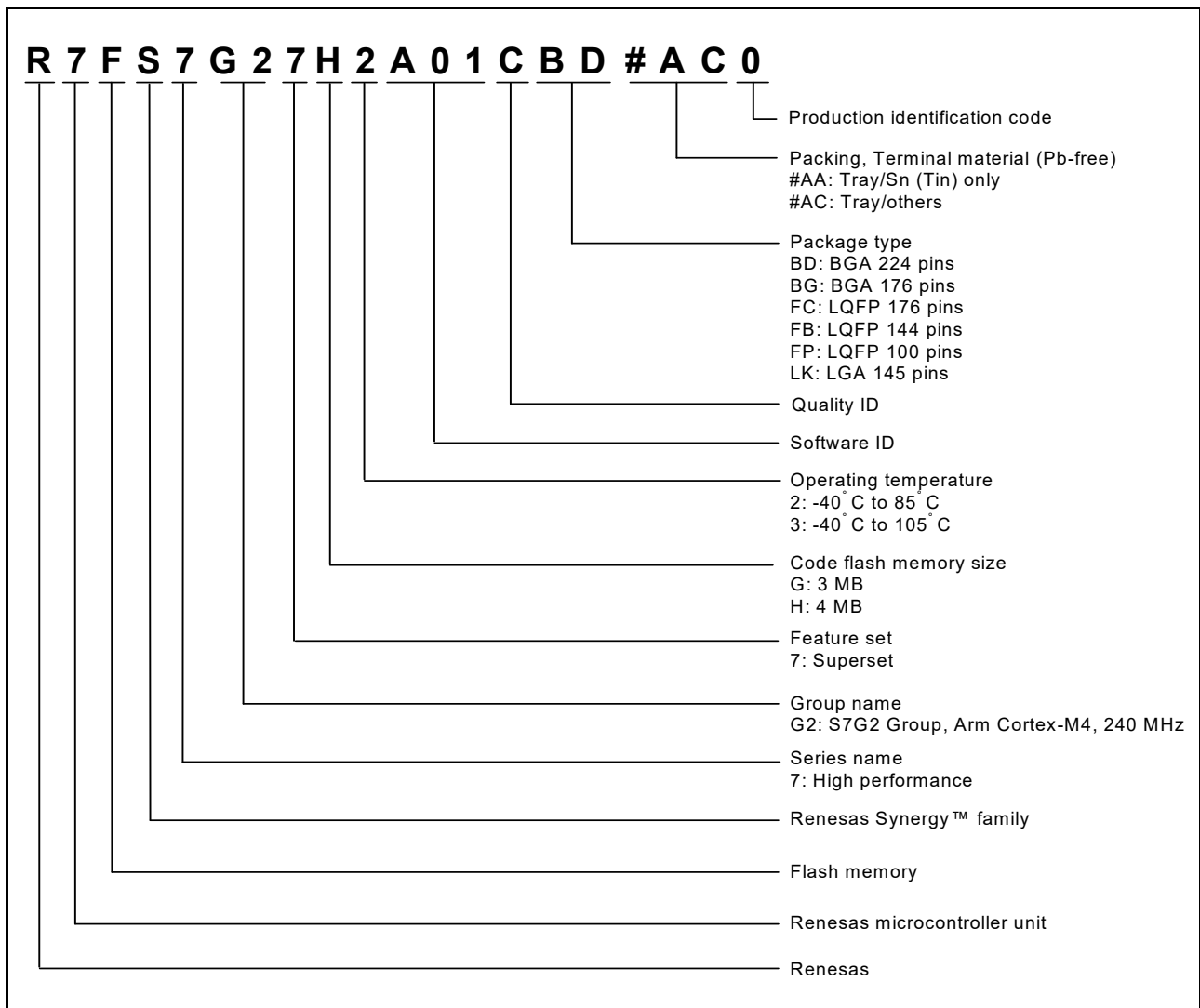


Figure 1.2 Part numbering scheme

Table 1.14 Product list

| Part number | Orderable part number | Package | Code flash | Data flash | SRAM | Operating temperature |
|------------------|-----------------------|--------------|------------|------------|--------|-----------------------|
| R7FS7G27H2A01CBD | R7FS7G27H2A01CBD#AC0 | PLBG0224GA-A | 4 MB | 64 KB | 640 KB | -40 to +85°C |
| R7FS7G27H2A01CBG | R7FS7G27H2A01CBG#AC0 | PLBG0176GE-A | | | | -40 to +85°C |
| R7FS7G27H3A01CFC | R7FS7G27H3A01CFC#AA0 | PLQP0176KB-A | | | | -40 to +105°C |
| R7FS7G27H2A01CLK | R7FS7G27H2A01CLK#AC0 | PTLG0145KA-A | | | | -40 to +85°C |
| R7FS7G27H3A01CFB | R7FS7G27H3A01CFB#AA0 | PLQP0144KA-B | | | | -40 to +105°C |
| R7FS7G27G2A01CBD | R7FS7G27G2A01CBD#AC0 | PLBG0224GA-A | 3 MB | | | -40 to +85°C |
| R7FS7G27G2A01CBG | R7FS7G27G2A01CBG#AC0 | PLBG0176GE-A | | | | -40 to +85°C |
| R7FS7G27G3A01CFC | R7FS7G27G3A01CFC#AA0 | PLQP0176KB-A | | | | -40 to +105°C |
| R7FS7G27G2A01CLK | R7FS7G27G2A01CLK#AC0 | PTLG0145KA-A | | | | -40 to +85°C |
| R7FS7G27G3A01CFB | R7FS7G27G3A01CFB#AA0 | PLQP0144KA-B | | | | -40 to +105°C |
| R7FS7G27G3A01CFP | R7FS7G27G3A01CFP#AA0 | PLQP0100KB-B | | | | -40 to +105°C |

1.4 Function Comparison

Table 1.15 Functional comparison

| Function | Part numbers | | | | | | | |
|-------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|------------------|------------|--|
| | R7FS7G27H2A01CBD/ R7FS7G27G2A01CBD | R7FS7G27H2A01CBG/ R7FS7G27G2A01CBG | R7FS7G27H3A01CFC/ R7FS7G27G3A01CFC | R7FS7G27H2A01CLK/ R7FS7G27G2A01CLK | R7FS7G27H3A01CFB/ R7FS7G27G3A01CFB | R7FS7G27G3A01CFP | | |
| Pin count | 224 | 176 | 176 | 145 | 144 | 100 | | |
| Package | BGA | BGA | LQFP | LGA | LQFP | LQFP | | |
| Code flash memory | 4/3 MB | | | | | 3 MB | | |
| Data flash memory | 64 KB | | | | | | | |
| SRAM | 640 KB | | | | | | | |
| | Parity | 608 KB | | | | | | |
| | DED | 32 KB | | | | | | |
| Standby SRAM | 8 KB | | | | | | | |
| System | CPU clock | 240 MHz | | | | | | |
| | Backup registers | 512 bytes | | | | | | |
| | ICU | Yes | | | | | | |
| | KINT | 8 | | | | | | |
| Event link | ELC | Yes | | | | | | |
| DMA | DTC | Yes | | | | | | |
| | DMAC | 8 | | | | | | |
| BUS | External bus | 16-bit bus | | | | | 8-bit bus | |
| | SDRAM | Yes | | | | | No | |
| Timers | GPT32EH | 4 | 4 | 4 | 4 | 4 | 4 | |
| | GPT32E | 4 | 4 | 4 | 4 | 4 | 3 | |
| | GPT32 | 6 | 6 | 6 | 6 | 6 | 5 | |
| | AGT | 2 | 2 | 2 | 2 | 2 | 2 | |
| | RTC | Yes | | | | | | |
| | WDT/IWDT | Yes | | | | | | |
| Communication | SCI | 10 | | | | | | |
| | IIC | 3 | | | | | 2 | |
| | SPI | 2 | | | | | | |
| | SSI | 2 | | | | | 1 | |
| | QSPI | 1 | | | | | Dual-SPI 1 | |
| | SDHI | 2 | | | | | | |
| | CAN | 2 | | | | | | |
| | USBFS | Yes | | | | | | |
| | USBHS | Yes | | | No | | | |
| | ETHERC | 2 | | | | | 1 | |
| Analog | ADC12 | 25 | 21 | 21 | 19 | 19 | 16 | |
| | DAC12 | 2 | | | | | | |
| | ACMPHS | 6 | | | | | | |
| | TSN | Yes | | | | | | |
| HMI | CTSUS | 18 | 12 | 12 | 18 | | 12 | |
| | KINT | 8 | | | | | | |
| Graphics | GLCDC | RGB888 | | | | | RGB565 | |
| | DRW | Yes | | | | | | |
| | JPEG | Yes | | | | | | |
| | PDC | Yes | | | | | No | |
| Data processing | CRC | Yes | | | | | | |
| | DOC | Yes | | | | | | |
| | SRC | Yes | | | | | | |
| Security | SCE7 | | | | | | | |

1.5 Pin Functions

Table 1.16 Pin functions (1 of 5)

| Function | Signal | I/O | Description |
|------------------------|------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power supply | VCC | Input | Power supply pin. Connect this pin to the system power supply. Connect it to VSS through a 0.1- μ F capacitor. Place the capacitor close to the pin. |
| | VCC_DCDC | Input | Switching regulator power supply pin. |
| | VLO | I/O | Switching regulator pin. |
| | VCL0 to VCL2 | Input | Connect this pin to VSS through a smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VCL_F | Input | |
| | VSS | Input | Ground pin. Connect to the system power supply (0 V). |
| | VBATT | Input | Backup power pin |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOU and XCIN. |
| | XCOU | Output | |
| | EBCLK | Output | Outputs the external bus clock for external devices |
| | SDCLK | Output | Outputs the SDRAM-dedicated clock |
| | CLKOUT | Output | Clock output pin |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state. |
| System control | RES | Input | Reset signal input pin. The MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Measurement reference clock input pin |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ15 | Input | Maskable interrupt request pins |
| KINT | KR00 to KR07 | Input | A key interrupt can be generated by inputting a falling edge to the key interrupt input pins |
| On-chip emulator | TMS | I/O | On-chip emulator or boundary scan pins |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TCLK | Output | This pin outputs the clock for synchronization with the trace data |
| | TDATA0 to TDATA3 | Output | Trace data output |
| | SWDIO | I/O | Serial wire debug data input/output pin |
| | SWCLK | Input | Serial wire clock pin |
| | SWO | Output | Serial wire trace output pin |
| External bus interface | RD | Output | Strobe signal indicating that reading from the external bus interface space is in progress, active-low |
| | WR | Output | Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active-low |
| | WR0, WR1 | Output | Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active-low |
| | BC0, BC1 | Output | Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active-low |
| | WAIT | Input | Input pin for wait request signals in access to the external space, active-low |
| | CS0 to CS7 | Output | Select signals for CS areas, active-low |
| | A00 to A23 | Output | Address bus |
| | D00 to D15 | I/O | Data bus |

Table 1.16 Pin functions (2 of 5)

| Function | Signal | I/O | Description |
|-----------------|------------------------------------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| SDRAM interface | CKE | Output | SDRAM clock enable signal |
| | SDCS | Output | SDRAM chip select signal, active-low |
| | RAS | Output | SDRAM low address strobe signal, active-low |
| | CAS | Output | SDRAM column address strobe signal, active-low |
| | WE | Output | SDRAM write enable signal, active-low |
| | DQM0 | Output | SDRAM I/O data mask enable signal for DQ07 to DQ00 |
| | DQM1 | Output | SDRAM I/O data mask enable signal for DQ15 to DQ08 |
| | A00 to A15 | Output | Address bus |
| DQ00 to DQ15 | I/O | Data bus | |
| GPT | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input | External trigger input pins |
| | GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B | I/O | Input capture, output compare, or PWM output pins. |
| | GTIU | Input | Hall sensor input pin U |
| | GTIV | Input | Hall sensor input pin V |
| | GTIW | Input | Hall sensor input pin W |
| | GTOUUP | Output | 3-phase PWM output for BLDC motor control (positive U phase) |
| | GTOULO | Output | 3-phase PWM output for BLDC motor control (negative U phase) |
| | GTOVUP | Output | 3-phase PWM output for BLDC motor control (positive V phase) |
| | GTOVLO | Output | 3-phase PWM output for BLDC motor control (negative V phase) |
| | GTOWUP | Output | 3-phase PWM output for BLDC motor control (positive W phase) |
| | GTOWLO | Output | 3-phase PWM output for BLDC motor control (negative W phase) |
| AGT | AGTEE0, AGTEE1 | Input | External event input enable signals |
| | AGTIO0, AGTIO1 | I/O | External event input and pulse output pins |
| | AGTO0, AGTO1 | Output | Pulse output pins |
| | AGTOA0, AGTOA1 | Output | Output compare match A output pins |
| | AGTOB0, AGTOB1 | Output | Output compare match B output pins |
| RTC | RTCOUT | Output | Output pin for 1-Hz or 64-Hz clock |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pins |
| SCI | SCK0 to SCK9 | I/O | Input/output pins for the clock (clock synchronous mode) |
| | RXD0 to RXD9 | Input | Input pins for received data (asynchronous mode/clock synchronous mode) |
| | TXD0 to TXD9 | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode) |
| | CTS0_RTS0 to CTS9_RTS9 | I/O | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low |
| | SCL0 to SCL9 | I/O | Input/output pins for the clock (simple IIC mode) |
| | SDA0 to SDA9 | I/O | Input/output pins for the data (simple IIC mode) |
| | SCK0 to SCK9 | I/O | Input/output pins for the clock (simple SPI mode) |
| | MISO0 to MISO9 | I/O | Input/output pins for slave transmission of data (simple SPI mode) |
| | MOSI0 to MOSI9 | I/O | Input/output pins for master transmission of data (simple SPI mode) |
| SS0 to SS9 | Input | Chip-select input pins (simple SPI mode), active-low | |
| IIC | SCL0 to SCL2 | I/O | Input/output pins for the clock |
| | SDA0 to SDA2 | I/O | Input/output pins for data |
| SSI | SSISCK0 | I/O | SSI serial bit clock pin |
| | SSISCK1 | | |
| | SSIWS0 | I/O | Word select pins |
| | SSIWS1 | | |
| | SSITXD0 | Output | Serial data output pins |
| | SSIRXD0 | Input | Serial data input pins |
| | SSIDATA1 | I/O | Serial data input/output pins |
| AUDIO_CLK | Input | External clock pin for audio (input oversampling clock) | |

Table 1.16 Pin functions (3 of 5)

| Function | Signal | I/O | Description |
|----------|--------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPI | RSPCKA, RSPCKB | I/O | Clock input/output pin |
| | MOSIA, MOSIB | I/O | Input or output pins for data output from the master |
| | MISOA, MISOB | I/O | Input or output pins for data output from the slave |
| | SSLA0, SSLB0 | I/O | Input or output pin for slave selection |
| | SSLA1 to SSLA3, SSLB1 to SSLB3 | Output | Output pins for slave selection |
| QSPI | QSPCLK | Output | QSPI clock output pin |
| | QSSL | Output | QSPI slave output pin |
| | QIO0 to QIO3 | I/O | Data0 to Data3 |
| CAN | CRX0, CRX1 | Input | Receive data |
| | CTX0, CTX1 | Output | Transmit data |
| USBFS | VCC_USB | Input | Power supply pins |
| | VSS_USB | Input | Ground pins |
| | USB_DP | I/O | D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus |
| | USB_DM | I/O | D- I/O pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus |
| | USB_VBUS | Input | USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller. |
| | USB_EXICEN | Output | Low-power control signal for external power supply (OTG) chip |
| | USB_VBUSEN | Output | VBUS (5 V) supply enable signal for external power supply chip |
| | USB_OVRCURA, USB_OVRCURB | Input | Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected. |
| | USB_ID | Input | Connect the MicroAB connector ID input signal to this pin during operation in OTG mode |
| USBHS | VCC_USBHS | Input | Power supply pin |
| | VSS1_USBHS | Input | Ground pin |
| | VSS2_USBHS | Input | Ground pin |
| | AVCC_USBHS | Input | Analog power supply pin for the USBHS |
| | AVSS_USBHS | Input | Analog ground pin for the USBHS. Must be shorted to the PVSS_USBHS pin. |
| USBHS | PVSS_USBHS | Input | PLL circuit ground pin for the USBHS. Must be shorted to the AVSS_USBHS pin. |
| | USBHS_RREF | I/O | USBHS reference current source pin. Connect this pin to the AVSS_USBHS pin through a 2.2-kΩ resistor ($\pm 1\%$). |
| | USBHS_DP | I/O | USB bus D+ data pin |
| | USBHS_DM | I/O | USB bus D- data pin |
| | USBHS_EXICEN | Output | Connect this pin to the OTG power supply IC |
| | USBHS_ID | Input | Connect this pin to the OTG power supply IC |
| | USBHS_VBUSEN | Output | VBUS power enable signal for USB |
| | USBHS_OVRCURA, USBHS_OVRCURB | Input | Overcurrent pin for USB |
| | USBHS_VBUS | Input | USB cable connection monitor input pin |

Table 1.16 Pin functions (4 of 5)

| Function | Signal | I/O | Description |
|----------|---------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------|
| ETHERC | REF50CK0, REF50CK1 | Input | 50-MHz reference clocks. These pins input reference signals for transmission/reception timing in RMII mode. |
| | RMII0_CRS_DV, RMII1_CRS_DV | Input | Indicate carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode |
| | RMII0_TXD0, RMII0_TXD1, RMII1_TXD0, RMII1_TXD1 | Output | 2-bit transmit data in RMII mode |
| | RMII0_RXD0, RMII0_RXD1, RMII1_RXD0, RMII1_RXD1 | Input | 2-bit receive data in RMII mode |
| | RMII0_TXD_EN, RMII1_TXD_EN | Output | Output pins for data transmit enable signals in RMII mode |
| | RMII0_RX_ER, RMII1_RX_ER | Input | Indicate an error occurred during reception of data in RMII mode |
| | ET0_CRS, ET1_CRS | Input | Carrier detection/data reception enable signals |
| | ET0_RX_DV, ET1_RX_DV | Input | Indicate valid receive data on ETn_ERXD3 to ETn_ERXD0 (n = 0, 1) |
| | ET0_EXOUT, ET1_EXOUT | Output | General-purpose external output pins |
| | ET0_LINKSTA, ET1_LINKSTA | Input | Input link status from the PHY-LSI |
| | ET0_ETXD0 to ET0_ETXD3, ET1_ETXD0 to ET1_ETXD3 | Output | 4 bits of MII transmit data |
| | ET0_ERXD0 to ET0_ERXD3, ET1_ERXD0 to ET1_ERXD3 | Input | 4 bits of MII receive data |
| | ET0_TX_EN, ET1_TX_EN | Output | Transmit enable signals. Function as signals indicating that transmit data is ready on ETn_ETXD3 to ETn_ETXD0 (n = 0, 1). |
| | ET0_TX_ER, ET1_TX_ER | Output | Transmit error pins. Function as signals notifying the PHY_LSI of an error during transmission. |
| | ET0_RX_ER, ET1_RX_ER | Input | Receive error pins. Function as signals to recognize an error during reception. |
| | ET0_TX_CLK, ET1_TX_CLK | Input | Transmit clock pins. These pins input reference signals for output timing from ETn_TX_EN, ETn_ETXD3 to ETn_ETXD0, and ETn_TX_ER (n = 0, 1). |
| | ET0_RX_CLK, ET1_RX_CLK | Input | Receive clock pins. These pins input reference signals for input timing to ETn_RX_DV, ETn_ERXD3 to ETn_ERXD0, and ETn_RX_ER (n = 0, 1). |
| | ET0_COL, ET1_COL | Input | Input collision detection signals |
| | ET0_WOL, ET1_WOL | Output | Receive Magic packets |
| | ET0_MDC, ET1_MDC | Output | Output reference clock signals for information transfer through ETn_MDIO (n = 0, 1) |
| ETHERC | ET0_MDIO, ET1_MDIO | I/O | Input or output bidirectional signals for exchange of management data with PHY-LSI |
| SDHI | SD0CLK, SD1CLK | Output | SD clock output pins |
| | SD0CMD, SD1CMD | I/O | Command output pin and response input signal pins |
| | SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7 | I/O | SD and MMC data bus pins |
| | SD0CD, SD1CD | Input | SD card detection pins |
| | SD0WP, SD1WP | Input | SD write-protect signals |

Table 1.16 Pin functions (5 of 5)

| Function | Signal | I/O | Description |
|---------------------|-----------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Analog power supply | AVCC0 | Input | Analog voltage supply pin. Connect this pin to VCC. |
| | AVSS0 | Input | Analog ground pin. Connect this pin to VSS. |
| | VREFH0 | Input | Analog reference voltage supply pin for the ADC12. Connect this pin to VCC when not using the ADC12. |
| | VREFL0 | Input | Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12. |
| | VREFH | Input | Reference voltage input pin for the ADC12 (unit 1) and D/A converter. This is used as the analog power supply for the respective modules. Connect this pin to VCC if the ADC12 (unit 1) or DAC12 is not in use. |
| | VREFL | Input | Reference ground pin for the ADC12 and D/A converter. This is used as the analog ground for the respective modules. Set this pin to the same potential as the VSS pin. |
| ADC12 | AN000 to AN006, AN016 to AN021 | Input | Input pins for the analog signals to be processed by the ADC12 |
| | AN100 to AN106, AN116 to AN120 | Input | |
| | ADTRG0 | Input | Input pins for the external trigger signals that start the A/D conversion, active-low |
| | ADTRG1 | Input | |
| | PGAVSS000/PGAVS S100 | Input | Differential input pins |
| DAC12 | DA0, DA1 | Output | Output pins for the analog signals processed by the D/A converter |
| ACMPHS | VCOU | Output | Comparator output pin |
| | IVREF0 to IVREF3 | Input | Reference voltage input pin for comparator |
| | IVCMP0 to IVCMP2 | Input | Analog voltage input pins for comparator |
| CTSU | TS00 to TS17 | Input | Capacitive touch detection pins (touch pins) |
| | TSCAP | - | Secondary power supply pin for the touch driver |
| I/O ports | P000 to P007 | Input | General-purpose input pins |
| | P008 to P011, P014, P015 | I/O | General-purpose input/output pins |
| | P100 to P115 | I/O | General-purpose input/output pins |
| | P200 | Input | General-purpose input pin |
| | P201 to P207, P212, P213 | I/O | General-purpose input/output pins |
| | P300 to P315 | I/O | General-purpose input/output pins |
| | P400 to P415 | I/O | General-purpose input/output pins |
| | P500 to P515 | I/O | General-purpose input/output pins |
| | P600 to P615 | I/O | General-purpose input/output pins |
| | P700 to P713 | I/O | General-purpose input/output pins |
| | P800 to P813 | I/O | General-purpose input/output pins |
| | P900 to P915 | I/O | General-purpose input/output pins |
| | PA00 to PA15 | I/O | General-purpose input/output pins |
| | PB00 to PB07 | I/O | General-purpose input/output pins |
| GLCDC | LCD_DATA00 to LCD_DATA23 | Output | Data output pins for panel |
| | LCD_TCON0 to LCD_TCON3 | Output | Output pins for panel timing adjustment |
| | LCD_CLK | Output | Panel clock output pin |
| | LCD_EXTCLK | Input | Panel clock source input pin |
| PDC | PIXCLK | Input | Image transfer clock pin |
| | VSYNC | Input | Vertical synchronization signal pin |
| | HSYNC | Input | Horizontal synchronization signal pin |
| | PIXD0 to PIXD7 | Input | 8-bit image data pins |
| | PCKO | Output | Output pin for dot clock |

1.6 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments.

| R7FS7G2xxxA01CBD | | | | | | | | | | | | | | | | |
|------------------|----------|----------------|----------|------|------|----------------|------------|------------|-------|-------|------|------|-------|--------|--------|----|
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
| 15 | P407 | P408 | P410 | P708 | VSS | USBHS_DM | PVSS_USBHS | P212/EXTAL | XCIN | VCL0 | P707 | P701 | P403 | P401 | P511 | 15 |
| 14 | USB_DP | USB_DM | P409 | P411 | P415 | USBHS_DP | AVSS_USBHS | P213/XTAL | XCOUT | VBATT | P706 | P700 | P402 | P514 | P512 | 14 |
| 13 | VCC_USB | VSS_USB | P207 | P412 | P709 | VCC_USBHS | USBHS_RREF | AVCC_USBHS | VSS | PB01 | P705 | P405 | P400 | P513 | P805 | 13 |
| 12 | P202 | P203 | P205 | P413 | P711 | VSS1_USBHS | VSS2_USBHS | VCC | PB05 | PB03 | VCC | P806 | P002 | P807 | P000 | 12 |
| 11 | P902 | P901 | P315 | P204 | P414 | P712 | PB07 | PB06 | PB02 | P702 | VSS | P004 | P008 | P001 | P005 | 11 |
| 10 | VCL1 | VSS | VSS | VCC | P313 | P710 | P713 | PB04 | P704 | P404 | P003 | P010 | P011 | P006 | P009 | 10 |
| 9 | VLO | VLO | P904 | P903 | P900 | P314 | P206 | PB00 | P406 | P515 | P007 | P014 | AVSS0 | VREFL0 | VREFH0 | 9 |
| 8 | VCC_DCDC | P200 | P201/MD | P910 | P909 | RES | P615 | P913 | P703 | P809 | VSS | P015 | VREFL | AVCC0 | VREFH | 8 |
| 7 | P911 | P912 | P311 | P308 | P908 | P907 | PA08 | PA13 | PA00 | P808 | VCC | P508 | P510 | VCC | VSS | 7 |
| 6 | P905 | P312 | P310 | P307 | P915 | P906 | PA11 | PA02 | PA01 | P606 | P812 | P506 | P507 | P509 | VCL2 | 6 |
| 5 | VSS | VCC | P309 | P306 | P914 | P300/TCK/SWCLK | PA12 | PA10 | PA03 | P607 | P811 | P505 | P502 | P503 | P504 | 5 |
| 4 | VSS | VCC | P304 | P305 | P114 | P608 | P609 | PA09 | PA04 | P107 | P106 | P804 | P501 | P803 | P500 | 4 |
| 3 | P303 | P301 | P112 | P113 | P115 | P613 | PA14 | VCC | PA05 | P603 | P600 | P105 | P104 | P810 | P802 | 3 |
| 2 | P302 | P108/TMS/SWDIO | P110/TDI | VSS | P611 | P612 | PA15 | VSS | PA06 | P604 | P601 | VCC | P103 | P800 | P801 | 2 |
| 1 | NC | P109/TDO | P111 | VCC | P610 | P614 | P813 | VCL_F | PA07 | P605 | P602 | VSS | P102 | P101 | P100 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

Figure 1.3 Pin assignment for 224-pin BGA (top view)

| R7FS7G2xxxA01CBG | | | | | | | | | | | | | | | | |
|------------------|----------|---------|----------------|----------|------|------------|------------|------------|-------|-------|------|------|-------|--------|--------|----|
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
| 15 | P407 | P409 | P411 | P414 | VSS | USBHS_DM | PVSS_USBHS | P212/EXTAL | XCIN | VCL0 | P707 | P703 | P700 | P405 | P401 | 15 |
| 14 | USB_DP | USB_DM | P410 | P412 | P415 | USBHS_DP | AVSS_USBHS | P213/XTAL | XCOUT | VBATT | P706 | P701 | P406 | P402 | P512 | 14 |
| 13 | P204 | VCC_USB | VSS_USB | P408 | P413 | VCC_USBHS | USBHS_RREF | AVCC_USBHS | VSS | PB01 | P704 | P404 | P400 | P511 | P805 | 13 |
| 12 | P313 | P202 | P207 | P206 | P205 | VSS1_USBHS | VSS2_USBHS | VCC | PB00 | P705 | P702 | P403 | P513 | P806 | P000 | 12 |
| 11 | P900 | P315 | P314 | P203 | | | | | | | | VCC | P001 | P004 | P002 | 11 |
| 10 | VCL1 | VSS | P901 | VSS | | | | | | | | VSS | P006 | P008 | P005 | 10 |
| 9 | VLO | VLO | RES | VCC | | | | | | | | P009 | AVSS0 | VREFL0 | VREFH0 | 9 |
| 8 | VCC_DCDC | P201/MD | P200 | P908 | | | | | | | | P010 | AVCC0 | VREFL | VREFH | 8 |
| 7 | P906 | P905 | P312 | P907 | | | | | | | | VCC | VSS | P015 | P014 | 7 |
| 6 | P310 | P309 | P307 | P311 | | | | | | | | P007 | P507 | P505 | VCL2 | 6 |
| 5 | P308 | P305 | VSS | VCC | | | | | | | | P003 | P503 | P504 | P506 | 5 |
| 4 | P306 | P304 | P300/TCK/SWCLK | P111 | VSS | P613 | PA09 | PA00 | P607 | VCC | VSS | VSS | VCC | P501 | P502 | 4 |
| 3 | P303 | P302 | P108/TMS/SWDIO | P110/TDI | VCC | P610 | VCC | VSS | P604 | P603 | P105 | P102 | P800 | P804 | P500 | 3 |
| 2 | P301 | P112 | P114 | P608 | P611 | P614 | PA10 | PA01 | P605 | P601 | P107 | P104 | P101 | P802 | P803 | 2 |
| 1 | P109/TDO | P113 | P115 | P609 | P612 | P615 | PA08 | VCL_F | P606 | P602 | P600 | P106 | P103 | P100 | P801 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

Figure 1.4 Pin assignment for 176-pin BGA (top view)

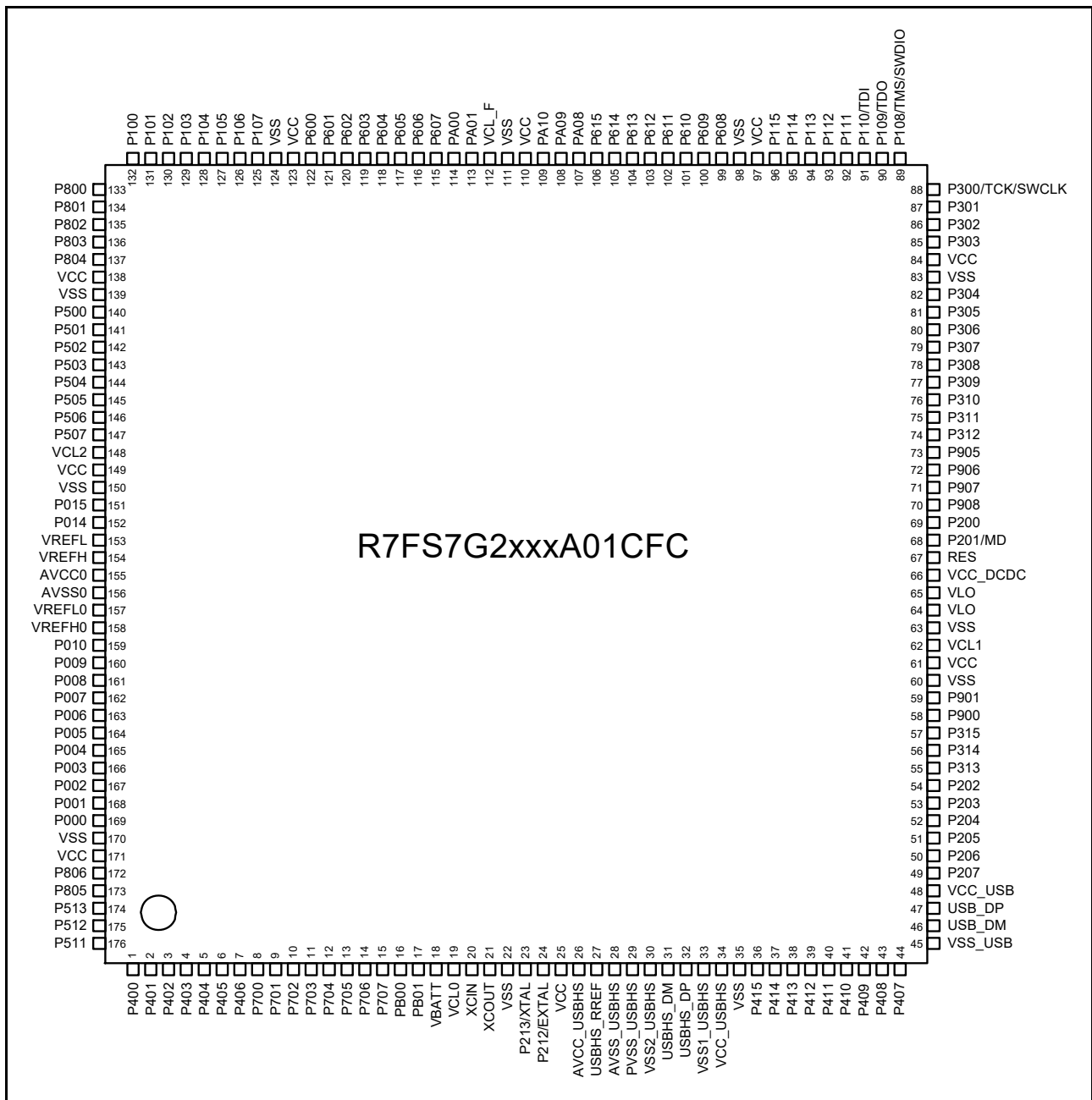


Figure 1.5 Pin assignment for 176-pin LQFP (top view)

R7FS7G2xxxA01CLK

| | A | B | C | D | E | F | G | H | J | K | L | M | N | | |
|----|--------------------|--------------------|------|----------|------|------|----------------|-------|-------|------|-------|--------|--------|-----|---|
| 13 | P407 | P409 | P412 | P708 | P711 | VCC | P212 /EXTAL | XCIN | VCL0 | P702 | P405 | P402 | P400 | 13 | |
| 12 | USB_DM | USB_DP | P410 | P414 | P710 | VSS | P213 /XTAL | XCOUT | VBATT | P701 | P404 | P511 | VCC | 12 | |
| 11 | VCC_USB | VSS_USB | P207 | P411 | P415 | P712 | P705 | P704 | P703 | P403 | P401 | P512 | VSS | 11 | |
| 10 | P205 | P206 | P204 | P408 | P413 | P709 | P713 | P700 | P406 | P003 | P000 | P002 | P001 | 10 | |
| 9 | P203 | P313 | P202 | VSS | | | | | | P004 | P006 | P009 | P008 | 9 | |
| 8 | VCL1 | VSS | P200 | VCC | | | | | | P005 | AVSS0 | VREFL0 | VREFH0 | 8 | |
| 7 | VLO | VLO | RES | P310 | | | | | | P007 | AVCC0 | VREFL | VREFH | 7 | |
| 6 | VCC_DCDC | P201/MD | P312 | P305 | | | | | | P505 | P506 | P015 | P014 | 6 | |
| 5 | P309 | P311 | P308 | P303 | NC | | | | | | P503 | P504 | VSS | VCC | 5 |
| 4 | P307 | P306 | P304 | P109/TDO | P114 | P608 | P604 | P600 | P105 | P500 | P502 | P501 | VCL2 | 4 | |
| 3 | VSS | VCC | P301 | P112 | P115 | P610 | P614 | P603 | P107 | P106 | P104 | VSS | VCC | 3 | |
| 2 | P302 | P300/TCK /SWCLK | P111 | VCC | P609 | P612 | VSS | P605 | P601 | VCC | P800 | P101 | P801 | 2 | |
| 1 | P108/TMS /SWDIO | P110/TDI | P113 | VSS | P611 | P613 | VCC | VCL_F | P602 | VSS | P103 | P102 | P100 | 1 | |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | | |

Figure 1.6 Pin assignment for 145-pin LGA (top view)

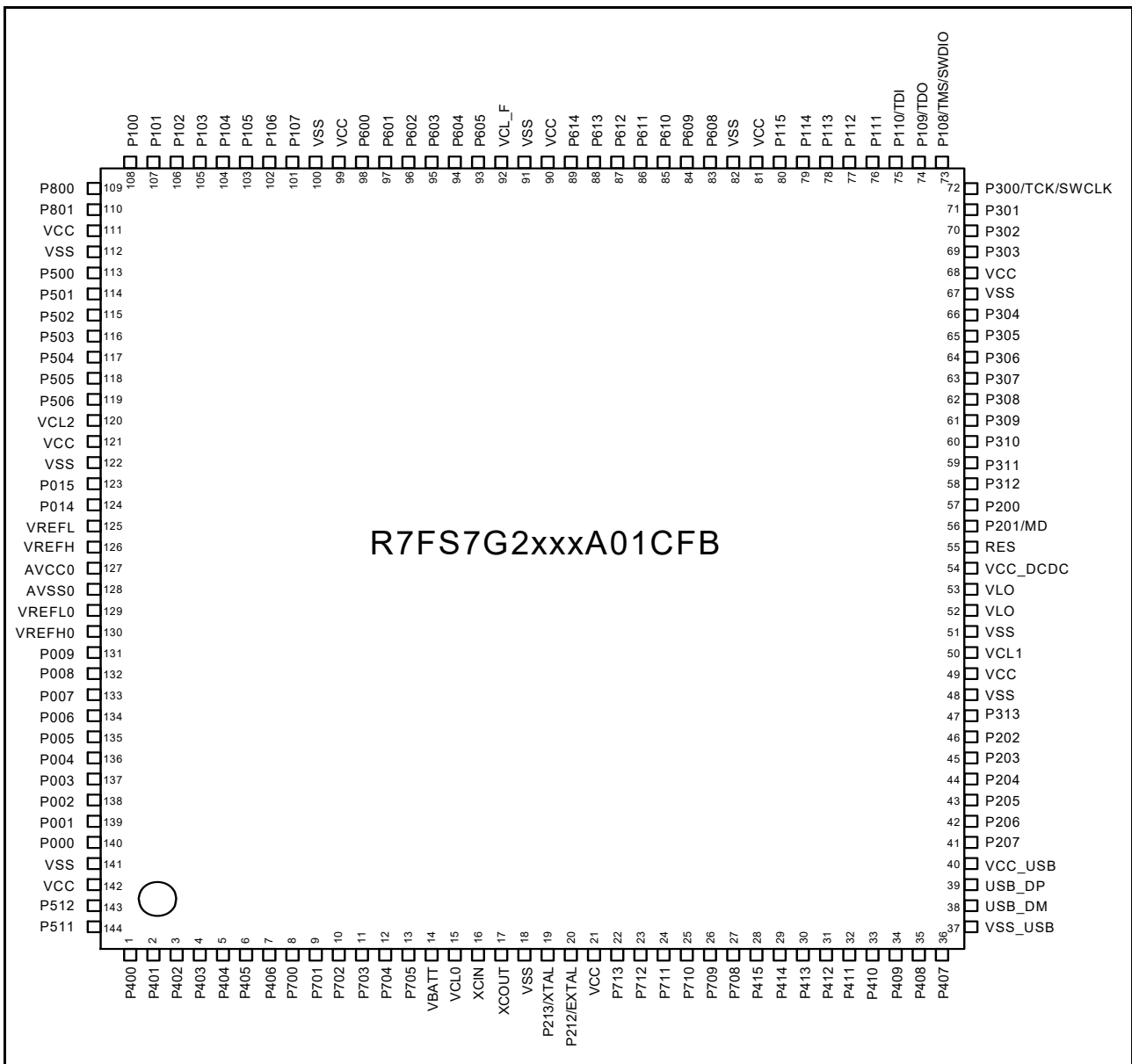


Figure 1.7 Pin assignment for 144-pin LQFP (top view)

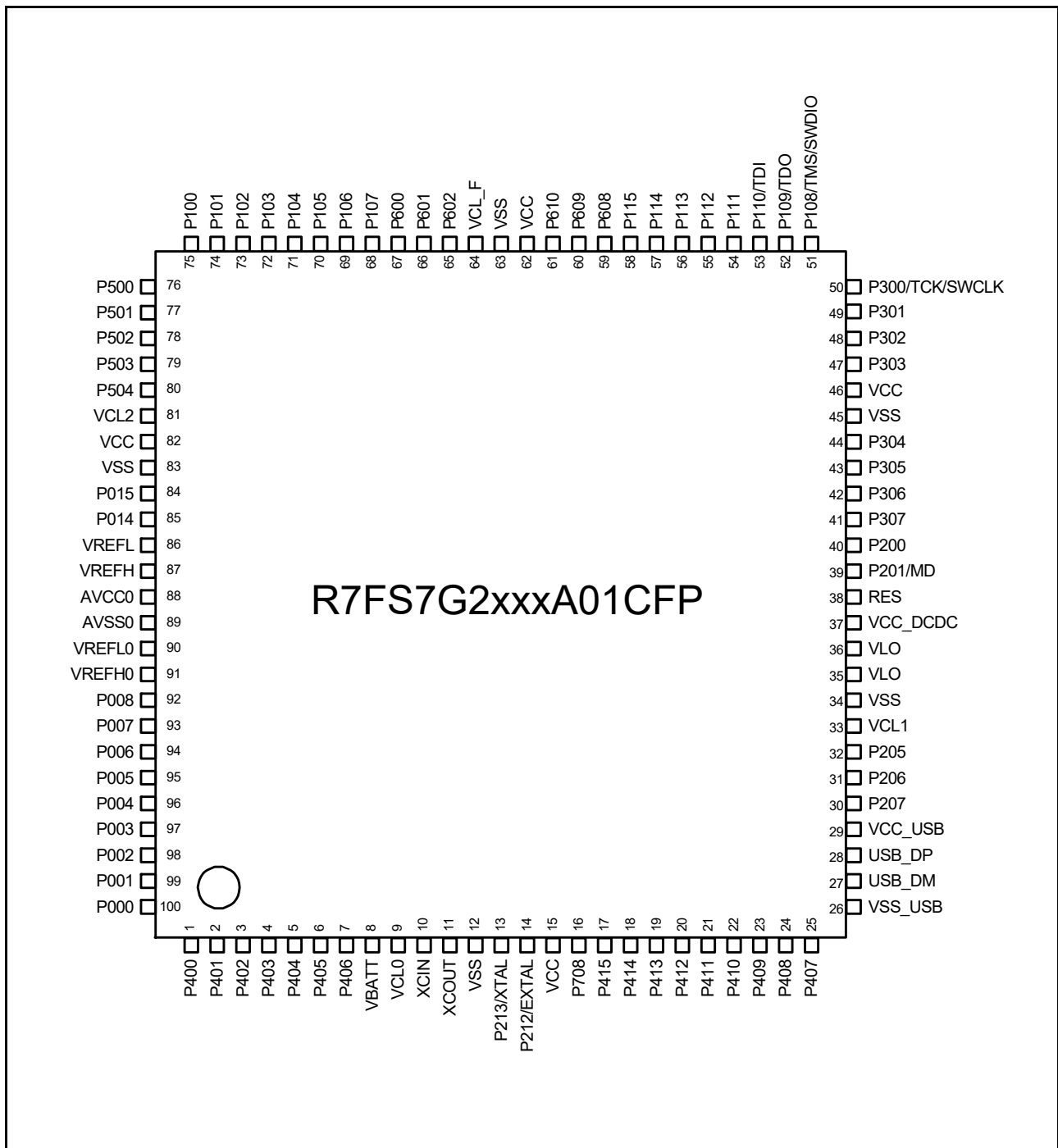


Figure 1.8 Pin assignment for 100-pin LQFP (top view)

1.7 Pin Lists

Table 1.17 Pin list (1 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | | Communication interfaces | | | | | | | | | | Analog | | HMI | | | |
|------------|--------|---------|--------|---------|---------|-----------------------------------|-----------------|----------|--------------|-------|---------------------------------------|-----------------------|-----------------------|------------|--------------------------|-----------------------------------------------|-------------------------------------------------------------|------------|-----------------------|-----------------------------|------------------------------|------------------|-------|------|--------|----------------------|------|------------|------------|---|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI1 (50 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC | | |
| N13 | N13 | 1 | N13 | 1 | 1 | - | IRQ 0 | P400 | - | - | - | - | GTI OC 6A_ A | - | - | SCK 4_B | SCK 7_A | SCL 0_A | - | AU DIO _CL _K | ET1 _TX _CL _K | - | - | - | - | AD TR G1 _B | - | - | - | |
| P15 | R15 | 2 | L11 | 2 | 2 | - | IRQ 5- DS | P401 | - | - | - | GTE TRG A_B | GTI OC 6B_ A | - | CTX 0_B | CTS 4_R TS4 _B/S S4_ B | TXD 7_A/ MO TS4 _B/S S7_ A/S DA7 _A | SDA 0_A | - | - | ET0 _M DC | ET0 _M DC | - | - | - | - | - | - | - | |
| N14 | P14 | 3 | M13 | 3 | 3 | - | IRQ 4- DS | P402 | - | - | AGT IO0_ B/A GTI O1_ B | - | - | RTC IC0 | CRX 0_B | - | RXD 7_A/ MIS O7 A/S CL7 _A | - | - | - | ET0 _M DIO | ET0 _M DIO | - | - | - | - | - | - | - | |
| N15 | M12 | 4 | K11 | 4 | 4 | - | - | P403 | - | - | AGT IO0_ C/A GTI O1_ C | GTI OC 3A_ B | RTC IC1 | - | - | CTS 7_R TS7 _A/ SS7 _A | - | - | SSI SC K0_ A | ET1 _M DC | ET1 _M DC | - | - | - | - | - | - | - | PIX D7 | |
| K10 | M13 | 5 | L12 | 5 | 5 | - | - | P404 | - | - | - | GTI OC 3B_ B | RTC IC2 | - | - | - | - | - | SSI WS 0_A | ET1 _M DIO | ET1 _M DIO | - | - | - | - | - | - | - | PIX D6 | |
| M13 | P15 | 6 | L13 | 6 | 6 | - | - | P405 | - | - | - | GTI OC 1A_ B | - | - | - | - | - | - | SSI TX D0_ A | ET1 _TX _E _N | RMI I1_ TX D_ EN | - | - | - | - | - | - | - | PIX D5 | |
| J9 | N14 | 7 | J10 | 7 | 7 | - | - | P406 | - | - | - | GTI OC 1B_ B | - | - | - | - | - | - | SSI RX D0_ A | ET1 _R X_ ER | RMI I1_ TX D1 | - | - | - | - | - | - | - | PIX D4 | |
| M14 | N15 | 8 | H10 | 8 | - | - | - | P700 | - | - | - | GTI OC 5A_ B | - | - | - | - | - | - | - | ET1 _ET XD 1 | RMI I1_ TX D0 | - | - | - | - | - | - | - | PIX D3 | |
| M15 | M14 | 9 | K12 | 9 | - | - | - | P701 | - | - | - | GTI OC 5B_ B | - | - | - | - | - | - | - | ET1 _ET XD 0 | RE F50 CK 1 | - | - | - | - | - | - | - | PIX D2 | |
| K11 | L12 | 10 | K13 | 10 | - | - | - | P702 | - | - | - | GTI OC 6A_ B | - | - | - | - | - | - | - | ET1 _E RX D1 | RMI I1_ RX D0 | - | - | - | - | - | - | - | PIX D1 | |
| J8 | M15 | 11 | J11 | 11 | - | - | - | P703 | - | - | - | GTI OC 6B_ B | - | - | - | - | - | - | - | ET1 _E RX D0 | RMI I1_ RX D1 | - | - | - | - | - | - | - | PIX D0 | |
| J10 | L13 | 12 | H11 | 12 | - | - | - | P704 | - | - | - | - | - | - | - | - | - | - | - | ET1 _R X_ CL _K | RMI I1_ RX _E _R | - | - | - | - | - | - | - | HSY NC | |
| L13 | K12 | 13 | G11 | 13 | - | - | - | P705 | - | - | - | - | - | - | - | - | - | - | - | ET1 _C RS | RMI I1_ CR S_ DV | - | - | - | - | - | - | - | PIX CLK | |
| L14 | L14 | 14 | - | - | - | - | IRQ 7 | P706 | - | - | - | - | - | - | - | RXD 3_B/ MIS O3 B/S CL3 _B | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| L15 | L15 | 15 | - | - | - | - | IRQ 8 | P707 | - | - | - | - | - | - | - | TXD 3_B/ MO SI3 _B/S DA3 _B | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| H9 | J12 | 16 | - | - | - | - | - | PB0 0 | - | - | - | - | - | - | - | SCK 3_B | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| J11 | - | - | - | - | - | - | - | PB0 2 | - | - | - | - | - | - | - | CTS 8_R TS8 _B/S S8_ B | - | - | - | ET1 _R X_ DV | - | - | - | - | - | - | - | - | - | - |

Table 1.17 Pin list (2 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | Communication interfaces | | | | | | | | | | Analog | | HMI | |
|------------|--------|---------|--------|---------|---------|--------------------------------|-----------|----------|--------------|-------|---------|-------------|-----|--------------------------|------------|-----------------------|-----------------------|-----|---------------|---------------|--------------|--------------|-------|--------|------------|---------------|------|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU |
| K12 | - | - | - | - | - | - | PB03 | - | - | - | - | - | - | - | - | - | - | - | ET1_C OL | - | - | - | - | - | - | - | |
| H10 | - | - | - | - | - | - | IRQ12 | PB04 | - | - | - | - | - | - | - | - | - | - | ET1_E RX D2 | - | - | - | - | - | - | - | |
| K13 | K13 | 17 | - | - | - | - | - | PB01 | - | - | - | - | - | - | - | - | - | - | - | - | USBHS_VBUS | - | - | - | - | - | |
| J12 | - | - | - | - | - | - | IRQ13 | PB05 | - | - | - | - | - | - | - | - | - | - | ET1_E RX D3 | - | - | - | - | - | - | - | |
| H11 | - | - | - | - | - | - | - | PB06 | - | - | - | - | - | - | - | - | - | - | ET1_W OL | ET1_W OL | - | - | - | - | - | - | |
| G11 | - | - | - | - | - | - | - | PB07 | - | - | - | - | - | - | - | - | - | - | ET1_LI NK STA | ET1_LI NK STA | - | - | - | - | - | - | |
| K14 | K14 | 18 | J12 | 14 | 8 | VBA TT | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| K15 | K15 | 19 | J13 | 15 | 9 | VCL 0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| J15 | J15 | 20 | H13 | 16 | 10 | XCI N | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| J14 | J14 | 21 | H12 | 17 | 11 | XCO UT | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| J13 | J13 | 22 | F12 | 18 | 12 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| H14 | H14 | 23 | G12 | 19 | 13 | XTA L | IRQ2 | P213 | - | - | - | GTE TRG C_A | - | - | - | - | - | - | - | - | - | - | - | - | AD TR G1_A | - | |
| H15 | H15 | 24 | G13 | 20 | 14 | EXT AL | IRQ3 | P212 | - | - | AGT EE1 | GTE TRG D_A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| H12 | H12 | 25 | F13 | 21 | 15 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| H13 | H13 | 26 | - | - | - | AVC C_U SBH S | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| G13 | G13 | 27 | - | - | - | USB HS_RREF | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| G14 | G14 | 28 | - | - | - | AVS S_U SBH S | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| G15 | G15 | 29 | - | - | - | PVS S_U SBH S | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| G12 | G12 | 30 | - | - | - | VSS 2_U SBH S | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| F15 | F15 | 31 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | USB HS_DM | - | |
| F14 | F14 | 32 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | USB HS_DP | - | |
| F12 | F12 | 33 | - | - | - | VSS 1_U SBH S | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| F13 | F13 | 34 | - | - | - | VCC_US BHS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| E15 | E15 | 35 | - | - | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |

Table 1.17 Pin list (3 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | | Timers | | | Communication interfaces | | | | | | | | | | Analog | | HMI | |
|------------|--------|---------|--------|---------|---------|--------------------------------|-----------|----------|--------------|-------|------------|--------------|-------------|-----|--------------------------|-----------------------|-----------------------|---------------|---------------|----------------|--------------|--------------|----------|------|--------|---------------|------|------------|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC |
| G10 | - | - | G10 | 22 | - | - | - | P713 | - | - | - | - | GTI OC 2A_B | - | - | - | - | - | ET1_E XO UT | ET1_E XO UT | - | - | - | - | TS1 7 | - | | |
| F11 | - | - | F11 | 23 | - | - | - | P712 | - | - | - | - | GTI OC 2B_B | - | - | - | - | - | - | - | - | - | - | - | TS1 6 | - | | |
| E12 | - | - | E13 | 24 | - | - | - | P711 | - | - | - | - | - | - | - | - | - | - | ET0_TX CL K | - | - | - | - | - | TS1 5 | - | | |
| F10 | - | - | E12 | 25 | - | - | - | P710 | - | - | - | - | - | - | - | - | - | - | ET0_TX_E R | - | - | - | - | - | TS1 4 | - | | |
| E13 | - | - | F10 | 26 | - | - | IRQ 10 | P709 | - | - | - | - | - | - | - | - | - | - | ET0_ET XD 2 | - | - | - | - | - | TS1 3 | - | | |
| D15 | - | - | D13 | 27 | 16 | CAC REF_B | IRQ 11 | P708 | - | - | - | - | - | - | - | - | - | - | ET0_ET XD 3 | - | - | - | - | - | TS1 2 | - | | |
| E14 | E14 | 36 | E11 | 28 | 17 | - | - | P415 | - | - | - | - | - | - | - | - | - | ET0_TX_E N | RMI 0_TX D_EN | - | - | - | - | - | TS1 1 | - | | |
| E11 | D15 | 37 | D12 | 29 | 18 | - | - | P414 | - | - | - | - | - | - | - | - | - | ET0_RX_X ER | RMI 0_TX D1 | - | SD0 WP | - | - | - | TS1 0 | - | | |
| D12 | E13 | 38 | E10 | 30 | 19 | - | - | P413 | - | - | GTO UUP_B | - | - | - | - | - | - | ET0_ET XD 1 | RMI 0_TX D0 | - | SD0 CLK | - | - | - | TS0 9 | - | | |
| D13 | D14 | 39 | C13 | 31 | 20 | - | - | P412 | - | - | GTO ULO_B | - | - | - | - | - | - | ET0_ET XD 0 | RE F50 CK 0 | - | SD0 CM D | - | - | - | TS0 8 | - | | |
| D14 | C15 | 40 | D11 | 32 | 21 | - | IRQ 4 | P411 | - | - | AGT OA1 | GTO VUP_B | GTI OC 9A_A | - | - | - | - | ET0_E RX D1 | RMI 0_RX D0 | - | SD0 DAT 0 | - | - | - | TS0 7 | - | | |
| C15 | C14 | 41 | C12 | 33 | 22 | - | IRQ 5 | P410 | - | - | AGT OB1 | GTO VLO_B | GTI OC 9B_A | - | - | - | - | ET0_E RX D0 | RMI 0_RX D1 | - | SD0 DAT 1 | - | - | - | TS0 6 | - | | |
| C14 | B15 | 42 | B13 | 34 | 23 | - | IRQ 6 | P409 | - | - | GTO WU_P_B | GTI OC 10A_A | - | - | - | - | - | ET0_RX_X CL K | RMI 0_RX_E R | USB HS_EXI CEN | - | - | - | - | TS0 5 | - | | |
| B15 | D13 | 43 | D10 | 35 | 24 | - | IRQ 7 | P408 | - | - | GTO WL_O_B | GTI OC 10B_A | - | - | - | - | - | ET0_C RS | RMI 0_CR S_DV | USB HS_I D | - | - | - | - | TS0 4 | - | | |
| A15 | A15 | 44 | A13 | 36 | 25 | - | - | P407 | - | - | - | - | - | - | - | - | - | ET0_E XO UT | ET0_E XO UT | - | - | - | AD TR GO | - | TS0 3 | - | | |
| B13 | C13 | 45 | B11 | 37 | 26 | VSS_US_B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | |
| B14 | B14 | 46 | A12 | 38 | 27 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | |
| A14 | A14 | 47 | B12 | 39 | 28 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | |

Table 1.17 Pin list (4 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | Communication interfaces | | | | | | | | | | Analog | | HMI | | | | | |
|------------|--------|---------|--------|---------|---------|--------------------------------|-----------|----------|--------------|-------|-----------|---------|-------------|--------------------------|------------|-----------------------|--------------------------|--------------------------|-----------|--------------|---------------|---------------|----------|--------|-------|---------------|-----------|------------|---|----------------|---|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC | | | |
| A13 | B13 | 48 | A11 | 40 | 29 | VCC_US_B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | | | |
| C13 | C12 | 49 | C11 | 41 | 30 | - | - | P207 | A17 | - | - | - | - | - | - | - | SS LB2_A | - | - | - | - | - | - | - | - | - | TS0_2 | | | | |
| G9 | D12 | 50 | B10 | 42 | 31 | - | IRQ 0-DS | P206 | WAIT | - | - | GTI U_A | - | - | - | USB_VB USE_N_A | RXD_4_A/MIS_04_A/S_CL4_A | SDA_1_A | SS LB1_A | SSI DA TA1_A | ET0_LI NK STA | ET0_LI NK STA | - | - | - | - | SD0 DAT 2 | - | - | TS0_1 | |
| C12 | E12 | 51 | A10 | 43 | 32 | CLK_OUT_A | IRQ 1-DS | P205 | A16 | - | AGT O1 | GTI V_A | GTI OC 4A_B | - | - | USB_OV RCU RA_A-DS | TXD_4_A/MO_S14_A/S_DA4_A | CTS_9_R TS9_A/SS9_A | SCL_1_A | SS LB0_A | SSI WS 1_A | ET0_W OL | ET0_W OL | - | - | - | SD0 DAT 3 | - | - | TSC AP_A | |
| D11 | A13 | 52 | C10 | 44 | - | CAC_REF_A | - | P204 | A18 | - | AGT IO1_A | GTI W_A | GTI OC 4B_B | - | - | USB_OV RCU RB_A-DS | SCK_4_A | SCK_9_A | SCL_0_B | RS PC KB_A | SSI SC K1_A | ET0_R X_DV | - | - | - | - | SD0 DAT 4 | - | - | TS0_0 | |
| B12 | D11 | 53 | A9 | 45 | - | - | IRQ 2-DS | P203 | A19 | - | - | - | GTI OC 5A_A | - | - | CTX_0_A | CTS_2_R TS2_A/S_S2_A | TXD_9_A/MO_S19_A/S_DA9_A | - | MO SIB_A | - | ET0_C OL | - | - | - | - | SD0 DAT 5 | - | - | TSC AP_B | |
| A12 | B12 | 54 | C9 | 46 | - | - | IRQ 3-DS | P202 | WR1/BC1 | - | - | - | GTI OC 5B_A | - | - | CRX_0_A | SCK_2_A | RXD_9_A/MIS_09_A/S_CL9_A | - | MIS OB_A | - | ET0_E RX D2 | - | - | - | - | SD0 DAT 6 | - | - | LCD_TC ON3_B | |
| E10 | A12 | 55 | B9 | 47 | - | - | - | P313 | A20 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | SD0 DAT 7 | - | - | LCD_TC ON2_B | |
| F9 | C11 | 56 | - | - | - | - | - | P314 | A21 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_TC ON1_B | |
| C11 | B11 | 57 | - | - | - | - | - | P315 | A22 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_TC ON0_B | |
| E9 | A11 | 58 | - | - | - | - | - | P900 | A23 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_CL K_B | |
| B11 | C10 | 59 | - | - | - | - | - | P901 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1_5_B | |
| A11 | - | - | - | - | - | - | - | P902 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA2_3_B | |
| C10 | D10 | 60 | D9 | 48 | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| D10 | D9 | 61 | D8 | 49 | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| D9 | - | - | - | - | - | - | - | P903 | - | - | - | - | GTI OC 7A_B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | SD0 CD | - | - | - |
| C9 | - | - | - | - | - | - | - | P904 | - | - | - | - | GTI OC 7B_B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A10 | A10 | 62 | A8 | 50 | 33 | VCL 1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B10 | B10 | 63 | B8 | 51 | 34 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A9 | A9 | 64 | A7 | 52 | 35 | VLO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B9 | B9 | 65 | B7 | 53 | 36 | VLO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A8 | A8 | 66 | A6 | 54 | 37 | VCC_DC DC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| H8 | - | - | - | - | - | - | - | P913 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| F8 | C9 | 67 | C7 | 55 | 38 | RES | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| C8 | B8 | 68 | B6 | 56 | 39 | MD | - | P201 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B8 | C8 | 69 | C8 | 57 | 40 | - | NMI | P200 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

Table 1.17 Pin list (5 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | | | Communication interfaces | | | | | | | | | | Analog | | | HMI | | | |
|------------|--------|---------|--------|---------|---------|--------------------------------|-----------|----------|--------------|-------|--------|-----|-------------|-----|------------|--------------------------|-----------------------|-----|-----------|-----|--------------|--------------|-------|------|-------|---------------|------|------------|-----|---|----------------|----------------|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC | | | | |
| B7 | - | - | - | - | - | - | - | P912 | - | - | - | - | GTI OC 8A_B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A7 | - | - | - | - | - | - | - | P911 | - | - | - | - | GTI OC 8B_B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| D8 | - | - | - | - | - | - | - | P910 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA2 2_B |
| E8 | - | - | - | - | - | - | - | P909 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA2 1_B | |
| E7 | D8 | 70 | - | - | - | - | - | P908 | CS7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 4_B | |
| F7 | D7 | 71 | - | - | - | - | - | P907 | CS6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 3_B | |
| F6 | A7 | 72 | - | - | - | - | - | P906 | CS5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 2_B | |
| A6 | B7 | 73 | - | - | - | - | - | P905 | CS4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 1_B |
| B6 | C7 | 74 | C6 | 58 | - | - | - | P312 | CS3 | CA S | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| C7 | D6 | 75 | B5 | 59 | - | - | - | P311 | CS2 | RA S | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA2 3_A |
| A4 | - | - | - | - | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B4 | - | - | - | - | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| C6 | A6 | 76 | D7 | 60 | - | - | - | P310 | A15 | A15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA2 2_A |
| C5 | B6 | 77 | A5 | 61 | - | - | - | P309 | A14 | A14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA2 1_A |
| D7 | A5 | 78 | C5 | 62 | - | - | - | P308 | A13 | A13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA2 0_A |
| D6 | C6 | 79 | A4 | 63 | 41 | - | - | P307 | A12 | A12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 9_A |
| D5 | A4 | 80 | B4 | 64 | 42 | - | - | P306 | A11 | A11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 8_A |
| D4 | B5 | 81 | D6 | 65 | 43 | - | IRQ 8 | P305 | A10 | A10 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 7_A |
| C4 | B4 | 82 | C4 | 66 | 44 | - | IRQ 9 | P304 | A09 | A09 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 6_A |
| A5 | C5 | 83 | A3 | 67 | 45 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B5 | D5 | 84 | B3 | 68 | 46 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| E6 | - | - | - | - | - | - | - | P915 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA2 0_B |
| E5 | - | - | - | - | - | - | - | P914 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 9_B |
| A3 | A3 | 85 | D5 | 69 | 47 | - | - | P303 | A08 | A08 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 5_A |

Table 1.17 Pin list (6 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | | Communication interfaces | | | | | | | | | | Analog | | HMI | | | |
|------------|--------|---------|--------|---------|---------|--------------------------------|-----------|----------|--------------|-----------|--------|-----------|-------------|-----|--------------------------|--------------------------|--------------------------|------------|-------------|-----|--------------|--------------|-------|------|--------|---------------|------|------------|----------------|----------------|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC | | |
| A2 | B3 | 86 | A2 | 70 | 48 | - | IRQ 5 | P302 | A07 | A07 | - | GTO UUP_A | GTI OC 4A_A | - | - | TXD 2_A/MO SI2 A/S DA2_A | - | - | SS LB3_B | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 4_A |
| B3 | A2 | 87 | C3 | 71 | 49 | - | IRQ 6 | P301 | A06 | A06 | - | GTO ULO_A | GTI OC 4B_A | - | - | RXD 2_A/MIS O2 A/S CL2_A | - | - | SS LB2_B | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 3_A |
| F5 | C4 | 88 | B2 | 72 | 50 | TCK/SW CLK | - | P300 | - | - | - | - | GTI OC 0A_A | - | - | - | - | - | SS LB1_B | - | - | - | - | - | - | - | - | - | - | |
| B2 | C3 | 89 | A1 | 73 | 51 | TMS/SW DIO | - | P108 | - | - | - | - | GTI OC 0B_A | - | - | CTS 9_R TS9_B/SS9_B | - | - | SS LB0_B | - | - | - | - | - | - | - | - | - | - | |
| B1 | A1 | 90 | D4 | 74 | 52 | CLK OUT B/T DO/SW O | - | P109 | - | - | - | GTO VUP_A | GTI OC 1A_A | - | CTX 1_A | - | TXD 9_B/MIS O9 B/S DA9_B | - | MO SIB_B | - | - | - | - | - | - | - | - | - | - | |
| C2 | D3 | 91 | B1 | 75 | 53 | TDI | IRQ 3 | P110 | - | - | - | GTO VLO_A | GTI OC 1B_A | - | CRX 1_A | CTS 2_R TS2_B/S S2_B | RXD 9_B/MIS O9 B/S CL9_B | - | MIS OB_B | - | - | - | - | - | VCO UT | - | - | - | | |
| C1 | D4 | 92 | C2 | 76 | 54 | - | IRQ 4 | P111 | A05 | A05 | - | - | GTI OC 3A_A | - | - | SCK 2_B | SCK 9_B | RS PC KB_B | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 2_A | |
| C3 | B2 | 93 | D3 | 77 | 55 | - | - | P112 | A04 | A04 | - | - | GTI OC 3B_A | - | - | TXD 2_B/MO SI2 B/S DA2_B | - | - | SSI SC KO_B | - | - | - | - | - | - | - | - | - | LCD_DA TA1 1_A | |
| D3 | B1 | 94 | C1 | 78 | 56 | - | - | P113 | A03 | A03 | - | - | - | - | - | RXD 2_B/MIS O2 B/S CL2_B | - | - | SSI WS 0_B | - | - | - | - | - | - | - | - | - | LCD_DA TA1 0_A | |
| E4 | C2 | 95 | E4 | 79 | 57 | - | - | P114 | A02 | A02 | - | - | - | - | - | - | - | - | SSI RX DO_B | - | - | - | - | - | - | - | - | - | LCD_DA TA0 9_A | |
| E3 | C1 | 96 | E3 | 80 | 58 | - | - | P115 | A01 | A01 | - | - | - | - | - | - | - | - | SSI TX DO_B | - | - | - | - | - | - | - | - | - | LCD_DA TA0 8_A | |
| D1 | E3 | 97 | D2 | 81 | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| D2 | E4 | 98 | D1 | 82 | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| F4 | D2 | 99 | F4 | 83 | 59 | - | - | P608 | A00/BC0 | A00/DQ M1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA0 7_A | |
| G4 | D1 | 100 | E2 | 84 | 60 | - | - | P609 | CS1 | CK E | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA0 6_A | |
| E1 | F3 | 101 | F3 | 85 | 61 | - | - | P610 | CS0 | WE | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA0 5_A | |
| E2 | E2 | 102 | E1 | 86 | - | - | - | P611 | - | SD CS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| F2 | E1 | 103 | F2 | 87 | - | - | - | P612 | D08 | DQ 08 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| F3 | F4 | 104 | F1 | 88 | - | - | - | P613 | D09 | DQ 09 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| F1 | F2 | 105 | G3 | 89 | - | - | - | P614 | D10 | DQ 10 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| G8 | F1 | 106 | - | - | - | - | - | P615 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 0_B | |

Table 1.17 Pin list (7 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | | Communication interfaces | | | | | | | | | | Analog | | HMI | |
|------------|--------|---------|--------|---------|---------|-----------------------------------|-----------|----------|--------------|----------|--------|-------------------------|-----|-----|--------------------------|-----------------------------------------------|--------------------------|-----|-----------|-----|-----------------|-----------------|-------|------|--------|------------------|--------------------------|------------|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC |
| G7 | G1 | 107 | - | - | - | - | - | PA0 8 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD _DA TA0 9_B | |
| G6 | - | - | - | - | - | - | - | PA11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD _DA TA1 8_B | |
| G5 | - | - | - | - | - | TCL K | - | PA1 2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| H4 | G4 | 108 | - | - | - | - | - | PA0 9 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD _DA TA0 8_B | |
| H7 | - | - | - | - | - | TDA TA0 | - | PA1 3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| G3 | - | - | - | - | - | TDA TA1 | - | PA1 4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| H5 | G2 | 109 | - | - | - | - | - | PA1 0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD _DA TA0 7_B | |
| G2 | - | - | - | - | - | TDA TA2 | - | PA1 5 | - | - | - | GTI OC 9A_ _B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| G1 | - | - | - | - | - | TDA TA3 | - | P813 | - | - | - | GTI OC 9B_ _B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| H3 | G3 | 110 | G1 | 90 | 62 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| H2 | H3 | 111 | G2 | 91 | 63 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| H1 | H1 | 112 | H1 | 92 | 64 | VCL _F | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| J1 | - | - | - | - | - | - | - | PA0 7 | - | - | - | GTI OC 10A_ _B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| J2 | - | - | - | - | - | - | - | PA0 6 | - | - | - | GTI OC 10B_ _B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| J3 | - | - | - | - | - | - | - | PA0 5 | - | - | - | GTI OC 11A_ _B | - | - | - | CTS 7_R TS7 _B/ SS7 _B | - | - | - | - | - | - | - | - | - | - | - | |
| J4 | - | - | - | - | - | - | - | PA0 4 | - | - | - | GTI OC 11B_ _B | - | - | - | SCK 7_B | - | - | - | - | - | - | - | - | - | - | - | |
| J5 | - | - | - | - | - | - | IRQ 9 | PA0 3 | - | - | - | - | - | - | - | RXD 7_B/ MIS 07 _B/S CL7 _B | - | - | - | - | - | - | - | - | - | - | - | |
| H6 | - | - | - | - | - | - | IRQ 10 | PA0 2 | - | - | - | - | - | - | - | TXD 7_B/ MO SI7 _B/S DA7 _B | - | - | - | - | - | - | - | - | - | - | - | |
| J6 | H2 | 113 | - | - | - | - | - | PA0 1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD _DA TA0 6_B | |
| J7 | H4 | 114 | - | - | - | - | - | PA0 0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD _DA TA0 5_B | |
| K5 | J4 | 115 | - | - | - | - | - | P607 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD _DA TA0 4_B | |
| K6 | J1 | 116 | - | - | - | - | - | P606 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD _DA TA0 3_B | |
| K1 | J2 | 117 | H2 | 93 | - | - | - | P605 | D11 | DQ 11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| K2 | J3 | 118 | G4 | 94 | - | - | - | P604 | D12 | DQ 12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| K3 | K3 | 119 | H3 | 95 | - | - | - | P603 | D13 | DQ 13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |

Table 1.17 Pin list (8 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | | Communication interfaces | | | | | | | | | | Analog | | HMI | |
|------------|--------|---------|--------|---------|---------|--------------------------------|-------------|----------|--------------|--------|-----------|-------------|-------------|-----|--------------------------|-----------------------|-----------------------|-----|-----------|-----|--------------|--------------|-------|------|--------|---------------|----------------|------------|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC |
| L1 | K1 | 120 | J1 | 96 | 65 | | | P602 | EBC LK | SD CLK | | | | | | | | | | | | | | | | | LCD_DA TA0 4_A | |
| L2 | K2 | 121 | J2 | 97 | 66 | | | P601 | WR/ WR0 | DQ M0 | | | | | | | | | | | | | | | | | LCD_DA TA0 3_A | |
| L3 | L1 | 122 | H4 | 98 | 67 | | | P600 | RD | | | | | | | | | | | | | | | | | | LCD_DA TA0 2_A | |
| M2 | K4 | 123 | K2 | 99 | - | VCC | | | | | | | | | | | | | | | | | | | | | | |
| M1 | L4 | 124 | K1 | 100 | - | VSS | | | | | | | | | | | | | | | | | | | | | | |
| K4 | L2 | 125 | J3 | 101 | 68 | | KR0 7 | P107 | D07 | DQ 07 | | | | | | | | | | | | | | | | | LCD_DA TA0 1_A | |
| L4 | M1 | 126 | K3 | 102 | 69 | | KR0 6 | P106 | D06 | DQ 06 | | | | | | | | | | | | | | | | | LCD_DA TA0 0_A | |
| M3 | L3 | 127 | J4 | 103 | 70 | | IRQ 0/K R05 | P105 | D05 | DQ 05 | | | | | | | | | | | | | | | | | LCD_TC ON3_A | |
| N3 | M2 | 128 | L3 | 104 | 71 | | IRQ 1/K R04 | P104 | D04 | DQ 04 | | | | | | | | | | | | | | | | | LCD_TC ON2_A | |
| N2 | N1 | 129 | L1 | 105 | 72 | | KR0 3 | P103 | D03 | DQ 03 | | | | | | | | | | | | | | | | | LCD_TC ON1_A | |
| N1 | M3 | 130 | M1 | 106 | 73 | | KR0 2 | P102 | D02 | DQ 02 | AGT 00 | GTO WL O_A | GTI OC 2B_A | | | | | | | | | | | | | | LCD_TC ON0_A | |
| P1 | N2 | 131 | M2 | 107 | 74 | | IRQ 1/K R01 | P101 | D01 | DQ 01 | AGT EE0 | GTE TRG B_A | | | | | | | | | | | | | | | LCD_CL K_A | |
| R1 | P1 | 132 | N1 | 108 | 75 | | IRQ 2/K R00 | P100 | D00 | DQ 00 | AGT IO0_A | GTE TRG A_A | | | | | | | | | | | | | | | LCD_EX TCL K_A | |
| P2 | N3 | 133 | L2 | 109 | - | | | P800 | D14 | DQ 14 | | | | | | | | | | | | | | | | | | |
| R2 | R1 | 134 | N2 | 110 | - | | | P801 | D15 | DQ 15 | | | | | | | | | | | | | | | | | | |
| K7 | - | - | - | - | - | | | P808 | - | - | | | | | | | | | | | | | | | | | | |
| K8 | - | - | - | - | - | | | P809 | - | - | | | | | | | | | | | | | | | | | | |
| P3 | - | - | - | - | - | | | P810 | - | - | | | | | | | | | | | | | | | | | | |
| R3 | P2 | 135 | - | - | - | | | P802 | - | - | | | | | | | | | | | | | | | | | LCD_DA TA0 2_B | |
| P4 | R2 | 136 | - | - | - | | | P803 | - | - | | | | | | | | | | | | | | | | | LCD_DA TA0 1_B | |
| M4 | P3 | 137 | - | - | - | | | P804 | - | - | | | | | | | | | | | | | | | | | LCD_DA TA0 0_B | |
| L5 | - | - | - | - | - | | | P811 | - | - | | | | | | | | | | | | | | | | | | |
| L6 | - | - | - | - | - | | | P812 | - | - | | | | | | | | | | | | | | | | | | |
| L7 | N4 | 138 | N3 | 111 | - | VCC | | | | | | | | | | | | | | | | | | | | | | |
| L8 | M4 | 139 | M3 | 112 | - | VSS | | | | | | | | | | | | | | | | | | | | | | |

Table 1.17 Pin list (9 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | | Timers | | | Communication interfaces | | | | | | | | | | Analog | | HMI | |
|------------|--------|---------|--------|---------|---------|--------------------------------|-----------|----------|--------------|-------|---------|-------------|-------------|-----|--------------------------|-----------------------|-------------------------|-------------------|-----------|-----|--------------|--------------|-------------|------------|--------|---------------|------|------------|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC |
| R4 | R3 | 140 | K4 | 113 | 76 | - | - | P500 | - | - | AGT_OA0 | GTV_U_B | GTV_OC11A_A | - | - | USB_VB_USE_N_B | - | - | - | - | - | - | SD1_CLK | AN016 | IVREF0 | - | - | |
| N4 | P4 | 141 | M4 | 114 | 77 | - | IRQ11 | P501 | - | - | AGT_OB0 | GTV_V_B | GTV_OC11B_A | - | - | USB_OV_RCU_RA_B | - | - | - | - | - | - | SD1_CMD | AN116 | IVREF1 | - | - | |
| N5 | R4 | 142 | L4 | 115 | 78 | - | IRQ12 | P502 | - | - | - | GTV_W_B | GTV_OC12A | - | - | USB_OV_RCU_RB_B | - | - | - | - | - | - | SD1_DAT0 | AN017 | IVCMP0 | - | - | |
| P5 | N5 | 143 | K5 | 116 | 79 | - | - | P503 | - | - | - | GTE_TRG_C_B | GTV_OC12B | - | - | USB_EXI_CEN_B | CTS6_RTS6_B/S_S6_B | SCK5_A | - | - | - | - | SD1_DAT1 | AN117 | - | - | - | |
| R5 | P5 | 144 | L5 | 117 | 80 | - | - | P504 | - | - | - | GTE_TRG_D_B | GTV_OC13A | - | - | USB_ID_B | SCK6_B | CTS5_RTS5_A/SS5_A | - | - | - | - | SD1_DAT2 | AN018 | - | - | - | |
| M5 | P6 | 145 | K6 | 118 | - | - | IRQ14 | P505 | - | - | - | - | GTV_OC13B | - | - | - | RXD6_B/MIS06_B/S_CL6_B | - | - | - | - | - | SD1_DAT3 | AN118 | - | - | - | |
| M6 | R5 | 146 | L6 | 119 | - | - | IRQ15 | P506 | - | - | - | - | - | - | - | - | TXD6_B/MO_S16_B/S_DA6_B | - | - | - | - | - | SD1_CD | AN019 | - | - | - | |
| N6 | N6 | 147 | - | - | - | - | - | P507 | - | - | - | - | - | - | - | - | CTS5_RTS5_B/SS5_B | - | - | - | - | - | SD1_WP | AN119 | - | - | - | |
| M7 | - | - | - | - | - | - | - | P508 | - | - | - | - | - | - | - | - | SCK5_B | - | - | - | - | - | AN020 | - | - | - | - | |
| P6 | - | - | - | - | - | - | - | P509 | - | - | - | - | - | - | - | - | TXD5_B/MO_S15_B/S_DA5_B | - | - | - | - | - | AN120 | - | - | - | - | |
| N7 | - | - | - | - | - | - | - | P510 | - | - | - | - | - | - | - | - | RXD5_B/MIS05_B/S_CL5_B | - | - | - | - | - | AN021 | - | - | - | - | |
| R6 | R6 | 148 | N4 | 120 | 81 | VCL2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| P7 | M7 | 149 | N5 | 121 | 82 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| R7 | N7 | 150 | M5 | 122 | 83 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| M8 | P7 | 151 | M6 | 123 | 84 | - | IRQ13 | P015 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN006/AN106 | DA1/IVCMP1 | - | - | - | |
| M9 | R7 | 152 | N6 | 124 | 85 | - | - | P014 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN005/AN105 | DA0/IVREF3 | - | - | - | |
| N8 | P8 | 153 | M7 | 125 | 86 | VREFL | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| R8 | R8 | 154 | N7 | 126 | 87 | VREFH | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| P8 | N8 | 155 | L7 | 127 | 88 | AVCC0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| N9 | N9 | 156 | L8 | 128 | 89 | AVSS0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| P9 | P9 | 157 | M8 | 129 | 90 | VREFL0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| R9 | R9 | 158 | N8 | 130 | 91 | VREFH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |

Table 1.17 Pin list (10 of 10)

| Pin number | | | | | | Power, System, CLK, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | Communication interfaces | | | | | | | | | | Analog | | HMI | |
|------------|--------|---------|--------|---------|---------|--------------------------------|-----------|----------|--------------|-------|--------|-------------|-----|--------------------------|--------------------------|-----------------------|-----------------------|-----|-----------|-------------|--------------|--------------|--------------|---------|-------|----------------|--------|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMI (60 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU |
| N10 | - | - | - | - | - | - | IRQ 15-DS | P011 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 104 | - | - | - | |
| M10 | M8 | 159 | - | - | - | - | IRQ 14-DS | P010 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 103 | - | - | - | |
| R10 | M9 | 160 | M9 | 131 | - | - | IRQ 13-DS | P009 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 004 | - | - | - | |
| N11 | P10 | 161 | N9 | 132 | 92 | - | IRQ 12-DS | P008 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 003 | - | - | - | |
| L9 | M6 | 162 | K7 | 133 | 93 | - | - | P007 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PG AV SS 100 | - | - | - | |
| P10 | N10 | 163 | L9 | 134 | 94 | - | IRQ 11-DS | P006 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 102 | IVC MP2 | - | - | |
| R11 | R10 | 164 | K8 | 135 | 95 | - | IRQ 10-DS | P005 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 101 | IVC MP2 | - | - | |
| M11 | P11 | 165 | K9 | 136 | 96 | - | IRQ 9-DS | P004 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 100 | IVC MP2 | - | - | |
| L10 | M5 | 166 | K10 | 137 | 97 | - | - | P003 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PG AV SS 000 | - | - | - | |
| N12 | R11 | 167 | M10 | 138 | 98 | - | IRQ 8-DS | P002 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 002 | IVC MP2 | - | - | |
| P11 | N11 | 168 | N10 | 139 | 99 | - | IRQ 7-DS | P001 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 001 | IVC MP2 | - | - | |
| R12 | R12 | 169 | L10 | 140 | 100 | - | IRQ 6-DS | P000 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN 000 | IVC MP2 | - | - | |
| L11 | M10 | 170 | N11 | 141 | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| L12 | M11 | 171 | N12 | 142 | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| M12 | P12 | 172 | - | - | - | - | - | P806 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_EX TCL K_B | |
| R13 | R13 | 173 | - | - | - | - | - | P805 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 7_B | |
| P12 | - | - | - | - | - | - | - | P807 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| P13 | N12 | 174 | - | - | - | - | - | P513 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DA TA1 6_B | |
| K9 | - | - | - | - | - | - | - | P515 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| R14 | R14 | 175 | M11 | 143 | - | - | IRQ 14 | P512 | - | - | - | GTI OC 0A_B | - | CTX 1_B | TXD 4_B/MO SI4_B/S DA4_B | - | SCL 2 | - | - | ET1_ET XD 2 | - | - | - | - | - | - | VSY NC |
| P14 | - | - | - | - | - | - | - | P514 | - | - | - | GTE TRG B_C | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| R15 | P13 | 176 | M12 | 144 | - | - | IRQ 15 | P511 | - | - | - | GTI OC 0B_B | - | CRX 1_B | RXD 4_B/MIS O4_B/S CL4_B | - | SDA 2 | - | - | ET1_TX_ER | - | - | - | - | - | - | PCK O |

Note: Some pin names have the added suffix of _A, _B, and _C. When assigning the IIC, SPI, and SSI functionality, select the functional pins with the same suffix. The other pins can be selected regardless of the suffix.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

$VCC = AVCC0 = VCC_USB = VBATT = 2.7$ to 3.6 V, $2.7 \leq VREFH0/VREFH \leq AVCC0$, $VCC_USBHS = AVCC_USBHS = 3.0$ to 3.6 V, $VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0$ V, $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

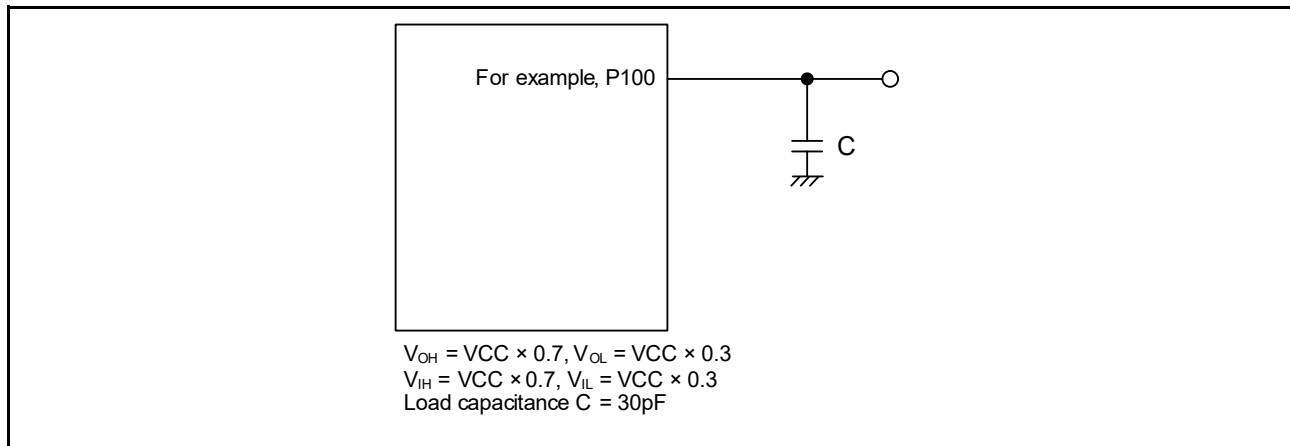


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specification for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

| Item | Symbol | Value | Unit |
|------------------------------------------------------------------------------------------|--------------------|-------------------------------|------|
| Power supply voltage | VCC, VCC_USB *2 | -0.3 to +4.6 | V |
| VBATT power supply voltage | VBATT | -0.3 to +4.6 | V |
| Input voltage (except for 5V-tolerant ports*1) | V_{in} | -0.3 to $VCC + 0.3$ | V |
| Input voltage (5V-tolerant ports*1) | V_{in} | -0.3 to $VCC + 4.6$ (max 5.8) | V |
| Reference power supply voltage | $VREFH/VREFH0$ | -0.3 to $AVCC0 + 0.3$ | V |
| Analog power supply voltage | $AVCC0$ *2 | -0.3 to +4.6 | V |
| USBHS power supply voltage | VCC_USBHS | -0.3 to +4.6 | V |
| USBHS analog power supply voltage | $AVCC_USBHS$ | -0.3 to +4.6 | V |
| Switching regulator power supply voltage | VCC_DCDC | -0.3 to +4.6 | V |
| Analog input voltage (except for P000 to P007) | V_{AN} | -0.3 to $AVCC0 + 0.3$ | V |
| Analog input voltage (P000 to P007) when PGA differential input is disabled | V_{AN} | -0.3 to $AVCC0 + 0.3$ | V |
| Analog input voltage (P000 to P002, P004 to P006) when PGA differential input is enabled | V_{AN} | -1.1 to $AVCC0 + 0.3$ | V |
| Analog input voltage (P003, P007) when PGA differential input is enabled | V_{AN} | -0.6 to $AVCC0 + 0.3$ | V |
| Operating temperature*3,*4 | T_{opr} | -40 to +85 -40 to +105 | °C |
| Storage temperature | T_{stg} | -55 to +125 | °C |

Note: See the Total Operating Time (TOT) Utility Calculator located under <http://www.renesas.com>. This utility calculator is provided for educational and evaluation purposes only and is subject to the accompanying disclaimer.

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, and PB01 are 5V-tolerant.

Note 2. Connect AVCC0 and VCC_USB to VCC.

Note 3. See [section 2.2.1, Tj/Ta Definition](#).

Note 4. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see [section 1.3, Part Numbering](#).

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

| Item | Symbol | Value | Min | Typ | Max | Unit |
|------------------------------------------|---------------------------------------------------------------------|--------------------------------------|-----|-----|-----|------|
| Power supply voltages | VCC | When USB/SDRAM is not used | 2.7 | - | 3.6 | V |
| | | When USB/SDRAM is used | 3.0 | - | 3.6 | V |
| | VSS | | - | 0 | - | V |
| USB power supply voltages | VCC_USB, VCC_USBHS | | - | VCC | - | V |
| | VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS | | - | 0 | - | V |
| Switching regulator power supply voltage | VCC_DCDC | When switching regulator is used | - | VCC | - | V |
| | | When switching regulator is not used | - | 0 | - | V |
| VBATT power supply voltage | VBATT | | 2.0 | | 3.6 | V |
| Analog power supply voltages | AVCC0 | | - | VCC | - | V |
| | AVSS0 | | - | 0 | - | V |

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T_a) -40 to +105°C

| Item | Symbol | Typ | Max | Unit | Test conditions |
|----------------------------------|--------|-----|-------|------|--------------------------------------------------------|
| Permissible junction temperature | Tj | - | 125 | °C | High-speed mode Low-speed mode Subosc-speed mode |
| | | | 105*1 | | |

Note: Make sure that $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$, where total power consumption = $(V_{CC} - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times V_{CC}$.

Note 1. The upper limit of operating temperature is 85°C or 105°C depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature as 85°C, then the maximum value of Tj is 105°C, otherwise it is 125°C.

2.2.2 I/O V_{IH} , V_{IL} Table 2.4 I/O V_{IH} , V_{IL}

| Item | | | | Symbol | Min | Typ | Max | Unit | | |
|----------------------------------------------------------|----------------------------------------|-----------------------------------------|-------------------------|--------------------------------------------|-------------------|------------------------|--------------------------|--------------------------------------------------------|------------------|---|
| Input voltage (except for Schmitt trigger input pins) | Peripheral function pin | EXTAL (external clock input), WAIT, SPI | | V_{IH} | $VCC \times 0.8$ | - | - | V | | |
| | | | | V_{IL} | - | - | $VCC \times 0.2$ | | | |
| | | D00 to D15, DQ00 to DQ15 | | V_{IH} | $VCC \times 0.7$ | - | - | | | |
| | | | | V_{IL} | - | - | $VCC \times 0.3$ | | | |
| | | ETHERC | | V_{IH} | 2.3 | - | - | | | |
| | | | | V_{IL} | - | - | $VCC \times 0.2$ | | | |
| | | IIC (SMBus)*1 | | V_{IH} | 2.1 | - | - | | | |
| | | | | V_{IL} | - | - | 0.8 | | | |
| | | IIC (SMBus)*2 | | V_{IH} | 2.1 | - | - | | | |
| | | | | V_{IL} | - | - | 0.8 | | | |
| | | Schmitt trigger input voltage | Peripheral function pin | IIC (except for SMBus)*1 | | V_{IH} | $VCC \times 0.7$ | - | - | V |
| | | | | | | V_{IL} | - | - | $VCC \times 0.3$ | |
| ΔV_T | $VCC \times 0.05$ | | | | | - | - | | | |
| IIC (except for SMBus)*2 | | | | V_{IH} | $VCC \times 0.7$ | - | $VCC + 3.6$ (max 5.8) | | | |
| | | | | V_{IL} | - | - | $VCC \times 0.3$ | | | |
| | | | | ΔV_T | $VCC \times 0.05$ | - | - | | | |
| 5V-tolerant ports*3*7 | | | | V_{IH} | $VCC \times 0.8$ | - | $VCC + 3.6$ (max 5.8) | | | |
| | | | | V_{IL} | - | - | $VCC \times 0.2$ | | | |
| | | | | ΔV_T | $VCC \times 0.05$ | - | - | | | |
| RTCIC0, RTCIC1, RTCIC2 | When using the Battery Backup Function | | | When VBATT power supply is selected | V_{IH} | $V_{BATT} \times 0.8$ | - | $V_{BATT} + 0.3$ | | |
| | | | | | V_{IL} | - | - | $V_{BATT} \times 0.2$ | | |
| | | | | | ΔV_T | $V_{BATT} \times 0.05$ | - | - | | |
| | | | | When VCC power supply is selected | V_{IH} | $VCC \times 0.8$ | - | Higher voltage, either $VCC + 0.3$ or $V_{BATT} + 0.3$ | | |
| | | | | | V_{IL} | - | - | $VCC \times 0.2$ | | |
| | | | | | ΔV_T | $VCC \times 0.05$ | - | - | | |
| | | | | When not using the Battery Backup Function | V_{IH} | $VCC \times 0.8$ | - | $VCC + 0.3$ | | |
| | | | | | V_{IL} | - | - | $VCC \times 0.2$ | | |
| | | | | | ΔV_T | $VCC \times 0.05$ | - | - | | |
| Other input pins*4 | | | | V_{IH} | $VCC \times 0.8$ | - | - | | | |
| | | | | V_{IL} | - | - | $VCC \times 0.2$ | | | |
| | | | | ΔV_T | $VCC \times 0.05$ | - | - | | | |
| Ports | 5V-tolerant ports*5*7 | | | V_{IH} | $VCC \times 0.8$ | - | $VCC + 3.6$ (max 5.8) | | | |
| | | | | V_{IL} | - | - | $VCC \times 0.2$ | | | |
| | | | | V_{IH} | $VCC \times 0.8$ | - | - | | | |
| | | V_{IL} | - | - | $VCC \times 0.2$ | | | | | |

Note 1. SCL0_B, SCL1_B, SDA1_B (total 3 pins).

Note 2. SCL0_A, SDA0_A, SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 7 pins).

Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 23 pins).

Note 4. All input pins except for the peripheral function pins already described in the table.

Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 22 pins).

Note 6. All input pins except for the ports already described in the table.

Note 7. When VCC is less than 2.7 V, the input voltage of 5V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5V-tolerant ports are electrically controlled so as not to violate the break down voltage.

2.2.3 I/O I_{OH} , I_{OL}

Table 2.5 I/O I_{OH} , I_{OL} (1 of 2)

| Item | | | Symbol | Min | Typ | Max | Unit | |
|-------------------------------------------------------|-------------------------------------------------------------------------------------------------------|----------------|----------|----------|-----|------|------|----|
| Permissible output current (average value per pin) | Ports P008 to P011, P201,P212 | - | I_{OH} | - | -- | -2.0 | mA | |
| | | | I_{OL} | - | - | 2.0 | mA | |
| | Ports P014, P015, P213, P400, P401, P511, P512 | - | I_{OH} | - | - | -4.0 | mA | |
| | | | I_{OL} | - | - | 4.0 | mA | |
| | Ports P402 to P404 | Low drive*1 | | I_{OH} | - | - | -2.0 | mA |
| | | | | I_{OL} | - | - | 2.0 | mA |
| | | Middle drive*2 | | I_{OH} | - | - | -4.0 | mA |
| | | | | I_{OL} | - | - | 4.0 | mA |
| | Ports P205, P206, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01 (total 24 pins) | Low drive*1 | | I_{OH} | - | - | -2.0 | mA |
| | | | | I_{OL} | - | - | 2.0 | mA |
| | | Middle drive*2 | | I_{OH} | - | - | -4.0 | mA |
| | | | | I_{OL} | - | - | 4.0 | mA |
| | | High drive*3 | | I_{OH} | - | - | -20 | mA |
| | | | | I_{OL} | - | - | 20 | mA |
| | Other output pins*4 | Low drive*1 | | I_{OH} | - | - | -2.0 | mA |
| | | | | I_{OL} | - | - | 2.0 | mA |
| | | Middle drive*2 | | I_{OH} | - | - | -4.0 | mA |
| | | | | I_{OL} | - | - | 4.0 | mA |
| | | High drive*3 | | I_{OH} | - | - | -16 | mA |
| | | | | I_{OL} | - | - | 16 | mA |
| Permissible output current (max value per pin) | Ports P008 to P011, P201,P212 | - | I_{OH} | - | - | -4.0 | mA | |
| | | | I_{OL} | - | - | 4.0 | mA | |
| | Ports P014, P015, P213, P400, P401, P511, P512 | - | I_{OH} | - | - | -8.0 | mA | |
| | | | I_{OL} | - | - | 8.0 | mA | |
| | Ports P402 to P404 | Low drive*1 | | I_{OH} | - | - | -4.0 | mA |
| | | | | I_{OL} | - | - | 4.0 | mA |
| | | Middle drive*2 | | I_{OH} | - | - | -8.0 | mA |
| | | | | I_{OL} | - | - | 8.0 | mA |
| | Ports P205, P206, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01 (total 24 pins) | Low drive*1 | | I_{OH} | - | - | -4.0 | mA |
| | | | | I_{OL} | - | - | 4.0 | mA |
| | | Middle drive*2 | | I_{OH} | - | - | -8.0 | mA |
| | | | | I_{OL} | - | - | 8.0 | mA |
| | | High drive*3 | | I_{OH} | - | - | -40 | mA |
| | | | | I_{OL} | - | - | 40 | mA |
| | Other output pins*4 | Low drive*1 | | I_{OH} | - | - | -4.0 | mA |
| | | | | I_{OL} | - | - | 4.0 | mA |
| | | Middle drive*2 | | I_{OH} | - | - | -8.0 | mA |
| | | | | I_{OL} | - | - | 8.0 | mA |
| | | High drive*3 | | I_{OH} | - | - | -32 | mA |
| | | | | I_{OL} | - | - | 32 | mA |

Table 2.5 I/O I_{OH} , I_{OL} (2 of 2)

| Item | | Symbol | Min | Typ | Max | Unit |
|------------------------------------------------------|----------------------------|-----------------------|-----|-----|-----|------|
| Permissible output current (max value total pins) | Maximum of all output pins | $\Sigma I_{OH} (max)$ | - | - | -80 | mA |
| | | $\Sigma I_{OL} (max)$ | - | - | 80 | mA |

Note 1. This is the value when low driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 2. This is the value when middle driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 3. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. When the following ports are configured for high driving ability, they shift to middle driving ability during Deep Software Standby mode: P203 to P207, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01.

Note 4. Except for P000 to P007, P200, which are input ports.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in the preceding table. The average output current indicates the average value of current measured during 100 μ s.

2.2.4 I/O V_{OH} , V_{OL} , and Other Characteristics

Table 2.6 I/O V_{OH} , V_{OL} , and other characteristics

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions |
|-----------------------------------------|------------------------------------------------------------------------------------------------------|------------|-----------|-----|-----|---------|--------------------------------------------------------------------|
| Output voltage | IIC | V_{OL} | - | - | 0.4 | V | $I_{OL} = 3.0$ mA |
| | | V_{OL} | - | - | 0.6 | | $I_{OL} = 6.0$ mA |
| | IIC*1 | V_{OL} | - | - | 0.4 | | $I_{OL} = 15.0$ mA (ICFER.FMPE = 1) |
| | | V_{OL} | - | 0.4 | - | | $I_{OL} = 20.0$ mA (ICFER.FMPE = 1) |
| | ETHERC | V_{OH} | VCC - 0.5 | - | - | | $I_{OH} = -1.0$ mA |
| | | V_{OL} | - | - | 0.4 | | $I_{OL} = 1.0$ mA |
| | Ports P205, P206, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01 (total 24 pins)*2 | V_{OH} | VCC - 1.0 | - | - | | $I_{OH} = -20$ mA VCC = 3.3 V |
| | | V_{OL} | - | - | 1.0 | | $I_{OL} = 20$ mA VCC = 3.3 V |
| | Other output pins | V_{OH} | VCC - 0.5 | - | - | | $I_{OH} = -1.0$ mA |
| | | V_{OL} | - | - | 0.5 | | $I_{OL} = 1.0$ mA |
| Input leakage current | RES | $ I_{in} $ | - | - | 5.0 | μ A | $V_{in} = 0$ V $V_{in} = 5.5$ V |
| | Ports P000 to P007, P200 | | - | - | 1.0 | | $V_{in} = 0$ V $V_{in} = VCC$ |
| Three-state leakage current (off state) | 5V-tolerant ports | $ I_{TS} $ | - | - | 5.0 | μ A | $V_{in} = 0$ V $V_{in} = 5.5$ V |
| | Other ports (except for ports P000 to P007, P200) | | - | - | 1.0 | | $V_{in} = 0$ V $V_{in} = VCC$ |
| Input pull-up MOS current | Ports P0 to PB (except for ports P000 to P007) | I_p | -300 | - | -10 | μ A | VCC = 2.7 to 3.6 V $V_{in} = 0$ V |
| Input capacitance | USB_DP, USB_DM, and ports P003, P007, P014, P015, P400, P415, P401, P511, P512 | C_{in} | - | - | 16 | pF | $V_{bias} = 0$ V Vamp = 20mV f = 1 MHz $T_a = 25^\circ$ C |
| | Other input pins | | - | - | 8 | | |

Note 1. SCL0_A, SDA0_A (total 2 pins).

Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. Even when high driving ability is selected, I_{OH} and I_{OL} shift to middle driving ability during Deep Software Standby mode.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1 of 2)

| Item | Symbol | LDO mode | | | DCDC mode | | | Unit | Test conditions | | | | | |
|------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|--------------------------------------------------------------|-----------------------------------------------------------------------|--------------------------------------------------------|-----------|-----|------|------|-----------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|-------------------|-----|----|-------------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | | | | | | | |
| Supply current*1 | Maximum*2 | I _{CC} *7 | - | - | 330 | - | - | 140 | mA | ICLK = 240 MHz PCLKA = 120 MHz*6 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz | | | | |
| | CoreMark®*4 | | - | 45 | - | - | 24 | - | | | | | | |
| | Normal mode*3 | | All peripheral clocks enabled, while (1) code executing from flash | - | 75 | - | - | 38 | | | - | | | |
| | | | All peripheral clocks disabled, while (1) code executing from flash*5 | - | 32 | - | - | 18 | | | - | | | |
| | Sleep mode*4 *5 | | - | 25 | 150 | - | 15 | 75 | | | | | | |
| | Increase during BGO operation | | Data flash P/E | - | 7 | - | - | 7 | | | - | | | |
| | | | Code flash P/E | - | 10 | - | - | 10 | | | - | | | |
| | Low-speed mode*4 | | - | 4.4 | - | - | 3 | - | | | ICLK = 1 MHz | | | |
| | Subosc-speed mode*4 | | - | 3 | - | - | 2 | - | | | ICLK = 32.768 kHz | | | |
| | Software Standby mode | | - | 2.4 | 110 | - | 1.2 | 55 | | | - | | | |
| | Deep Software Standby mode | | Power supplied to Standby SRAM and USB resume detecting unit | | - | 37 | 255 | - | | | 37 | 255 | μA | V _{BATT} ≠ V _{CC} |
| | | | | | - | 37 | 285 | - | | | 37 | 285 | μA | V _{BATT} = V _{CC} |
| | | | Power not supplied to SRAM or USB resume detecting unit | Power-on reset circuit low-power function disabled | - | 25 | 50 | - | | | 25 | 50 | μA | V _{BATT} ≠ V _{CC} |
| | | | | Power-on reset circuit low-power function enabled | - | 25 | 80 | - | | | 25 | 80 | μA | V _{BATT} = V _{CC} |
| | | | Increase when the RTC and AGT are operating | When the low-speed on-chip oscillator (LOCO) is in use | - | 16 | 35 | - | | | 16 | 35 | μA | V _{BATT} ≠ V _{CC} |
| When a crystal oscillator for low clock loads is in use | | - | | 16 | 65 | - | 16 | 65 | μA | V _{BATT} = V _{CC} | | | | |
| When a crystal oscillator for standard clock loads is in use | | - | | 9 | - | - | 9 | - | μA | - | | | | |
| RTC operating while V _{CC} is off (with the battery backup function, only the RTC and sub-clock oscillator operate) | | When a crystal oscillator for low clock loads is in use | - | 1.0 | - | - | 1.0 | - | μA | - | | | | |
| | | When a crystal oscillator for standard clock loads is in use | - | 3.0 | - | - | 3.0 | - | μA | - | | | | |
| | | | - | 0.9 | - | - | 0.9 | - | μA | V _{BATT} = 2.0 V, V _{CC} = 0 V | | | | |
| | | - | 1.6 | - | - | 1.6 | - | μA | V _{BATT} = 3.3 V, V _{CC} = 0 V | | | | | |
| | | - | 1.7 | - | - | 1.7 | - | μA | V _{BATT} = 2.0 V, V _{CC} = 0 V | | | | | |
| | | - | 3.3 | - | - | 3.3 | - | μA | V _{BATT} = 3.3 V, V _{CC} = 0 V | | | | | |
| Analog power supply current | During 12-bit A/D conversion | | - | 0.8 | 1.1 | - | 0.8 | 1.1 | mA | - | | | | |
| | During 12-bit A/D conversion with S/H amp | | - | 2.3 | 3.3 | - | 2.3 | 3.3 | mA | - | | | | |
| | PGA (1ch) | | - | 1 | 3 | - | 1 | 3 | mA | - | | | | |
| | ACMPHS (1unit) | | - | 100 | 150 | - | 100 | 150 | μA | - | | | | |
| | Temperature sensor | | - | 0.1 | 0.2 | - | 0.1 | 0.2 | mA | - | | | | |
| | During D/A conversion (per unit) | Without AMP output | - | 0.1 | 0.2 | - | 0.1 | 0.2 | mA | - | | | | |
| | | With AMP output | - | 0.5 | 0.8 | - | 0.5 | 0.8 | mA | - | | | | |
| | Waiting for A/D, D/A conversion (all units) | | - | 0.9 | 1.6 | - | 0.9 | 1.6 | mA | - | | | | |
| | ADC12, DAC12 in standby modes (all units)*8 | | - | 2 | 6 | - | 2 | 6 | μA | - | | | | |
| Reference power supply current (VREFH0) | During 12-bit A/D conversion (unit 0) | | - | 70 | 120 | - | 70 | 120 | μA | - | | | | |
| | Waiting for 12-bit A/D conversion (unit 0) | | - | 0.07 | 0.4 | - | 0.07 | 0.4 | μA | - | | | | |
| | ADC12 in standby modes (unit 0) | | - | 0.07 | 0.2 | - | 0.07 | 0.2 | μA | - | | | | |

Table 2.7 Operating and standby current (2 of 2)

| Item | Symbol | | LDO mode | | | DCDC mode | | | Unit | Test conditions |
|----------------------------------------|-------------------------------------------------------------|--------------------|----------|------|------|-----------|------|------|------|------------------------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | | |
| Reference power supply current (VREFH) | During 12-bit A/D conversion (unit 1) | | - | 70 | 120 | - | 70 | 120 | μA | - |
| | During D/A conversion (per unit) | Without AMP output | - | 0.24 | 0.4 | - | 0.24 | 0.4 | mA | - |
| | | With AMP output | - | 0.1 | 0.2 | - | 0.1 | 0.2 | mA | - |
| | Waiting for 12-bit A/D (unit 1), D/A (all units) conversion | | - | 0.07 | 0.4 | - | 0.07 | 0.4 | μA | - |
| | ADC12 unit 1 in standby modes | | - | 0.07 | 0.2 | - | 0.07 | 0.2 | μA | - |
| USB operating current | Low speed | USB | - | 3.5 | 6.5 | - | 3.5 | 6.5 | mA | VCC_USB |
| | | USBHS | - | 10.5 | 13.5 | - | 10.5 | 13.5 | mA | VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0) |
| | | USBHS | - | 2.8 | 3.6 | - | 2.8 | 3.6 | mA | VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1) |
| | Full speed | USB | - | 4.0 | 10.0 | - | 4.0 | 10.0 | mA | VCC_USB |
| | | USBHS | - | 14 | 22 | - | 14 | 22 | mA | VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0) |
| | | USBHS | - | 6.5 | 13.0 | - | 6.5 | 13.0 | mA | VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1) |
| | High speed | USBHS | - | 50 | 65 | - | 50 | 65 | mA | VCC_USBHS = AVCC_USBHS |
| | Standby mode (direct power down) | USBHS | - | 0.5 | 3.0 | - | 0.5 | 3.0 | μA | VCC_USBHS = AVCC_USBHS |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. This does not include the BGO operation.

Note 4. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 5. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to be divided by 64 (3.75 MHz).

Note 6. When using ETHERC, PCLKA frequency is:

$$12.5\text{MHz} \leq \text{PCLKA} \leq 120\text{MHz}$$

Note 7. I_{CC} depends on $f_{(ICLK)}$ and is calculated as follows:

- High-speed mode (Maximum)

- LDO mode: $I_{CC} \text{ max} = 0.90 \text{ [mA/MHz]} \times f \text{ [MHz]} + 114 \text{ [mA]}$

- DCDC mode: $I_{CC} \text{ max} = 0.35 \text{ [mA/MHz]} \times f \text{ [MHz]} + 57 \text{ [mA]}$

- High-speed mode (Normal mode/all peripheral clocks disabled)

- LDO mode: $I_{CC} \text{ typ} = 0.10 \text{ [mA/MHz]} \times f \text{ [MHz]} + 6.9 \text{ [mA]}$

- DCDC mode: $I_{CC} \text{ typ} = 0.06 \text{ [mA/MHz]} \times f \text{ [MHz]} + 4.4 \text{ [mA]}$

- Low-speed mode (ICLK 1 MHz max)

- LDO mode: $I_{CC} \text{ typ} = 0.10 \text{ [mA/MHz]} \times f \text{ [MHz]} + 4.3 \text{ [mA]}$

- DCDC mode: $I_{CC} \text{ typ} = 0.06 \text{ [mA/MHz]} \times f \text{ [MHz]} + 3.0 \text{ [mA]}$

- Sleep mode

- LDO mode: $I_{CC} \text{ max} = 0.15 \text{ [mA/MHz]} \times f \text{ [MHz]} + 114 \text{ [mA]}$

- DCDC mode: $I_{CC} \text{ max} = 0.07 \text{ [mA/MHz]} \times f \text{ [MHz]} + 57 \text{ [mA]}$

Note 8. When the MSTPCRD.MSTPD16 (ADC120 Module Stop bit) and MSTPCRD.MSTPD15 (ADC121 Module Stop bit) are in the module-stop state.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.8 Rise and fall gradient characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------|--------|--------|-----|-----|------|-----------------|
| VCC rising gradient | SrVCC | 0.0084 | - | 20 | ms/V | - |
| VCC falling gradient*1 | SfVCC | 0.0084 | - | - | ms/V | - |

Note 1. This applies when VBATT is used.

Table 2.9 Rise and fall gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds $VCC \pm 10\%$, the allowable voltage change rising and falling gradient $dt/dVCC$ must be met.

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------------------------------------|--------------|-----|-----|-----|------|-------------------------------------------------|
| Allowable ripple frequency | $f_{r(VCC)}$ | - | - | 10 | kHz | Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.2$ |
| | | - | - | 1 | MHz | Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.08$ |
| | | - | - | 10 | MHz | Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | $dt/dVCC$ | 1.0 | - | - | ms/V | When VCC change exceeds $VCC \pm 10\%$ |

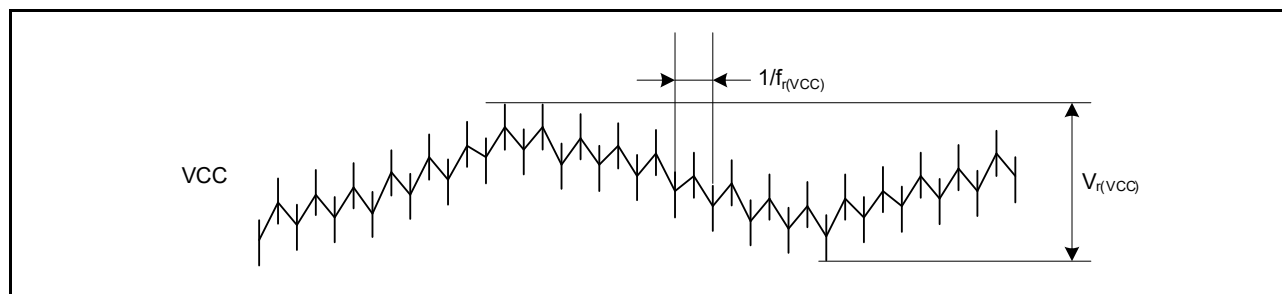


Figure 2.2 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.10 Operation frequency value in high-speed mode

| Item | Symbol | Min | Typ | Max | Unit | |
|---------------------|-----------------------------------|-------------|-----|-----|------|-----|
| Operation frequency | System clock (ICLK)*2 | f | - | - | 240 | MHz |
| | Peripheral module clock (PCLKA)*2 | | - | - | 120 | |
| | Peripheral module clock (PCLKB)*2 | | - | - | 60 | |
| | Peripheral module clock (PCLKC)*2 | | _*3 | - | 60 | |
| | Peripheral module clock (PCLKD)*2 | | - | - | 120 | |
| | Flash interface clock (FCLK)*2 | | _*1 | - | 60 | |
| | External bus clock (BCLK)*2 | | - | - | 120 | |
| | EBCLK pin output | | - | - | 60 | |
| | SDCLK pin output | VCC ≥ 3.0 V | - | - | 120 | |

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.

Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.11 Operation frequency value in low-speed mode

| Item | Symbol | Min | Typ | Max | Unit | |
|---------------------|--------------------------------------|-----|-----|-----|------|-----|
| Operation frequency | System clock (ICLK)*2 | f | - | - | 1 | MHz |
| | Peripheral module clock (PCLKA)*2 | | - | - | 1 | |
| | Peripheral module clock (PCLKB)*2 | | - | - | 1 | |
| | Peripheral module clock (PCLKC)*2,*3 | | _*3 | - | 1 | |
| | Peripheral module clock (PCLKD)*2 | | - | - | 1 | |
| | Flash interface clock (FCLK)*1,*2 | | - | - | 1 | |
| | External bus clock (BCLK) | | - | - | 1 | |
| | EBCLK pin output | | - | - | 1 | |

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.

Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 2.12 Operation frequency value in Subosc-speed mode

| Item | Symbol | Min | Typ | Max | Unit | |
|---------------------|--------------------------------------|-----|------|-----|------|-----|
| Operation frequency | System clock (ICLK)*2 | f | 29.4 | - | 36.1 | kHz |
| | Peripheral module clock (PCLKA)*2 | | - | - | 36.1 | |
| | Peripheral module clock (PCLKB)*2 | | - | - | 36.1 | |
| | Peripheral module clock (PCLKC)*2,*3 | | - | - | 36.1 | |
| | Peripheral module clock (PCLKD)*2 | | - | - | 36.1 | |
| | Flash interface clock (FCLK)*1,*2 | | 29.4 | - | 36.1 | |
| | External bus clock (BCLK)*2 | | - | - | 36.1 | |
| | EBCLK pin output | | - | - | 36.1 | |

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.

Note 3. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.13 Clock timing except for sub-clock oscillator

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions |
|-------------------------------------------------------------|-------------|-----------------|---------|--------|---------|---------|-----------------------------------------|
| EBCLK pin output cycle time | | t_{Bcyc} | 16.6 | - | - | ns | Figure 2.3 |
| EBCLK pin output high pulse width | | t_{CH} | 3.3 | - | - | ns | |
| EBCLK pin output low pulse width | | t_{CL} | 3.3 | - | - | ns | |
| EBCLK pin output rise time | | t_{Cr} | - | - | 5.0 | ns | |
| EBCLK pin output fall time | | t_{Cf} | - | - | 5.0 | ns | |
| SDCLK pin output cycle time | | t_{SDcyc} | 8.33 | - | - | ns | |
| SDCLK pin output high pulse width | | t_{CH} | 1.0 | - | - | ns | |
| SDCLK pin output low pulse width | | t_{CL} | 1.0 | - | - | ns | |
| SDCLK pin output rise time | | t_{Cr} | - | - | 3.0 | ns | |
| SDCLK pin output fall time | | t_{Cf} | - | - | 3.0 | ns | |
| EXTAL external clock input cycle time | | t_{EXcyc} | 41.66 | - | - | ns | Figure 2.4 |
| EXTAL external clock input high pulse width | | t_{EXH} | 15.83 | - | - | ns | |
| EXTAL external clock input low pulse width | | t_{EXL} | 15.83 | - | - | ns | |
| EXTAL external clock rise time | | t_{EXr} | - | - | 5.0 | ns | |
| EXTAL external clock fall time | | t_{EXf} | - | - | 5.0 | ns | |
| Main clock oscillator frequency | | f_{MAIN} | 8 | - | 24 | MHz | - |
| Main clock oscillation stabilization wait time (crystal) *1 | | $t_{MAINOSCWT}$ | - | - | ~*1 | ms | Figure 2.5 |
| LOCO clock oscillation frequency | | f_{LOCO} | 29.4912 | 32.768 | 36.0448 | kHz | - |
| LOCO clock oscillation stabilization wait time | | t_{LOCOWT} | - | - | 60.4 | μ s | Figure 2.6 |
| ILOCO clock oscillation frequency | | f_{ILOCO} | 13.5 | 15 | 16.5 | kHz | - |
| MOCO clock oscillation frequency | | F_{MOCO} | 7.2 | 8 | 8.8 | MHz | - |
| MOCO clock oscillation stabilization wait time | | t_{MOCOWT} | - | - | 15.0 | μ s | - |
| HOCO clock oscillator oscillation frequency | Without FLL | f_{HOCO16} | 15.61 | 16 | 16.39 | MHz | $-20 \leq T_a \leq 105^\circ\text{C}$ |
| | | f_{HOCO18} | 17.56 | 18 | 18.44 | | |
| | | f_{HOCO20} | 19.52 | 20 | 20.48 | | |
| | | f_{HOCO16} | 15.52 | 16 | 16.48 | | |
| | | f_{HOCO18} | 17.46 | 18 | 18.54 | | |
| | | f_{HOCO20} | 19.40 | 20 | 20.60 | | |
| | With FLL | f_{HOCO16} | 15.91 | 16 | 16.09 | | SOSC frequency is 32.768kHz \pm 50ppm |
| | | f_{HOCO18} | 17.90 | 18 | 18.10 | | |
| | | f_{HOCO20} | 19.89 | 20 | 20.11 | | |
| HOCO clock oscillation stabilization wait time *2 | | t_{HOCOWT} | - | - | 64.7 | μ s | - |
| FLL stabilization wait time | | t_{FLLWT} | - | - | 3 | ms | - |
| PLL clock frequency | | f_{PLL} | 120 | - | 240 | MHz | - |
| PLL clock oscillation stabilization wait time | | t_{PLLWT} | - | - | 174.9 | μ s | Figure 2.7 |

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.

After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.14 Clock timing for the sub-clock oscillator

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|-----------------------------------------------|----------------|-----|--------|-----|------|-----------------|
| Sub-clock frequency | f_{SUB} | - | 32.768 | - | kHz | - |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | - | - | -*1 | s | Figure 2.8 |

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. Two times the oscillation wait time is recommended.

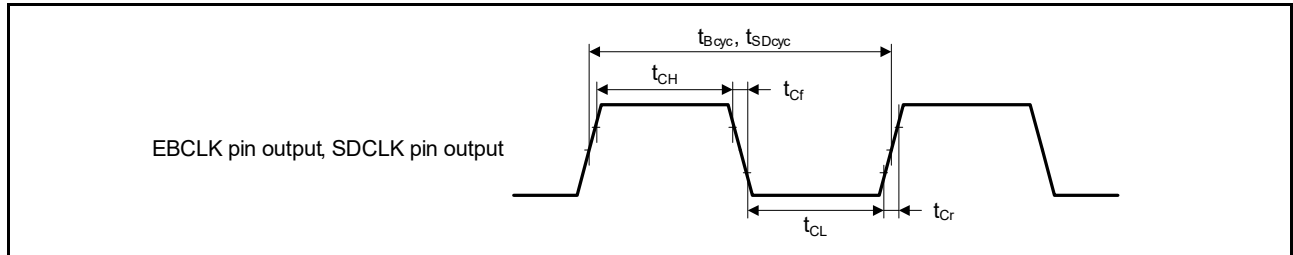


Figure 2.3 EBCLK and SDCLK output timing

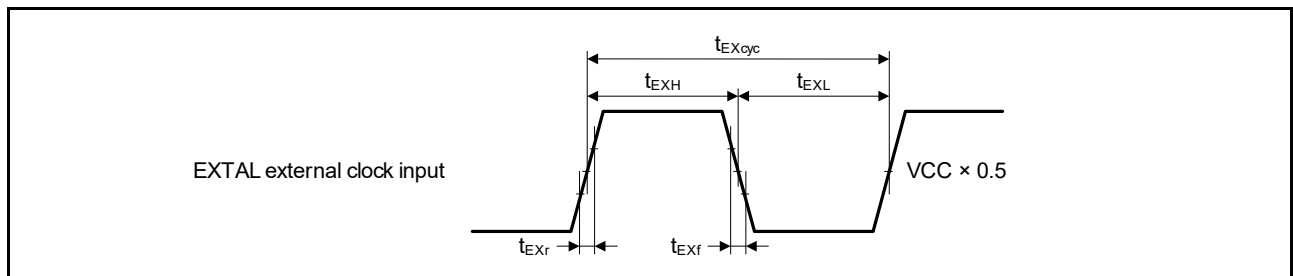


Figure 2.4 EXTAL external clock input timing

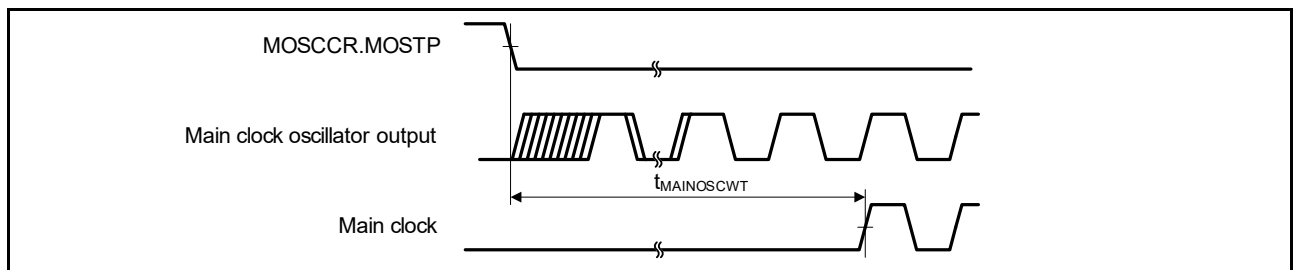


Figure 2.5 Main clock oscillation start timing

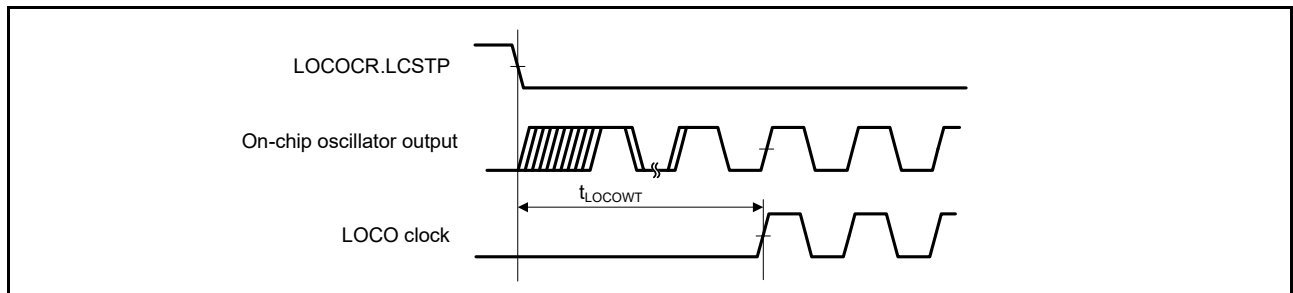


Figure 2.6 LOCO clock oscillation start timing

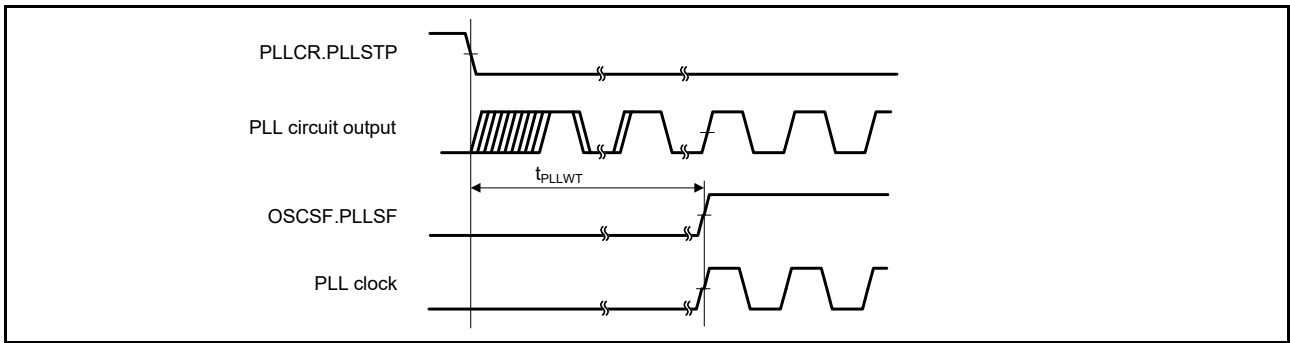


Figure 2.7 PLL clock oscillation start timing

Note: Only operate the PLL is operated after main clock oscillation has stabilized.

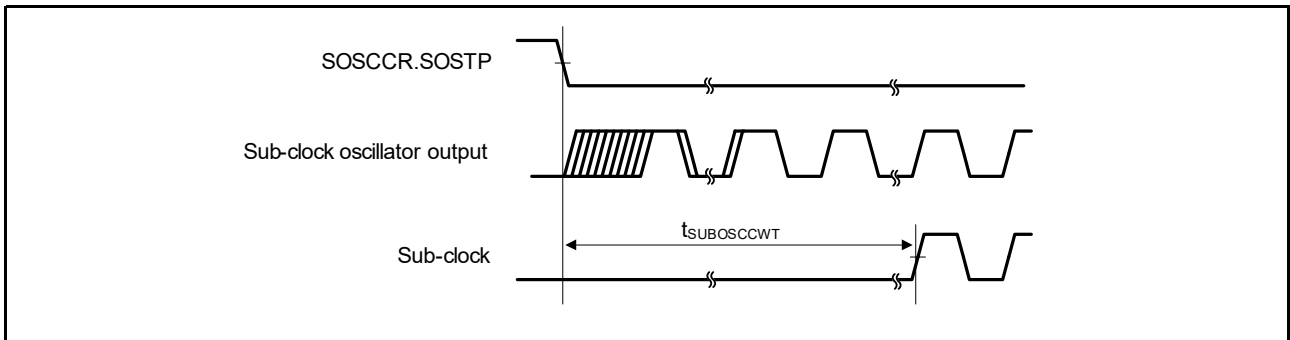


Figure 2.8 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.15 Reset timing

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | | |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|-------------|-------------|------|---------|-----------------|-------------|------------|
| RES pulse width | Power-on | LDO mode | t_{RESWP} | 1 | - | - | ms | Figure 2.9 |
| | | DCDC mode | | 1.5 | - | - | ms | |
| | Deep Software Standby mode | t_{RESWD} | 0.6 | - | - | ms | Figure 2.10 | |
| | Software Standby mode, Subosc-speed mode | t_{RESWS} | 0.3 | - | - | ms | | |
| | All other | t_{RESW} | 200 | - | - | μ s | | |
| Wait time after RES cancellation | t_{RESWT} | - | - | 33.4 | μ s | Figure 2.9 | | |
| Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM DED error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset) | t_{RESW2} | - | - | 390 | μ s | - | | |

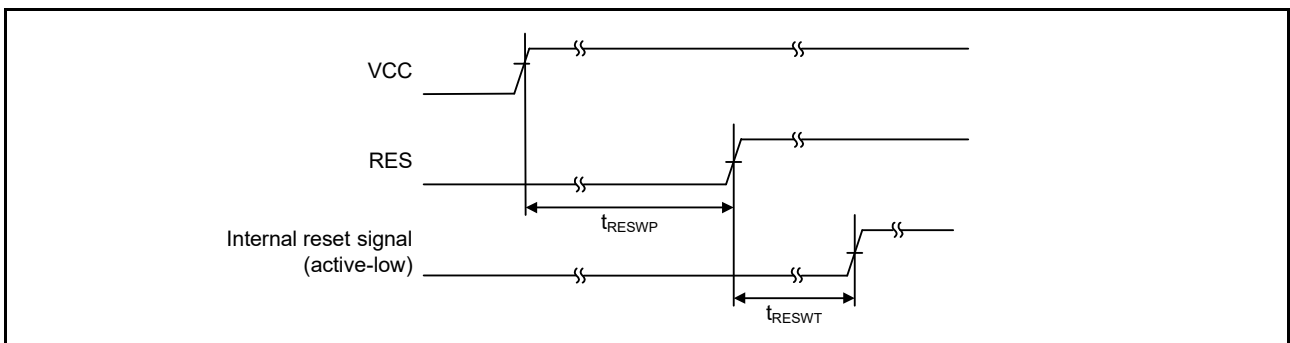


Figure 2.9 Power-on reset timing

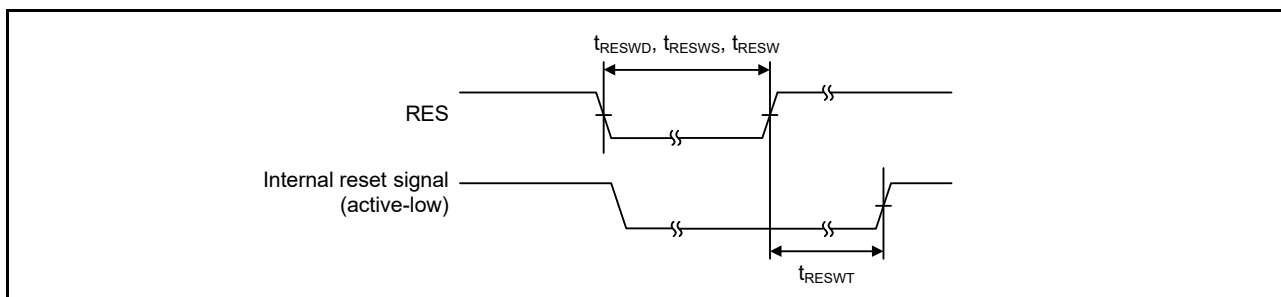


Figure 2.10 Reset input timing

2.3.4 Wakeup Timing and Duration

Table 2.16 Timing of recovery from low power modes and duration

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | | |
|------------------------------------------------------------|-----------------------------------------------------------|---------------------------------------------------------|--------------------|-----|------------------|----------------------|-------------|------------------------------------------------------------|
| Recovery time from Software Standby mode*1 | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator*2 | t _{SBYMC} | - | - | 2.8 | ms | Figure 2.11 The division ratio of all oscillators is 1. |
| | | System clock source is PLL with main clock oscillator*3 | t _{SBYPC} | - | - | 3.2 | ms | |
| | External clock input to main clock oscillator | System clock source is main clock oscillator*4 | t _{SBYEX} | - | - | 280 | μs | |
| | | System clock source is PLL with main clock oscillator*5 | t _{SBYPE} | - | - | 700 | μs | |
| | | System clock source is sub-clock oscillator*8 | t _{SBYSC} | - | - | 1.3 | ms | |
| | | System clock source is LOCO*8 | t _{SBYLO} | - | - | 1.4 | ms | |
| | | System clock source is HOCO clock oscillator*6 | t _{SBYHO} | - | - | 300 | μs | |
| | | System clock source is MOCO clock oscillator*7 | t _{SBYMO} | - | - | 300 | μs | |
| Recovery time from Deep Software Standby mode | t _{DSBY} | - | - | 1.0 | ms | Figure 2.12 | | |
| Wait time after cancellation of Deep Software Standby mode | t _{DSBYWT} | 31 | - | 32 | t _{cyc} | | | |
| Recovery time from Software Standby mode to Snooze mode | High-speed mode when system clock source is HOCO (20 MHz) | t _{SNZ} | - | - | 68 | μs | Figure 2.13 | |
| | High-speed mode when system clock source is MOCO (8 MHz) | t _{SNZ} | - | - | 14*9 | μs | | |
| Normal mode duration*10 | System clock source is main clock oscillator | t _{NML} | -*11 | - | - | t _{cycmosc} | Figure 2.11 | |
| | System clock source is PLL with main clock oscillator | | | | | | | |

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:

Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).

Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:

$$t_{SBYMC} (\text{MOSCWTCR} = Xh) = t_{SBYMC} (\text{MOSCWTCR} = 05h) + (t_{MAINOSCWT} (\text{MOSCWTCR} = Xh) - t_{MAINOSCWT} (\text{MOSCWTCR} = 05h))$$

Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following

equation:

$$t_{\text{SBYMC}}(\text{MOSCWTCR} = \text{Xh}) = t_{\text{SBYMC}}(\text{MOSCWTCR} = 05\text{h}) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = \text{Xh}) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 05\text{h}))$$

Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:

$$t_{\text{SBYMC}}(\text{MOSCWTCR} = \text{Xh}) = t_{\text{SBYMC}}(\text{MOSCWTCR} = 00\text{h}) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = \text{Xh}) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 00\text{h}))$$

Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:

$$t_{\text{SBYMC}}(\text{MOSCWTCR} = \text{Xh}) = t_{\text{SBYMC}}(\text{MOSCWTCR} = 00\text{h}) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = \text{Xh}) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 00\text{h}))$$

Note 6. The HOCO frequency is 20 MHz.

Note 7. The MOCO frequency is 8 MHz.

Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.

Note 9. When the SNZCR.RXDREQEN bit is set to 0, 86 μs is added as the power supply recovery time.

Note 10. This defines the duration of Normal mode after a transition from Snooze to Normal mode.

The following cases are valid uses of the main clock oscillator:

- The crystal resonator is connected to main clock oscillator
- The external clock is input to main clock oscillator.

The following cases are excluded:

- The main clock resonator is not connected to the system clock source
- Transition is made from Software Standby to Normal mode.

Note 11. The same value as set in MOSCWTCR.MSTS[3:0]. Duration of Normal mode must be longer than the main clock oscillator wait time.

MOSCWTCR: Main Clock Oscillator Wait Control Register

t_{cycmosc} : Main clock oscillator frequency cycle.

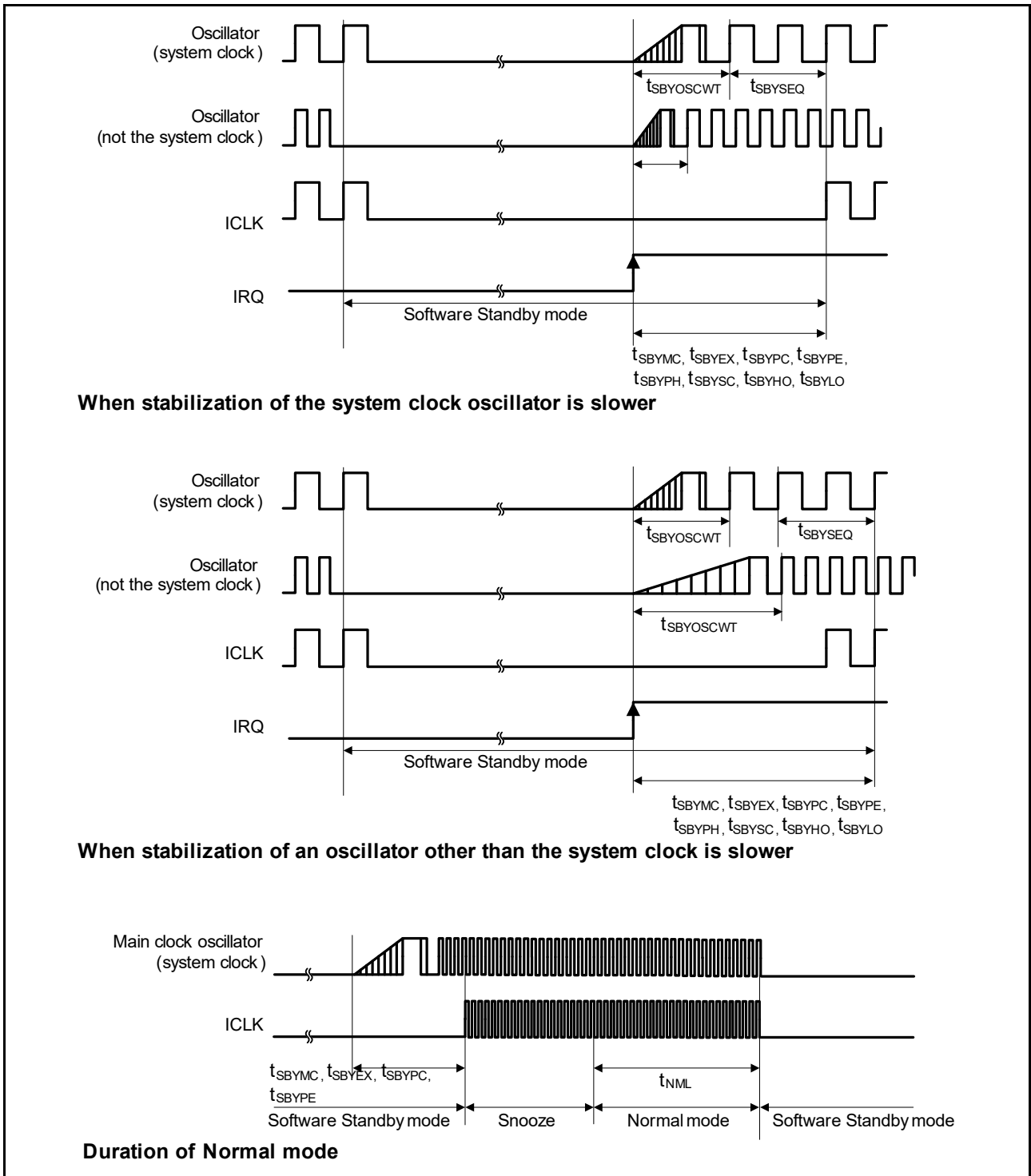


Figure 2.11 Software Standby mode cancellation timing and duration

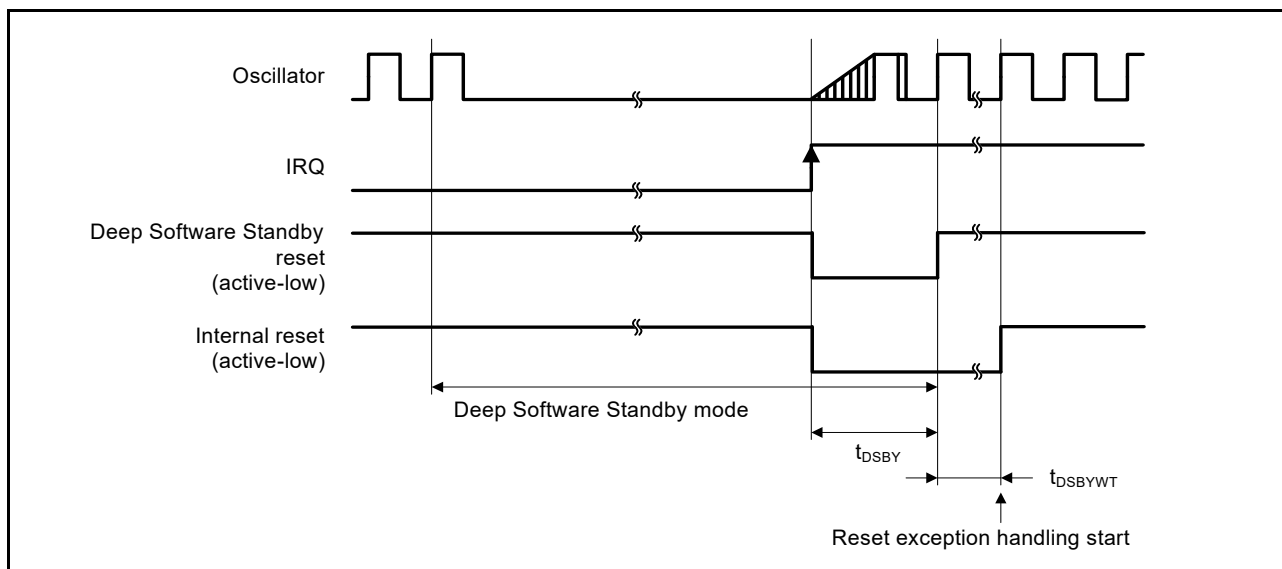


Figure 2.12 Deep Software Standby mode cancellation timing

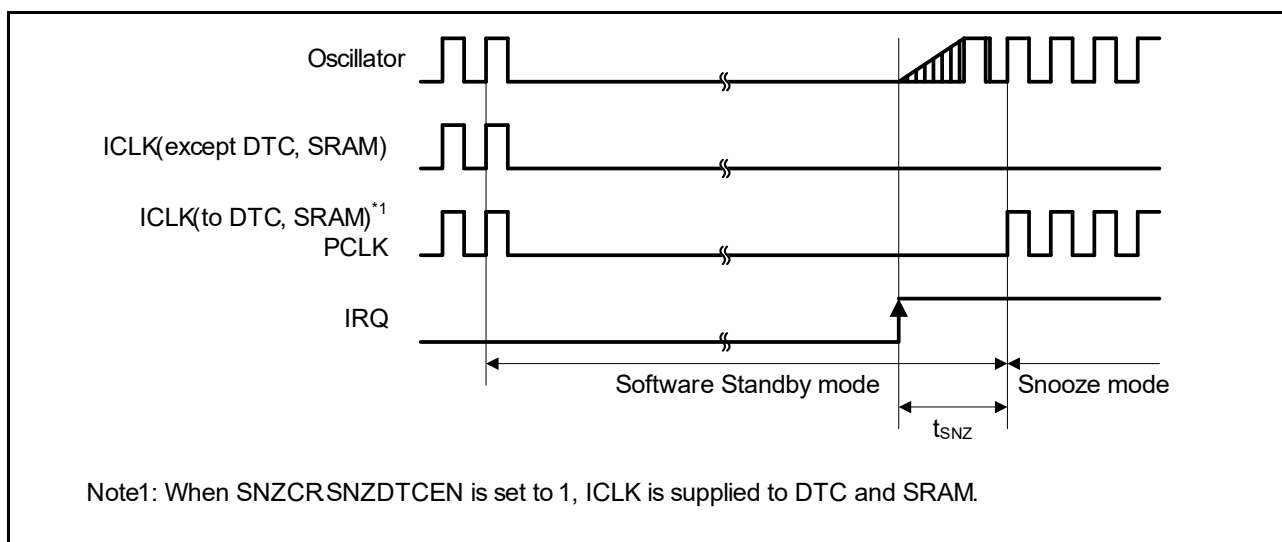


Figure 2.13 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | |
|-----------------|-------------------|------------------------------------|-----|-----|------|-----------------------------|-----------------------------------------|
| NMI pulse width | t_{NMIW} | 200 | - | - | ns | NMI digital filter disabled | $t_{\text{Pcyc}} \times 2 \leq 200$ ns |
| | | $t_{\text{Pcyc}} \times 2^{*1}$ | - | - | | | $t_{\text{Pcyc}} \times 2 > 200$ ns |
| | | 200 | - | - | | NMI digital filter enabled | $t_{\text{NMICK}} \times 3 \leq 200$ ns |
| | | $t_{\text{NMICK}} \times 3.5^{*2}$ | - | - | | | $t_{\text{NMICK}} \times 3 > 200$ ns |
| IRQ pulse width | t_{IRQW} | 200 | - | - | ns | IRQ digital filter disabled | $t_{\text{Pcyc}} \times 2 \leq 200$ ns |
| | | $t_{\text{Pcyc}} \times 2^{*1}$ | - | - | | | $t_{\text{Pcyc}} \times 2 > 200$ ns |
| | | 200 | - | - | | IRQ digital filter enabled | $t_{\text{IRQCK}} \times 3 \leq 200$ ns |
| | | $t_{\text{IRQCK}} \times 3.5^{*3}$ | - | - | | | $t_{\text{IRQCK}} \times 3 > 200$ ns |

Note: 200 ns minimum in Software Standby mode.

Note 1. t_{Pcyc} indicates the PCLKB cycle.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

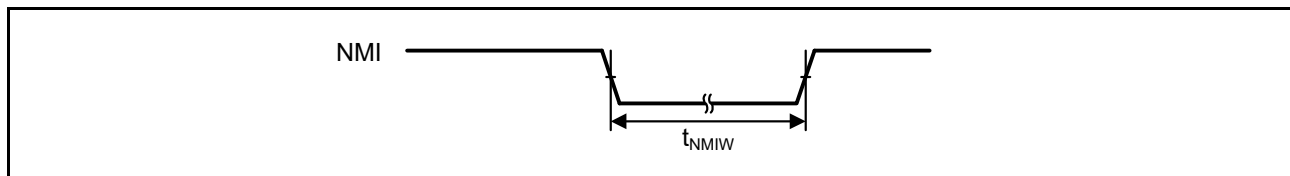


Figure 2.14 NMI interrupt input timing

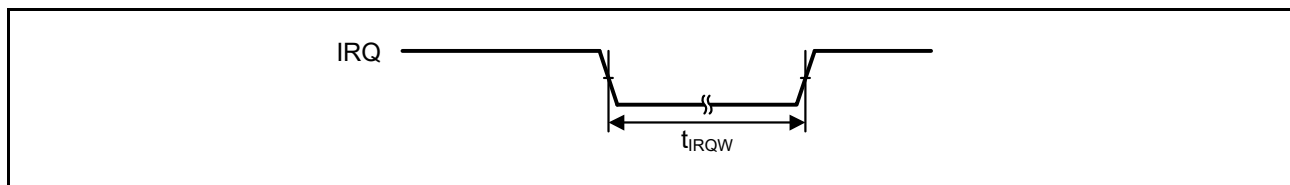


Figure 2.15 IRQ interrupt input timing

2.3.6 Bus Timing

Table 2.18 Bus timing

Condition 1: When using the CS area controller (CSC).

BCLK = 8 to 60 MHz

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF

EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.

Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).

BCLK = SDCLK = 8 to 120 MHz

VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF

High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.

BCLK = SDCLK = 8 to 60 MHz

VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF

High drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | Symbol | Min | Max | Unit | Test conditions |
|--------------------------------|------------|------|------|------|-------------------------------|
| Address delay | t_{AD} | - | 12.5 | ns | Figure 2.16 to Figure 2.19 |
| Byte control delay | t_{BCD} | - | 12.5 | ns | |
| CS delay | t_{CSD} | - | 12.5 | ns | |
| RD delay | t_{RSD} | - | 12.5 | ns | |
| Read data setup time | t_{RDS} | 12.5 | - | ns | |
| Read data hold time | t_{RDH} | 0 | - | ns | |
| WR/WRn delay | t_{WRD} | - | 12.5 | ns | |
| Write data delay | t_{WDD} | - | 12.5 | ns | |
| Write data hold time | t_{WDH} | 0 | - | ns | |
| WAIT setup time | t_{WTS} | 12.5 | - | ns | |
| WAIT hold time | t_{WTH} | 0 | - | ns | |
| Address delay 2 (SDRAM) | t_{AD2} | 0.8 | 6.8 | ns | Figure 2.21 to Figure 2.27 |
| CS delay 2 (SDRAM) | t_{CSD2} | 0.8 | 6.8 | ns | |
| DQM delay (SDRAM) | t_{DQMD} | 0.8 | 6.8 | ns | |
| CKE delay (SDRAM) | t_{CKED} | 0.8 | 6.8 | ns | |
| Read data setup time 2 (SDRAM) | t_{RDS2} | 2.9 | - | ns | |
| Read data hold time 2 (SDRAM) | t_{RDH2} | 1.5 | - | ns | |
| Write data delay 2 (SDRAM) | t_{WDD2} | - | 6.8 | ns | |
| Write data hold time 2 (SDRAM) | t_{WDH2} | 0.8 | - | ns | |
| WE delay (SDRAM) | t_{WED} | 0.8 | 6.8 | ns | |
| RAS delay (SDRAM) | t_{RASD} | 0.8 | 6.8 | ns | |
| CAS delay (SDRAM) | t_{CASD} | 0.8 | 6.8 | ns | |

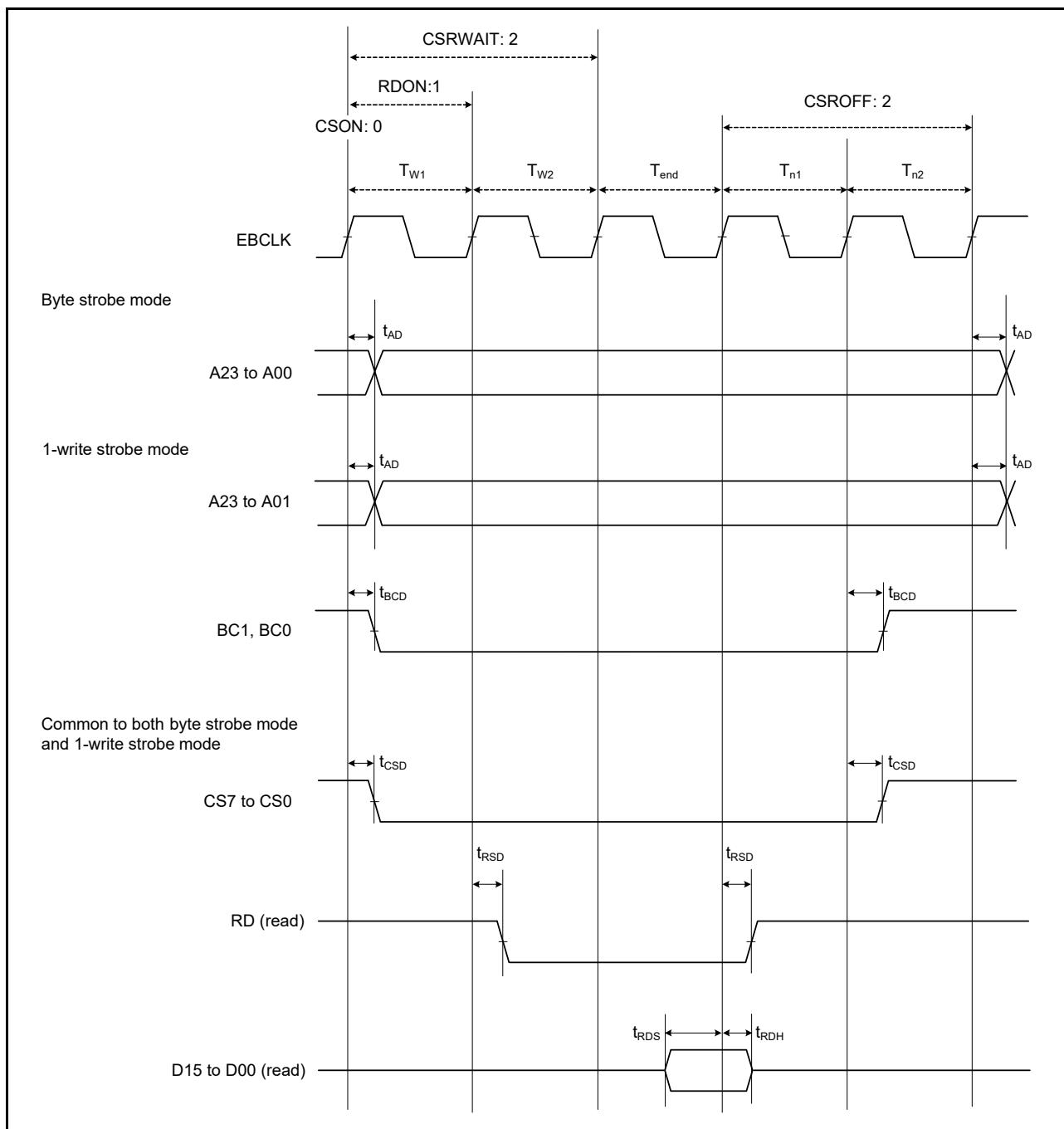


Figure 2.16 External bus timing for normal read cycle with bus clock synchronized

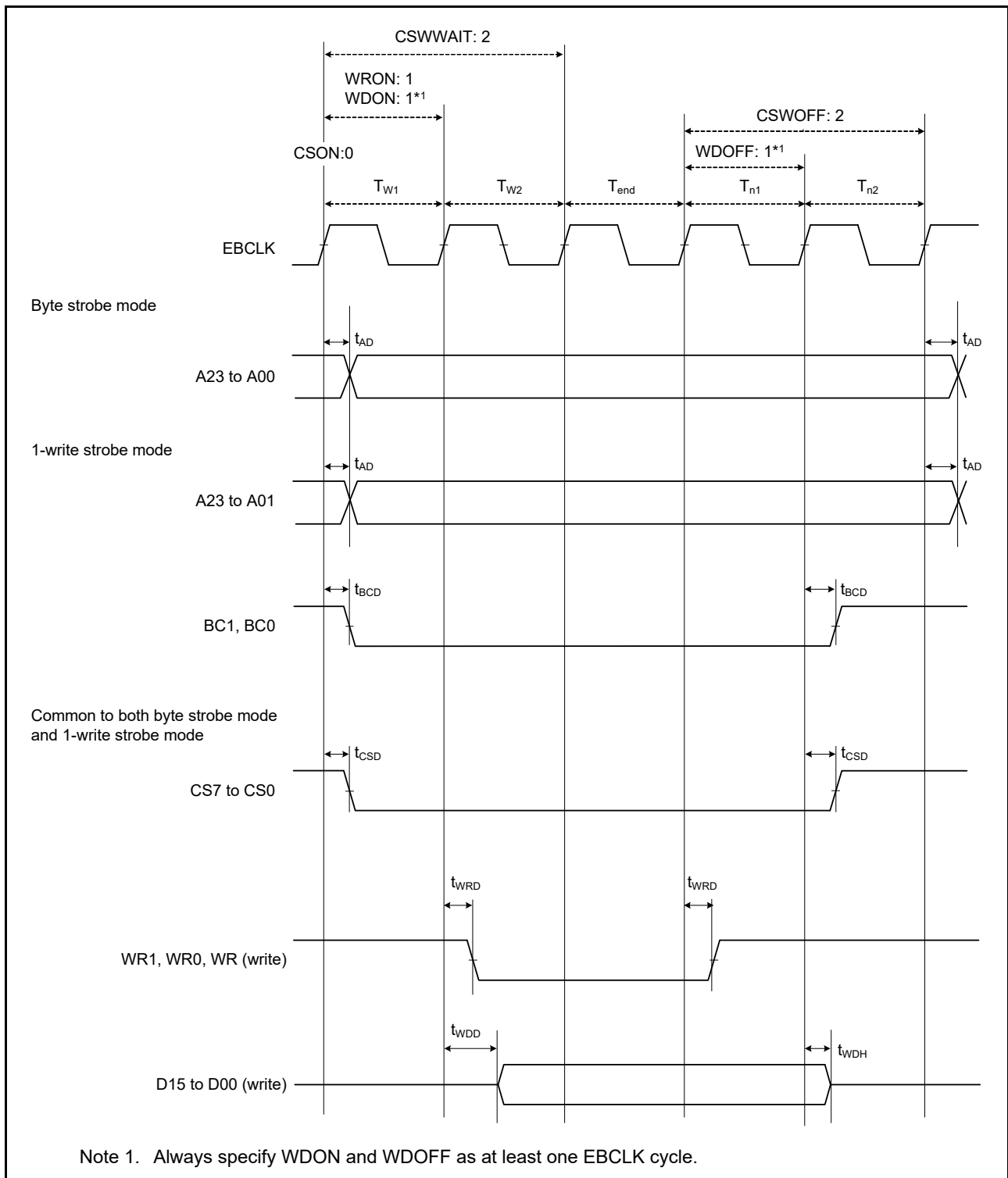


Figure 2.17 External bus timing for normal write cycle with bus clock synchronized

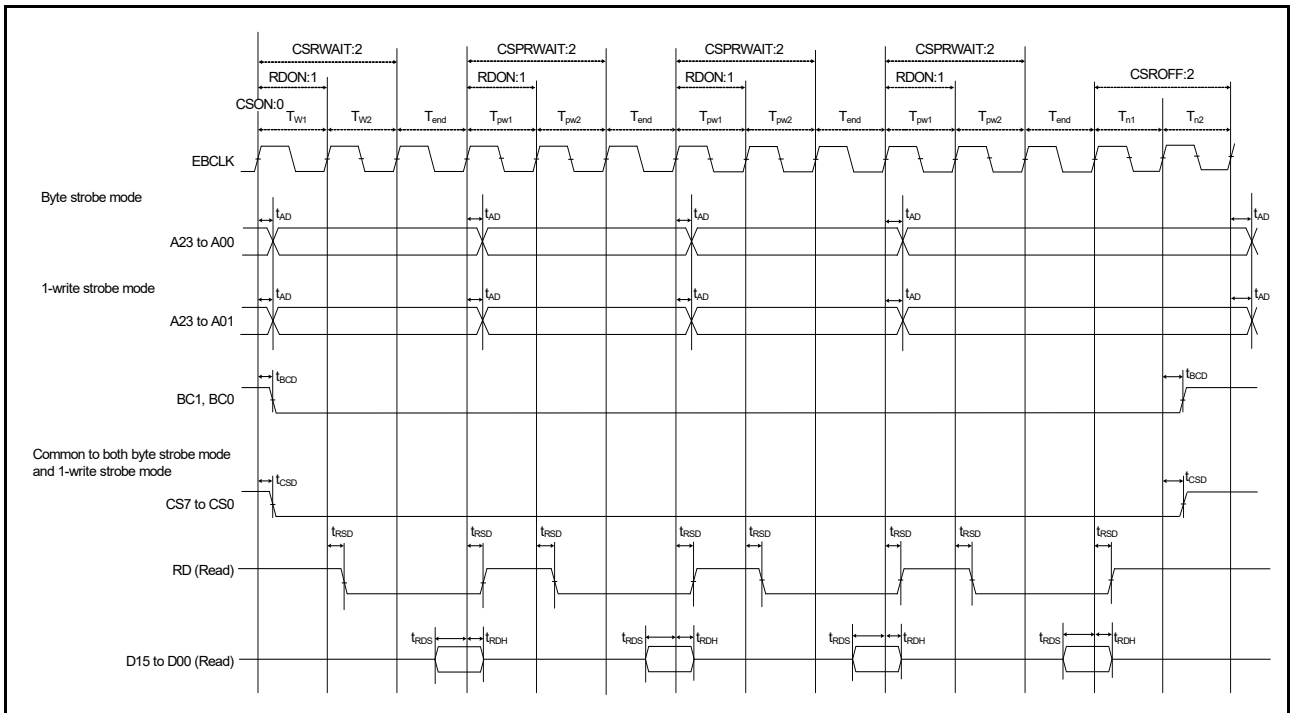
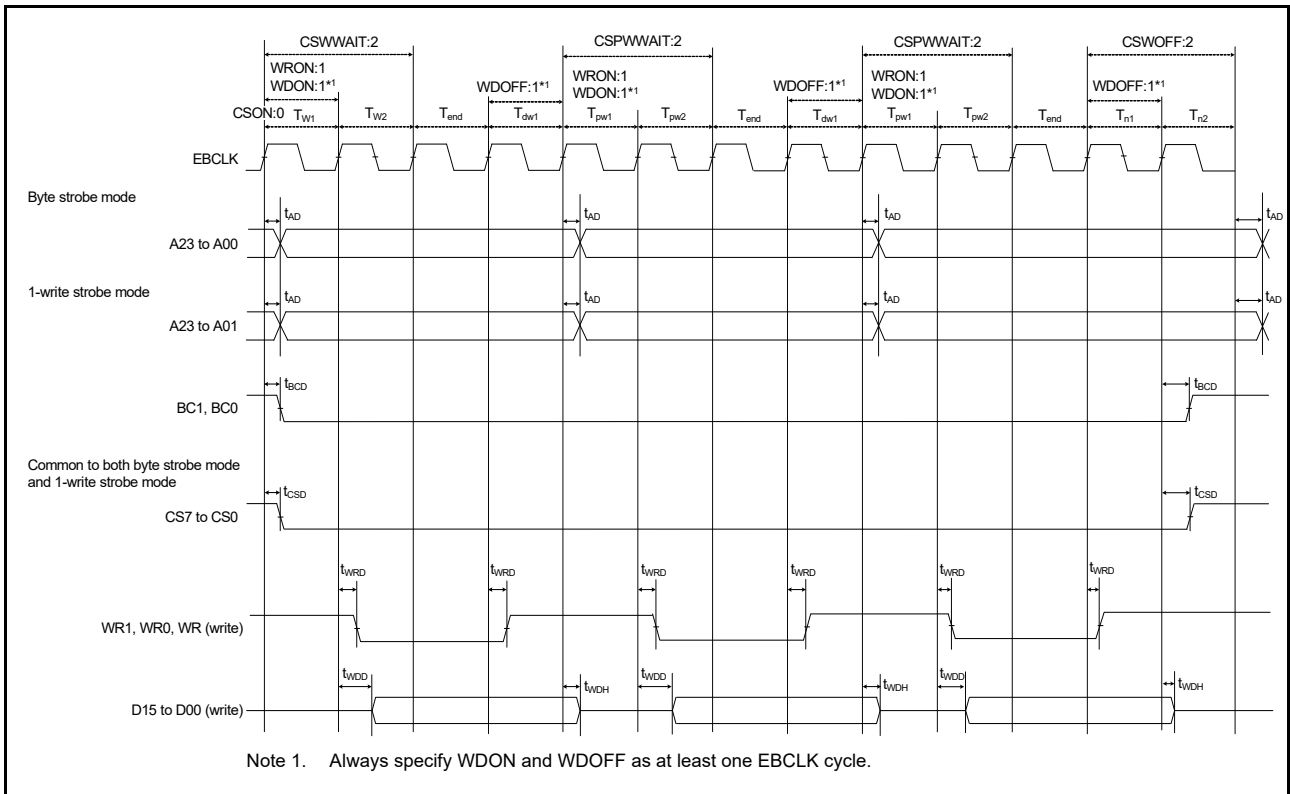


Figure 2.18 External bus timing for page read cycle with bus clock synchronized



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.19 External bus timing for page write cycle with bus clock synchronized

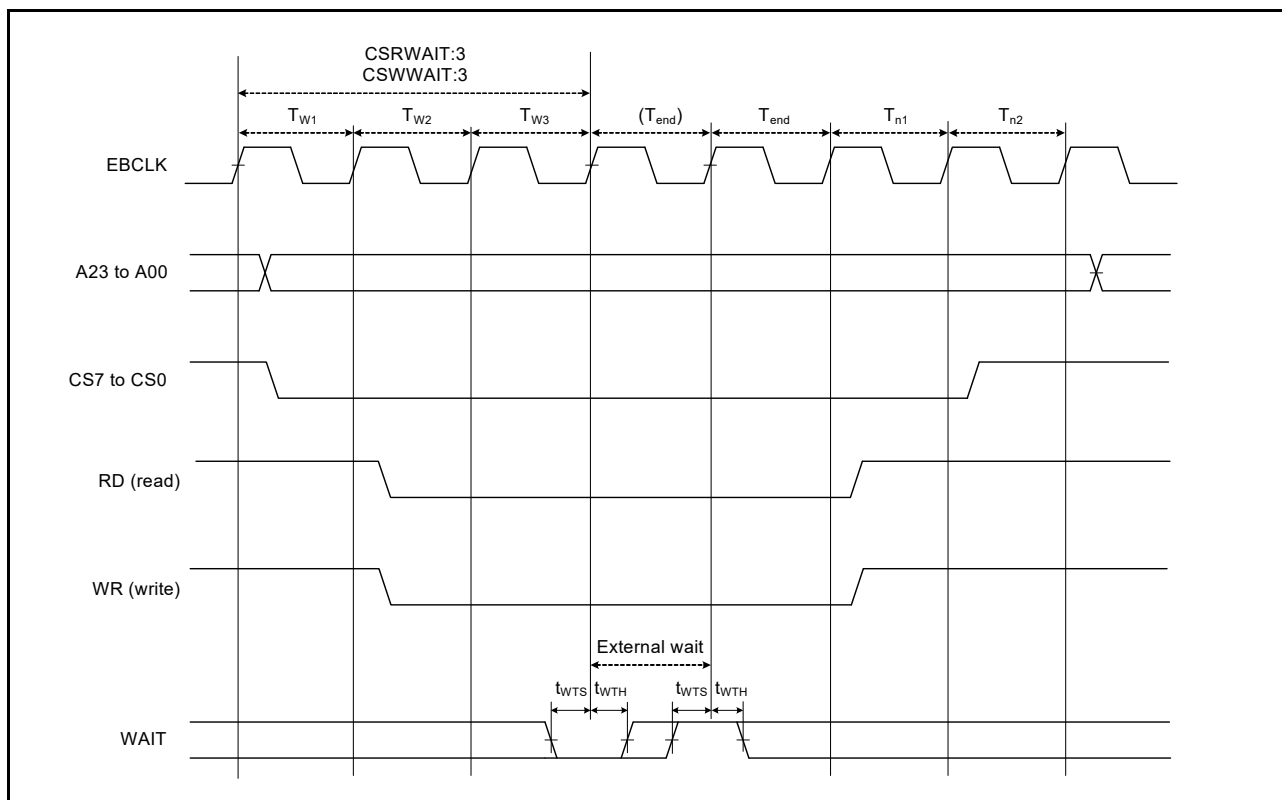


Figure 2.20 External bus timing for external wait control

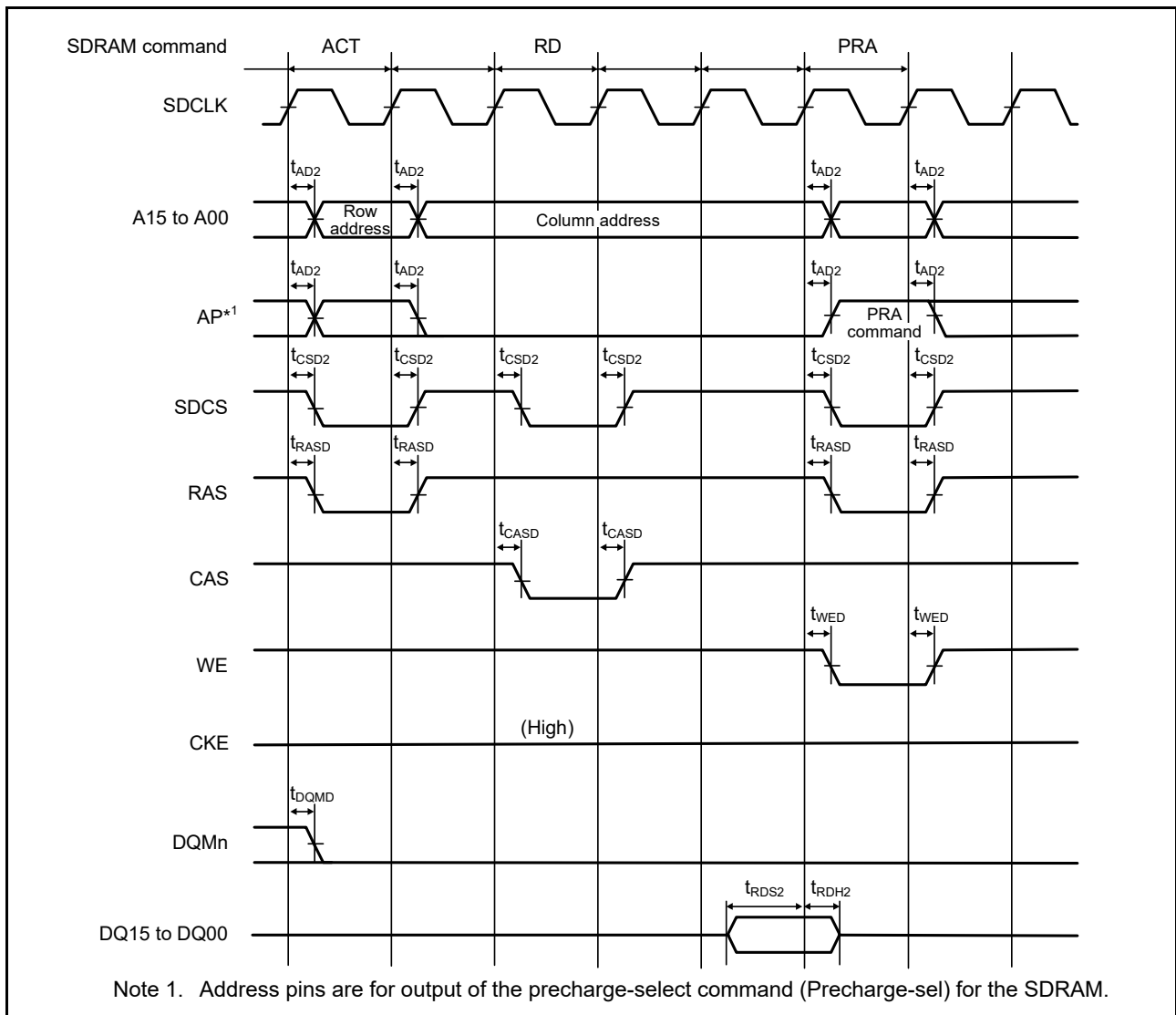


Figure 2.21 SDRAM single read timing

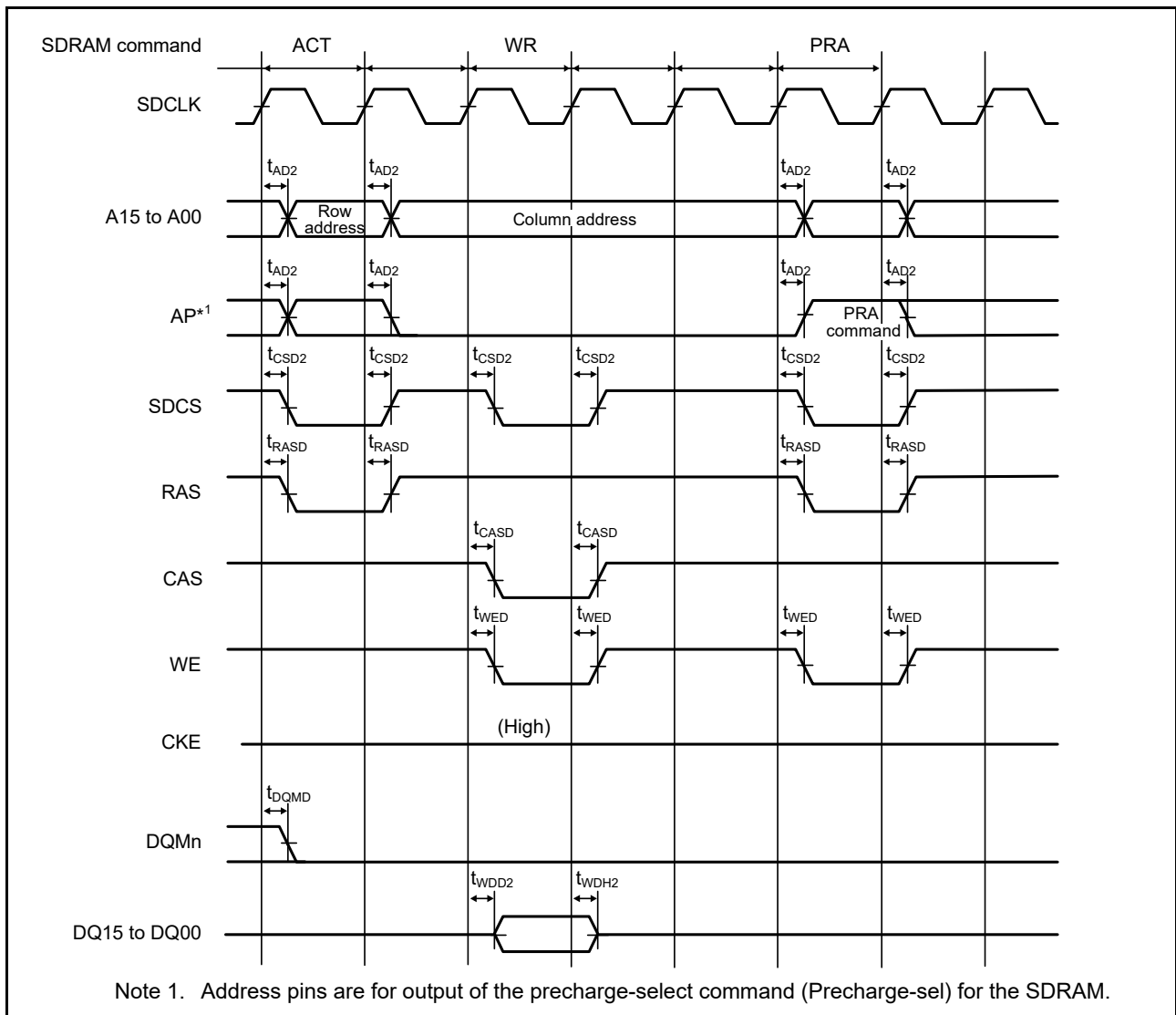


Figure 2.22 SDRAM single write timing

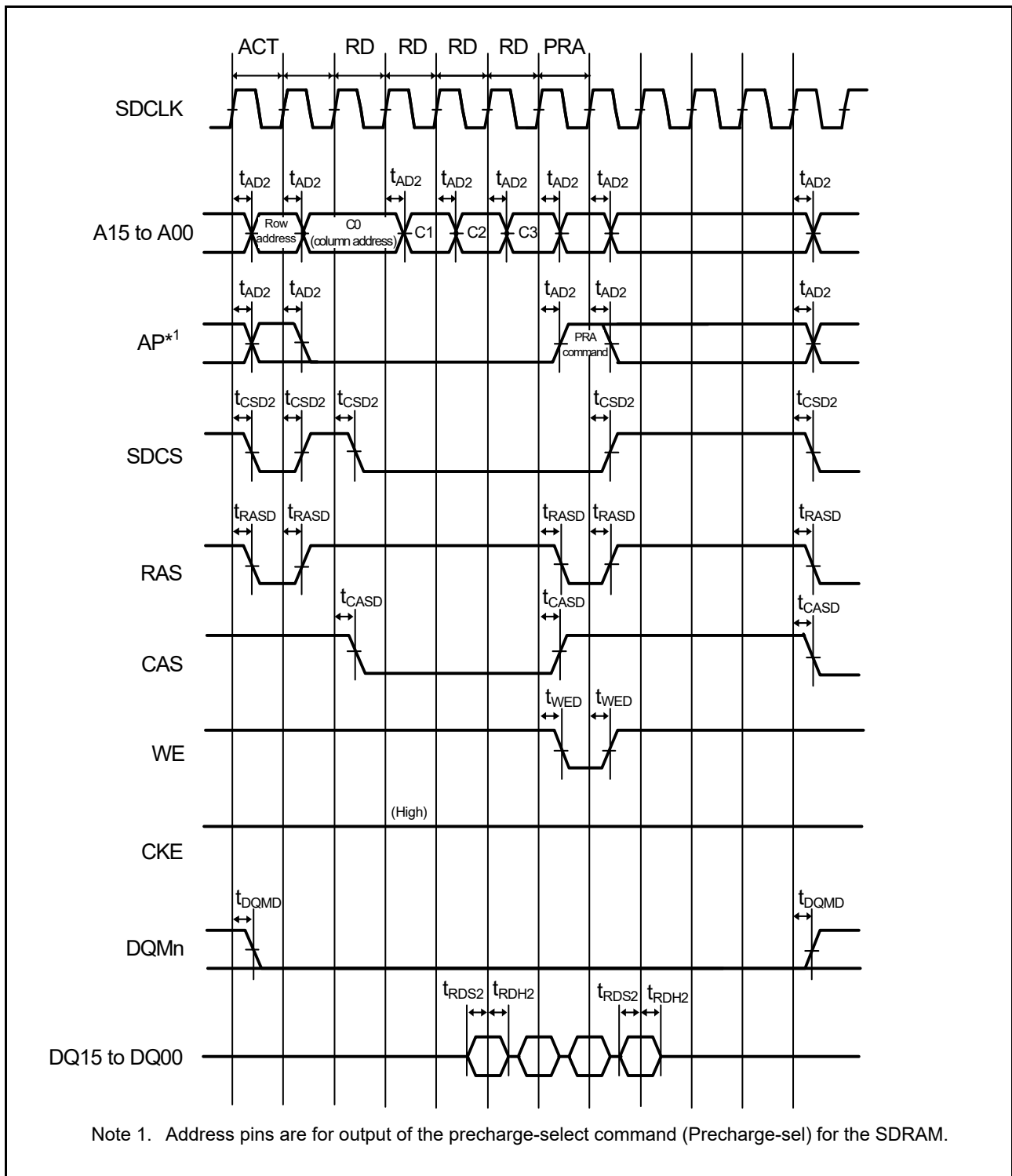


Figure 2.23 SDRAM multiple read timing

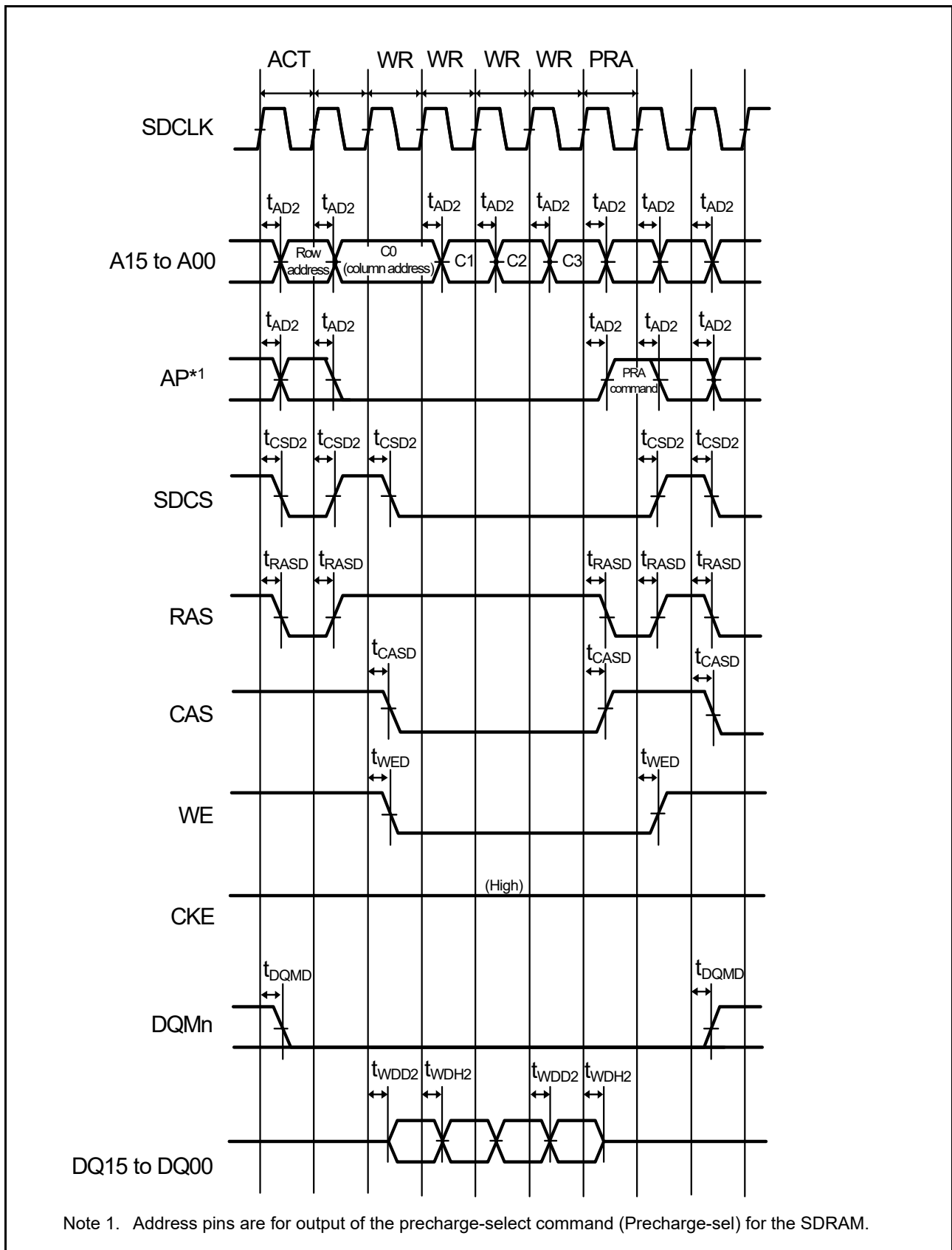


Figure 2.24 SDRAM multiple write timing

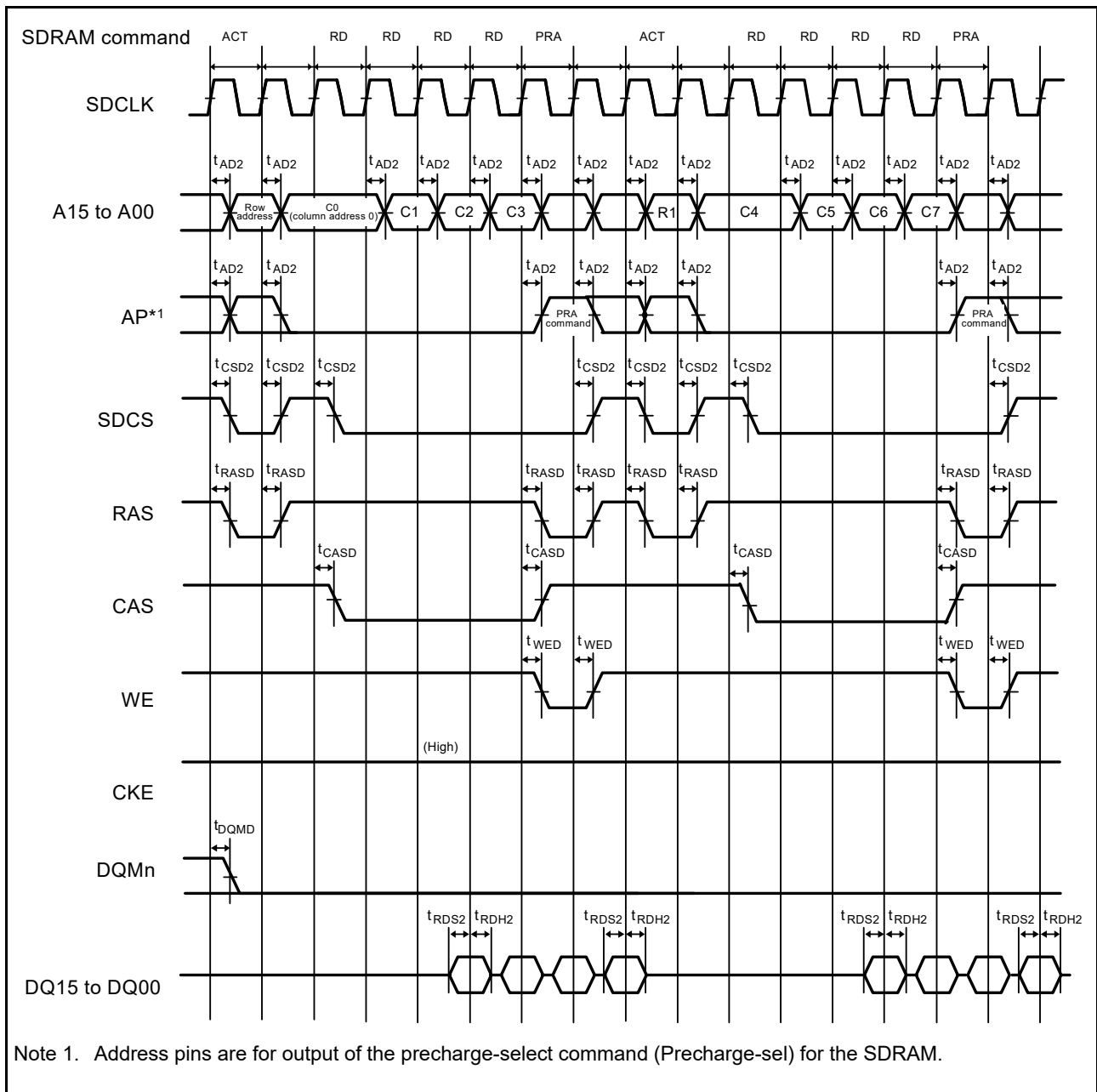


Figure 2.25 SDRAM multiple read line stride timing

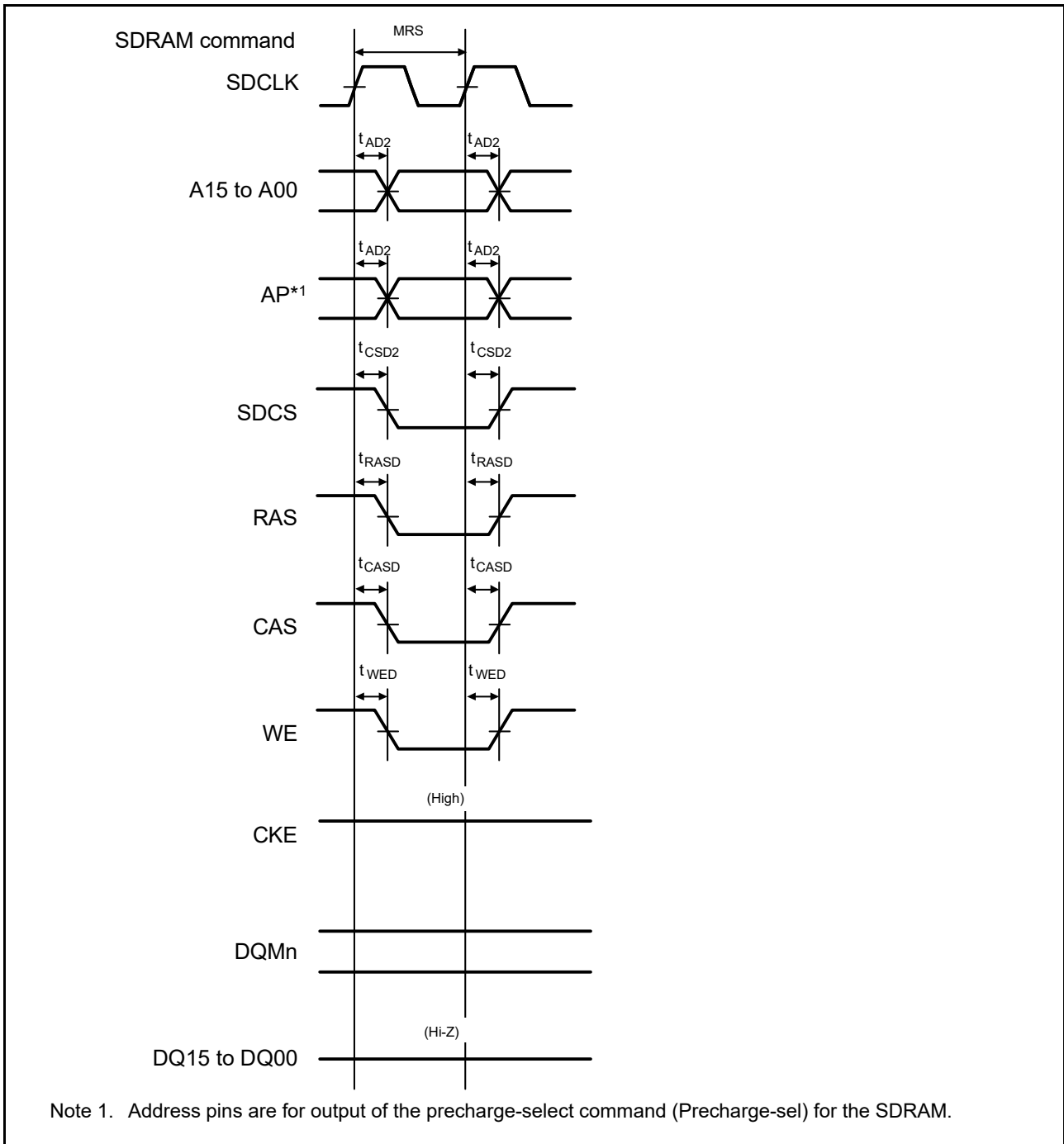


Figure 2.26 SDRAM mode register set timing

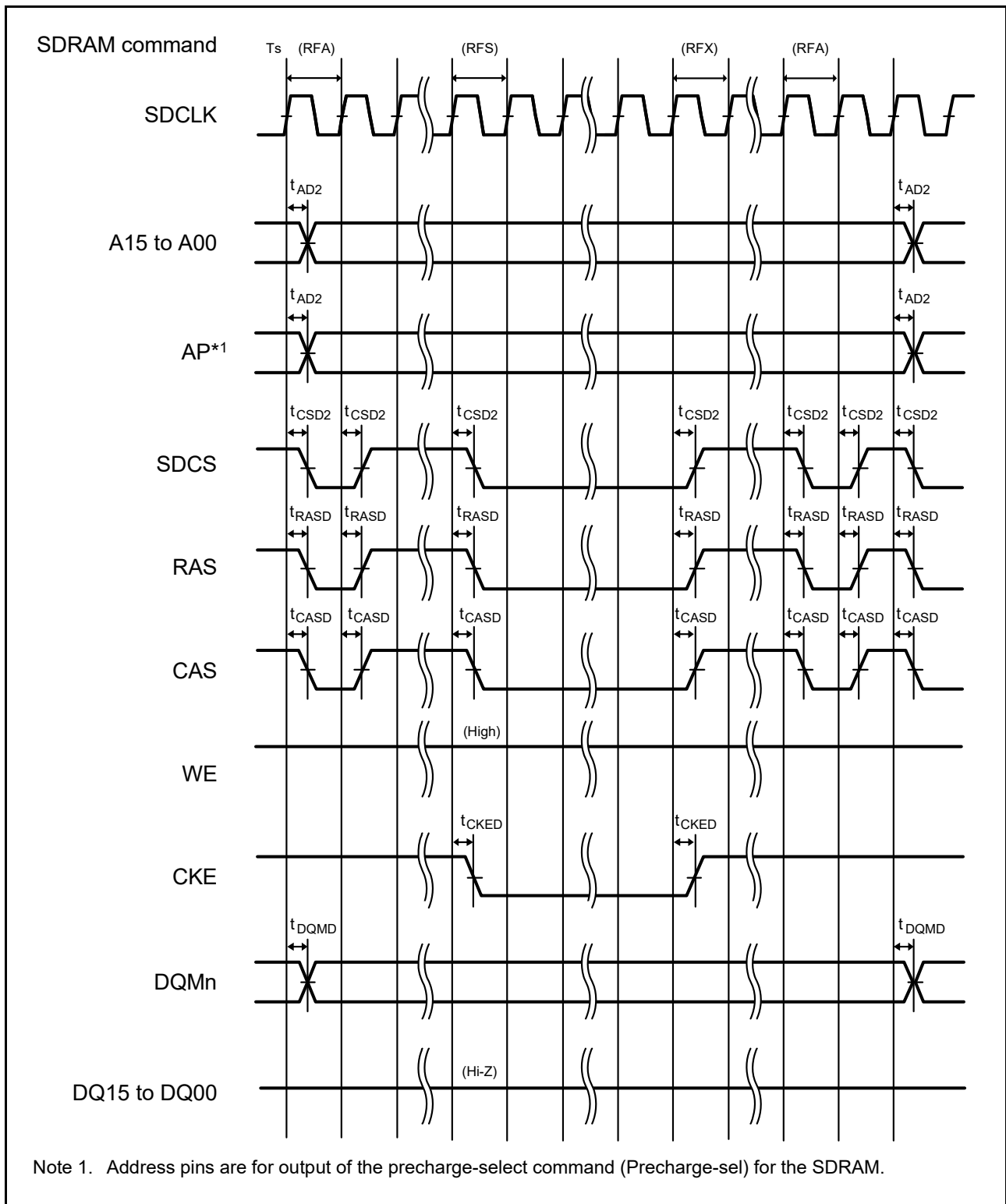


Figure 2.27 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing

GPT32 Conditions:

Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: GTIOC6A_A, GTIOC6B_A, GTIOC3A_B, GTIOC3B_B, GTIOC0A_B, GTIOC0B_B, GTIOC9A_B, GTIOC9B_B.

High drive output is selected in the port drive capability bit in the PmnPFS register for all other pins.

AGT Conditions:

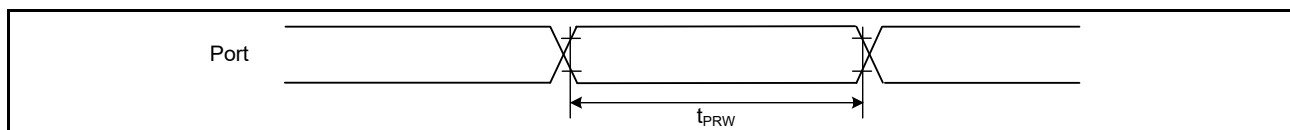
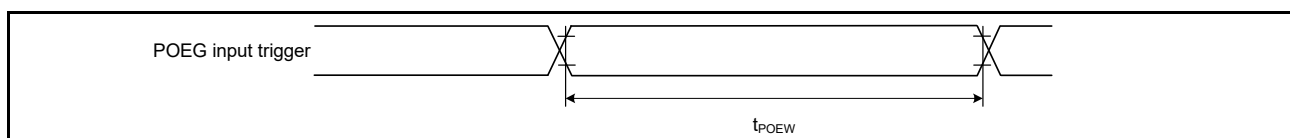
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | | Symbol | Min | Max | Unit | Test conditions | |
|--------------------------------------------------------------------------------------------------|----------------------------------------------------------------|------------------------------|------------------|-----|-------------|-----------------|-------------|
| I/O ports | Input data pulse width | t_{PRW} | 1.5 | - | t_{Pcyc} | Figure 2.28 | |
| POEG | POEG input trigger pulse width | t_{POEW} | 3 | - | t_{Pcyc} | Figure 2.29 | |
| GPT32 | Input capture pulse width | Single edge | 1.5 | - | t_{PDcyc} | Figure 2.30 | |
| | | Dual edge | 2.5 | - | | | |
| | GTIOCxY_Z output skew (x = 0 to 7, Y = A or B, Z = A or B) | Middle drive buffer | t_{GTISK}^{*2} | - | 4 | ns | Figure 2.31 |
| | | High drive buffer | | - | 4 | | |
| | GTIOCxY_Z output skew (x = 8 to 13, Y = A or B, Z = A or B) | Middle drive buffer | | - | 4 | | |
| | | High drive buffer | | - | 4 | | |
| GTIOCxY_Z output skew (x = 0 to 13, Y = A or B, Z = A or B) | Middle drive buffer | - | | 6 | | | |
| | High drive buffer | - | | 6 | | | |
| OPS output skew GTOUUP_x, GTOULO_x, GTOVUP_x, GTOVLO_x, GTOWUP_x, GTOWLO_x (x = A or B) | | t_{GTOSK}^{*2} | - | 5 | ns | Figure 2.32 | |
| GPT(PWM Delay Generation Circuit) | GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A) | t_{HRSK}^{*3} | - | 2.0 | ns | Figure 2.33 | |
| AGT | AGTIO, AGTEE input cycle | t_{ACYC}^{*1} | 100 | - | ns | Figure 2.34 | |
| | AGTIO, AGTEE input high width, low width | t_{ACKWH} , t_{ACKWL} | 40 | - | ns | | |
| | AGTIO, AGTO, AGTOA, AGTOB output cycle | t_{ACYC2} | 62.5 | - | ns | | |
| ADC12 | ADC12 trigger input pulse width | t_{TRGW} | 1.5 | - | t_{Pcyc} | Figure 2.35 | |
| KINT | KRn (n = 00 to 07) pulse width | t_{KR} | 250 | - | ns | Figure 2.36 | |

Note 1. t_{Pcyc} : PCLKB cycle, t_{PDcyc} : PCLKD cycle.

Note 2. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.

Note 3. The load is 30 pF.

Note 4. Constraints on AGTIO input: $t_{Pcyc} \times 2$ (t_{Pcyc} : PCLKB cycle) < t_{ACYC} .**Figure 2.28 I/O ports input timing****Figure 2.29 POEG input trigger timing**

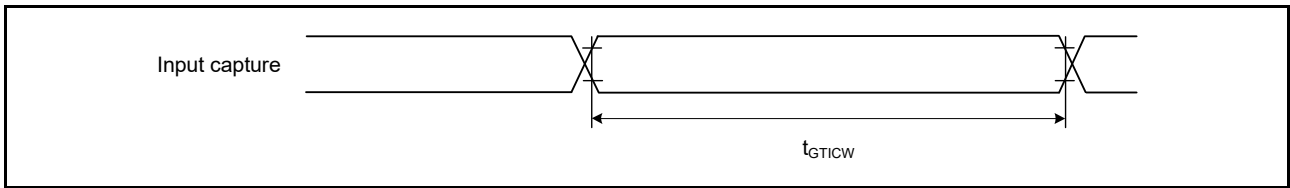


Figure 2.30 GPT32 input capture timing

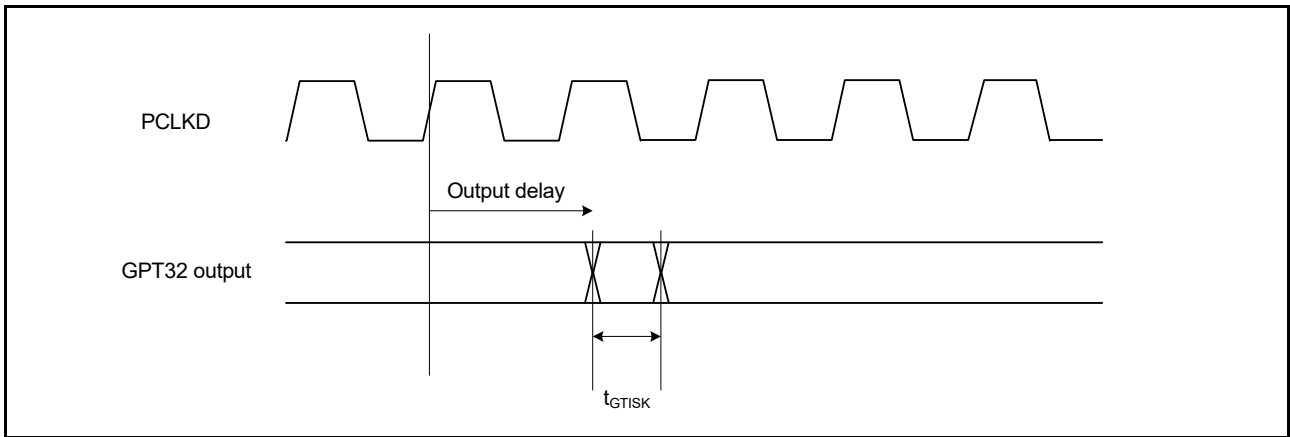


Figure 2.31 GPT32 output delay skew

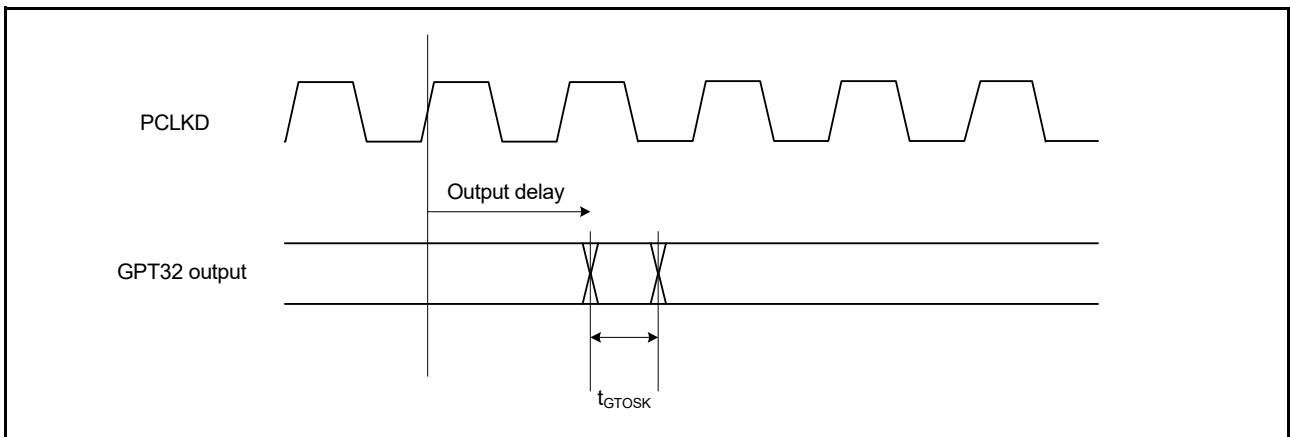


Figure 2.32 GPT32 output delay skew for OPS

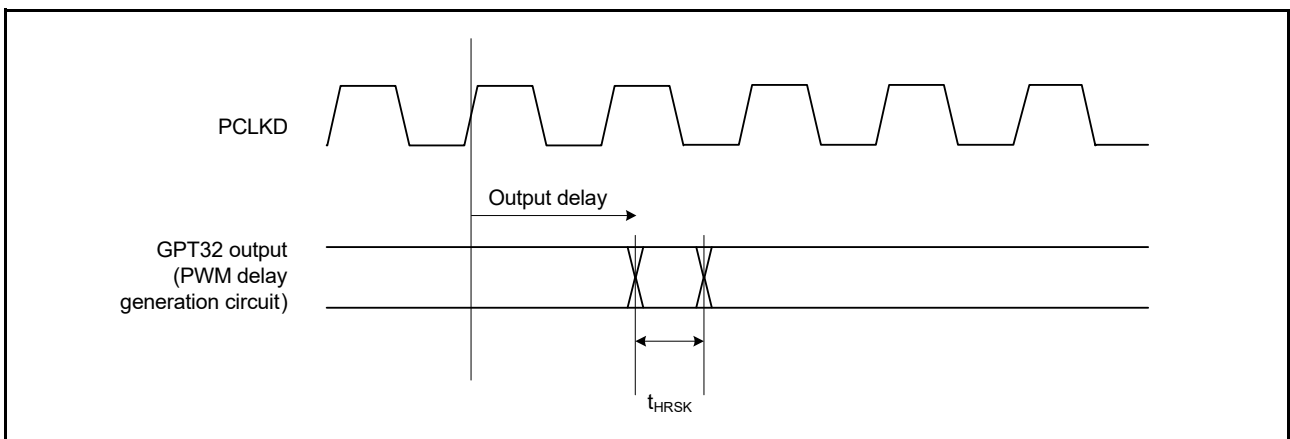


Figure 2.33 GPT32 (PWM Delay Generation Circuit) output delay skew

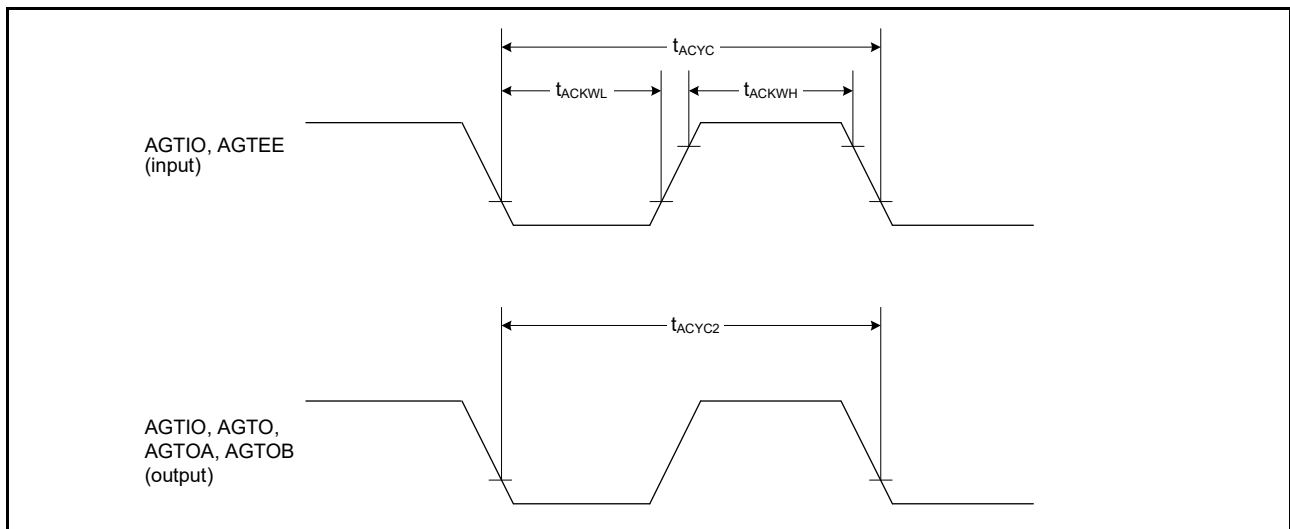


Figure 2.34 AGT input/output timing

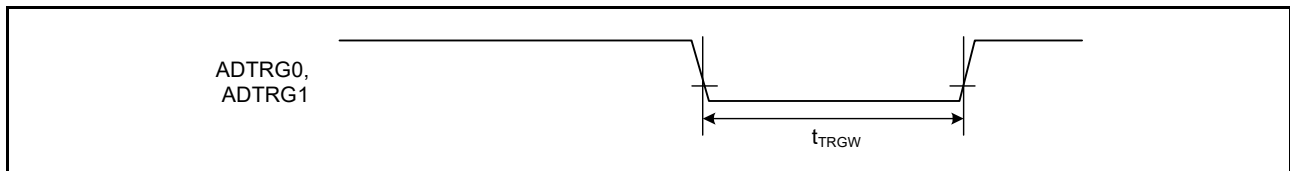


Figure 2.35 ADC12 trigger input timing

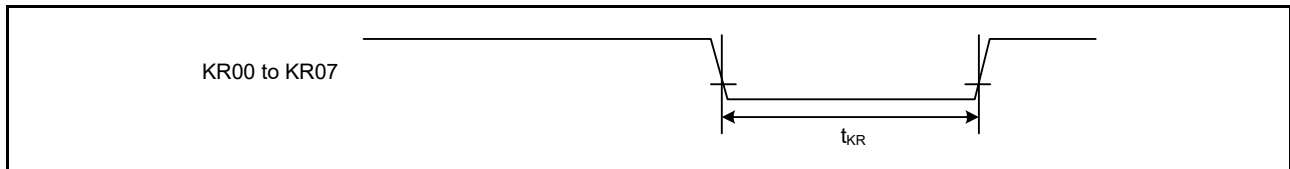


Figure 2.36 Key interrupt input timing

2.3.8 PWM Delay Generation Circuit Timing

Table 2.20 PWM Delay Generation Circuit timing

| Item | Min | Typ | Max | Unit | Test conditions |
|---------------------|-----|------|-----|------|-----------------|
| Operation frequency | 80 | - | 120 | MHz | - |
| Resolution | - | 260 | - | ps | PCLKD = 120 MHz |
| DNL*1 | - | ±2.0 | - | LSB | - |

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.9 CAC Timing

Table 2.21 CAC timing

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | | |
|------|--------------------------|-----------------------------------|--------------|-------------------------------------------|------|-----------------|----|---|
| CAC | CACREF input pulse width | $t_{PBcyc} \leq t_{cac} \times 2$ | t_{CACREF} | $4.5 \times t_{cac} + 3 \times t_{PBcyc}$ | - | - | ns | - |
| | | $t_{PBcyc} > t_{cac} \times 2$ | | $5 \times t_{cac} + 6.5 \times t_{PBcyc}$ | - | - | ns | |

Note 1. t_{PBcyc} : PCLKB cycle.

Note 2. t_{cac} : CAC count clock source cycle.

2.3.10 SCI Timing

Table 2.22 SCI timing (1)

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9 (except for SCK4_B, SCK7_A).
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | | | Symbol | Min | Max | Unit*1 | Test conditions |
|-------------------------|--------------------------|-------------------|------------|-----|-----|-------------|-----------------|
| SCI | Input clock cycle | Asynchronous | t_{Scyc} | 4 | - | t_{Pcyc} | Figure 2.37 |
| | | Clock synchronous | | 6 | - | | |
| | Input clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | |
| | Input clock rise time | | t_{SCKr} | - | 5 | ns | |
| | Input clock fall time | | t_{SCKf} | - | 5 | ns | |
| | Output clock cycle | Asynchronous | t_{Scyc} | 6 | - | t_{Pcyc} | |
| | | Clock synchronous | | 4 | - | | |
| | Output clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | |
| | Output clock rise time | | t_{SCKr} | - | 5 | ns | |
| | Output clock fall time | | t_{SCKf} | - | 5 | ns | |
| Transmit data delay | Clock synchronous | t_{TXD} | - | 25 | ns | Figure 2.38 | |
| Receive data setup time | Clock synchronous | t_{RXS} | 15 | - | ns | | |
| Receive data hold time | Clock synchronous | t_{RXH} | 5 | - | ns | | |

Note 1. t_{Pcyc} : PCLKA cycle.

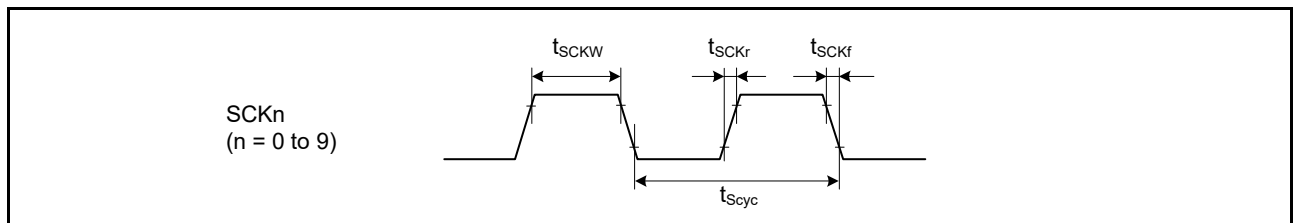


Figure 2.37 SCK clock input/output timing

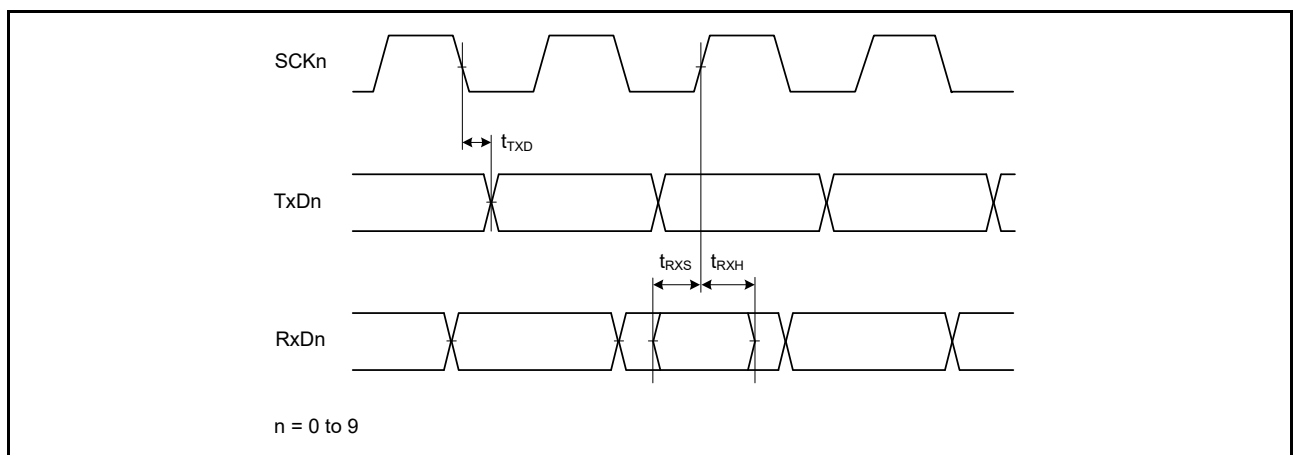


Figure 2.38 SCI input/output timing in clock synchronous mode

Table 2.23 SCI timing (2)

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9 (except for SCK4_B, SCK7_A).

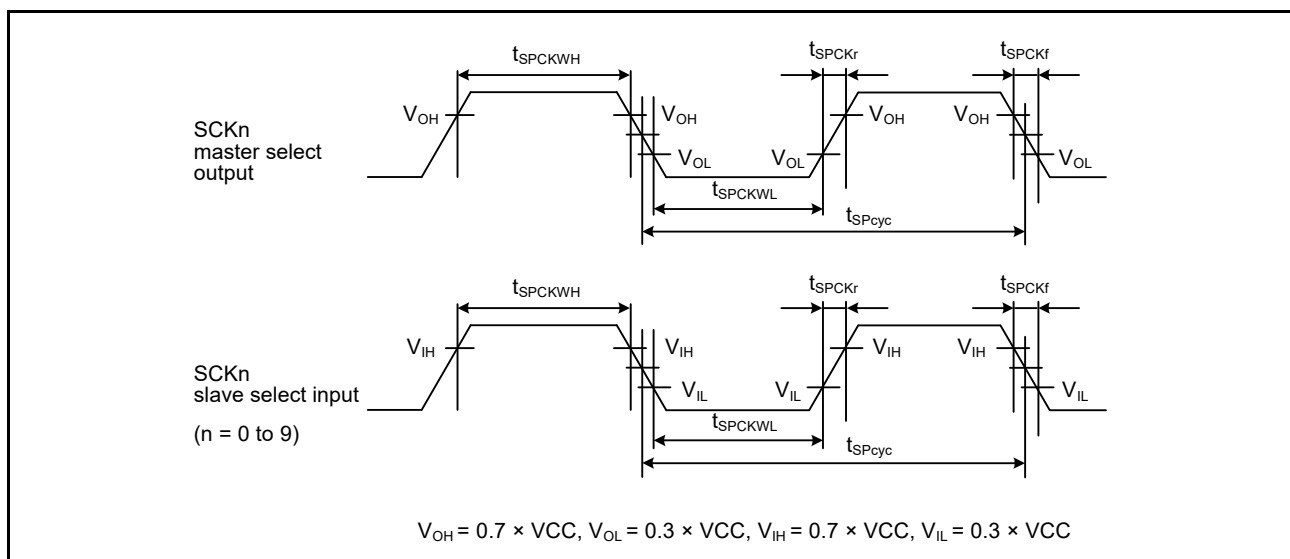
For the SCK4_B and SCK7_A pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

For the MISO1_A pins, low drive output is selected in the port drive capability bit in the PmnPFS register.

For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | Symbol | Min | Max | Unit | Test conditions | |
|------------|---------------------------------|---------------------------|--------------------------------------------------|--------------------------------------------------|-----------------|-------------------------------|
| Simple SPI | SCK clock cycle output (master) | t_{SPcyc} | 4 (PCLKA \leq 60 MHz) 8 (PCLKA $>$ 60 MHz) | 65536 | t_{Pcyc} | Figure 2.39 |
| | SCK clock cycle input (slave) | - | 6 (PCLKA \leq 60 MHz) 12 (PCLKA $>$ 60 MHz) | 65536 | | |
| | SCK clock high pulse width | t_{SPCKWH} | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock low pulse width | t_{SPCKWL} | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock rise and fall time | t_{SPCKr} , t_{SPCKf} | - | 20 | ns | |
| | Data input setup time | t_{SU} | 33.3 | - | ns | Figure 2.40 to Figure 2.43 |
| | Data input hold time | t_H | 33.3 | - | ns | |
| | SS input setup time | t_{LEAD} | 1 | - | t_{SPcyc} | |
| | SS input hold time | t_{LAG} | 1 | - | t_{SPcyc} | |
| | Data output delay | t_{OD} | - | 33.3 | ns | |
| | Data output hold time | t_{OH} | -10 | - | ns | |
| | Data rise and fall time | t_{Dr} , t_{Df} | - | 16.6 | ns | |
| | SS input rise and fall time | t_{SSLr} , t_{SSLf} | - | 16.6 | ns | |
| | Slave access time | t_{SA} | - | 4 (PCLKA \leq 60 MHz) 8 (PCLKA $>$ 60 MHz) | t_{Pcyc} | Figure 2.43 |
| | Slave output release time | t_{REL} | - | 5 (PCLKA \leq 60 MHz) 10 (PCLKA $>$ 60 MHz) | t_{Pcyc} | |

Note: MISO1_A is not supported in these specifications.

**Figure 2.39 SCI simple SPI mode clock timing**

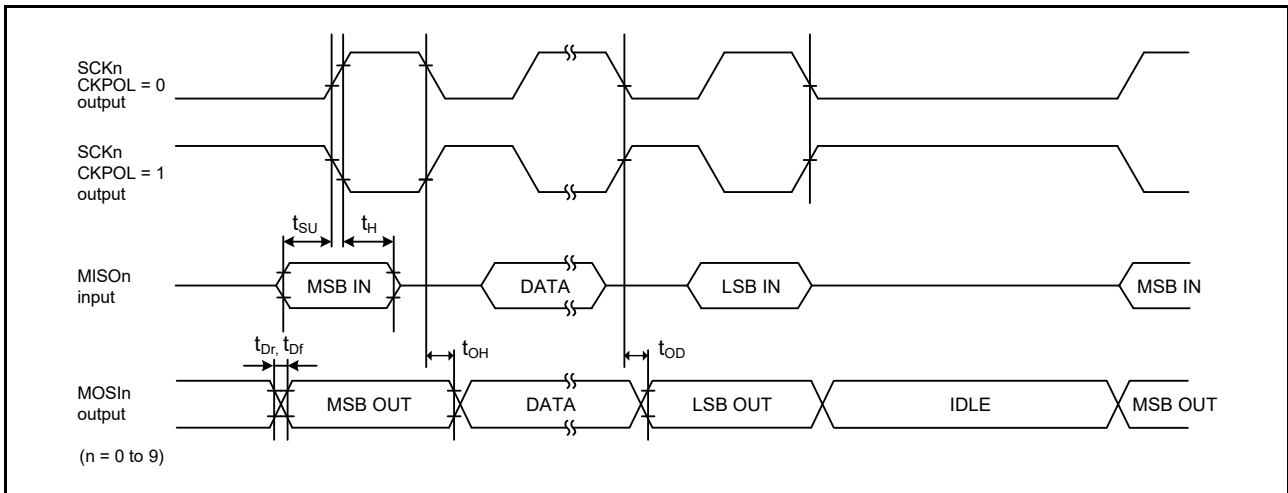


Figure 2.40 SCI simple SPI mode timing for master when CKPH = 1

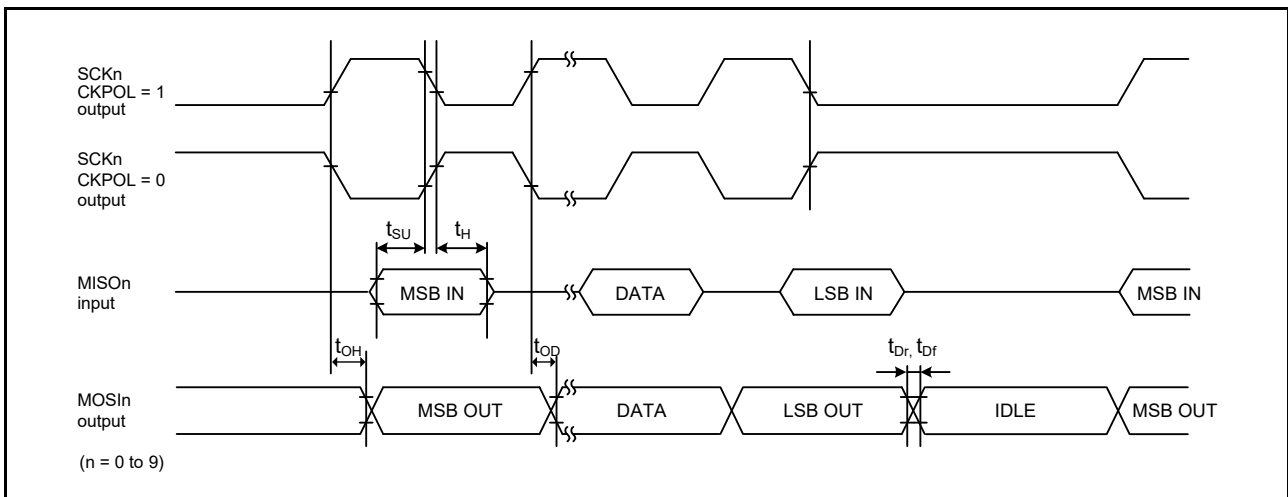


Figure 2.41 SCI simple SPI mode timing for master when CKPH = 0

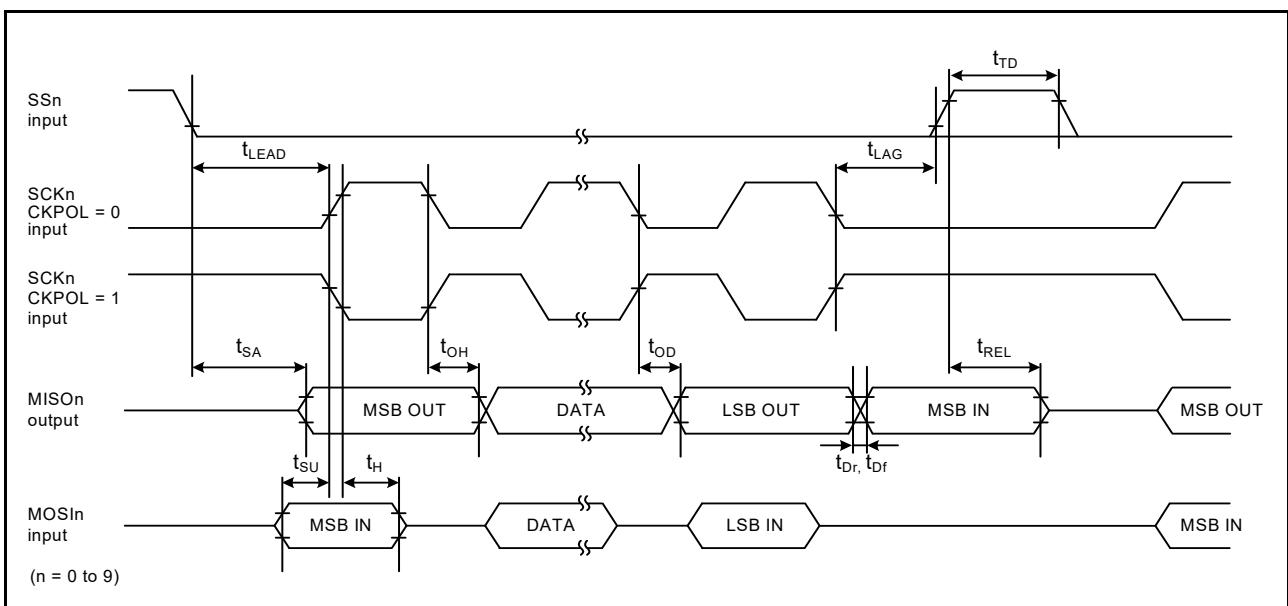


Figure 2.42 SCI simple SPI mode timing for slave when CKPH = 1

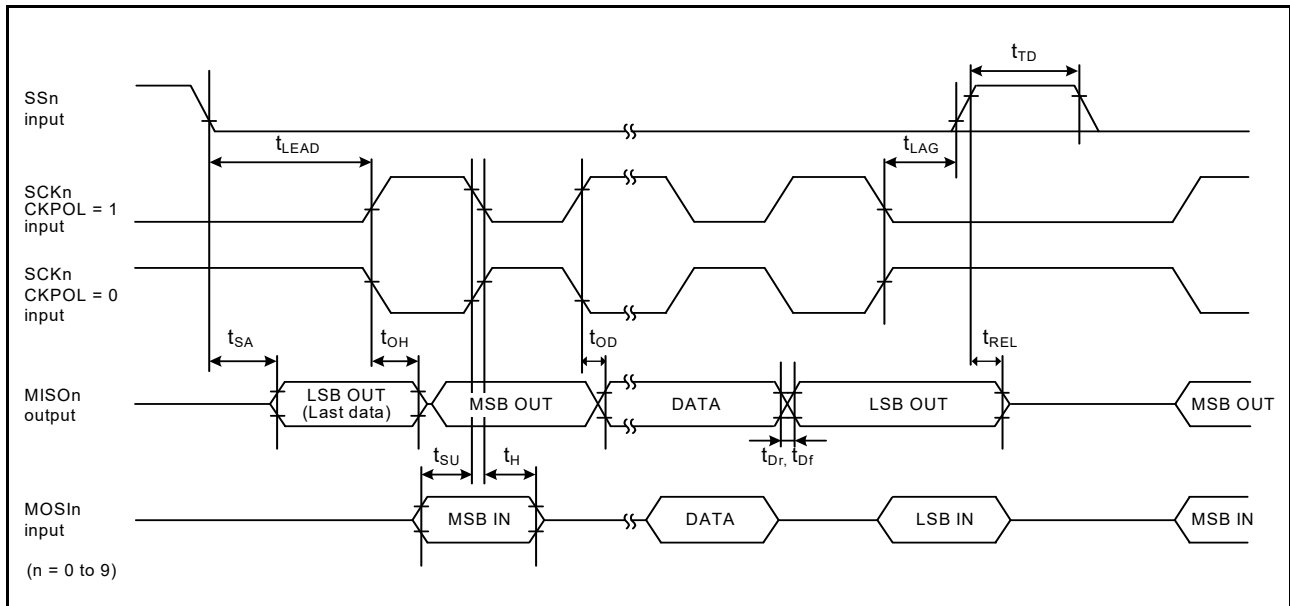


Figure 2.43 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3)

Conditions: For the SCL1_A pins, low drive output is selected in the port drive capability bit in the PmnPFS register. For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | Symbol | Min | Max | Unit | Test conditions | |
|----------------------------|------------------------------------|------------|-----|-----------------------|-----------------|-------------|
| Simple IIC (Standard mode) | SDA input rise time | t_{Sr} | - | 1000 | ns | Figure 2.44 |
| | SDA input fall time | t_{Sf} | - | 300 | ns | |
| | SDA input spike pulse removal time | t_{SP} | 0 | $4 \times t_{IICcyc}$ | ns | |
| | Data input setup time | t_{SDAS} | 250 | - | ns | |
| | Data input hold time | t_{SDAH} | 0 | - | ns | |
| | SCL, SDA capacitive load | C_b^{*1} | - | 400 | pF | |
| Simple IIC (Fast mode) | SDA input rise time | t_{Sr} | - | 300 | ns | Figure 2.44 |
| | SDA input fall time | t_{Sf} | - | 300 | ns | |
| | SDA input spike pulse removal time | t_{SP} | 0 | $4 \times t_{IICcyc}$ | ns | |
| | Data input setup time | t_{SDAS} | 100 | - | ns | |
| | Data input hold time | t_{SDAH} | 0 | - | ns | |
| | SCL, SDA capacitive load | C_b^{*1} | - | 400 | pF | |

Note: SCL1_A output is not supported in these specifications.

t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle.

Note 1. C_b indicates the total capacity of the bus line.

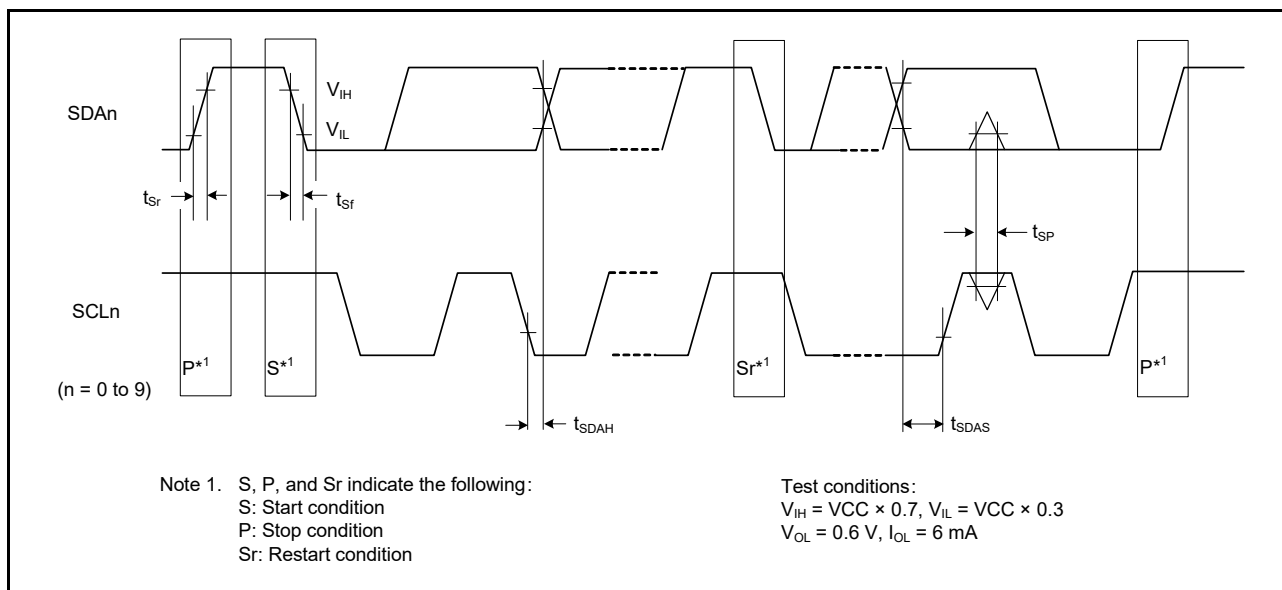


Figure 2.44 SCI simple IIC mode timing

2.3.11 SPI Timing

Table 2.25 SPI timing

Conditions:

(1) Middle drive output is selected with the port drive capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.

| Item | | Symbol | Min | Max | Unit*1 | Test conditions | |
|----------------------------------|-------------------|----------------------|-----------------------------------------------|------------------------------------------|--------|---------------------------------------------|--------------------------|
| SPI | RSPCK clock cycle | Master | t_{SPCyc} | 2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz) | 4096 | t_{Pcyc} | Figure 2.45 C = 30 pF |
| | | Slave | | 6 | 4096 | | |
| RSPCK clock high pulse width | Master | t_{SPCKWH} | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | - | ns | | |
| | Slave | | | $3 \times t_{Pcyc}$ | | | - |
| RSPCK clock low pulse width | Master | t_{SPCKWL} | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | - | ns | | |
| | Slave | | | $3 \times t_{Pcyc}$ | | | - |
| RSPCK clock rise and fall time | Master | t_{SPCKr} | - | 5 | ns | | |
| | Slave | t_{SPCKf} | - | 1 | μs | | |
| Data input setup time | Master | t_{SU} | | - | ns | Figure 2.46 to Figure 2.51 C = 30 pF | |
| | Slave | | | 5 | | | - |
| Data input hold time | Master | t_{HF}^{*4} | 0 | - | ns | - | |
| | Master | t_H | t_{Pcyc} | - | | | |
| | Slave | t_H | 20 | - | | - | |
| SSL setup time | Master | t_{LEAD} | $N \times t_{SPCyc} - 10^{*2}$ | $N \times t_{SPCyc} + 100^{*2}$ | ns | - | |
| | Slave | | | $6 \times t_{Pcyc}$ | - | ns | - |
| SSL hold time | Master | t_{LAG} | $N \times t_{SPCyc} - 10^{*3}$ | $N \times t_{SPCyc} + 100^{*3}$ | ns | - | |
| | Slave | | | $6 \times t_{Pcyc}$ | - | ns | - |
| Data output delay | Master | t_{OD} | | 6.3 | ns | Figure 2.46 to Figure 2.51 C = 30 pF | |
| | Slave | | | - | | | 20 |
| Data output hold time | Master | t_{OH} | | - | ns | | |
| | Slave | | | 0 | | | - |
| Successive transmission delay | Master | t_{TD} | | $t_{SPCyc} + 2 \times t_{Pcyc}$ | ns | | |
| | Slave | | | $6 \times t_{Pcyc}$ | | | |
| MOSI and MISO rise and fall time | Output | t_{Dr}, t_{Df} | | 5 | ns | | |
| | Input | | | - | 1 | | μs |
| SSL rise and fall time | Output | t_{SSLr}, t_{SSLf} | | 5 | ns | | |
| | Input | | | - | 1 | | μs |
| Slave access time | | t_{SA} | | $2 \times t_{Pcyc} + 28$ | ns | Figure 2.50 and Figure 2.51 C = 30 pF | |
| Slave output release time | | t_{REL} | | $2 \times t_{Pcyc} + 28$ | | | |

Note 1. t_{Pcyc} : PCLKA cycle.

Note 2. N is set to an integer from 1 to 8 by the SPCKD register.

Note 3. N is set to an integer from 1 to 8 by the SSLND register.

Note 4. PCLKA division ratio set to 1/2.

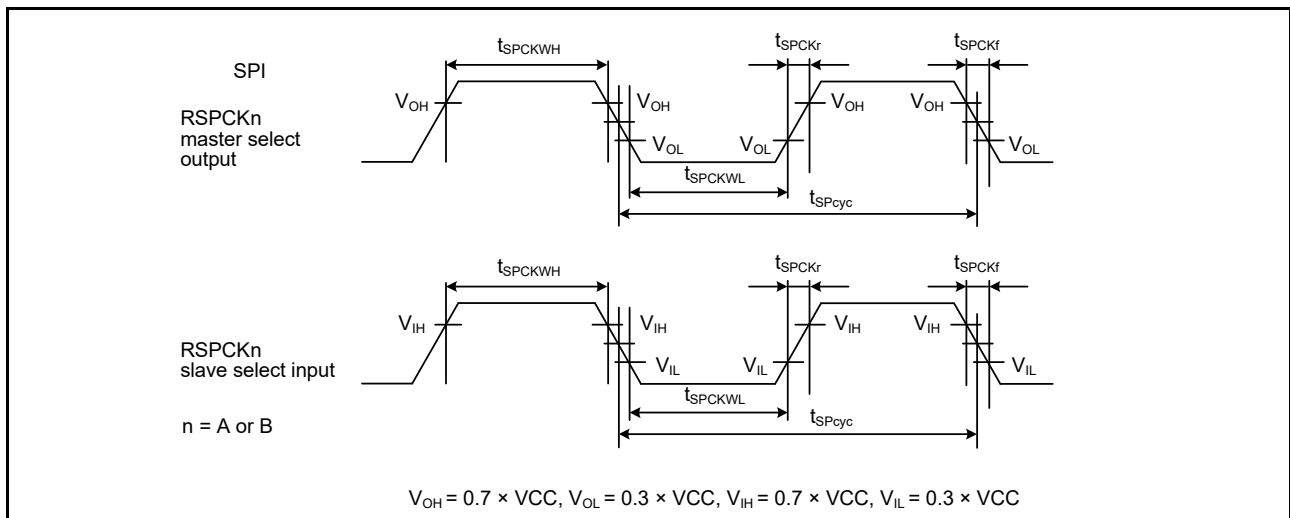


Figure 2.45 SPI clock timing

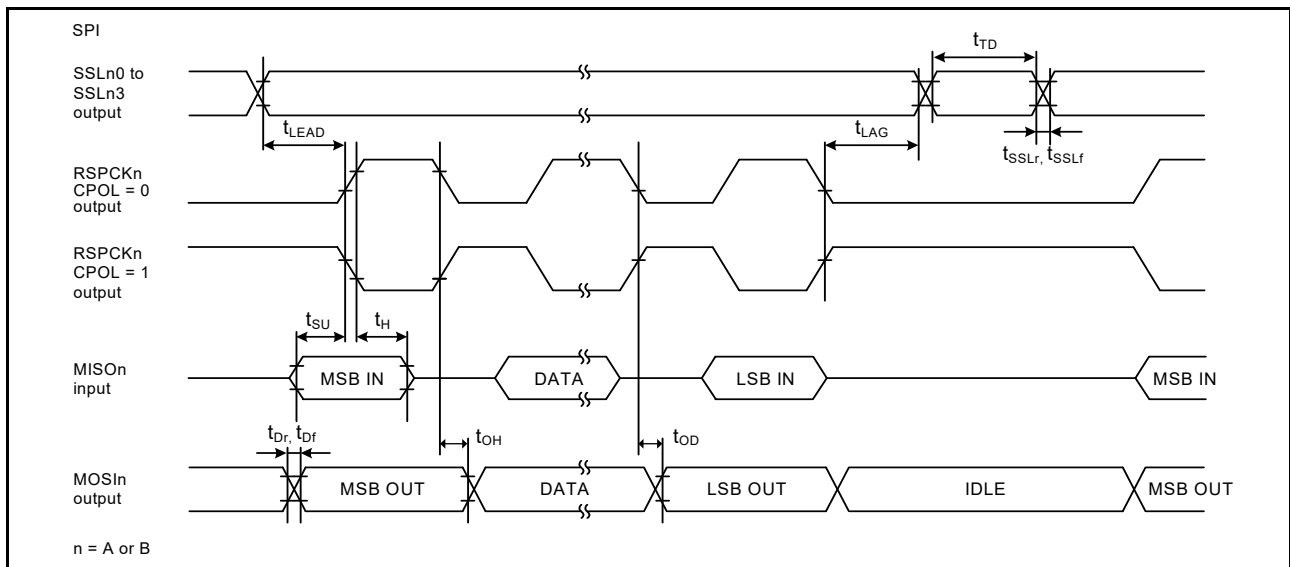


Figure 2.46 SPI timing for master when CPHA = 0

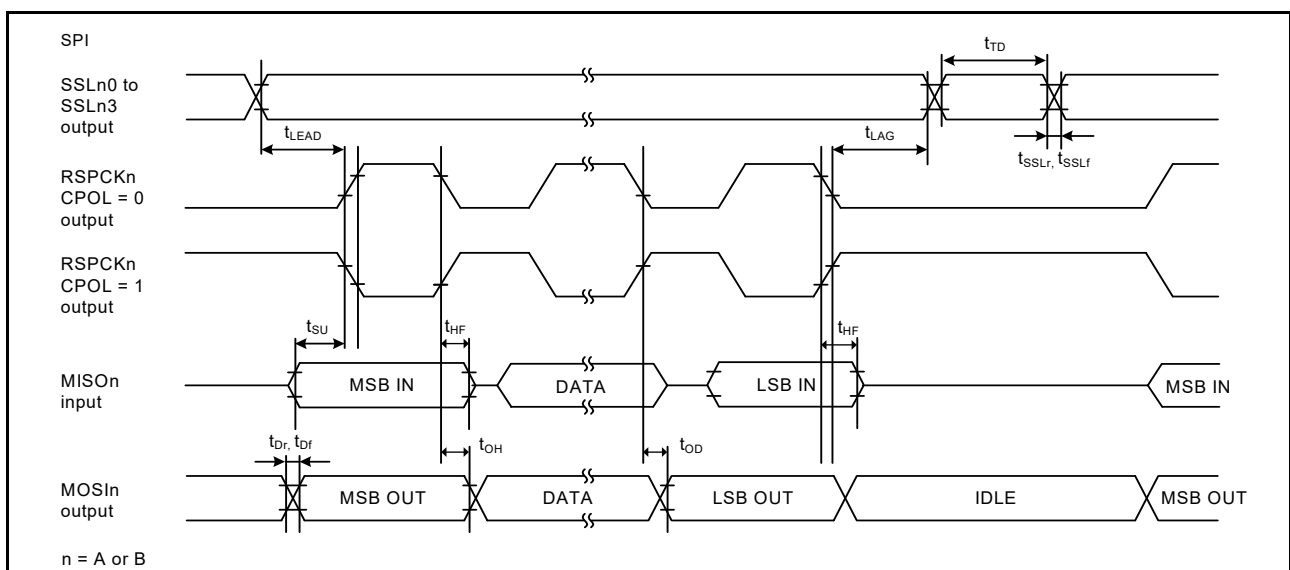


Figure 2.47 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

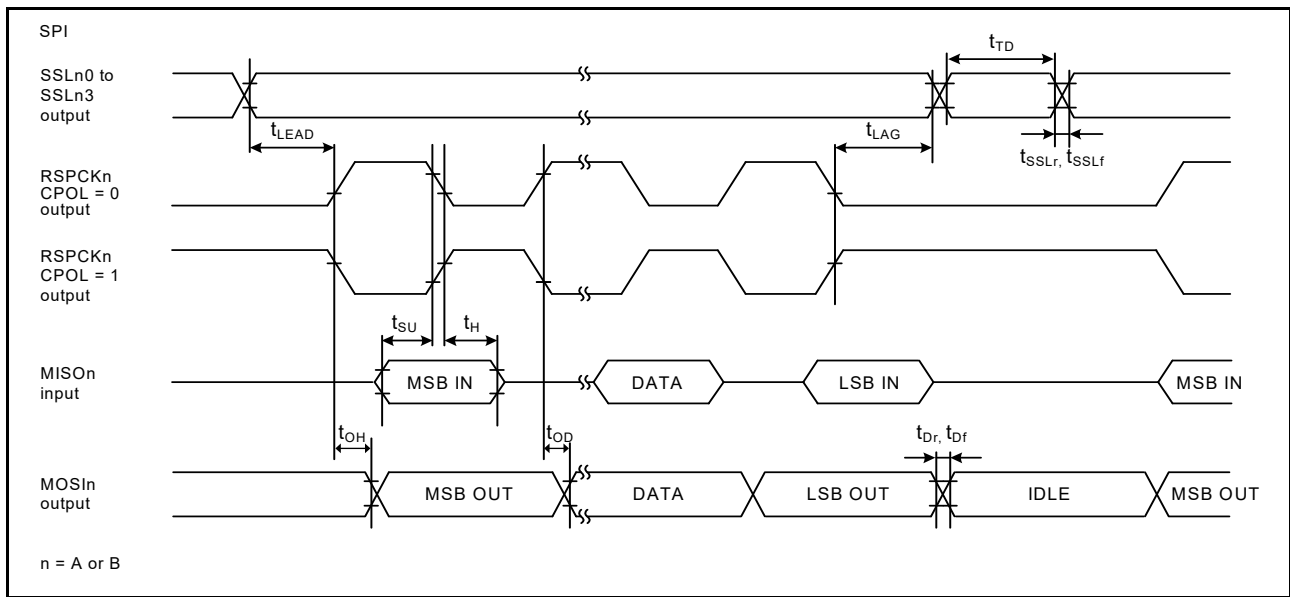


Figure 2.48 SPI timing for master when CPHA = 1

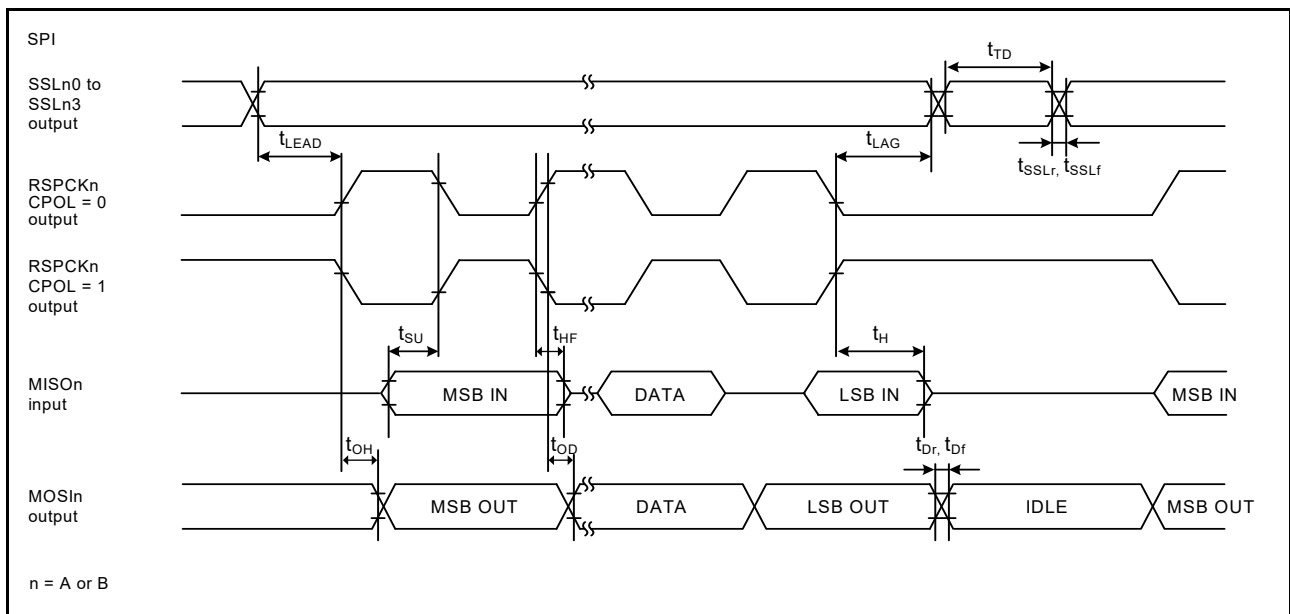


Figure 2.49 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

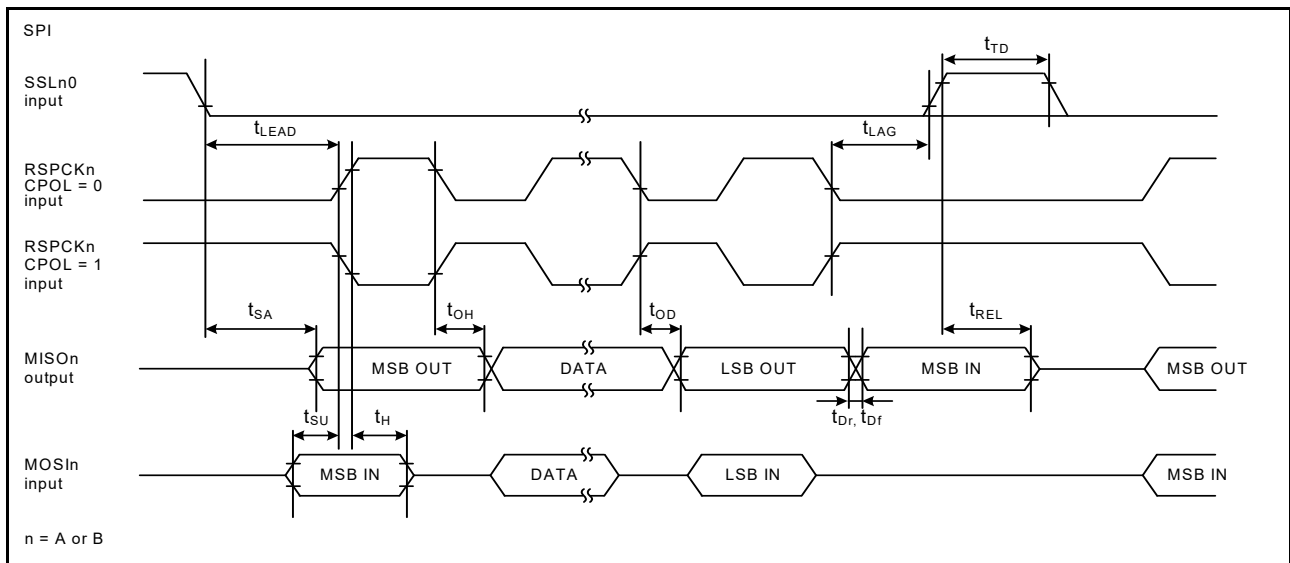


Figure 2.50 SPI timing for slave when CPHA = 0

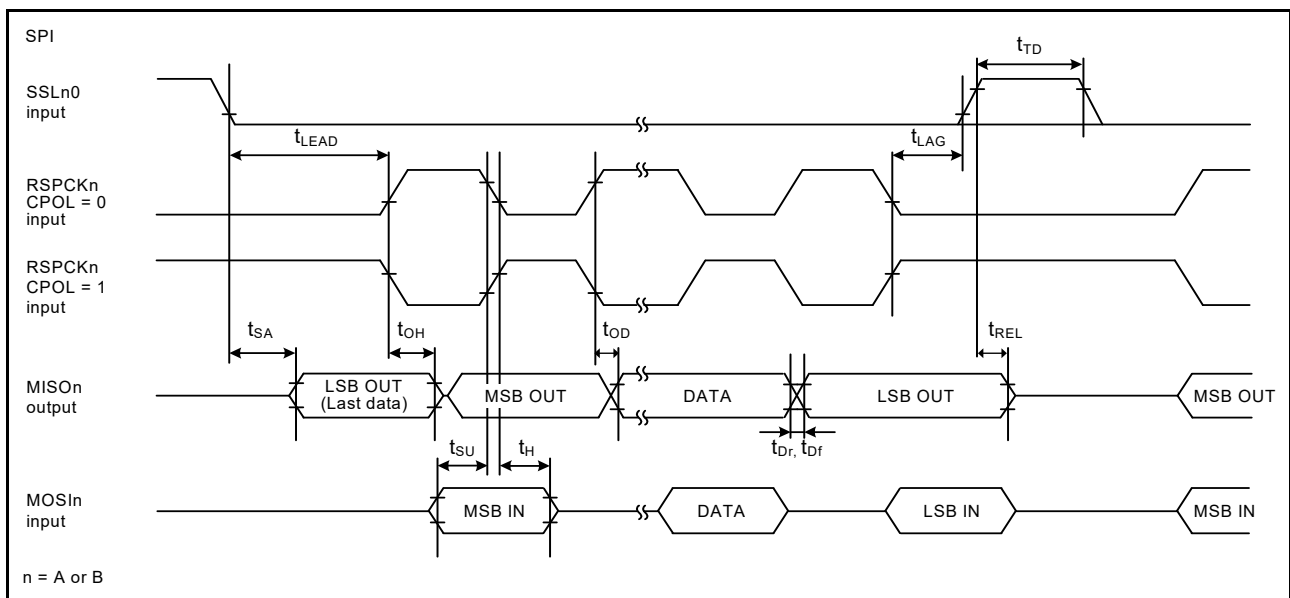


Figure 2.51 SPI timing for slave when CPHA = 1

2.3.12 QSPI Timing

Table 2.26 QSPI timing

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | Symbol | Min | Max | Unit*1 | Test conditions | |
|------|-------------------------------|-------------|-------------------------------------|---------------------------------------|-----------------|-------------|
| QSPI | QSPCK clock cycle | t_{QScyc} | 2 | 48 | t_{Pcyc} | Figure 2.52 |
| | QSPCK clock high pulse width | t_{QSWH} | $t_{QScyc} \times 0.4$ | - | ns | |
| | QSPCK clock low pulse width | t_{QSWL} | $t_{QScyc} \times 0.4$ | - | ns | |
| | Data input setup time | t_{Su} | 11 | - | ns | Figure 2.53 |
| | Data input hold time | t_{IH} | 0 | - | ns | |
| | QSSL setup time | t_{LEAD} | $(N+0.5) \times t_{QScyc} - 5^{*2}$ | $(N+0.5) \times t_{QScyc} + 100^{*2}$ | ns | |
| | QSSL hold time | t_{LAG} | $(N+0.5) \times t_{QScyc} - 5^{*3}$ | $(N+0.5) \times t_{QScyc} + 100^{*3}$ | ns | |
| | Data output delay | t_{OD} | - | 4 | ns | |
| | Data output hold time | t_{OH} | -3.3 | - | ns | |
| | Successive transmission delay | t_{TD} | 1 | 16 | t_{QScyc} | |

Note 1. t_{Pcyc} : PCLKA cycle.

Note 2. N is set to 0 or 1 in SFMSLD.

Note 3. N is set to 0 or 1 in SFMSHD.

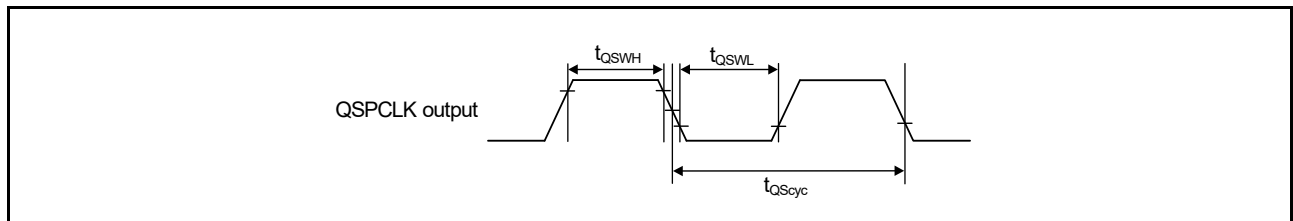


Figure 2.52 QSPI clock timing

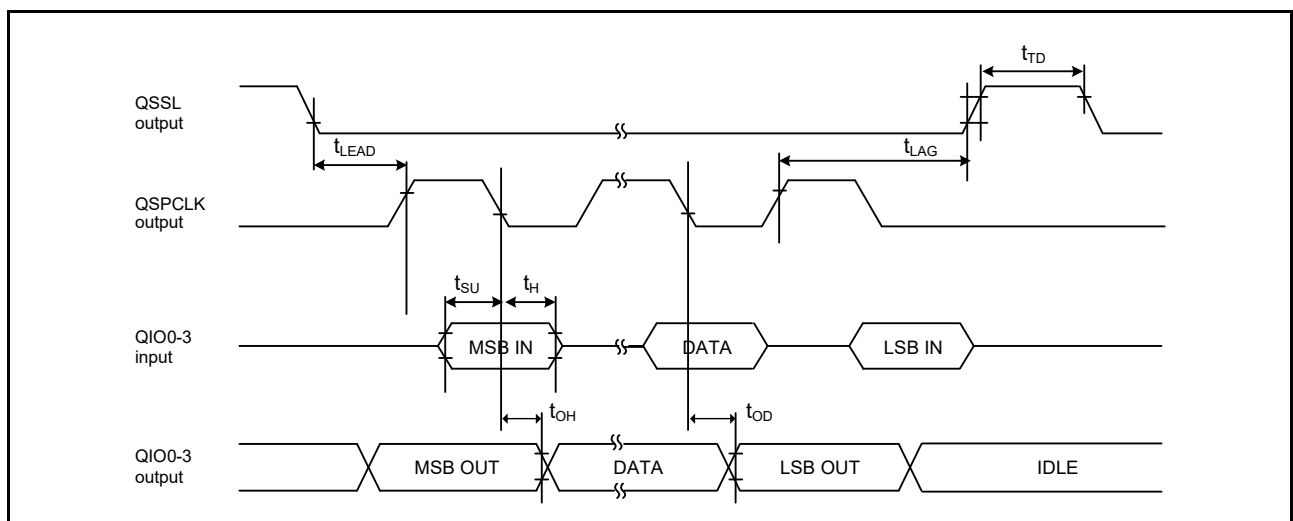


Figure 2.53 Transmit and receive timing

2.3.13 IIC Timing

Table 2.27 IIC timing (1) (1 of 2)

Conditions:

(1) Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B. The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

(2) Use pins that have a letter appended to their names, for example “_A” or “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Item | Symbol | Min*1 | Max | Unit | Test conditions | |
|----------------------------------------------------|------------------------------------------------------------------|------------|-----------------------------------------------------|---------------------------|-----------------|-------------|
| IIC (Standard mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | t_{SCL} | $6 (12) \times t_{IICcyc} + 1300$ | - | ns | Figure 2.54 |
| | SCL input high pulse width | t_{SCLH} | $3 (6) \times t_{IICcyc} + 300$ | - | ns | |
| | SCL input low pulse width | t_{SCLL} | $3 (6) \times t_{IICcyc} + 300$ | - | ns | |
| | SCL, SDA input rise time | t_{Sr} | - | 1000 | ns | |
| | SCL, SDA input fall time | t_{Sf} | - | 300 | ns | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1 (4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 300$ | - | ns | |
| | SDA input bus free time when wakeup function is enabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | - | ns | |
| | START condition input hold time when wakeup function is disabled | t_{STAH} | $t_{IICcyc} + 300$ | - | ns | |
| | START condition input hold time when wakeup function is enabled | t_{STAH} | $1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$ | - | ns | |
| | Repeated START condition input setup time | t_{STAS} | 1000 | - | ns | |
| | STOP condition input setup time | t_{STOS} | 1000 | - | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | - | ns | |
| | Data input hold time | t_{SDAH} | 0 | - | ns | |
| SCL, SDA capacitive load | C_b | - | 400 | pF | | |

Table 2.27 IIC timing (1) (2 of 2)

Conditions:

(1) Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B. The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

(2) Use pins that have a letter appended to their names, for example “_A” or “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Item | Symbol | Min*1 | Max | Unit | Test conditions | |
|--------------------------|------------------------------------------------------------------|------------|-----------------------------------------------------|--------------------------|-----------------|-------------|
| IIC (Fast mode) | SCL input cycle time | t_{SCL} | $6 (12) \times t_{IICyc} + 600$ | - | ns | Figure 2.54 |
| | SCL input high pulse width | t_{SCLH} | $3 (6) \times t_{IICyc} + 300$ | - | ns | |
| | SCL input low pulse width | t_{SCLL} | $3 (6) \times t_{IICyc} + 300$ | - | ns | |
| | SCL, SDA input rise time | t_{Sr} | $20 \times (\text{external pullup voltage}/5.5V)^2$ | 300 | ns | |
| | SCL, SDA input fall time | t_{Sf} | $20 \times (\text{external pullup voltage}/5.5V)^2$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1 (4) \times t_{IICyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | t_{BUF} | $3 (6) \times t_{IICyc} + 300$ | - | ns | |
| | SDA input bus free time when wakeup function is enabled | t_{BUF} | $3 (6) \times t_{IICyc} + 4 \times t_{Pcyc} + 300$ | - | ns | |
| | START condition input hold time when wakeup function is disabled | t_{STAH} | $t_{IICyc} + 300$ | - | ns | |
| | START condition input hold time when wakeup function is enabled | t_{STAH} | $1(5) \times t_{IICyc} + t_{Pcyc} + 300$ | - | ns | |
| | Repeated START condition input setup time | t_{STAS} | 300 | - | ns | |
| | STOP condition input setup time | t_{STOS} | 300 | - | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICyc} + 50$ | - | ns | |
| | Data input hold time | t_{SDAH} | 0 | - | ns | |
| SCL, SDA capacitive load | C_b | - | 400 | pF | | |

Note: t_{IICyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.

Table 2.28 IIC timing (2)

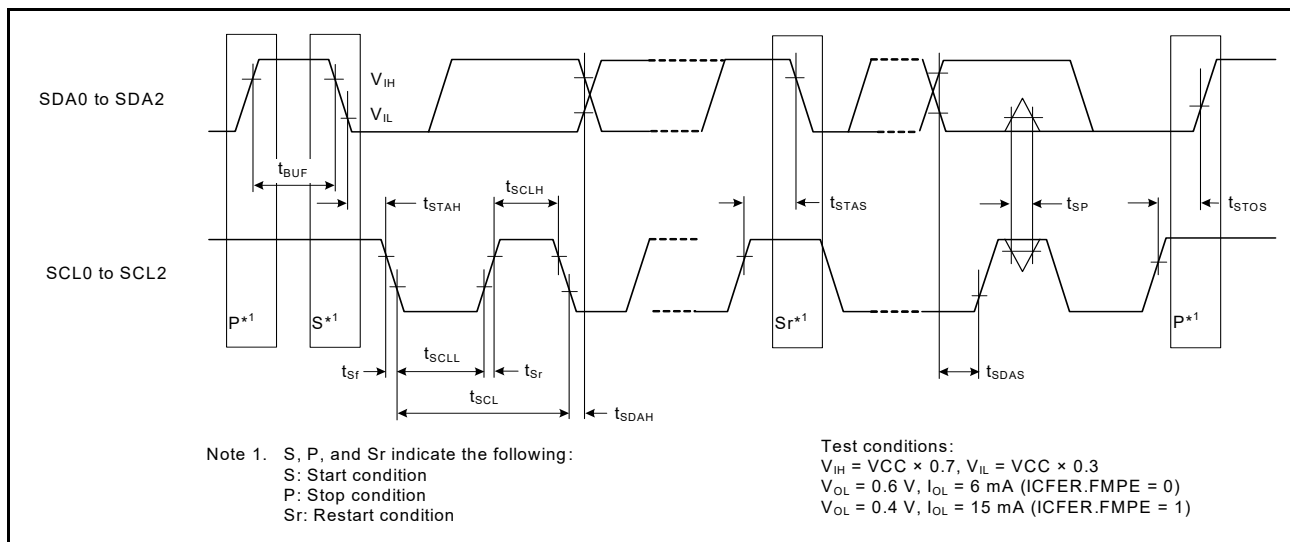
Conditions:

(1) Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.

| Item | Symbol | Min*1,*2 | Max | Unit | Test conditions | |
|---------------------------------------|------------------------------------------------------------------|------------|----------------------------------------------------|---------------------------|-----------------|-------------|
| IIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | t_{SCL} | $6 (12) \times t_{IICcyc} + 240$ | - | ns | Figure 2.54 |
| | SCL input high pulse width | t_{SCLH} | $3 (6) \times t_{IICcyc} + 120$ | - | ns | |
| | SCL input low pulse width | t_{SCLL} | $3 (6) \times t_{IICcyc} + 120$ | - | ns | |
| | SCL, SDA input rise time | t_{Sr} | - | 120 | ns | |
| | SCL, SDA input fall time | t_{Sf} | - | 120 | ns | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1 (4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 120$ | - | ns | |
| | SDA input bus free time when wakeup function is enabled | t_{BUF} | $3(6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 120$ | - | ns | |
| | Start condition input hold time when wakeup function is disabled | t_{STAH} | $t_{IICcyc} + 120$ | - | ns | |
| | START condition input hold time when wakeup function is enabled | t_{STAH} | $1(5) \times t_{IICcyc} + t_{Pcyc} + 120$ | - | ns | |
| | Restart condition input setup time | t_{STAS} | 120 | - | ns | |
| | Stop condition input setup time | t_{STOS} | 120 | - | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 30$ | - | ns | |
| | Data input hold time | t_{SDAH} | 0 | - | ns | |
| | SCL, SDA capacitive load | C_b | - | 550 | pF | |

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. C_b indicates the total capacity of the bus line.**Figure 2.54 I²C bus interface input/output timing**

2.3.14 SSI Timing

Table 2.29 SSI timing

Conditions:

(1) Middle drive output is selected with the port drive capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the SSI interface, the AC portion of the electrical characteristics is measured for each group.

| Item | Symbol | Min | Max | Unit | Test conditions | |
|------|------------------------------------------|-------------|-----|-------|-----------------|-------------|
| SSI | AUDIO_CLK input frequency | t_{AUDIO} | - | 50 | MHz | - |
| | Output clock period | t_O | 150 | 64000 | ns | Figure 2.55 |
| | Input clock period | t_I | 150 | 64000 | ns | |
| | Clock high pulse width | t_{HC} | 60 | - | ns | |
| | Clock low pulse width | t_{LC} | 60 | - | ns | |
| | Clock rise time | t_{RC} | - | 25 | ns | |
| | Data delay | t_{DTR} | -5 | 25 | ns | |
| | Set-up time | t_{SR} | 25 | - | ns | |
| | Hold time | t_{HTR} | 25 | - | ns | |
| | SSIDATA output delay from WS change time | T_{DTRW} | - | 25 | ns | Figure 2.58 |

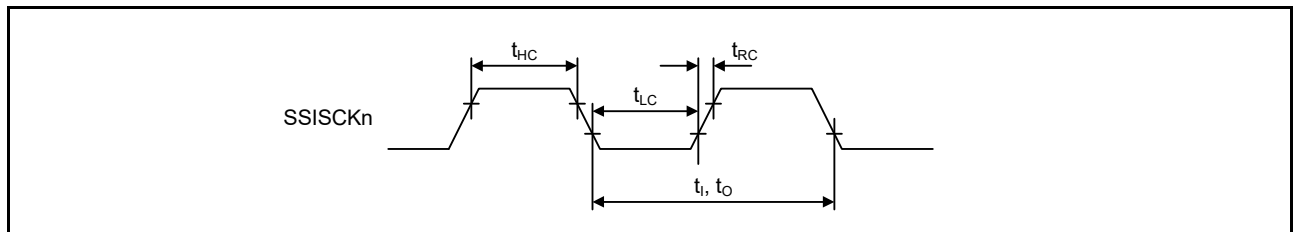


Figure 2.55 SSI clock input/output timing

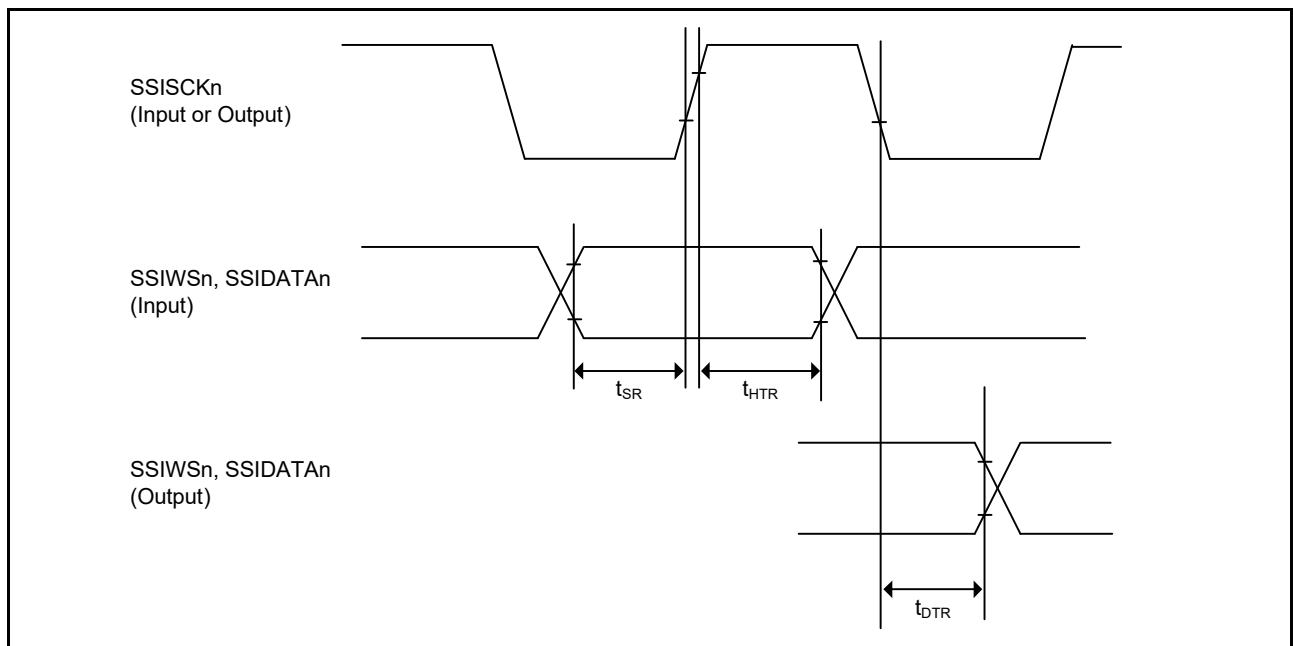


Figure 2.56 SSI data transmit and receive timing when SSICR.SCKP = 0

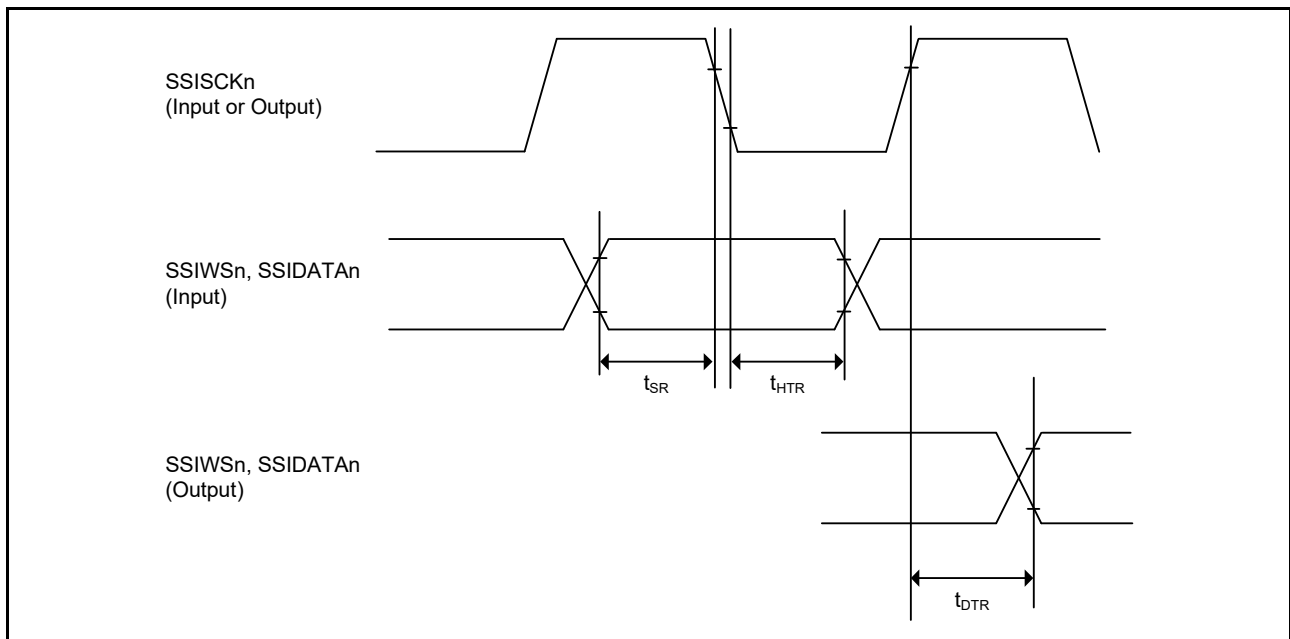


Figure 2.57 SSI data transmit and receive timing when SSICR.SCKP = 1

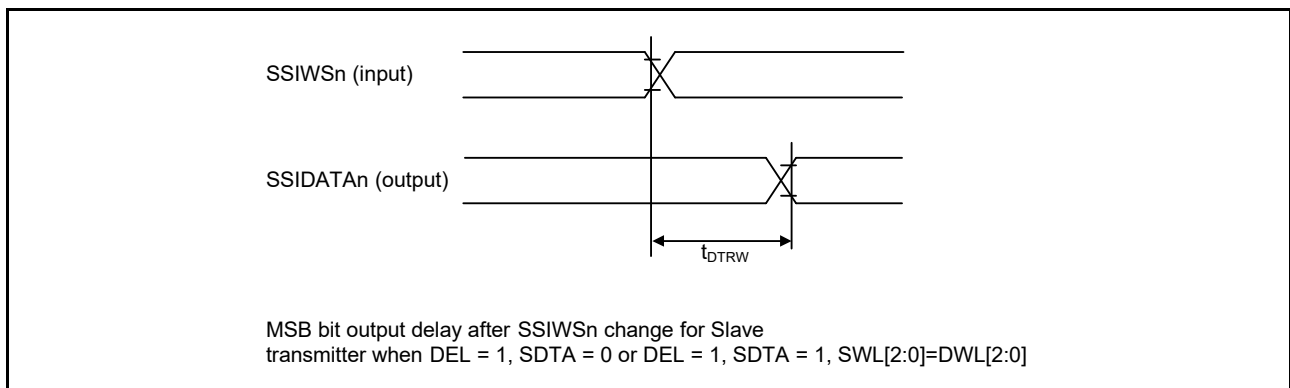


Figure 2.58 SSI data output delay after SSIWSn change

2.3.15 SD/MMC Host Interface Timing

Table 2.30 SD/MMC Host Interface signal timing

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.
Clock duty ratio is 50%.

| Item | Symbol | Min | Max | Unit | Test conditions |
|-------------------------------|--------------|-----|-----|------|-----------------|
| SDCLK clock cycle | T_{SDCYC} | 20 | - | ns | Figure 2.59 |
| SDCLK clock high pulse width | T_{SDWH} | 6.5 | - | ns | |
| SDCLK clock low pulse width | T_{SDWL} | 6.5 | - | ns | |
| SDCLK clock rise time | T_{SDLH} | - | 3 | ns | |
| SDCLK clock fall time | T_{SDHL} | - | 3 | ns | |
| SDCMD/SDDAT output data delay | T_{SDODLY} | -6 | 5 | ns | |
| SDCMD/SDDAT input data setup | T_{SDIS} | 4 | - | ns | |
| SDCMD/SDDAT input data hold | T_{SDIH} | 2 | - | ns | |

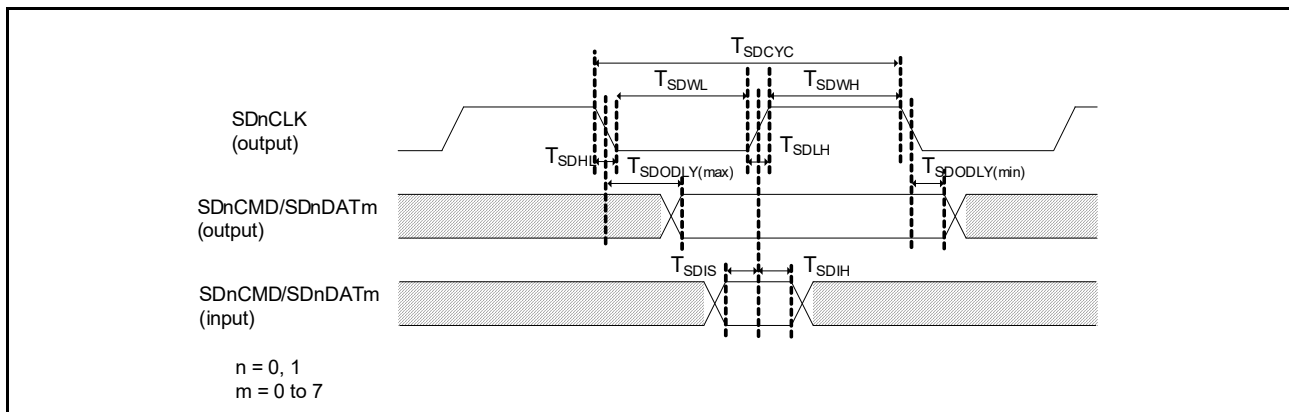


Figure 2.59 SD/MMC Host Interface signal timing

2.3.16 ETHERC Timing

Table 2.31 ETHERC timing

Conditions: ETHERC (RMII): Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO, ET1_MDC, and ET1_MDIO

For other pins, high drive output is selected in the port drive capability bit in the PmnPFS register.

ETHERC (MII): Middle drive output is selected in the port drive capability bit in the PmnPFS register

n = 0, 1.

| Item | Symbol | Min | Max | Unit | Test conditions | |
|----------------------|------------------------------------|---------------|------|--------------|-----------------|----------------------------|
| ETHERC (RMII) | REF50CKn cycle time | T_{ck} | 20 | - | ns | Figure 2.60 to Figure 2.63 |
| | REF50CKn frequency, typical 50 MHz | - | - | 50 + 100 ppm | MHz | |
| | REF50CKn duty | - | 35 | 65 | % | |
| | REF50CKn rise/fall time | $T_{ckr/ckf}$ | 0.5 | 3.5 | ns | |
| | RMIIIn_XXXX*1 output delay | T_{co} | 2.5 | 12.0 | ns | |
| | RMIIIn_XXXX*2 setup time | T_{su} | 3 | - | ns | |
| | RMIIIn_XXXX*2 hold time | T_{hd} | 1 | - | ns | |
| | RMIIIn_XXXX*1, *2 rise/fall time | T_r/T_f | 0.4 | 4 | ns | |
| ETn_WOL output delay | t_{WOLd} | 1 | 23.5 | ns | Figure 2.64 | |
| ETHERC (MII) | ETn_TX_CLK cycle time | t_{Tcyc} | 40 | - | ns | - |
| | ETn_TX_EN output delay | t_{TENd} | 1 | 20 | ns | Figure 2.65 |
| | ETn_ETXD0 to ET_ETXD3 output delay | t_{MTDd} | 1 | 20 | ns | |
| | ETn_CRS setup time | t_{CRSs} | 10 | - | ns | Figure 2.66 |
| | ETn_CRS hold time | t_{CRSh} | 10 | - | ns | |
| | ETn_COL setup time | t_{COLs} | 10 | - | ns | Figure 2.66 |
| | ETn_COL hold time | t_{COLh} | 10 | - | ns | |
| | ETn_RX_CLK cycle time | t_{TRcyc} | 40 | - | ns | - |
| | ETn_RX_DV setup time | t_{RDVs} | 10 | - | ns | Figure 2.67 |
| | ETn_RX_DV hold time | t_{RDVh} | 10 | - | ns | |
| | ETn_ERXD0 to ET_ERXD3 setup time | t_{MRDs} | 10 | - | ns | Figure 2.68 |
| | ETn_ERXD0 to ET_ERXD3 hold time | t_{MRDh} | 10 | - | ns | |
| | ETn_RX_ER setup time | t_{RERs} | 10 | - | ns | Figure 2.68 |
| | ETn_RX_ER hold time | t_{RESh} | 10 | - | ns | |
| ETn_WOL output delay | t_{WOLd} | 1 | 23.5 | ns | Figure 2.69 | |

Note 1. RMIIIn_TXD_EN, RMIIIn_TXD1, RMIIIn_TXD0.

Note 2. RMIIIn_CRS_DV, RMIIIn_RXD1, RMIIIn_RXD0, RMIIIn_RX_ER.

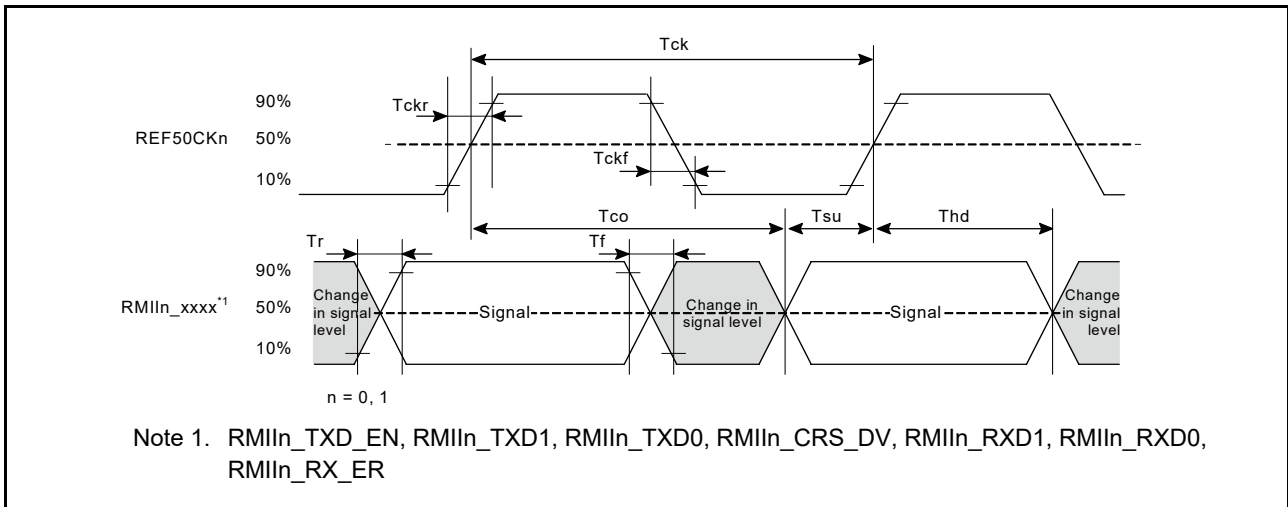


Figure 2.60 REF50CKn and RMII signal timing (n = 0 and 1)

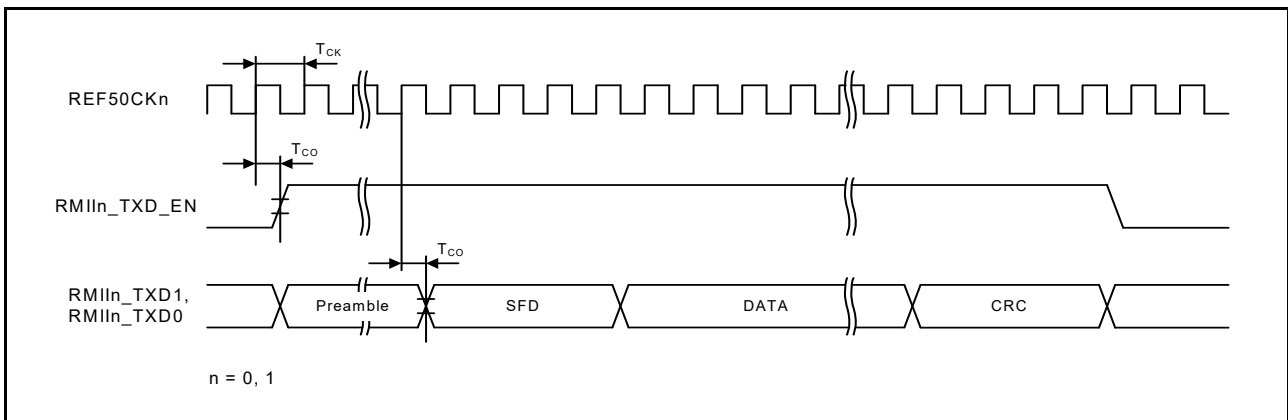


Figure 2.61 RMII transmission timing

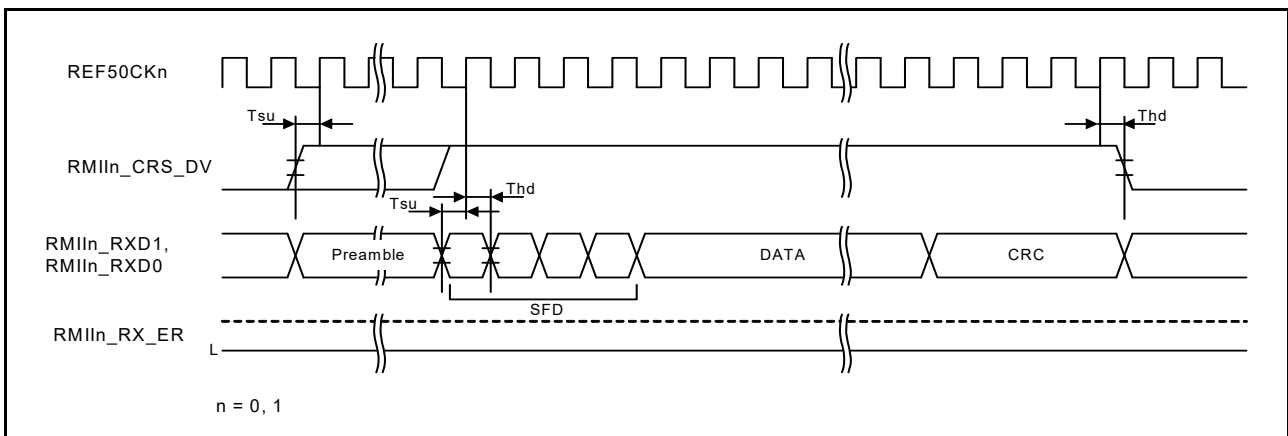


Figure 2.62 RMII reception timing in normal operation

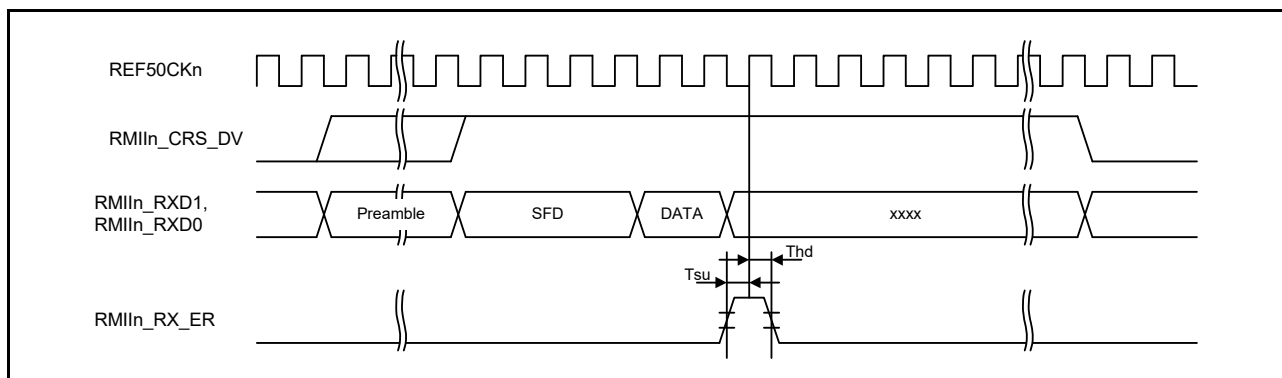


Figure 2.63 RMII reception timing when an error occurs

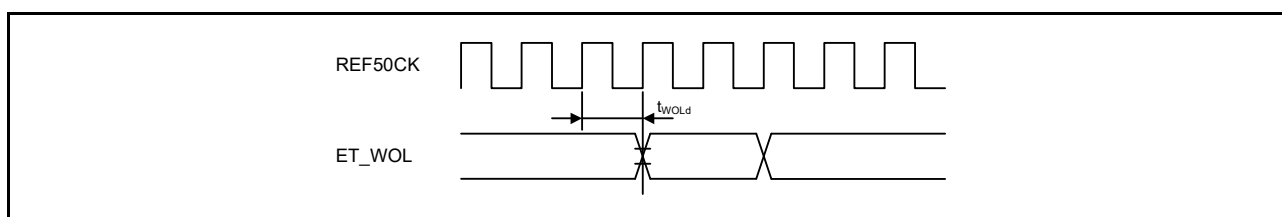


Figure 2.64 WOL output timing for RMII

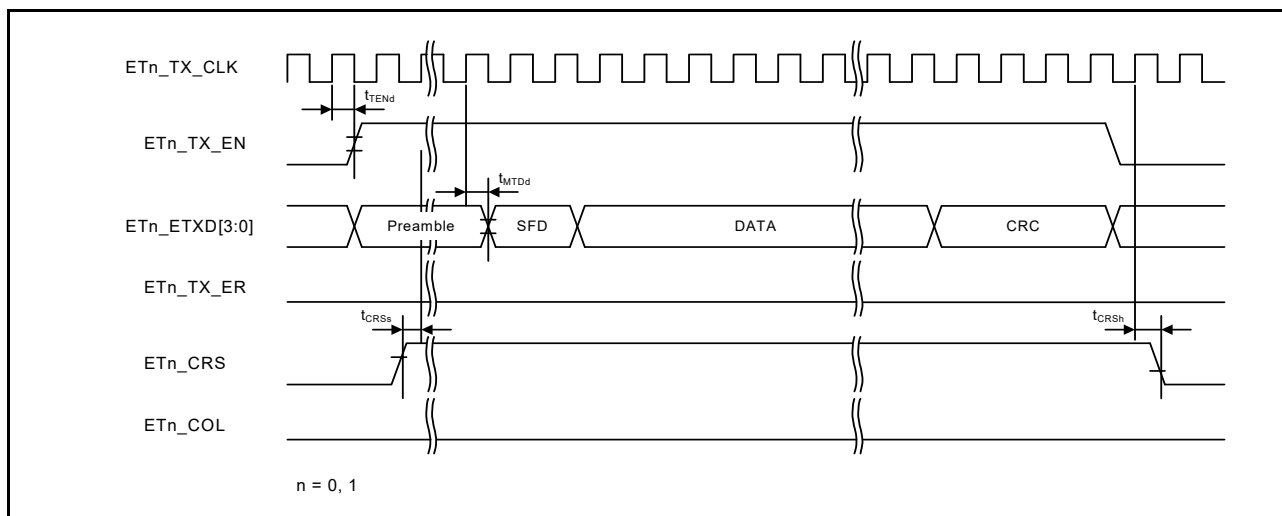


Figure 2.65 MII transmission timing in normal operation

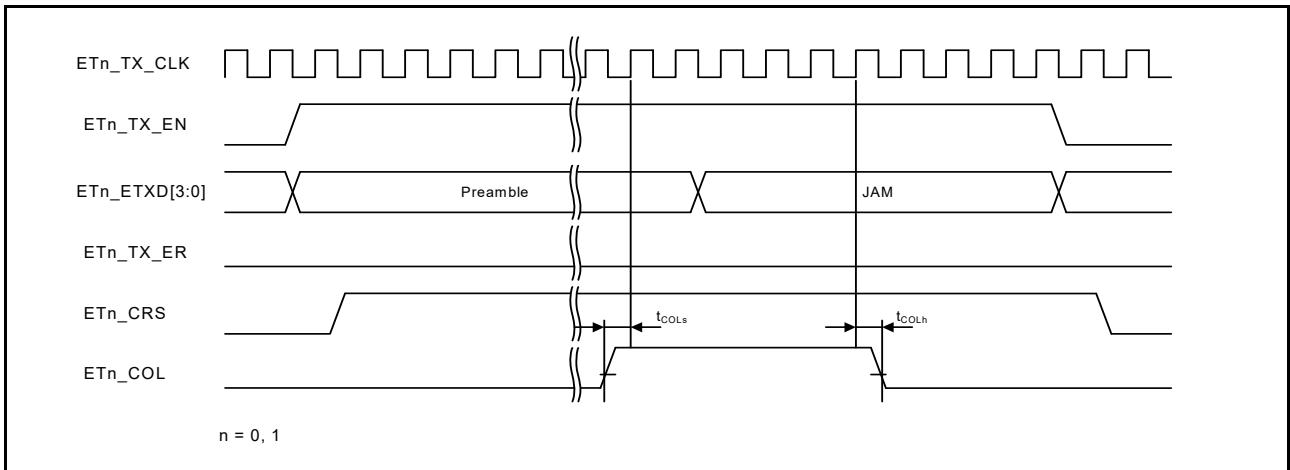


Figure 2.66 MII transmission timing when a conflict occurs

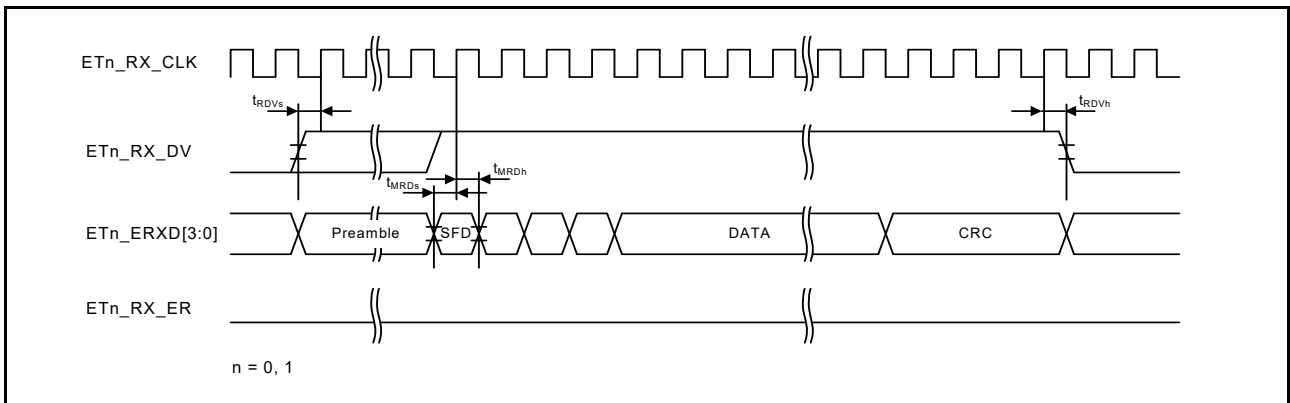


Figure 2.67 MII reception timing in normal operation

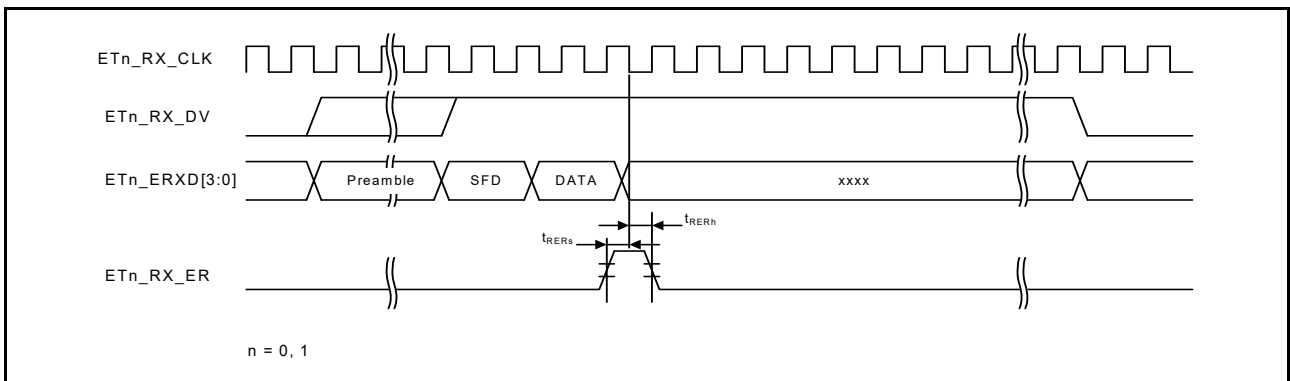


Figure 2.68 MII reception timing when an error occurs

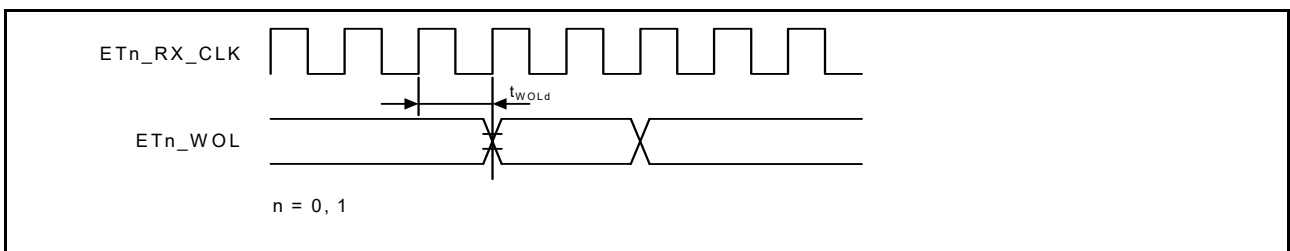


Figure 2.69 WOL output timing for MII

2.3.17 PDC Timing

Table 2.32 PDC timing

Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF

| Item | Symbol | Min | Max | Unit | Test conditions | |
|------|-------------------------------|--------------|--------------------------------------------|------|-----------------|-------------|
| PDC | PIXCLK input cycle time | t_{PIXcyc} | 37 | - | ns | Figure 2.70 |
| | PIXCLK input high pulse width | t_{PIXH} | 10 | - | ns | |
| | PIXCLK input low pulse width | t_{PIXL} | 10 | - | ns | |
| | PIXCLK rise time | t_{PIXr} | - | 5 | ns | |
| | PIXCLK fall time | t_{PIXf} | - | 5 | ns | |
| PDC | PCKO output cycle time | t_{PCKcyc} | $2 \times t_{PBcyc}$ | - | ns | Figure 2.71 |
| | PCKO output high pulse width | t_{PCKH} | $(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$ | - | ns | |
| | PCKO output low pulse width | t_{PCKL} | $(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$ | - | ns | |
| | PCKO rise time | t_{PCKr} | - | 5 | ns | |
| | PCKO fall time | t_{PCKf} | - | 5 | ns | |
| PDC | VSYNV/HSYNC input setup time | t_{SYNCS} | 10 | - | ns | Figure 2.72 |
| | VSYNV/HSYNC input hold time | t_{SYNCH} | 5 | - | ns | |
| | PIXD input setup time | t_{PIXDS} | 10 | - | ns | |
| | PIXD input hold time | t_{PIXDH} | 5 | - | ns | |

Note 1. t_{PBcyc} : PCLKB cycle.

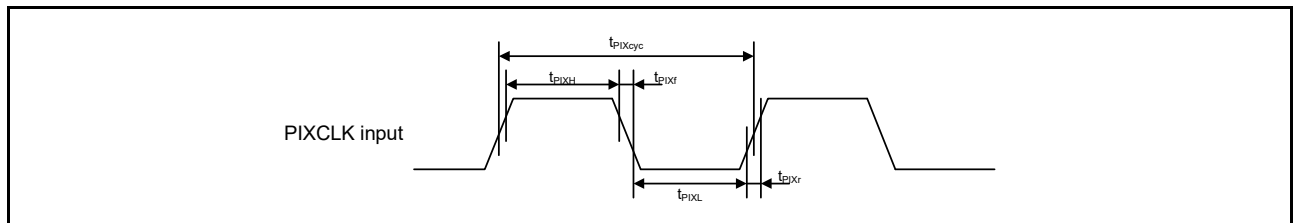


Figure 2.70 PDC input clock timing

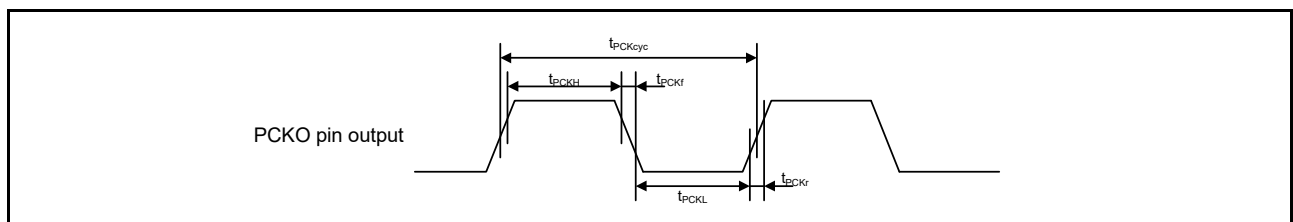


Figure 2.71 PDC output clock timing

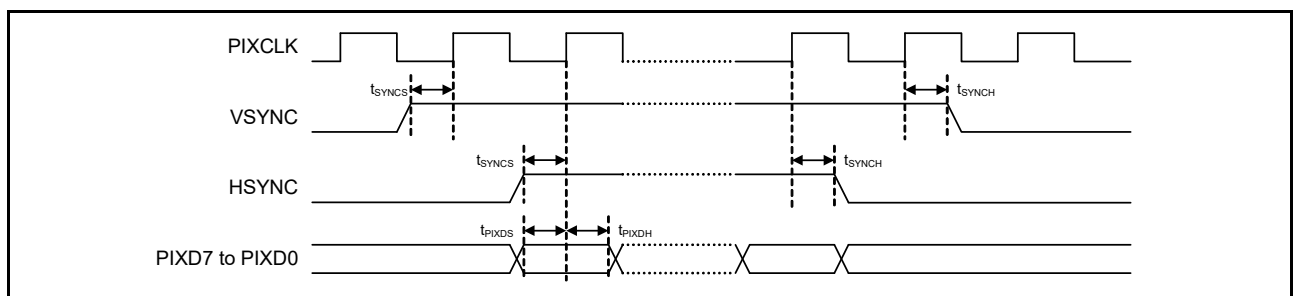


Figure 2.72 PDC AC timing

2.3.18 Graphics LCD Controller Timing

Table 2.33 Graphics LCD Controller timing

Conditions:

LCD_CLK: High drive output is selected in the port drive capability bit in the PmnPFS register.

LCD_DATA: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | |
|-----------------------------------------|--------------------------|----------|------|------|---------------|-----------------|-------------|
| LCD_EXTCLK input clock frequency | $t_{E_{cyc}}$ | - | - | 60*1 | MHz | Figure 2.73 | |
| LCD_EXTCLK input clock low pulse width | t_{WL} | 0.45 | - | 0.55 | $t_{E_{cyc}}$ | | |
| LCD_EXTCLK input clock high pulse width | t_{WH} | 0.45 | - | 0.55 | | | |
| LCD_CLK output clock frequency | $t_{L_{cyc}}$ | - | - | 60*1 | MHz | Figure 2.74 | |
| LCD_CLK output clock low pulse width | t_{LOL} | 0.4 | - | 0.6 | $t_{L_{cyc}}$ | Figure 2.74 | |
| LCD_CLK output clock high pulse width | t_{LOH} | 0.4 | - | 0.6 | $t_{L_{cyc}}$ | Figure 2.74 | |
| LCD data output delay timing | _A or _B combinations*2 | t_{DD} | -3.5 | - | 4 | ns | Figure 2.75 |
| | _A and _B combinations*3 | | -5.0 | - | 5.5 | | |

Note 1. Parallel RGB888, 666,565: Maximum 54 MHz

Serial RGB888: Maximum 60 MHz (4x speed)

Note 2. Use pins that have a letter appended to their names, for instance, “_A” or “_B”, to indicate

Note 3. Pins of group “_A” and “_B” combinations are used.

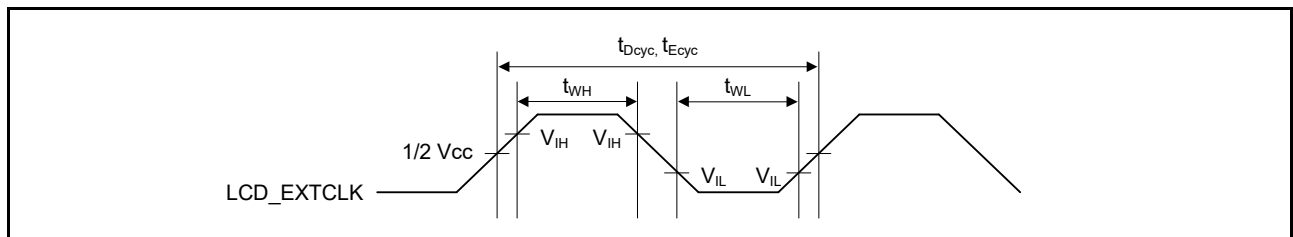


Figure 2.73 LCD_EXTCLK clock input timing

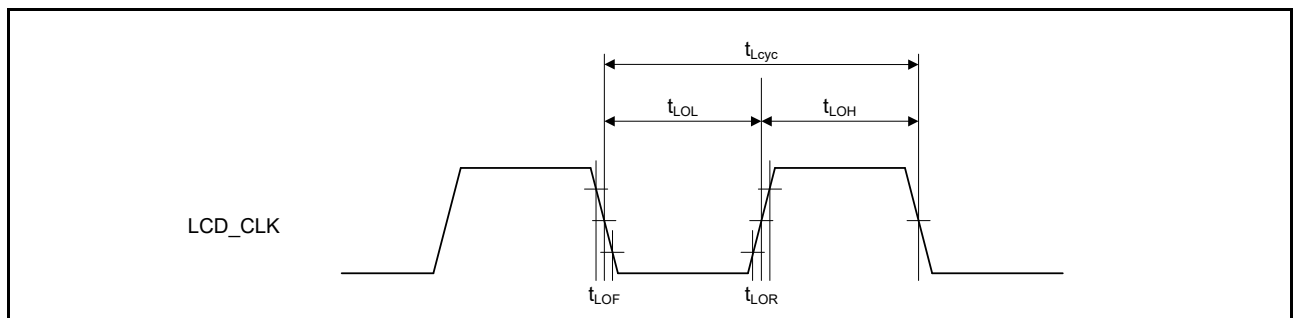


Figure 2.74 LCD_CLK clock output timing

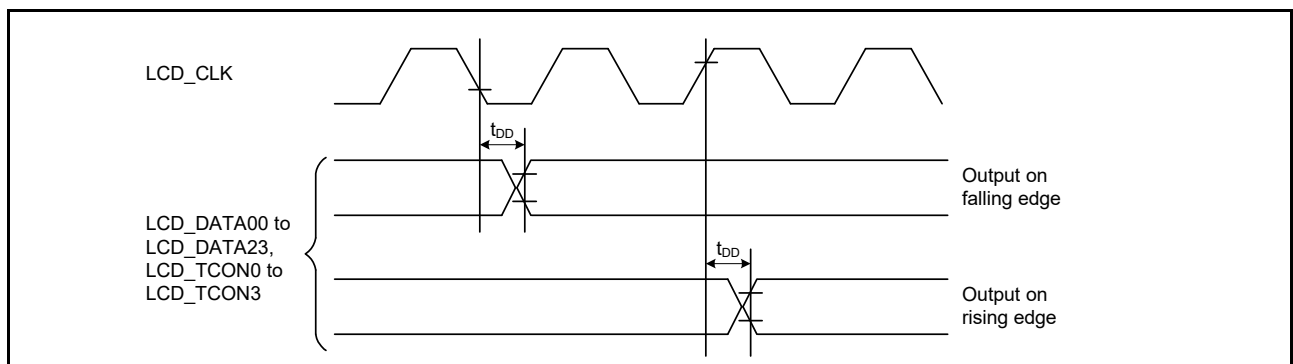


Figure 2.75 Display output timing

2.4 USB Characteristics

2.4.1 USBHS Timing

Table 2.34 USBHS low-speed characteristics for host only (USBHS_DP and USBHS_DM pin characteristics)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | |
|------------------------------------|--------------------------------------------------|-------------------|-------|-----|-------|-----------------|-------------------------|
| Input characteristics | Input high voltage | V_{IH} | 2.0 | - | - | V | |
| | Input low voltage | V_{IL} | - | - | 0.8 | V | |
| | Differential input sensitivity | V_{DI} | 0.2 | - | - | V | USBHS_DP - USBHS_DM |
| | Differential common-mode range | V_{CM} | 0.8 | - | 2.5 | V | |
| Output characteristics | Output high voltage | V_{OH} | 2.8 | - | 3.6 | V | $I_{OH} = -200 \mu A$ |
| | Output low voltage | V_{OL} | 0.0 | - | 0.3 | V | $I_{OL} = 2 \text{ mA}$ |
| | Cross-over voltage | V_{CRS} | 1.3 | - | 2.0 | V | |
| | Rise time | t_{LR} | 75 | - | 300 | ns | |
| | Fall time | t_{LF} | 75 | - | 300 | ns | |
| | Rise/fall time ratio | t_{LR} / t_{LF} | 80 | - | 125 | % | t_{LR} / t_{LF} |
| Pull-up, Pull-down characteristics | USBHS_DP and USBHS_DM pull-down resistors (host) | R_{pd} | 14.25 | - | 24.80 | kΩ | |

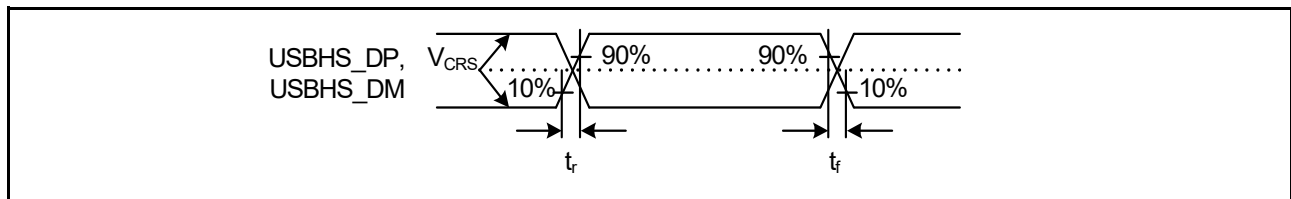


Figure 2.76 USBHS_DP and USBHS_DM output timing in low-speed mode

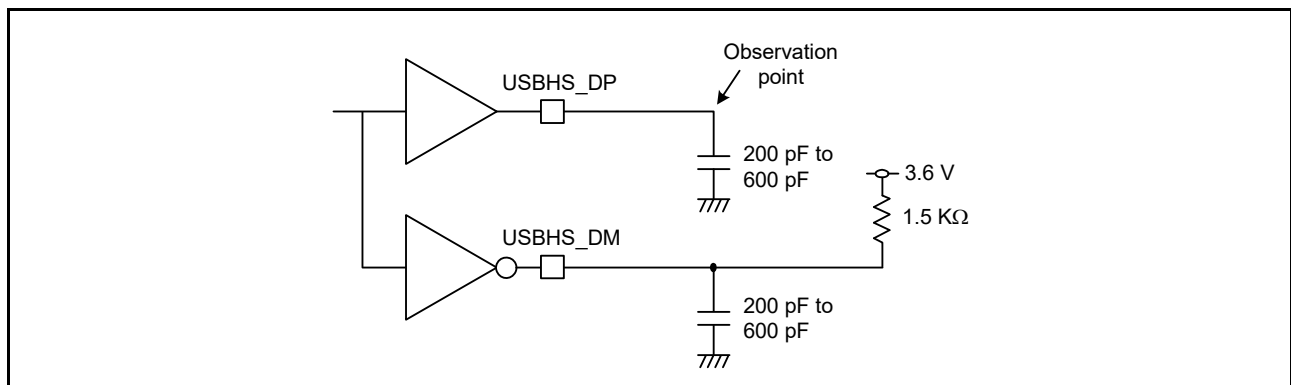


Figure 2.77 Test circuit in low-speed mode

Table 2.35 USBHS full-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | |
|------------------------|---------------------------------------------|-------------------|-------|-----|--------|-----------------|------------------------------------------------------------|
| Input characteristics | Input high voltage | V_{IH} | 2.0 | - | - | V | - |
| | Input low voltage | V_{IL} | - | - | 0.8 | V | - |
| | Differential input sensitivity | V_{DI} | 0.2 | - | - | V | USBHS_DP - USBHS_DM |
| | Differential common-mode range | V_{CM} | 0.8 | - | 2.5 | V | - |
| Output characteristics | Output high voltage | V_{OH} | 2.8 | - | 3.6 | V | $I_{OH} = -200 \mu A$ |
| | Output low voltage | V_{OL} | 0.0 | - | 0.3 | V | $I_{OL} = 2 \text{ mA}$ |
| | Cross-over voltage | V_{CRS} | 1.3 | - | 2.0 | V | - |
| | Rise time | t_{LR} | 4 | - | 20 | ns | - |
| | Fall time | t_{LF} | 4 | - | 20 | ns | - |
| | Rise/fall time ratio | t_{LR} / t_{LF} | 90 | - | 111.11 | % | t_{FR} / t_{FF} |
| | Output resistance | Z_{DRV} | 40.5 | - | 49.5 | Ω | Rs Not used (PHYSET.REPSEL[1:0] = 01b and PHYSET.HSEB = 0) |
| DC characteristics | USBHS_DM pull-up resistor (device) | R_{pu} | 0.900 | - | 1.575 | kΩ | During idle state |
| | | | 1.425 | - | 3.090 | kΩ | During transmission and reception |
| | USBHS_DP/USBHS_DM pull-down resistor (host) | R_{pd} | 14.25 | - | 24.80 | kΩ | - |

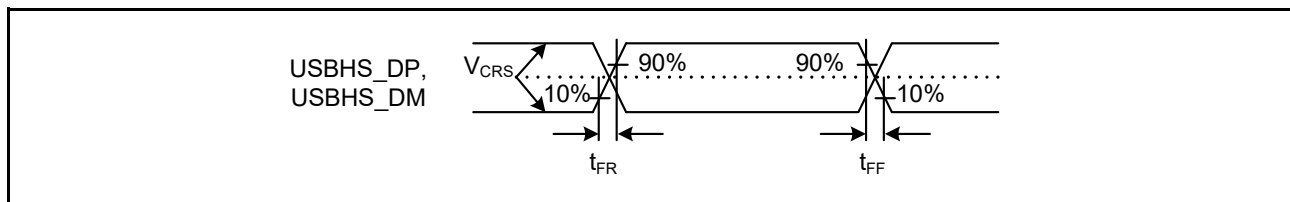
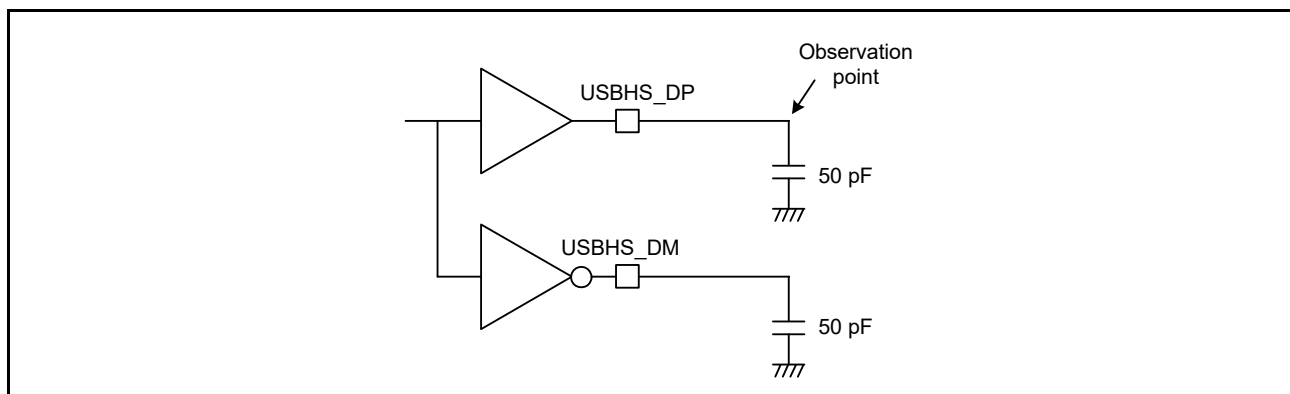
**Figure 2.78 USBHS_DP and USBHS_DM output timing in full-speed mode****Figure 2.79 Test circuit in full-speed mode**

Table 2.36 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | |
|------------------------|-------------------------------------|--------------|-------|-----|------|-----------------|-------------|
| Input characteristics | Squelch detect sensitivity | V_{HSSQ} | 100 | - | 150 | mV | Figure 2.80 |
| | Disconnect detect sensitivity | V_{HSDSC} | 525 | - | 625 | mV | Figure 2.81 |
| | Common-mode voltage | V_{HSCM} | -50 | - | 500 | mV | - |
| Output characteristics | Idle state | V_{HSOI} | -10.0 | - | 10 | mV | - |
| | Output high voltage | V_{HSOH} | 360 | - | 440 | mV | |
| | Output low voltage | V_{HSOL} | -10.0 | - | 10 | mV | |
| | Chirp J output voltage (difference) | V_{CHIRPJ} | 700 | - | 1100 | mV | |
| | Chirp K output voltage (difference) | V_{CHIRPK} | -900 | - | -500 | mV | |
| AC characteristics | Rise time | t_{HSR} | 500 | - | - | ps | Figure 2.82 |
| | Fall time | t_{HSF} | 500 | - | - | ps | |
| | Output resistance | Z_{HSDRV} | 40.5 | - | 49.5 | Ω | - |

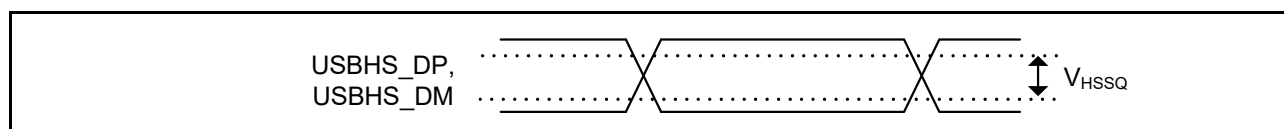


Figure 2.80 USBHS_DP and USBHS_DM squelch detect sensitivity in high-speed mode

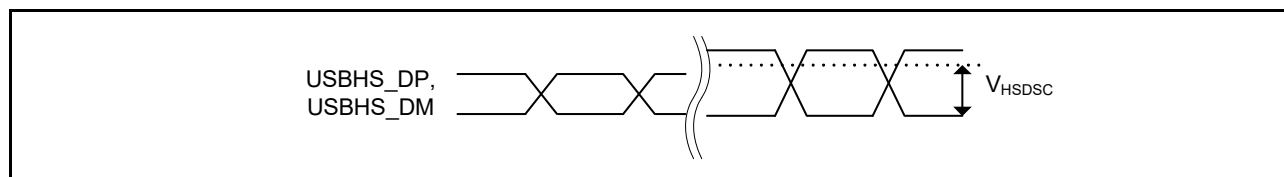


Figure 2.81 USBHS_DP and USBHS_DM disconnect detect sensitivity in high-speed mode

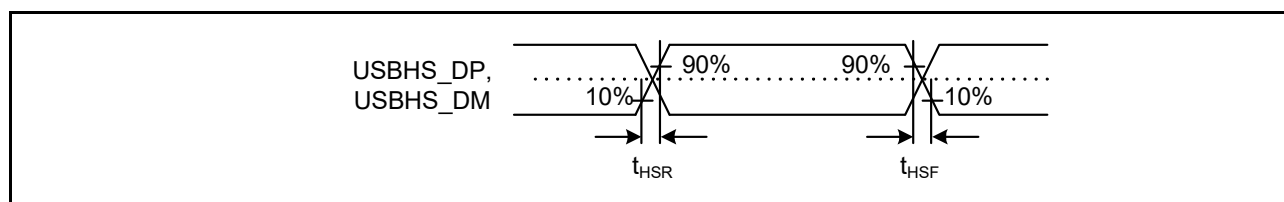


Figure 2.82 USBHS_DP and USBHS_DM output timing in high-speed mode

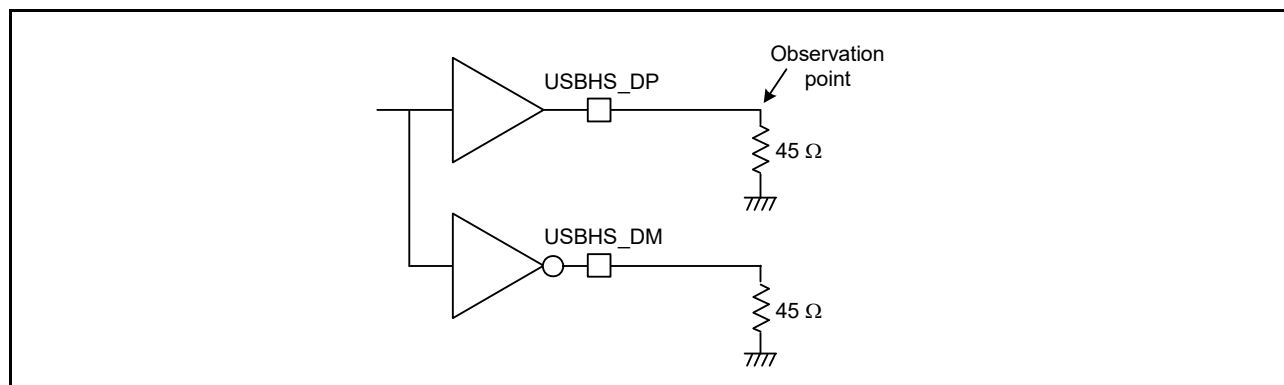


Figure 2.83 Test circuit in high-speed mode

Table 2.37 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

| Item | Symbol | Min | Max | Unit | Test conditions | |
|--------------------------------|------------------------|----------------|------|------|-----------------|-------------------------|
| Battery Charging Specification | D+ sink current | I_{DP_SINK} | 25 | 175 | μA | - |
| | D- sink current | I_{DM_SINK} | 25 | 175 | μA | - |
| | DCD source current | I_{DP_SRC} | 7 | 13 | μA | - |
| | Data detection voltage | V_{DAT_REF} | 0.25 | 0.4 | V | - |
| | D+ source voltage | V_{DP_SRC} | 0.5 | 0.7 | V | Output current = 250 μA |
| | D- source voltage | V_{DM_SRC} | 0.5 | 0.7 | V | Output current = 250 μA |

2.4.2 USBFS Timing

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---------------------------------------|----------------------------------------------------------------|-------------------|-------|-----|-------|-----------------|-------------------------|
| Input characteristics | Input high voltage | V_{IH} | 2.0 | - | - | V | - |
| | Input low voltage | V_{IL} | - | - | 0.8 | V | - |
| | Differential input sensitivity | V_{DI} | 0.2 | - | - | V | USB_DP - USB_DM |
| | Differential common-mode range | V_{CM} | 0.8 | - | 2.5 | V | - |
| Output characteristics | Output high voltage | V_{OH} | 2.8 | - | 3.6 | V | $I_{OH} = -200 \mu A$ |
| | Output low voltage | V_{OL} | 0.0 | - | 0.3 | V | $I_{OL} = 2 \text{ mA}$ |
| | Cross-over voltage | V_{CRS} | 1.3 | - | 2.0 | V | Figure 2.84 |
| | Rise time | t_{LR} | 75 | - | 300 | ns | |
| | Fall time | t_{LF} | 75 | - | 300 | ns | |
| | Rise/fall time ratio | t_{LR} / t_{LF} | 80 | - | 125 | % | t_{LR} / t_{LF} |
| Pull-up and pull-down characteristics | USB_DP and USB_DM pull-down resistance in host controller mode | R_{pd} | 14.25 | - | 24.80 | kΩ | - |

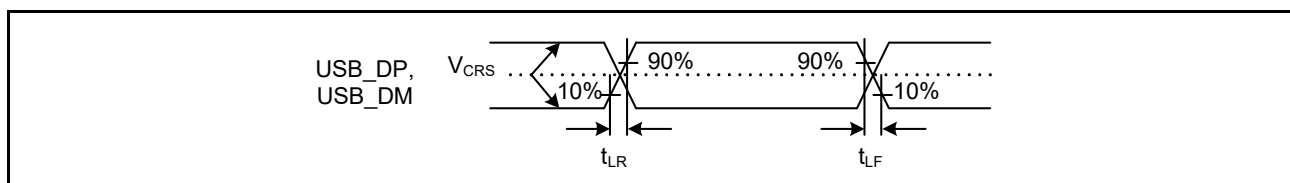
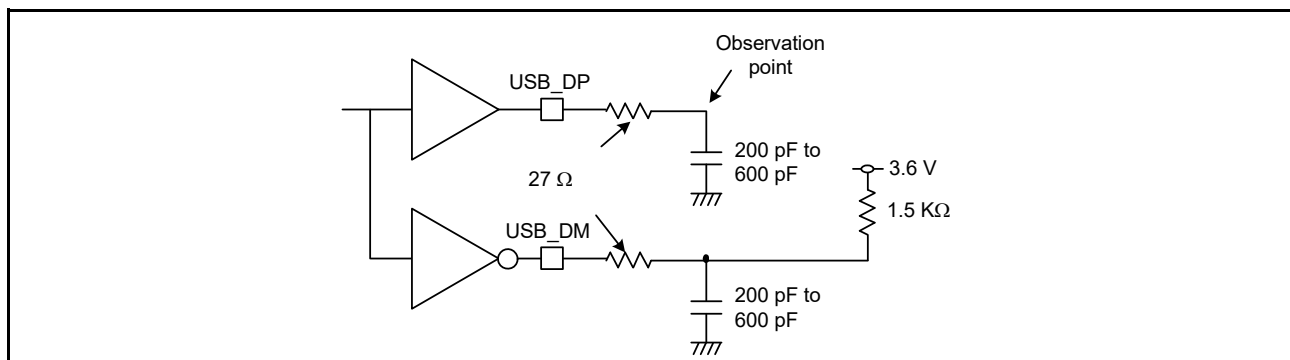
**Figure 2.84 USB_DP and USB_DM output timing in low-speed mode****Figure 2.85 Test circuit in low-speed mode**

Table 2.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, $2.7 \leq VREFH0/VREFH \leq AVCC0$, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---------------------------------------|----------------------------------------------------------------|-------------------|-------|-----|--------|-----------------|-----------------------------------|
| Input characteristics | Input high voltage | V_{IH} | 2.0 | - | - | V | - |
| | Input low voltage | V_{IL} | - | - | 0.8 | V | - |
| | Differential input sensitivity | V_{DI} | 0.2 | - | - | V | USB_DP - USB_DM |
| | Differential common-mode range | V_{CM} | 0.8 | - | 2.5 | V | - |
| Output characteristics | Output high voltage | V_{OH} | 2.8 | - | 3.6 | V | $I_{OH} = -200 \mu A$ |
| | Output low voltage | V_{OL} | 0.0 | - | 0.3 | V | $I_{OL} = 2 \text{ mA}$ |
| | Cross-over voltage | V_{CRS} | 1.3 | - | 2.0 | V | Figure 2.86 |
| | Rise time | t_{LR} | 4 | - | 20 | ns | |
| | Fall time | t_{LF} | 4 | - | 20 | ns | |
| | Rise/fall time ratio | t_{LR} / t_{LF} | 90 | - | 111.11 | % | t_{FR} / t_{FF} |
| | Output resistance | Z_{DRV} | 28 | - | 44 | Ω | USBFS: $R_s = 27 \Omega$ included |
| Pull-up and pull-down characteristics | DM pull-up resistance in device controller mode | R_{pu} | 0.900 | - | 1.575 | k Ω | During idle state |
| | | | 1.425 | - | 3.090 | k Ω | During transmission and reception |
| | USB_DP and USB_DM pull-down resistance in host controller mode | R_{pd} | 14.25 | - | 24.80 | k Ω | - |

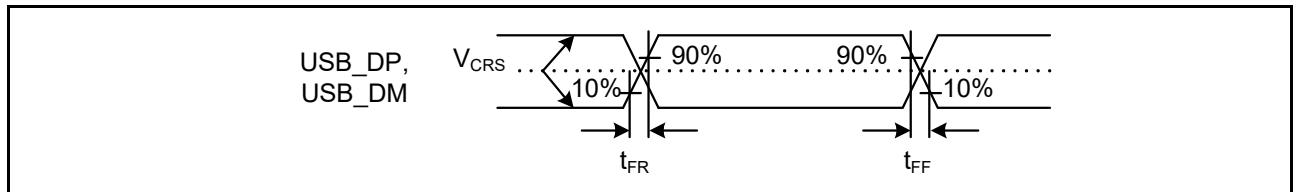


Figure 2.86 USB_DP and USB_DM output timing in full-speed mode

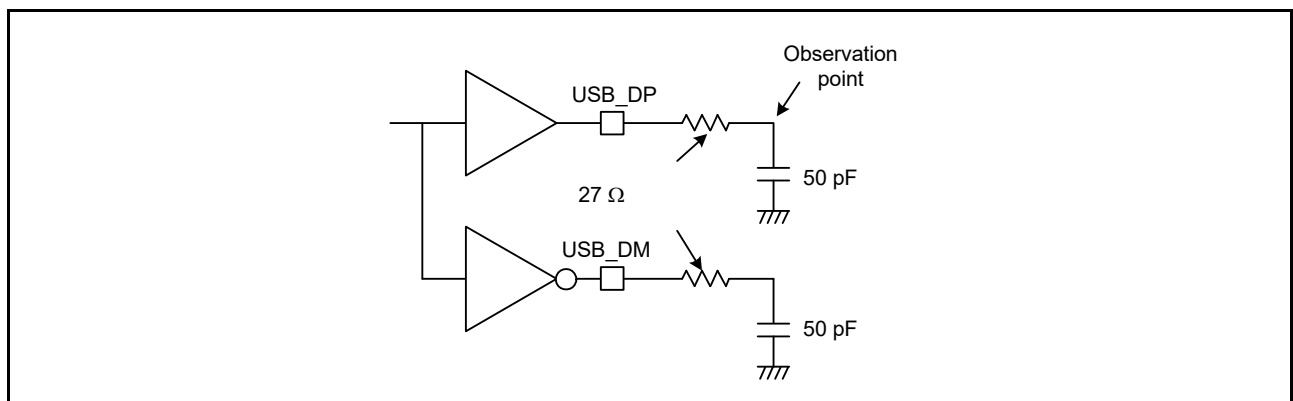


Figure 2.87 Test circuit in full-speed mode

2.5 ADC12 Characteristics

Table 2.40 A/D conversion characteristics for unit 0

Conditions: PCLKC = 1 to 60 MHz

| Item | | | Min | Typ | Max | Unit | Test conditions |
|------------------------------------------------------------------------|-----------------------------------------------------|-------------------------------------------------|---------------------|------|--------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| Frequency | | | 1 | - | 60 | MHz | - |
| Analog input capacitance | | | - | - | 30 | pF | - |
| Quantization error | | | - | ±0.5 | - | LSB | - |
| Resolution | | | - | - | 12 | Bits | - |
| Channel-dedicated sample-and-hold circuits in use (AN000 to AN002) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 1.06 (0.4 + 0.25)*2 | - | - | μs | <ul style="list-style-type: none"> Sampling of channel-dedicated sample-and-hold circuits in 24 states Sampling in 15 states |
| | Offset error | | - | ±1.5 | ±3.5 | LSB | AN000 to AN002 = 0.25 V |
| | Full-scale error | | - | ±1.5 | ±3.5 | LSB | AN000 to AN002 = VREFH0- 0.25 V |
| | Absolute accuracy | | - | ±2.5 | ±5.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±1.0 | ±2.0 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.5 | ±3.0 | LSB | - |
| | Holding characteristics of sample-and hold circuits | | - | - | 20 | μs | - |
| | Dynamic range | | 0.25 | - | VREFH 0-0.25 | V | - |
| Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.88 (0.667)*2 | - | - | μs | Sampling in 40 states |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| High-precision channels (AN003 to AN006) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.48 (0.267)*2 | - | - | μs | Sampling in 16 states |
| | | Max. = 300Ω | 0.40 (0.183)*2 | - | - | μs | Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0 |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| Normal-precision channels (AN016 to AN021) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.88 (0.667)*2 | - | - | μs | Sampling in 40 states |
| | Offset error | | - | ±1.0 | ±5.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±5.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±7.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±4.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±5.5 | LSB | - |

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.41 A/D conversion characteristics for unit 1

Conditions: PCLKC = 1 to 60 MHz

| Item | | | Min | Typ | Max | Unit | Test conditions |
|------------------------------------------------------------------------|-----------------------------------------------------|-------------------------------------------------|------------------------|------|--------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Frequency | | | 1 | - | 60 | MHz | - |
| Analog input capacitance | | | - | - | 30 | pF | - |
| Quantization error | | | - | ±0.5 | - | LSB | - |
| Resolution | | | - | - | 12 | Bits | - |
| Channel-dedicated sample-and-hold circuits in use (AN100 to AN102) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 1.06 (0.4 + 0.25)*2 | - | - | μs | <ul style="list-style-type: none"> • Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states |
| | Offset error | | - | ±1.5 | ±3.5 | LSB | AN100 to AN102 = 0.25 V |
| | Full-scale error | | - | ±1.5 | ±3.5 | LSB | AN100 to AN102 = VREFH - 0.25 V |
| | Absolute accuracy | | - | ±2.5 | ±5.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±1.0 | ±2.0 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.5 | ±3.0 | LSB | - |
| | Holding characteristics of sample-and hold circuits | | - | - | 20 | μs | - |
| Dynamic range | | | 0.25 | - | VREFH - 0.25 | V | - |
| Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.88 (0.667)*2 | - | - | μs | Sampling in 40 states |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| High-precision channels (AN103 to AN106) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.48 (0.267)*2 | - | - | μs | Sampling in 16 states |
| | | Max. = 300Ω | 0.40 (0.183)*2 | - | - | μs | Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0 |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| Normal-precision channels (AN116 to AN120) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.88 (0.667)*2 | - | - | μs | Sampling in 40 states |
| | Offset error | | - | ±1.0 | ±5.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±5.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±7.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±4.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±5.5 | LSB | - |

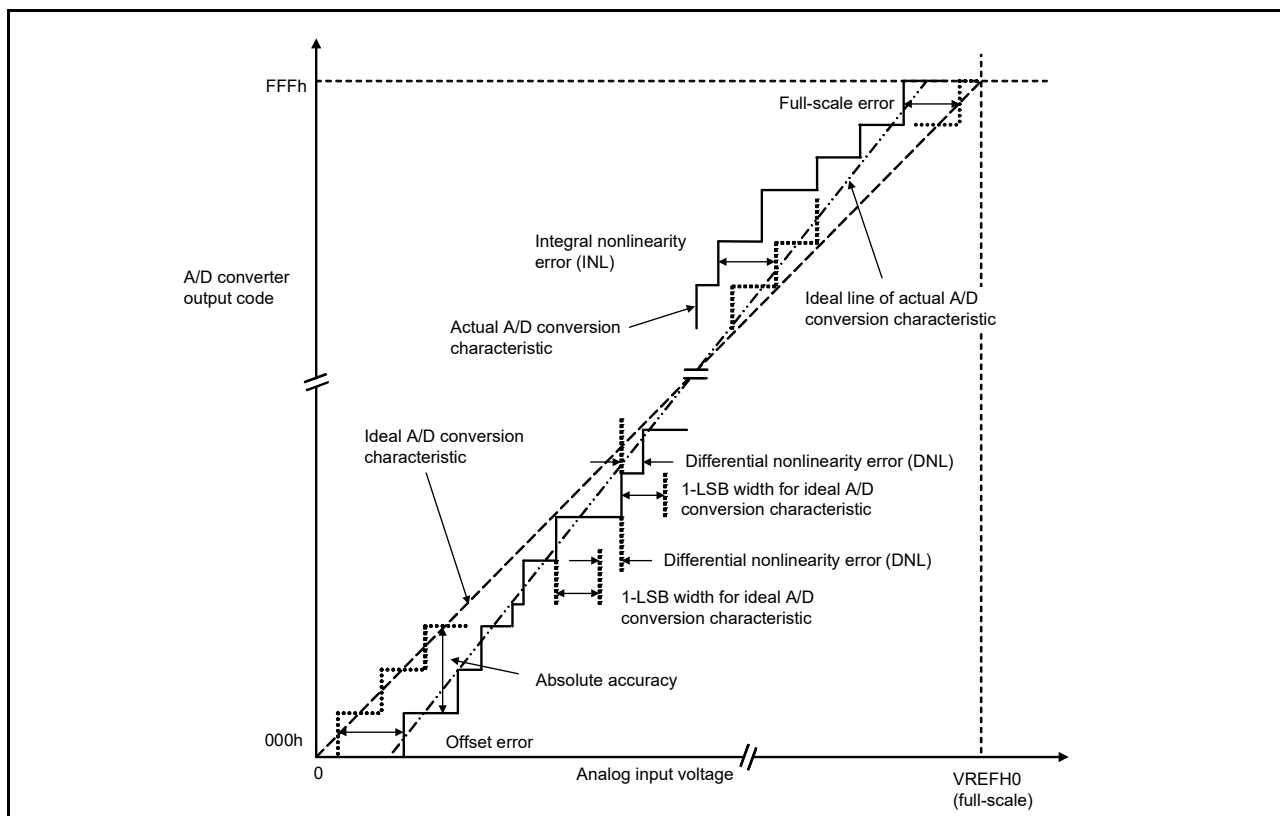
Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.42 A/D internal reference voltage characteristics

| Item | Min | Typ | Max | Unit | Test conditions |
|--------------------------------|------|------|------|---------------|-----------------|
| A/D internal reference voltage | 1.20 | 1.25 | 1.30 | V | - |
| Sampling time | 4.15 | - | - | μs | - |

**Figure 2.88 Illustration of ADC12 characteristic terms****Absolute accuracy**

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage $V_{REFH0} = 3.072\text{ V}$, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of $\pm 5\text{ LSB}$ means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics

Table 2.43 D/A conversion characteristics

| Item | Min | Typ | Max | Unit | Test conditions |
|--------------------------|-----|------|-------------|------|-----------------------|
| Resolution | - | - | 12 | Bits | - |
| Without output amplifier | | | | | |
| Absolute accuracy | - | - | ±24 | LSB | Resistive load 2 MΩ |
| INL | - | ±2.0 | ±8.0 | LSB | Resistive load 2 MΩ |
| DNL | | ±1.0 | ±2.0 | LSB | - |
| Output impedance | - | 7.5 | - | kΩ | - |
| Conversion time | - | - | 3.0 | μs | Capacitive load 20 pF |
| Output voltage range | 0 | - | VREFH | V | - |
| With output amplifier | | | | | |
| INL | - | ±2.0 | ±4.0 | LSB | - |
| DNL | - | ±1.0 | ±2.0 | LSB | - |
| Conversion time | - | - | 4.0 | μs | - |
| Resistive load | 5 | - | - | kΩ | - |
| Capacitive load | - | - | 50 | pF | - |
| Output voltage range | 0.2 | - | VREFH - 0.2 | V | - |

2.7 TSN Characteristics

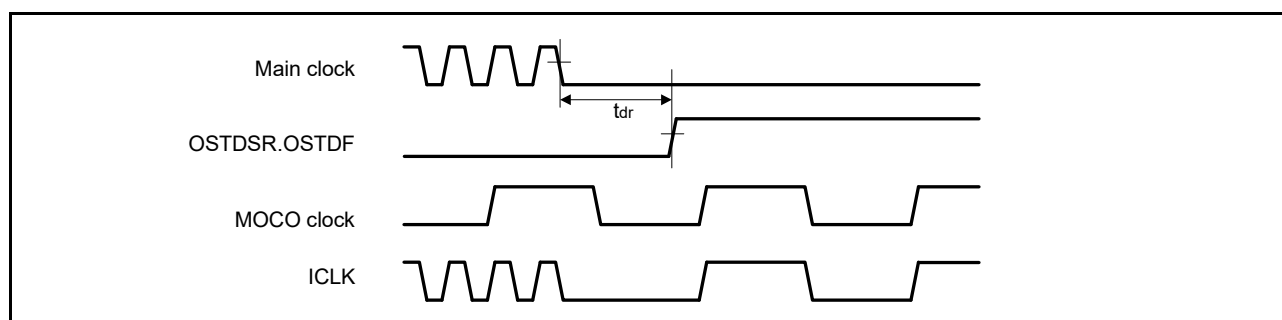
Table 2.44 TSN characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|-------------------------------|--------------------|------|------|-----|-------|-----------------|
| Relative accuracy | - | - | ±1.0 | - | °C | - |
| Temperature slope | - | - | 4.1 | - | mV/°C | - |
| Output voltage (at 25°C) | - | - | 1.24 | - | V | - |
| Temperature sensor start time | t _{START} | - | - | 30 | μs | - |
| Sampling time | - | 4.15 | - | - | μs | - |

2.8 OSC Stop Detect Characteristics

Table 2.45 Oscillation stop detection circuit characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------|-----------------|-----|-----|-----|------|-----------------|
| Detection time | t _{dr} | - | - | 1 | ms | Figure 2.89 |


Figure 2.89 Oscillation stop detection timing

2.9 POR and LVD Characteristics

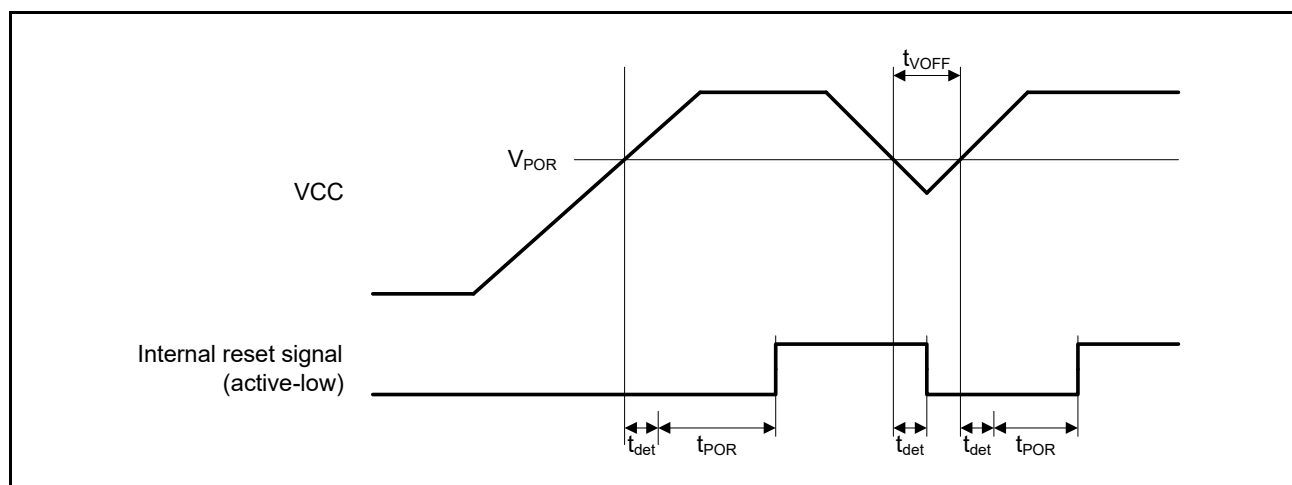
Table 2.46 Power-on reset circuit and voltage detection circuit characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | | |
|---------------------------------------------------------|----------------------------------|---------------------------------|-----------|------|---------|----------------------------|-------------|-------------|
| Voltage detection level | Power-on reset (POR) | Module-stop function disabled*1 | V_{POR} | 2.5 | 2.6 | 2.7 | V | Figure 2.90 |
| | | Module-stop function enabled*2 | | 2.0 | 2.35 | 2.7 | | |
| | Voltage detection circuit (LVD0) | V_{det0_1} | 2.84 | 2.94 | 3.04 | | Figure 2.91 | |
| | | V_{det0_2} | 2.77 | 2.87 | 2.97 | | | |
| | | V_{det0_3} | 2.70 | 2.80 | 2.90 | | | |
| | Voltage detection circuit (LVD1) | V_{det1_1} | 2.89 | 2.99 | 3.09 | | Figure 2.92 | |
| | | V_{det1_2} | 2.82 | 2.92 | 3.02 | | | |
| | | V_{det1_3} | 2.75 | 2.85 | 2.95 | | | |
| | Voltage detection circuit (LVD2) | V_{det2_1} | 2.89 | 2.99 | 3.09 | | Figure 2.93 | |
| | | V_{det2_2} | 2.82 | 2.92 | 3.02 | | | |
| | | V_{det2_3} | 2.75 | 2.85 | 2.95 | | | |
| | Internal reset time | Power-on reset time | t_{POR} | - | 4.6 | - | ms | Figure 2.90 |
| LVD0 reset time | | t_{LVD0} | - | 0.70 | - | Figure 2.91 | | |
| LVD1 reset time | | t_{LVD1} | - | 0.57 | - | Figure 2.92 | | |
| LVD2 reset time | | t_{LVD2} | - | 0.57 | - | Figure 2.93 | | |
| Minimum VCC down time | t_{VOFF} | 200 | - | - | μ s | Figure 2.90, Figure 2.91 | | |
| Response delay | t_{det} | - | - | 200 | μ s | Figure 2.90 to Figure 2.93 | | |
| LVD operation stabilization time (after LVD is enabled) | $T_{d(E-A)}$ | - | - | 10 | μ s | Figure 2.92, Figure 2.93 | | |
| Hysteresis width (LVD1 and LVD2) | V_{LVH} | - | 80 | - | mV | | | |

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for POR and LVD.

Note 2. The low-power function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 3. The low-power function is enabled and DEEPCUT[1:0] = 11b.

**Figure 2.90 Power-on reset timing**

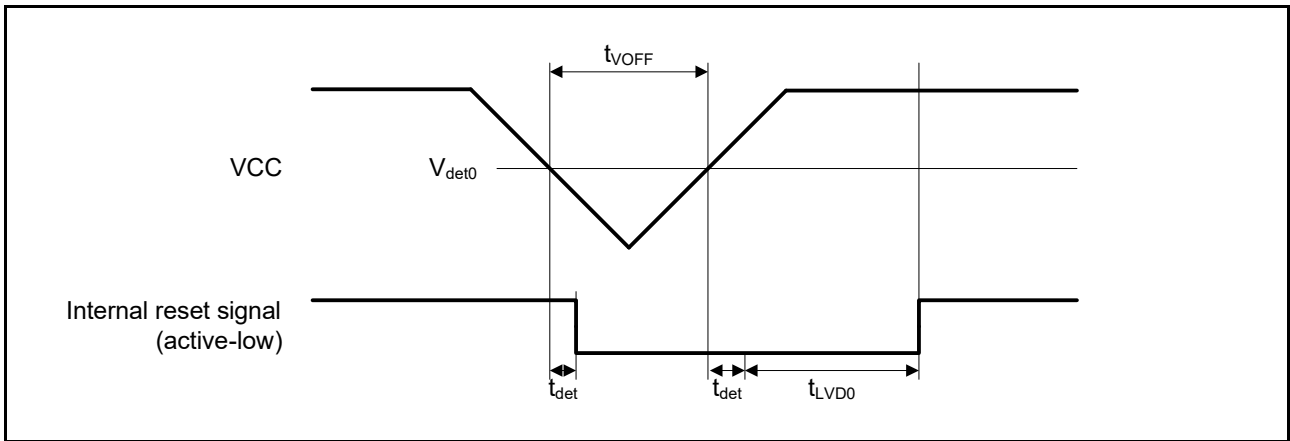


Figure 2.91 Voltage detection circuit timing (V_{det0})

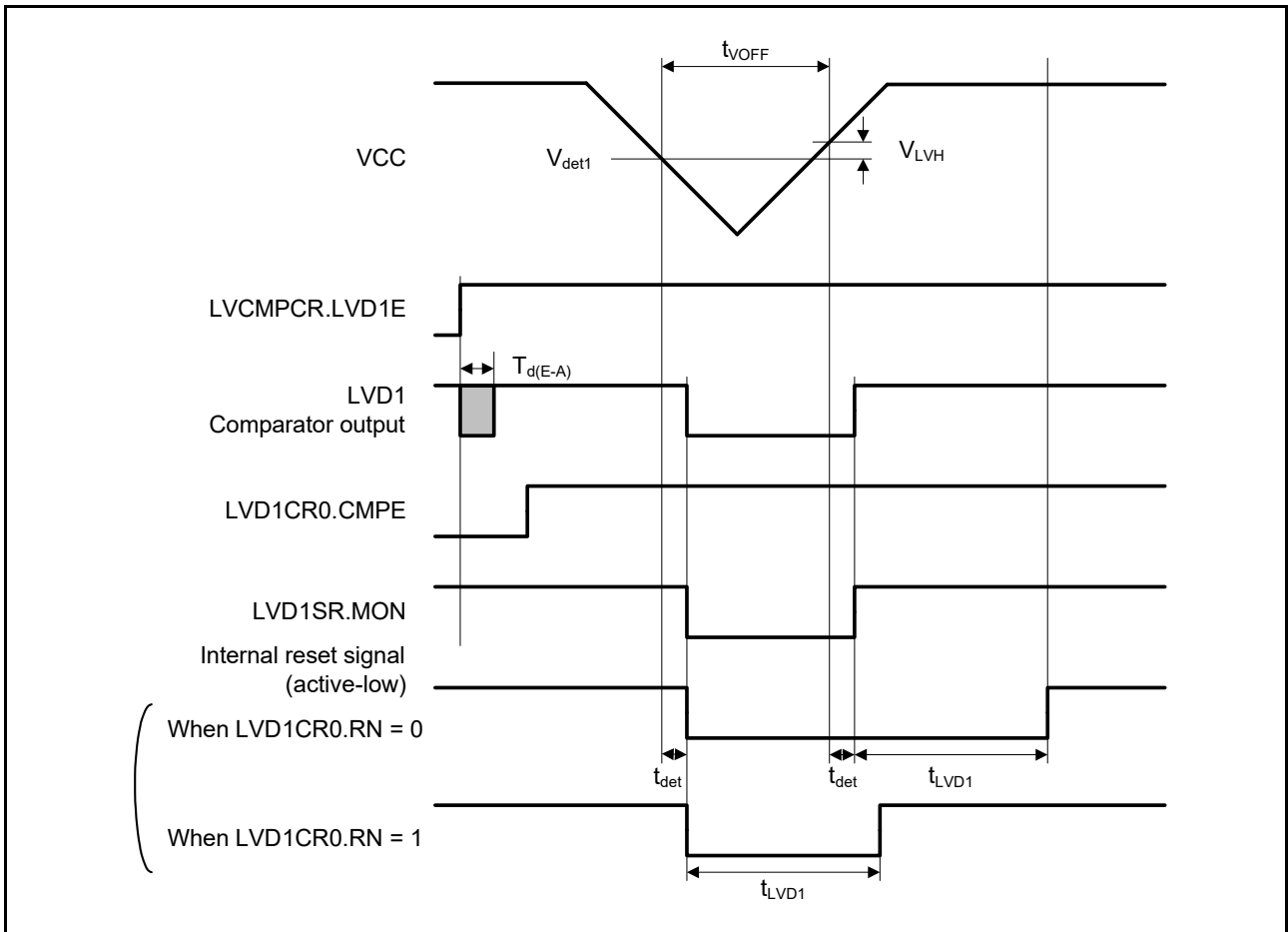


Figure 2.92 Voltage detection circuit timing (V_{det1})

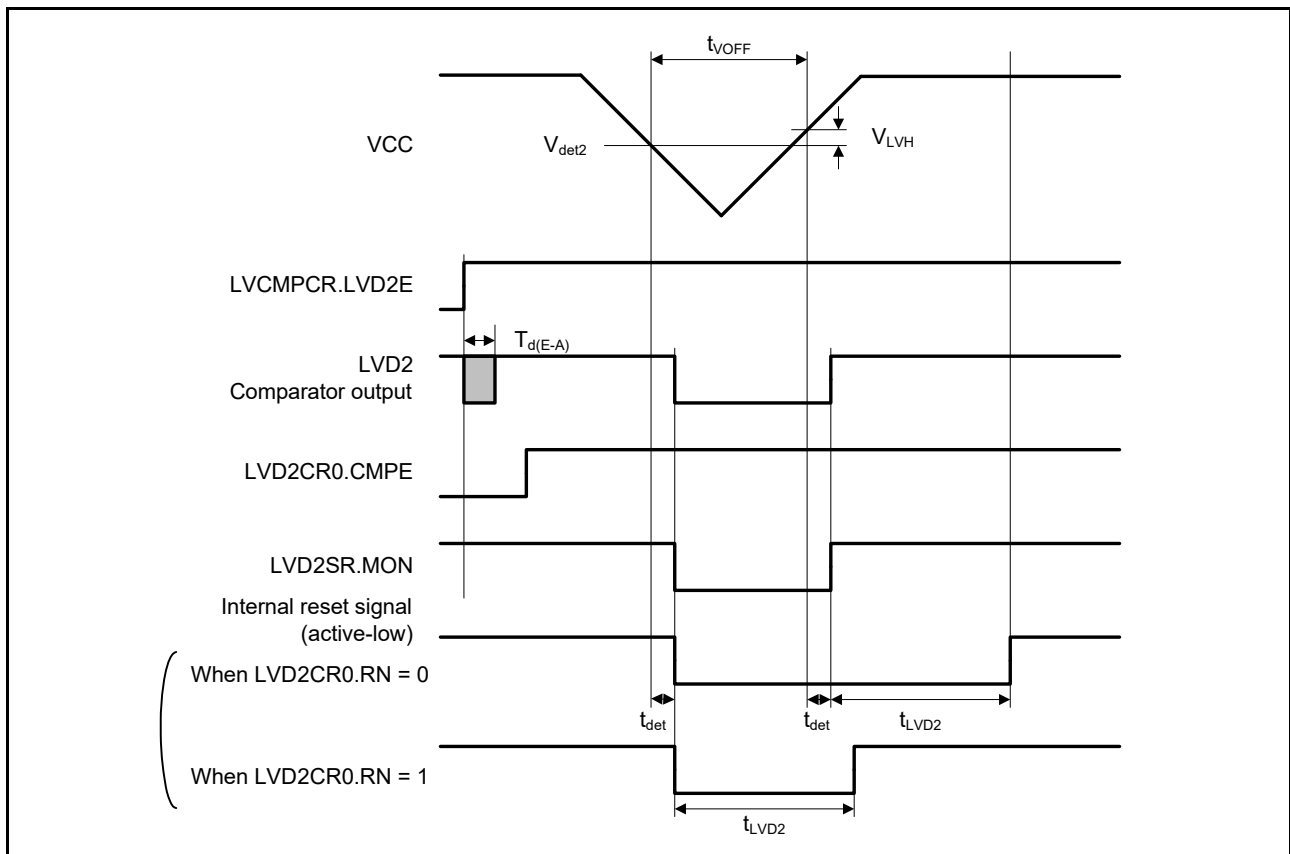


Figure 2.93 Voltage detection circuit timing (V_{det2})

2.10 VBATT Characteristics

Table 2.47 Battery backup function characteristics

Conditions: $VCC = AVCC0 = VCC_USB = 2.7$ to 3.6 V, 2.7 V $\leq VREFH0/VRFEH \leq AVCC0$, $VBATT = 2.0$ to 3.6 V

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------------------------------------------------------|----------------|------|------|------|---------|-----------------|
| Voltage level for switching to battery backup | $V_{DETBATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 2.94 |
| Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop | V_{BATTSW} | 2.70 | - | - | V | |
| VCC-off period for starting power supply switching | $t_{VOFFBATT}$ | 200 | - | - | μ s | |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

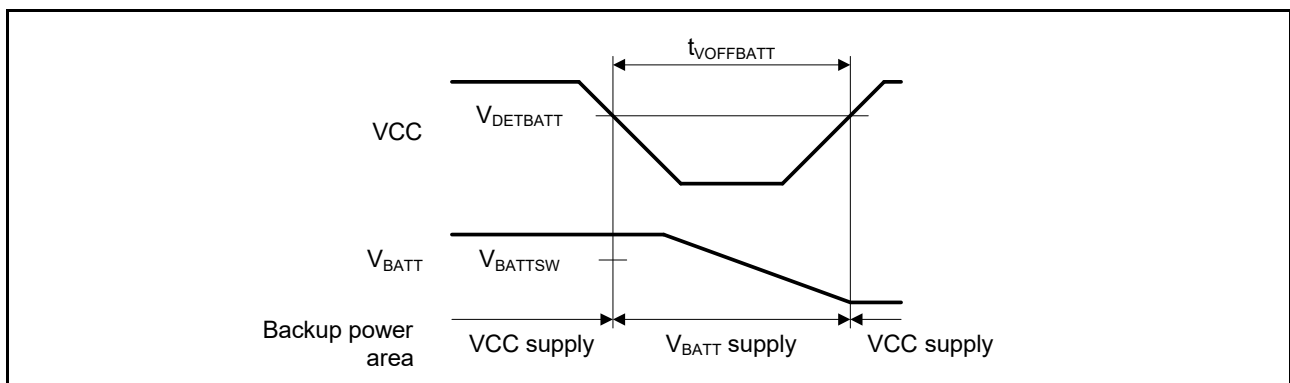


Figure 2.94 Battery backup function characteristics

2.11 CTSU Characteristics

Table 2.48 CTSU characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------------------|-----------------|-----|-----|-----|------|-----------------------------------------------|
| External capacitance connected to TSCAP pin | C_{tscap} | 9 | 10 | 11 | nF | - |
| TS pin capacitive load | C_{base} | - | - | 50 | pF | - |
| Permissible output high current | ΣI_{oH} | - | - | -40 | mA | When the mutual capacitance method is applied |

2.12 Comparator Characteristics

Table 2.49 ACPHS characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------|--------|------|------|-------|------|--------------------|
| Reference voltage range | VREF | 0 | - | AVCC0 | V | - |
| Input voltage range | VI | 0 | - | AVCC0 | V | - |
| Internal reference voltage | - | 1.20 | 1.25 | 1.30 | V | - |
| Output delay*1 | Td | - | 50 | 100 | ns | VI = VREF ± 100 mV |

Note 1. This value is the internal propagation delay.

2.13 PGA Characteristics

Table 2.50 PGA characteristics in single mode (1 of 2)

| Item | Symbol | Min | Typ | Max | Unit |
|----------------------------|----------------------|----------------------|---------------------|----------------------|------|
| PGAVSS input voltage range | PGAVSS | 0 | - | 0 | V |
| | AIN0 (G = 2.000) | $0.050 \times AVCC0$ | - | $0.45 \times AVCC0$ | V |
| | AIN1 (G = 2.500) | $0.047 \times AVCC0$ | - | $0.360 \times AVCC0$ | V |
| | AIN2 (G = 2.667) | $0.046 \times AVCC0$ | - | $0.337 \times AVCC0$ | V |
| | AIN3 (G = 2.857) | $0.046 \times AVCC0$ | - | $0.32 \times AVCC0$ | V |
| | AIN4 (G = 3.077) | $0.045 \times AVCC0$ | - | $0.292 \times AVCC0$ | V |
| | AIN5 (G = 3.333) | $0.044 \times AVCC0$ | - | $0.265 \times AVCC0$ | V |
| | AIN6 (G = 3.636) | $0.042 \times AVCC0$ | - | $0.247 \times AVCC0$ | V |
| | AIN7 (G = 4.000) | $0.040 \times AVCC0$ | - | $0.212 \times AVCC0$ | V |
| | AIN8 (G = 4.444) | $0.036 \times AVCC0$ | - | $0.191 \times AVCC0$ | V |
| | AIN9 (G = 5.000) | $0.033 \times AVCC0$ | - | $0.17 \times AVCC0$ | V |
| | AIN10 (G = 5.714) | $0.031 \times AVCC0$ | - | $0.148 \times AVCC0$ | V |
| | AIN11 (G = 6.667) | $0.029 \times AVCC0$ | - | $0.127 \times AVCC0$ | V |
| | AIN12 (G = 8.000) | $0.027 \times AVCC0$ | - | $0.09 \times AVCC0$ | V |
| | AIN13 (G = 10.000) | $0.025 \times AVCC0$ | - | $0.08 \times AVCC0$ | V |
| AIN14 (G = 13.333) | $0.023 \times AVCC0$ | - | $0.06 \times AVCC0$ | V | |

Table 2.50 PGA characteristics in single mode (2 of 2)

| Item | Symbol | Min | Typ | Max | Unit |
|---------------------|---------------------|------|-----|-----|------|
| Gain error | Gerr0 (G = 2.000) | -1.0 | - | 1.0 | % |
| | Gerr1 (G = 2.500) | -1.0 | - | 1.0 | % |
| | Gerr2 (G = 2.667) | -1.0 | - | 1.0 | % |
| | Gerr3 (G = 2.857) | -1.0 | - | 1.0 | % |
| | Gerr4 (G = 3.077) | -1.0 | - | 1.0 | % |
| | Gerr5 (G = 3.333) | -1.5 | - | 1.5 | % |
| | Gerr6 (G = 3.636) | -1.5 | - | 1.5 | % |
| | Gerr7 (G = 4.000) | -1.5 | - | 1.5 | % |
| | Gerr8 (G = 4.444) | -2.0 | - | 2.0 | % |
| | Gerr9 (G = 5.000) | -2.0 | - | 2.0 | % |
| | Gerr10 (G = 5.714) | -2.0 | - | 2.0 | % |
| | Gerr11 (G = 6.667) | -2.0 | - | 2.0 | % |
| | Gerr12 (G = 8.000) | -2.0 | - | 2.0 | % |
| | Gerr13 (G = 10.000) | -2.0 | - | 2.0 | % |
| Gerr14 (G = 13.333) | -2.0 | - | 2.0 | % | |
| Offset error | Voff | -8 | - | 8 | mV |

Table 2.51 PGA characteristics in differential mode

| Item | Symbol | Min | Typ | Max | Unit | |
|----------------------------------------------|------------|-----------|------|------|------|---|
| PGAVSS input voltage range | PGAVSS | -0.3 | - | 0.3 | V | |
| Differential input voltage range (G = 1.500) | AIN-PGAVSS | -0.5 | - | 0.5 | V | |
| Input voltage range (G = 2.333) | | -0.4 | - | 0.4 | V | |
| Input voltage range (G = 4.000) | | -0.2 | - | 0.2 | V | |
| Input voltage range (G = 5.667) | | -0.15 | - | 0.15 | V | |
| Gain error | Gerr | G = 1.500 | -2.5 | - | 2.5 | % |
| | | G = 2.333 | -2 | - | 2 | |
| | | G = 4.000 | -1 | - | 1 | |
| | | G = 5.667 | -1 | - | 1 | |

2.14 Flash Memory Characteristics

2.14.1 Code Flash Memory Characteristics

Table 2.52 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

| Item | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | |
|----------------------------------------------|----------|--------------|-----|-----|------------------------|-----|-----|------|----|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time $N_{PEC} \leq 100$ times | 256-byte | t_{P256} | - | 0.9 | 13.2 | - | 0.4 | 6 | ms |
| | 8-KB | t_{P8K} | - | 29 | 176 | - | 13 | 80 | ms |
| | 32-KB | t_{P32K} | - | 116 | 704 | - | 52 | 320 | ms |
| Programming time $N_{PEC} > 100$ times | 256-byte | t_{P256} | - | 1.1 | 15.8 | - | 0.5 | 7.2 | ms |
| | 8-KB | t_{P8K} | - | 35 | 212 | - | 16 | 96 | ms |
| | 32-KB | t_{P32K} | - | 140 | 848 | - | 64 | 384 | ms |
| Erasure time $N_{PEC} \leq 100$ times | 8-KB | t_{E8K} | - | 71 | 216 | - | 39 | 120 | ms |
| | 32-KB | t_{E32K} | - | 254 | 864 | - | 141 | 480 | ms |

Table 2.52 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

| Item | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | |
|--------------------------------------------------------------|--------------------|-------------------|-----|-----|------------------------|--------|-----|------|-------|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Erasure time N _{PEC} > 100 times | 8-KB | t _{E8K} | - | 85 | 260 | - | 47 | 144 | ms |
| | 32-KB | t _{E32K} | - | 304 | 1040 | - | 169 | 576 | ms |
| Reprogramming/erase cycle*1 | N _{PEC} | 1000*2 | - | - | - | 1000*2 | - | - | Times |
| Suspend delay during programming | t _{SPD} | - | - | 264 | - | - | 120 | - | μs |
| First suspend delay during erasure in suspend priority mode | t _{SESD1} | - | - | 216 | - | - | 120 | - | μs |
| Second suspend delay during erasure in suspend priority mode | t _{SESD2} | - | - | 1.7 | - | - | 1.7 | - | ms |
| Suspend delay during erasure in erasure priority mode | t _{SEED} | - | - | 1.7 | - | - | 1.7 | - | ms |
| Forced stop command | t _{FD} | - | - | 32 | - | - | 20 | - | μs |
| Data hold time*3*4 | t _{DRP} | 20 | - | - | 20 | - | - | - | Years |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For example, when 256-byte programming is performed 32 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 3. This indicates the characteristics when reprogramming is performed within the specified range, including the minimum value.

Note 4. This result is obtained from reliability testing.

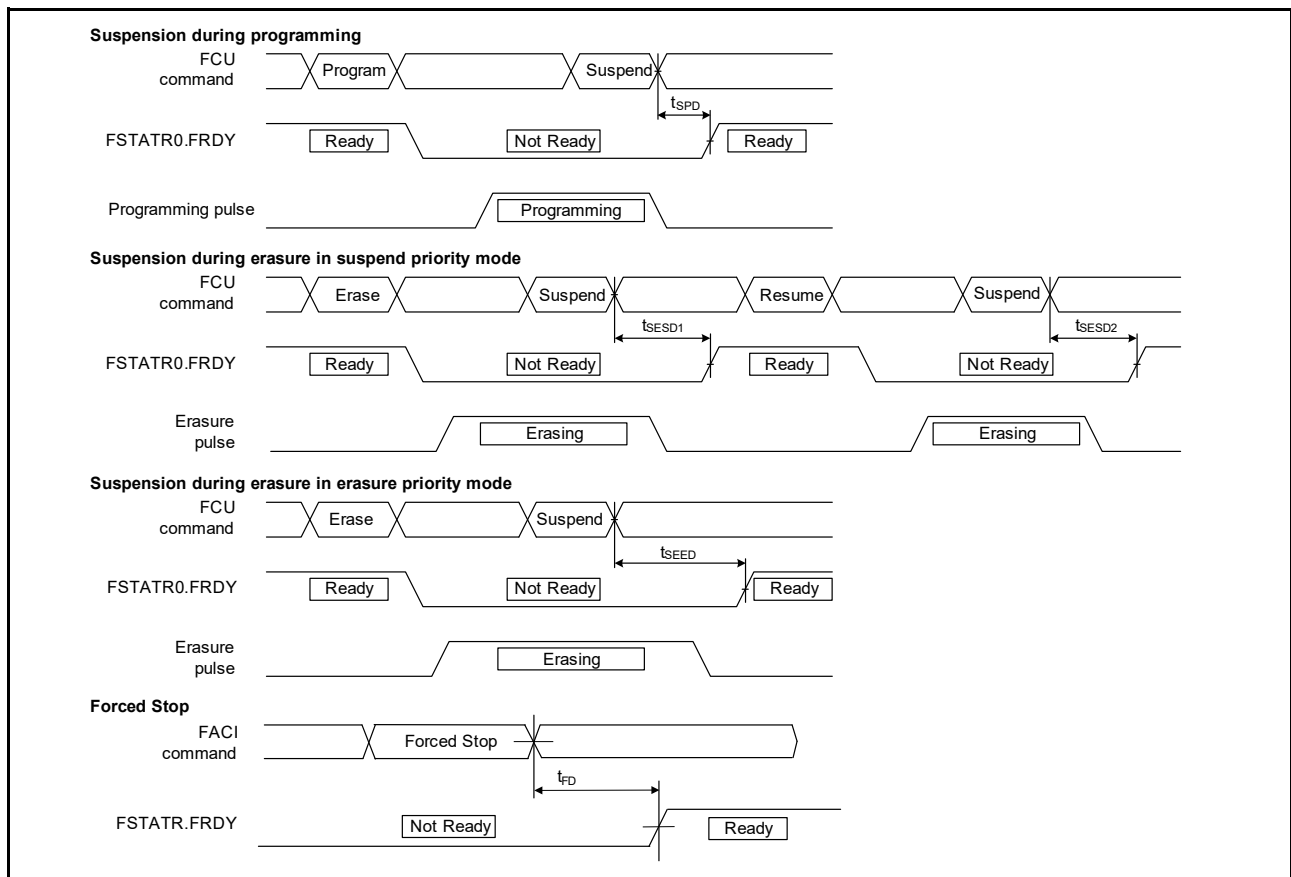


Figure 2.95 Suspend and forced stop timing for flash memory programming and erasure

2.14.2 Data Flash Memory Characteristics

Table 2.53 Data flash memory characteristics

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

| Item | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit |
|--------------------------------------------------------------|---------|---------------------|--------------|------|-----|------------------------|------|-----|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Programming time | 4-byte | t _{DP4} | - | 0.36 | 3.8 | - | 0.16 | 1.7 | ms |
| Erase time | 64-byte | t _{DE64} | - | 3.1 | 18 | - | 1.7 | 10 | ms |
| Blank check time | 4-byte | t _{DBC4} | - | - | 84 | - | - | 30 | μs |
| Reprogramming/erase cycle*1 | | N _{DPEC} | 125000*2 | - | - | 125000*2 | - | - | - |
| Suspend delay during programming | | t _{DSPD} | - | - | 264 | - | - | 120 | μs |
| First suspend delay during erasure in suspend priority mode | | t _{DSESD1} | - | - | 216 | - | - | 120 | μs |
| Second suspend delay during erasure in suspend priority mode | | t _{DSESD2} | - | - | 300 | - | - | 300 | μs |
| Suspend delay during erasing in erasure priority mode | | t _{DSEED} | - | - | 300 | - | - | 300 | μs |
| Forced stop command | | t _{FD} | - | - | 32 | - | - | 20 | μs |
| Data hold time*3 *4 | | t _{DDRP} | 20 | - | - | 20 | - | - | Year |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 3. This indicates the characteristics when reprogramming is performed within the specified range, including the minimum value.

Note 4. This result is obtained from reliability testing.

2.15 Boundary Scan

Table 2.54 Boundary scan characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|--------------------------------------|--------------|-------------|-----|-----|------|-----------------|
| TCK clock cycle time | t_{TCKcyc} | 100 | - | - | ns | Figure 2.96 |
| TCK clock high pulse width | t_{TCKH} | 45 | - | - | ns | |
| TCK clock low pulse width | t_{TCKL} | 45 | - | - | ns | |
| TCK clock rise time | t_{TCKr} | - | - | 5 | ns | |
| TCK clock fall time | t_{TCKf} | - | - | 5 | ns | |
| TMS setup time | t_{TMSS} | 20 | - | - | ns | Figure 2.97 |
| TMS hold time | t_{TMSh} | 20 | - | - | ns | |
| TDI setup time | t_{TDis} | 20 | - | - | ns | |
| TDI hold time | t_{TDIH} | 20 | - | - | ns | |
| TDO data delay | t_{TDOD} | - | - | 40 | ns | Figure 2.98 |
| Boundary scan circuit startup time*1 | T_{BSSTUP} | t_{RESWP} | - | - | - | |

Note 1. Boundary scan does not function until the power-on reset becomes negative.

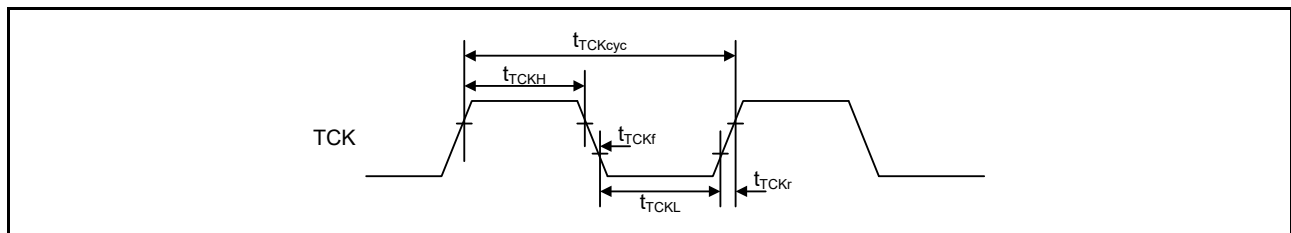


Figure 2.96 Boundary scan TCK timing

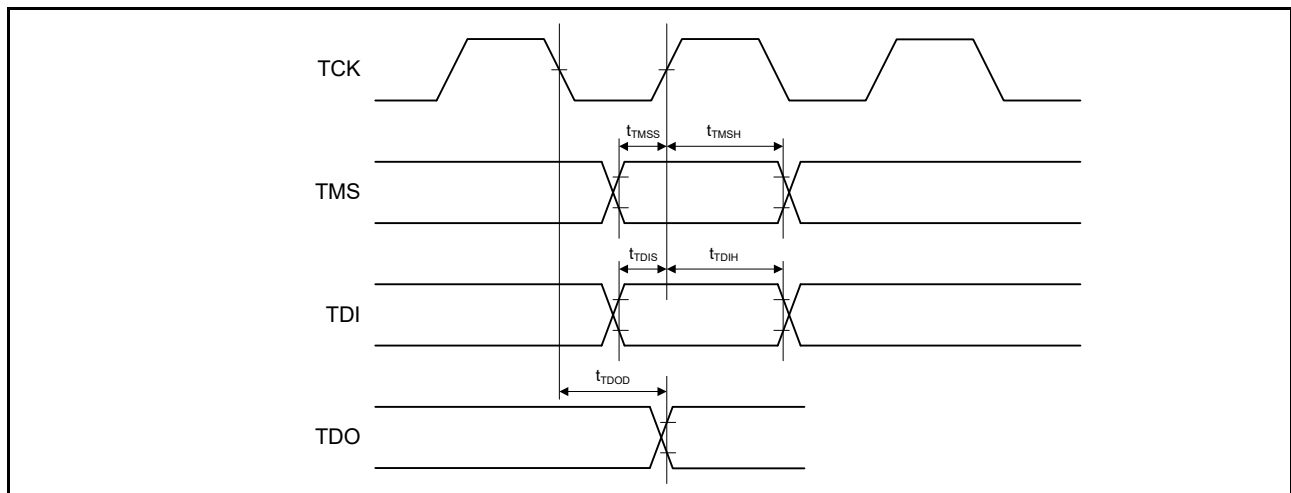


Figure 2.97 Boundary scan input/output timing

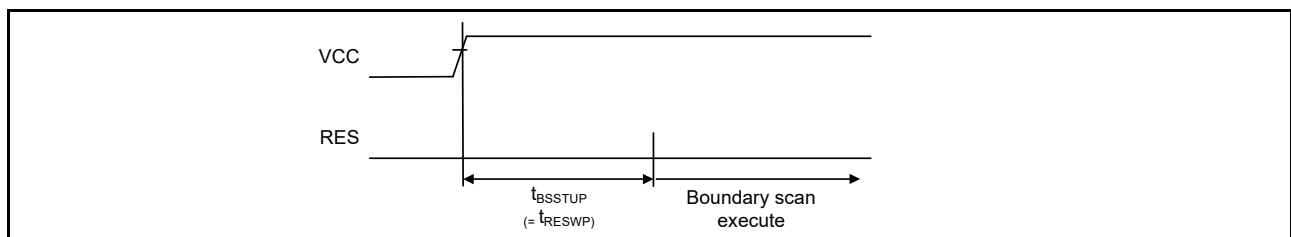


Figure 2.98 Boundary scan circuit startup timing

2.16 Joint Test Action Group (JTAG)

Table 2.55 JTAG

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------|--------------|-----|-----|-----|------|-----------------|
| TCK clock cycle time | t_{TCKcyc} | 40 | - | - | ns | Figure 2.96 |
| TCK clock high pulse width | t_{TCKH} | 15 | - | - | ns | |
| TCK clock low pulse width | t_{TCKL} | 15 | - | - | ns | |
| TCK clock rise time | t_{TCKr} | - | - | 5 | ns | |
| TCK clock fall time | t_{TCKf} | - | - | 5 | ns | |
| TMS setup time | t_{TMSS} | 8 | - | - | ns | Figure 2.97 |
| TMS hold time | t_{TMSH} | 8 | - | - | ns | |
| TDI setup time | t_{TDIS} | 8 | - | - | ns | |
| TDI hold time | t_{TDIH} | 8 | - | - | ns | |
| TDO data delay time | t_{TDOD} | - | - | 28 | ns | |

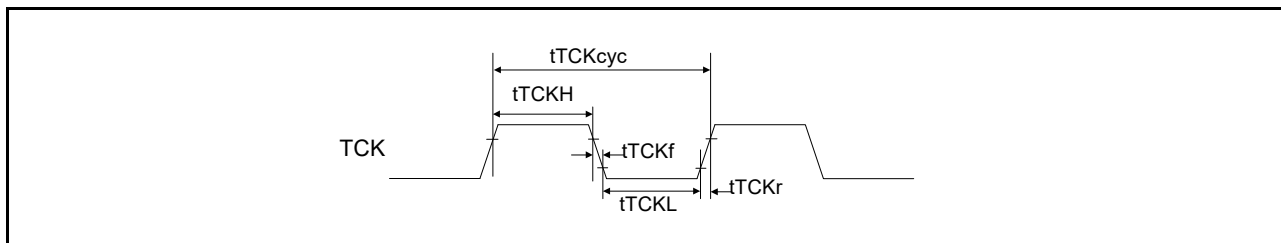


Figure 2.99 JTAG TCK timing

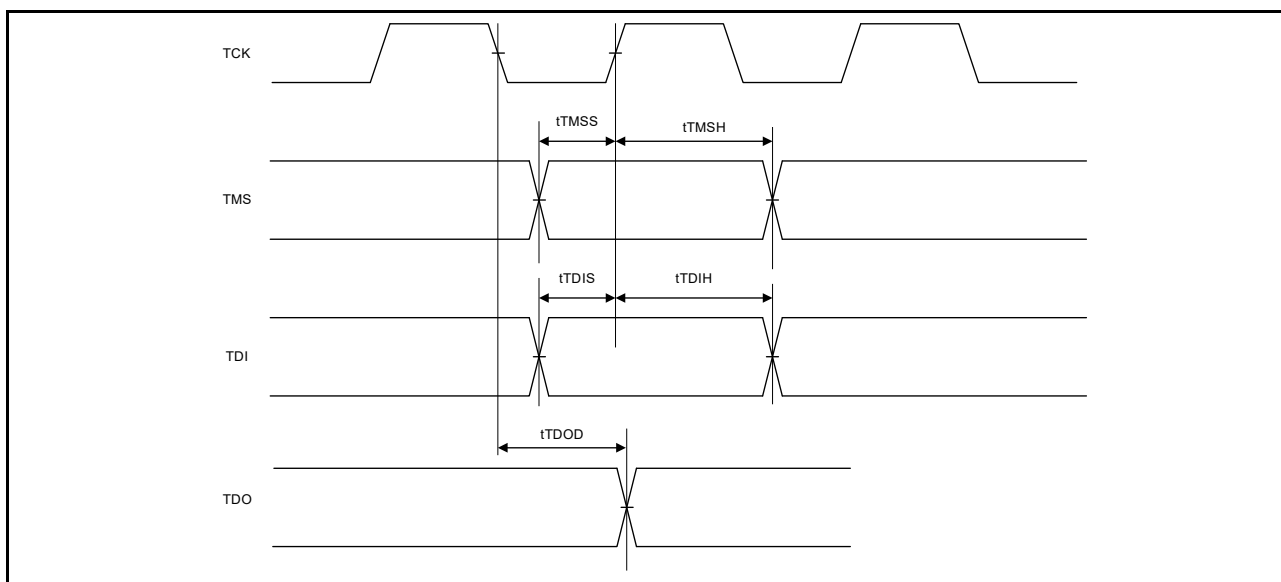


Figure 2.100 JTAG input/output timing

2.17 Serial Wire Debug (SWD)

Table 2.56 SWD

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------------|---------------|-----|-----|-----|------|-----------------|
| SWCLK clock cycle time | $t_{SWCKcyc}$ | 40 | - | - | ns | Figure 2.101 |
| SWCLK clock high pulse width | t_{SWCKH} | 15 | - | - | ns | |
| SWCLK clock low pulse width | t_{SWCKL} | 15 | - | - | ns | |
| SWCLK clock rise time | t_{SWCKr} | - | - | 5 | ns | |
| SWCLK clock fall time | t_{SWCKf} | - | - | 5 | ns | |
| SWDIO setup time | t_{SWDS} | 8 | - | - | ns | Figure 2.102 |
| SWDIO hold time | t_{SWDH} | 8 | - | - | ns | |
| SWDIO data delay time | t_{SWDD} | 2 | - | 28 | ns | |

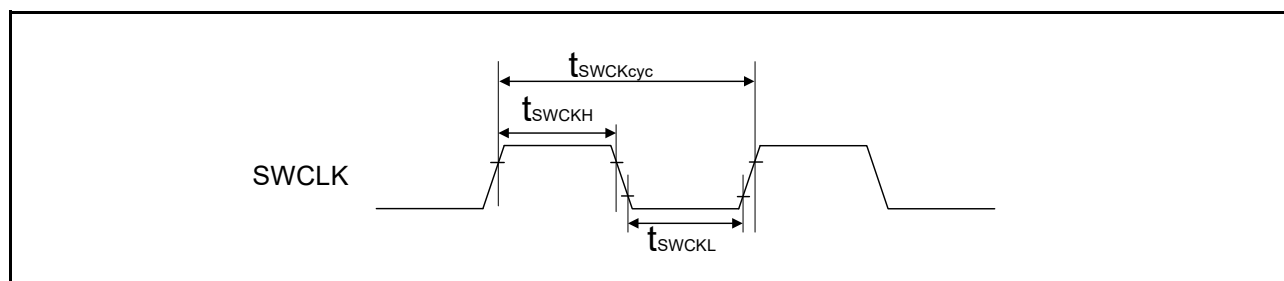


Figure 2.101 SWD SWCLK timing

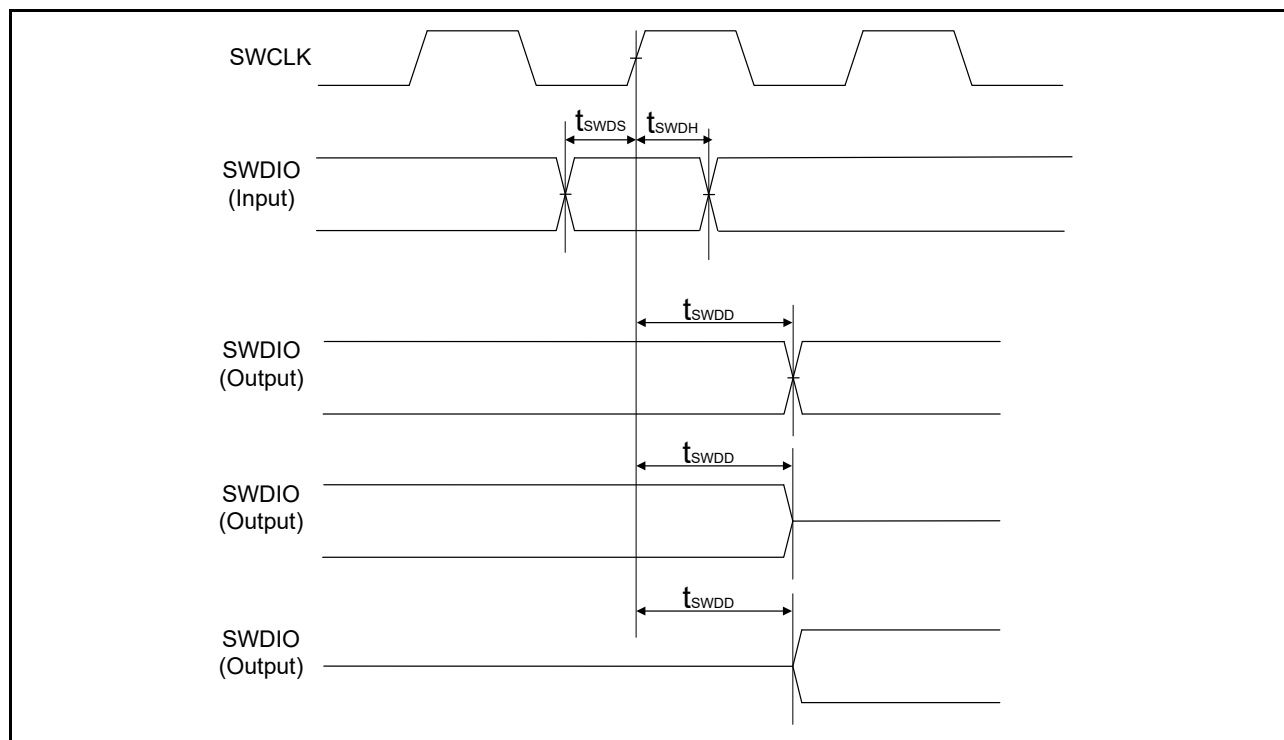


Figure 2.102 SWD input/output timing

2.18 Embedded Trace Macro Interface (ETM)

Table 2.57 ETM

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|-----------------------------|---------------|------|-----|-----|------|-----------------|
| TCLK clock cycle time | $t_{TCLKcyc}$ | 16.6 | - | - | ns | Figure 2.103 |
| TCLK clock high pulse width | t_{TCLKH} | 5.8 | - | - | ns | |
| TCLK clock low pulse width | t_{TCLKL} | 5.8 | - | - | ns | |
| TCLK clock rise time | t_{TCLKr} | - | - | 2.5 | ns | |
| TCLK clock fall time | t_{TCLKf} | - | - | 2.5 | ns | |
| TDATA0-3 output setup time | t_{TRDS} | 1.6 | - | - | ns | Figure 2.104 |
| TDATA0-3 output hold time | t_{TRDH} | 1.6 | - | - | ns | |

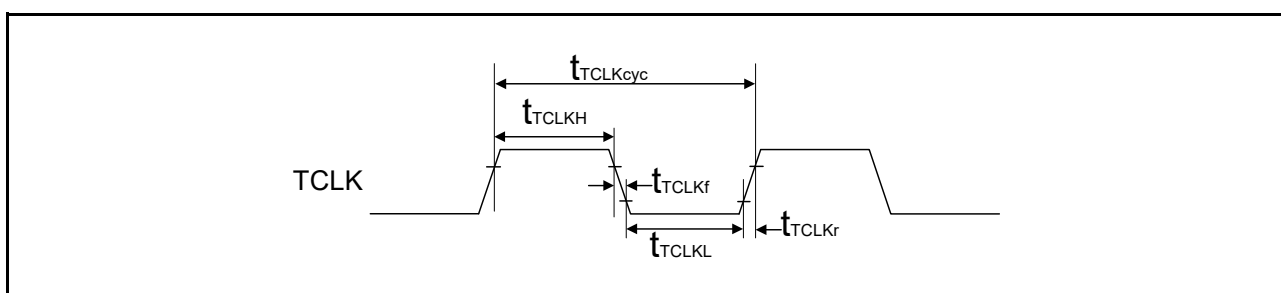


Figure 2.103 ETM TCLK timing

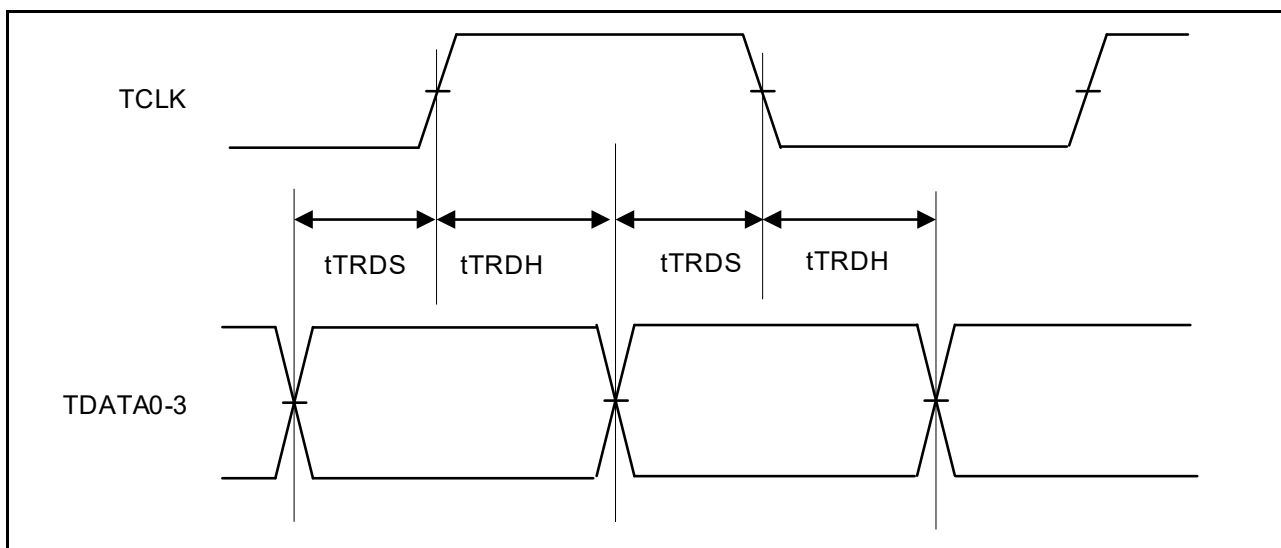


Figure 2.104 ETM output timing

Appendix 1. Package Dimensions

For information on the latest version of the package dimensions or mountings, go to “Packages” on the Renesas Electronics Corporation website.

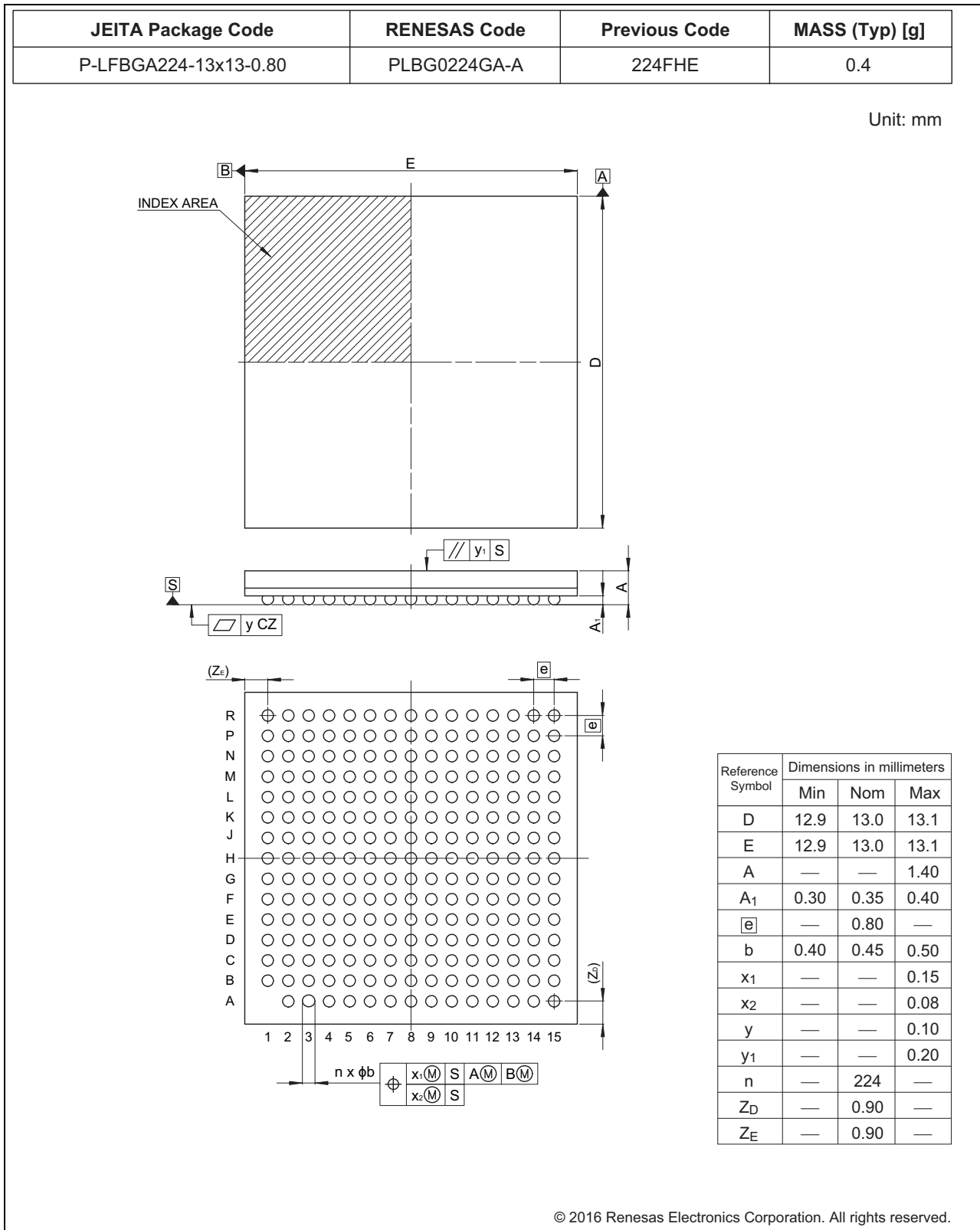


Figure 1.1 224-pin BGA

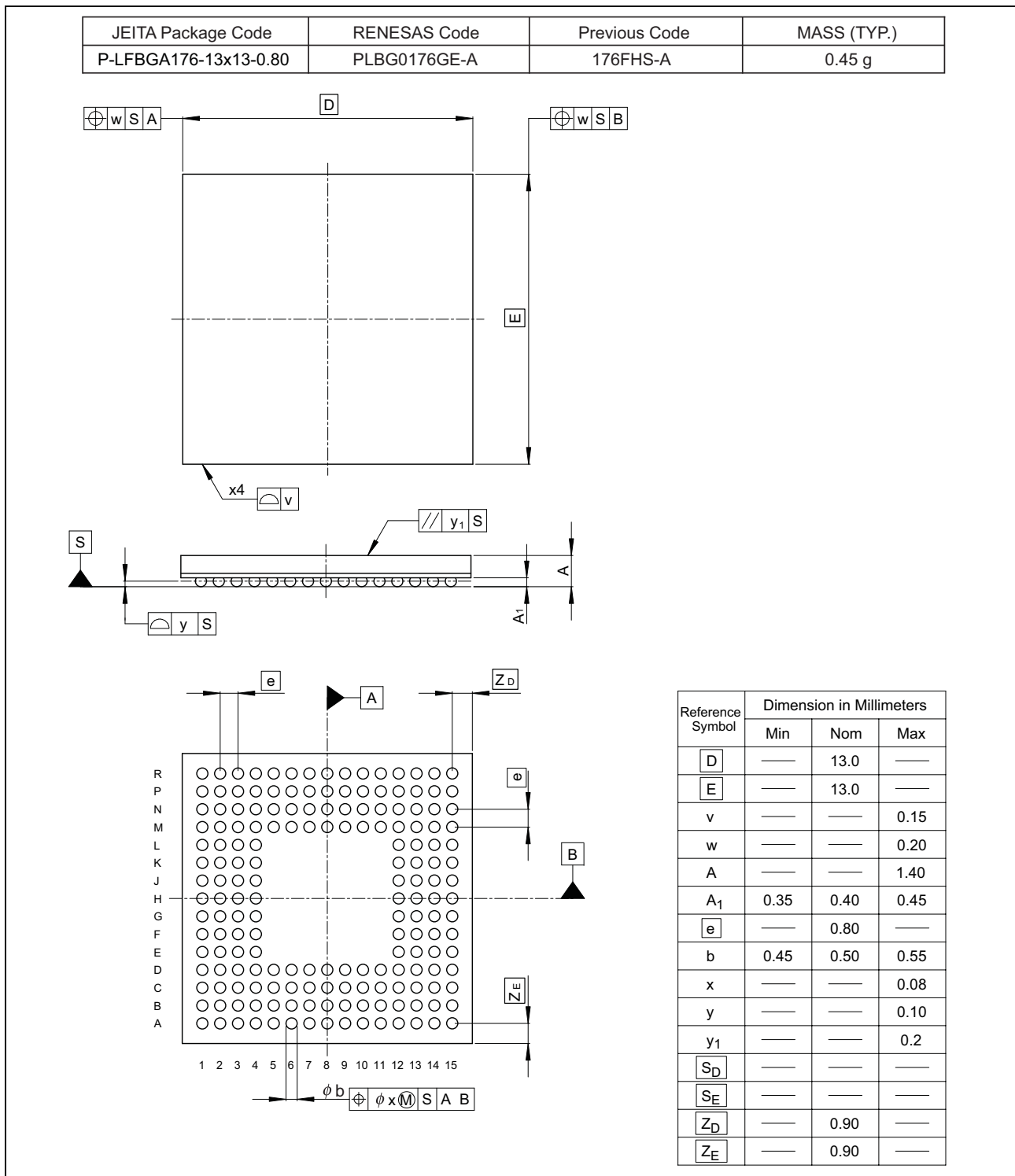


Figure 1.2 176-pin BGA

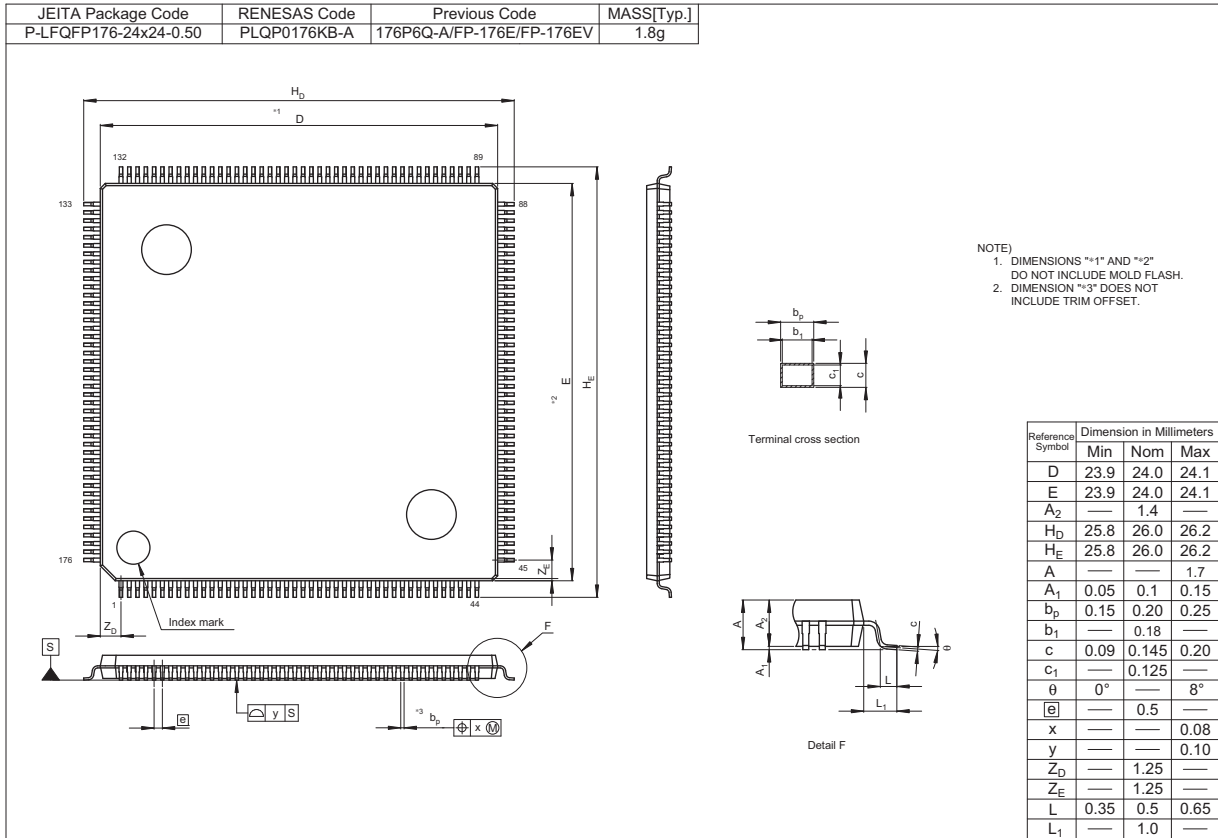


Figure 1.3 176-pin LQFP

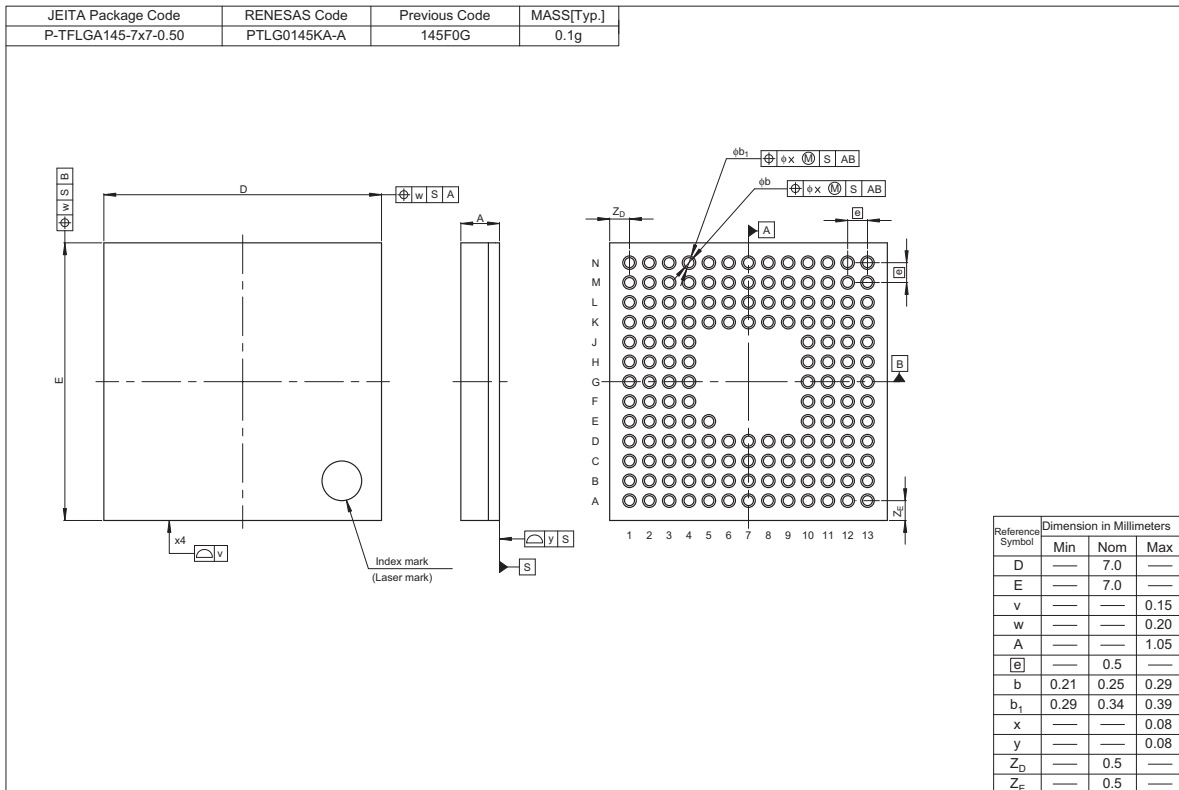


Figure 1.4 145-pin LGA

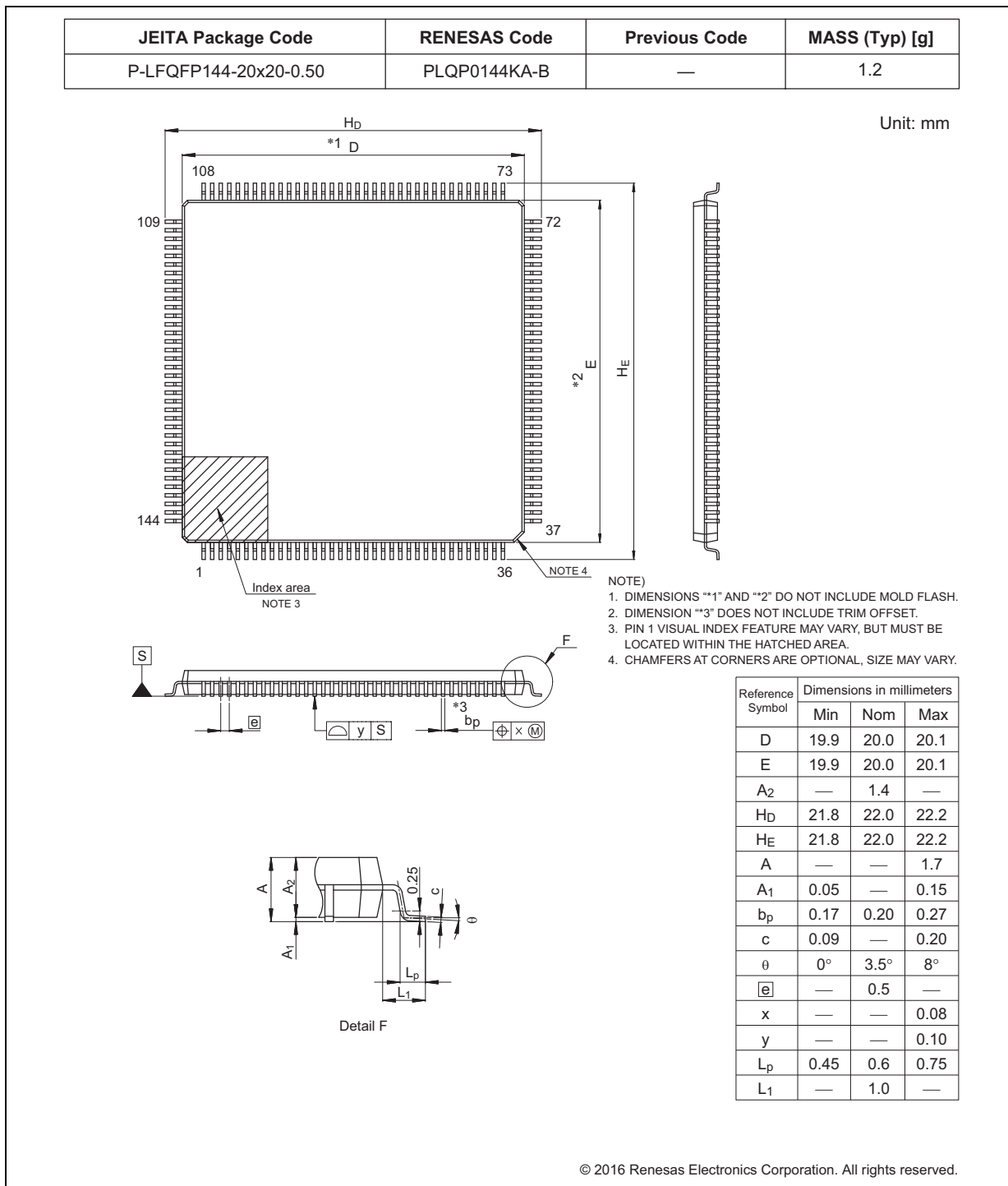
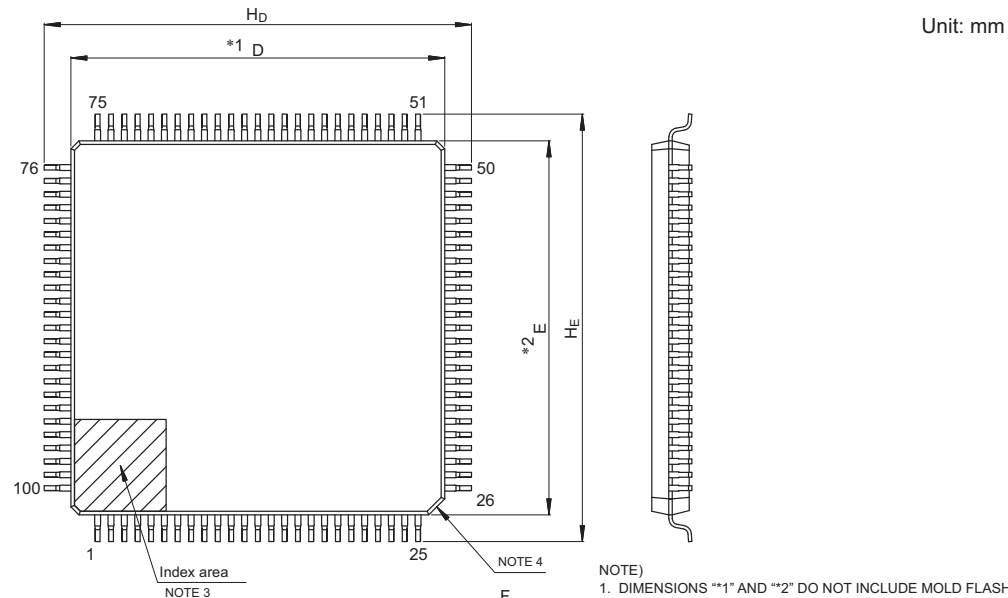


Figure 1.5 144-pin LQFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|-----------------------|--------------|---------------|----------------|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |



- NOTE)
1. DIMENSIONS **1" AND **2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3" DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|------------------|---------------------------|------|------|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| A ₂ | — | 1.4 | — |
| H _D | 15.8 | 16.0 | 16.2 |
| H _E | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| A ₁ | 0.05 | — | 0.15 |
| b _p | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| ⓔ | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| L _p | 0.45 | 0.6 | 0.75 |
| L ₁ | — | 1.0 | — |

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Figure 1.6 100-pin LQFP

| Rev. | Date | Summary |
|------|--------------|------------------|
| 1.00 | Feb 23, 2016 | 1st release |
| 1.30 | Jan 3, 2018 | Updated for 1.30 |
| 1.40 | Aug, 2018 | Updated for 1.40 |

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S7G2 Microcontroller Group Datasheet

Publication Date: Rev.1.40 Aug 6, 2018

Published by: Renesas Electronics Corporation

General Precautions

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



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ВЧ соединители, коаксиальные кабели,
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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