

# 256-Kbit (32 K × 8) Byte-wide F-RAM Memory

## Features

- 256-Kbit ferroelectric random access memory (F-RAM) logically organized as 32 K × 8
  - High-endurance 100 trillion (10<sup>14</sup>) read/writes
  - 151-year data retention (see the [Data Retention and Endurance](#) table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- SRAM and EEPROM compatible
  - Industry-standard 32 K × 8 SRAM and EEPROM pinout
  - 70-ns access time, 130-ns cycle time
- Superior to battery-backed SRAM modules
  - No battery concerns
  - Monolithic reliability
  - True surface mount solution, no rework steps
  - Superior for moisture, shock, and vibration
  - Resistant to negative voltage undershoots
- Low power consumption
  - Active current 15 mA (max)
  - Standby current 25 μA (typ)
- Voltage operation: V<sub>DD</sub> = 4.5 V to 5.5 V

- Industrial temperature: -40 °C to +85 °C
- 28-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant

## Functional Overview

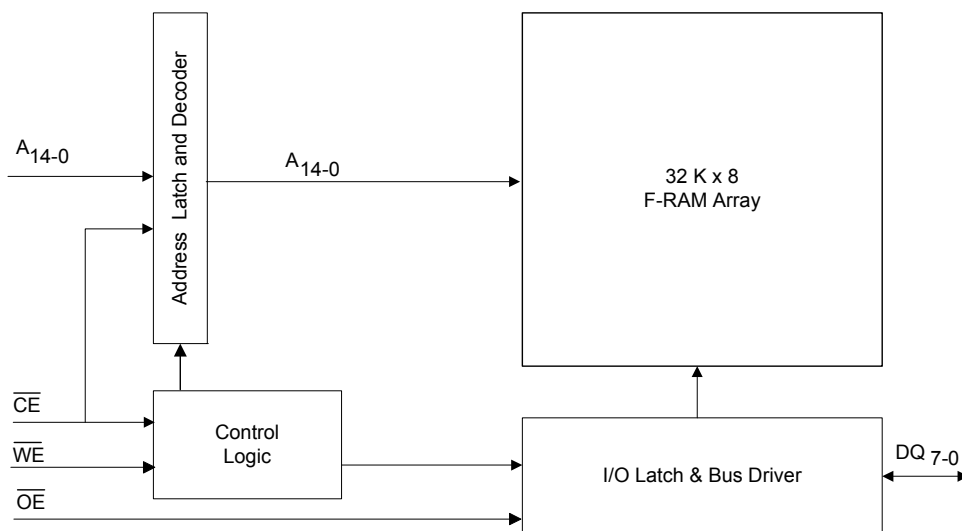
The FM1808B is a 32 K × 8 nonvolatile memory that reads and writes similar to a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 151 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make the F-RAM superior to other types of memory.

The FM1808B operation is similar to that of other RAM devices and therefore, it can be used as a drop-in replacement for a standard SRAM in a system. Minimum read and write cycle times are equal. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM1808B ideal for nonvolatile memory applications requiring frequent or rapid writes.

The device is available in a 28-pin SOIC surface mount package. Device specifications are guaranteed over the industrial temperature range -40 °C to +85 °C.

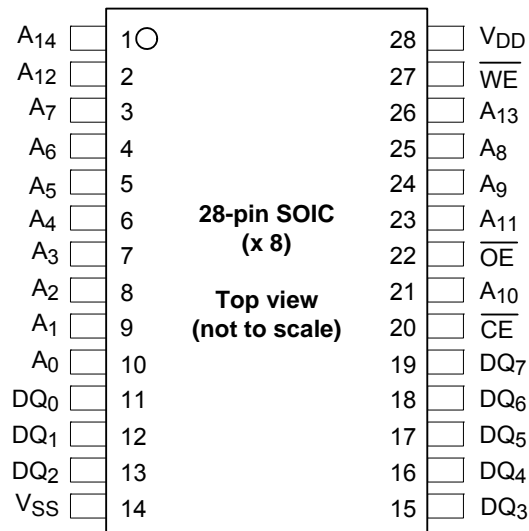
For a complete list of related documentation, click [here](#).

## Logic Block Diagram



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**Pinout**
**Figure 1. 28-pin SOIC pinout**

**Pin Definitions**

| Pin Name                         | I/O Type     | Description  |
|----------------------------------|--------------|--|
| A <sub>14</sub> –A <sub>0</sub>  | Input        | <b>Address inputs:</b> The 15 address lines select one of 32,768 bytes in the F-RAM array.   |
| DQ <sub>7</sub> –DQ <sub>0</sub> | Input/Output | <b>Data I/O Lines:</b> 8-bit bidirectional data bus for accessing the F-RAM array.   |
| $\overline{WE}$                  | Input        | <b>Write Enable:</b> A write cycle begins when $\overline{WE}$ is asserted. Asserting $\overline{WE}$ LOW causes the FM1808B to write the contents of the data bus to the address location latched by the falling edge of $\overline{CE}$ .                      |
| $\overline{CE}$                  | Input        | <b>Chip Enable:</b> The device is selected when $\overline{CE}$ is LOW. Asserting $\overline{CE}$ LOW causes the address to be latched internally. Address changes that occur after $\overline{CE}$ goes LOW will be ignored until the next falling edge occurs. |
| $\overline{OE}$                  | Input        | <b>Output Enable:</b> When $\overline{OE}$ is LOW, the FM1808B drives the data bus when the valid read data is available. Deasserting $\overline{OE}$ HIGH tristates the DQ pins.  |
| V <sub>SS</sub>                  | Ground       | Ground for the device. Must be connected to the ground of the system.  |
| V <sub>DD</sub>                  | Power supply | Power supply input to the device.  |
| NC                               | No connect   | No connect. This pin is not connected to the die.  |

## Device Operation

The FM1808B is a byte-wide F-RAM memory logically organized as  $32,768 \times 8$  and accessed using an industry-standard parallel interface. All data written to the part is immediately nonvolatile with no delay. Functional operation of the F-RAM memory is the same as SRAM type devices, except the FM1808B requires a falling edge of  $\overline{CE}$  to start each memory cycle. See the [Functional Truth Table on page 13](#) for a complete description of read and write modes.

## Memory Architecture

Users access 32,768 memory locations, each with 8 data bits through a parallel interface. The complete 15-bit address specifies each of the 32,768 bytes uniquely. The F-RAM array is organized as 4092 rows of 8-bytes each. This row segmentation has no effect on operation, however the user can group data into blocks by its endurance characteristics as explained in the [Endurance](#) section.

The cycle time is the same for read and write memory operations. This simplifies memory controller logic and timing circuits. Likewise the access time is the same for read and write memory operations. When  $\overline{CE}$  is deasserted HIGH, a pre-charge operation begins, and is required of every memory cycle. Thus unlike SRAM, the access and cycle times are not equal. Writes occur immediately at the end of the access with no delay. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed.

It is the user's responsibility to ensure that  $V_{DD}$  remains within datasheet tolerances to prevent incorrect operation. Also proper voltage level and timing relationships between  $V_{DD}$  and  $\overline{CE}$  must be maintained during power-up and power-down events. See ["Power Cycle Timing"](#) on page 12.

## Memory Operation

The FM1808B is designed to operate in a manner similar to other byte-wide memory products. For users familiar with BBSRAM, the performance is comparable but the byte-wide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the differences result from the higher write performance of F-RAM technology including NoDelay writes and much higher write endurance.

## Read Operation

A read operation begins on the falling edge of  $\overline{CE}$ . At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle must be completed internally even if  $\overline{CE}$  goes inactive. Data becomes available on the bus after the access time is met.

After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM1808B will drive the data bus when  $\overline{OE}$  is asserted LOW and the memory access time is met. If  $\overline{OE}$  is asserted after the memory access time is met, the data bus will be driven with valid

data. If  $\overline{OE}$  is asserted before completing the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven to the bus. When  $\overline{OE}$  is deasserted HIGH, the data bus will remain in a HI-Z state.

## Write Operation

In the FM1808B, writes occur in the same interval as reads. The FM1808B supports both  $\overline{CE}$  and  $\overline{WE}$  controlled write cycles. In both cases, the address is latched on the falling edge of  $\overline{CE}$ .

In a  $\overline{CE}$ -controlled write, the  $\overline{WE}$  signal is asserted before beginning the memory cycle. That is,  $\overline{WE}$  is LOW when the device is activated with the chip enable. In this case, the device begins the memory cycle as a write. The FM1808B will not drive the data bus regardless of the state of  $\overline{OE}$ .

In a  $\overline{WE}$ -controlled write, the memory cycle begins on the falling edge of  $\overline{CE}$ . The  $\overline{WE}$  signal falls after the falling edge of  $\overline{CE}$ . Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of  $\overline{OE}$  until  $\overline{WE}$  falls. The  $\overline{CE}$  and  $\overline{WE}$  controlled write timing cases are shown in the [page 12](#).

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever comes first. A valid write operation requires the user to meet the access time specification before deasserting  $\overline{WE}$  or  $\overline{CE}$ . The data setup time indicates the interval during which data cannot change before the end of the write access.

Unlike other nonvolatile memory technologies, there is no write delay with F-RAM. Because the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

## Pre-charge Operation

The pre-charge operation is an internal condition in which the memory state is prepared for a new access. All memory cycles consist of a memory access and a pre-charge. Pre-charge is user-initiated by driving the  $\overline{CE}$  signal HIGH. It must remain HIGH for at least the minimum pre-charge time,  $t_{PC}$ .

The user determines the beginning of this operation since a pre-charge will not begin until  $\overline{CE}$  rises. However, the device has a maximum  $\overline{CE}$  LOW time specification that must be satisfied.

## Endurance

Internally, a F-RAM operates with a read and restore mechanism. Therefore, each read and write cycle involves a change of state. The memory architecture is based on an array of rows and columns. Each read or write access causes an endurance cycle for an entire row. In the FM1808B, a row is 64 bits wide. Every 8-byte boundary marks the beginning of a new row. Endurance can be optimized by ensuring frequently accessed data is located in different rows. Regardless, F-RAM

offers substantially higher write endurance than other nonvolatile memories. The rated endurance limit of  $10^{14}$  cycles will allow 150,000 accesses per second to the same row for over 20 years.

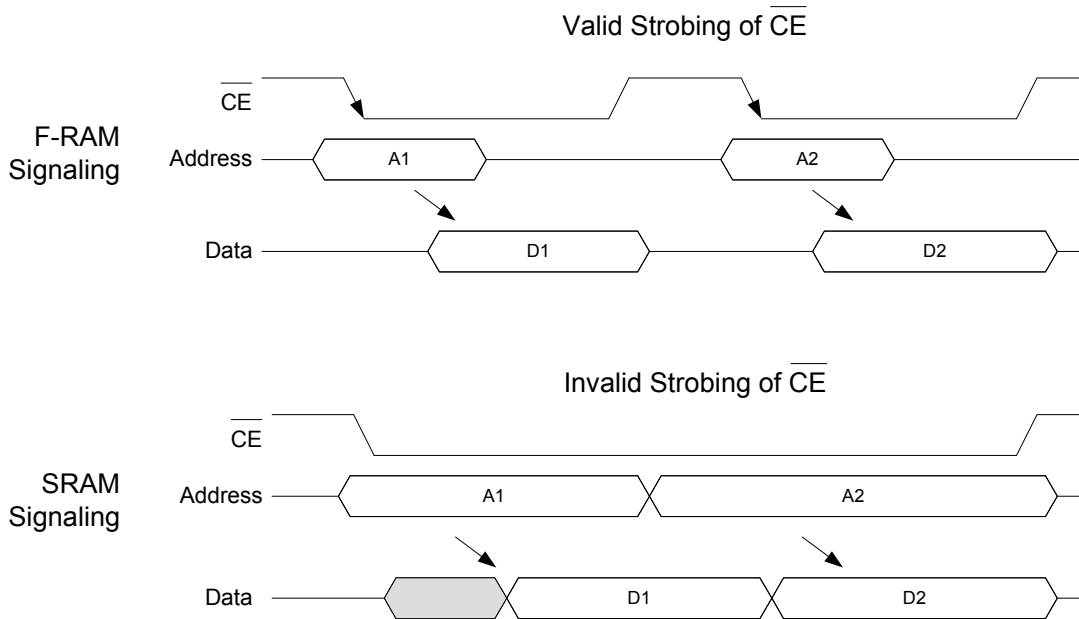
### F-RAM Design Considerations

When designing with F-RAM for the first time, users of SRAM will recognize a few minor differences. First, byte-wide F-RAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of  $\overline{CE}$ , users cannot ground it as they might with SRAM.

Users who are modifying existing designs to use F-RAM should examine the memory controller for timing compatibility of address and control pins. Each memory access must be qualified with a LOW transition of  $\overline{CE}$ . In many cases, this is the only change required. An example of the signal relationships is shown in Figure 2 below. Also shown is a common SRAM signal relationship that will not work for the FM1808B.

The reason for  $\overline{CE}$  to strobe for each address is twofold: it latches the new address and creates the necessary pre-charge period while  $\overline{CE}$  is HIGH.

Figure 2. Chip Enable and Memory Address Relationships



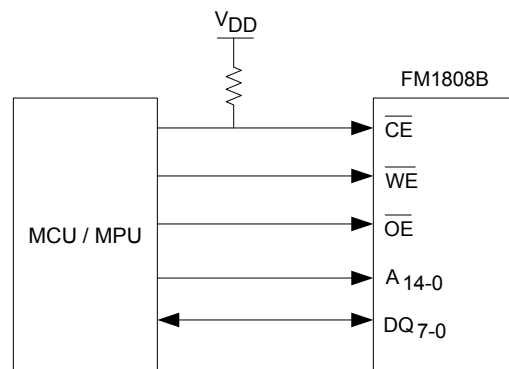
A second design consideration relates to the level of  $V_{DD}$  during operation. Battery-backed SRAMs are forced to monitor  $V_{DD}$  in order to switch to battery backup. They typically block user access below a certain  $V_{DD}$  level in order to prevent loading the battery with current demand from an active SRAM. The user can be abruptly cut off from access to the nonvolatile memory in a power down situation with no warning or indication.

F-RAM memories do not need this system overhead. The memory will not block access at any  $V_{DD}$  level that complies with the specified operating range. The user should take measures to prevent the processor from accessing memory when  $V_{DD}$  is out-of-tolerance. The common design practice of holding a processor in reset during power-down may be sufficient. It is recommended that chip enable is pulled HIGH and allowed to track  $V_{DD}$  during power-up and power-down cycles. It is the user's responsibility to ensure that chip enable is HIGH to prevent accesses below  $V_{DD}$  min. (4.5 V).

Figure 3 shows a pull-up resistor on  $\overline{CE}$ , which will keep the pin HIGH during power cycles, assuming the MCU / MPU pin

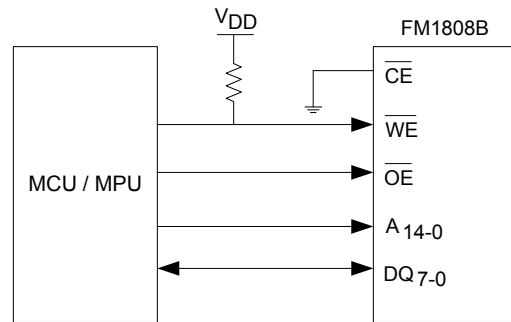
tristates during the reset condition. The pull-up resistor value should be chosen to ensure the CE pin tracks  $V_{DD}$  to a high enough value, so that the current drawn when  $\overline{CE}$  is LOW is not an issue.

Figure 3. Use of Pull-up Resistor on  $\overline{CE}$



Note that if  $\overline{CE}$  is tied to ground, the user must be sure  $\overline{WE}$  is not LOW at power-up or power-down events. If the chip is enabled and  $\overline{WE}$  is LOW during power cycles, data will be corrupted. Figure 4 shows a pull-up resistor on  $\overline{WE}$ , which will keep the pin HIGH during power cycles, assuming the MCU / MPU pin tristates during the reset condition. The pull-up resistor value should be chosen to ensure the  $\overline{WE}$  pin tracks  $V_{DD}$  to a high enough value, so that the current drawn when  $\overline{WE}$  is LOW is not an issue.

Figure 4. Use of Pull-up Resistor on  $\overline{WE}$



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

|   |   |
|---|---|
| Storage temperature   | -55 °C to +125 °C   |
| Maximum junction temperature                                  | 95 °C   |
| Supply voltage on V <sub>DD</sub> relative to V <sub>SS</sub> | -1.0 V to + 7.0 V   |
| Voltage applied to outputs in High Z state                    | -0.5 V to V <sub>DD</sub> + 0.5 V                               |
| Input voltage   | -1.0 V to + 7.0 V and V <sub>IN</sub> < V <sub>DD</sub> + 1.0 V |
| Transient voltage (< 20 ns) on any pin to ground potential    | -2.0 V to V <sub>CC</sub> + 2.0 V                               |
| Package power dissipation capability (T <sub>A</sub> = 25 °C) | 1.0 W   |

|   |          |
|---|----------|
| Surface mount Pb soldering temperature (3 seconds)  | +260 °C  |
| DC output current (1 output at a time, 1s duration) | 15 mA    |
| Static discharge voltage                            |          |
| Human Body Model (AEC-Q100-002 Rev. E)              | 4 kV     |
| Charged Device Model (AEC-Q100-011 Rev. B)          | 1.25 kV  |
| Machine Model (AEC-Q100-003 Rev. E)                 | 300 V    |
| Latch-up current                                    | > 140 mA |

## Operating Range

| Range      | Ambient Temperature (T <sub>A</sub> ) | V <sub>DD</sub> |
|------------|---------------------------------------|-----------------|
| Industrial | -40 °C to +85 °C                      | 4.5 V to 5.5 V  |

## DC Electrical Characteristics

Over the [Operating Range](#)

| Parameter        | Description                    | Test Conditions   | Min                   | Typ <sup>[1]</sup> | Max                   | Unit |
|------------------|--------------------------------|---|-----------------------|--------------------|-----------------------|------|
| V <sub>DD</sub>  | Power supply voltage           |   | 4.5                   | 5.0                | 5.5                   | V    |
| I <sub>DD</sub>  | V <sub>DD</sub> supply current | V <sub>DD</sub> = 5.5 V, $\overline{CE}$ cycling at min. cycle time. All inputs toggling at CMOS levels (0.2 V or V <sub>DD</sub> - 0.2 V), all DQ pins unloaded. | -                     | -                  | 15                    | mA   |
| I <sub>SB1</sub> | Standby current (TTL)          | V <sub>DD</sub> = 5.5 V, $\overline{CE}$ at V <sub>IH</sub> . All other pins are static and at TTL levels (0.2 V or V <sub>DD</sub> - 0.2 V)                      | -                     | -                  | 1.8                   | mA   |
| I <sub>SB2</sub> | Standby current (CMOS)         | V <sub>DD</sub> = 5.5 V, $\overline{CE}$ at V <sub>IH</sub> . All other pins are static and at CMOS levels (0.2 V or V <sub>DD</sub> - 0.2 V)                     | -                     | 25                 | 50                    | μA   |
| I <sub>LI</sub>  | Input leakage current          | V <sub>IN</sub> between V <sub>DD</sub> and V <sub>SS</sub>   | -                     | -                  | ±1                    | μA   |
| I <sub>LO</sub>  | Output leakage current         | V <sub>OUT</sub> between V <sub>DD</sub> and V <sub>SS</sub>  | -                     | -                  | ±1                    | μA   |
| V <sub>IH</sub>  | Input HIGH voltage             |   | 2.0                   | -                  | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL</sub>  | Input LOW voltage              |   | -0.3                  | -                  | 0.8                   | V    |
| V <sub>OH1</sub> | Output HIGH voltage            | I <sub>OH</sub> = -2.0 mA   | 2.4                   | -                  | -                     | V    |
| V <sub>OH2</sub> | Output HIGH voltage            | I <sub>OH</sub> = -100 μA   | V <sub>DD</sub> - 0.2 | -                  | -                     | V    |
| V <sub>OL1</sub> | Output LOW voltage             | I <sub>OL</sub> = 4.2 mA  | -                     | -                  | 0.4                   | V    |
| V <sub>OL2</sub> | Output LOW voltage             | I <sub>OL</sub> = 150 μA  | -                     | -                  | 0.2                   | V    |

## Data Retention and Endurance

| Parameter       | Description    | Test condition             | Min              | Max | Unit   |
|-----------------|----------------|----------------------------|------------------|-----|--------|
| T <sub>DR</sub> | Data retention | At +85 °C                  | 10               | -   | Years  |
|                 |                | At +75 °C                  | 38               | -   |        |
|                 |                | At +65 °C                  | 151              | -   |        |
| NV <sub>C</sub> | Endurance      | Over operating temperature | 10 <sup>14</sup> | -   | Cycles |

### Note

1. Typical values are at 25 °C, V<sub>DD</sub> = V<sub>DD</sub> (typ). Not 100% tested.

**Capacitance**

| Parameter        | Description                   | Test Conditions  | Max | Unit |
|------------------|-------------------------------|--|-----|------|
| C <sub>I/O</sub> | Input/Output capacitance (DQ) | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>DD</sub> = V <sub>DD</sub> (Typ) | 8   | pF   |
| C <sub>IN</sub>  | Input capacitance             |  | 6   | pF   |

**Thermal Resistance**

| Parameter       | Description                              | Test Conditions   | 28-pin SOIC | Unit |
|-----------------|--|---|-------------|------|
| Θ <sub>JA</sub> | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 58          | °C/W |
| Θ <sub>JC</sub> | Thermal resistance (junction to case)    |   | 26          | °C/W |

**AC Test Conditions**

- Input pulse levels .....0 V to 3V
- Input rise and fall times (10%–90%) ..... ≤ 10 ns
- Input and output timing reference levels ..... 1.5
- Output load capacitance ..... 100 pF

Figure 5. AC Test Loads





## AC Switching Characteristics

Over the [Operating Range](#)

| Parameters <sup>[2]</sup>          |                   | Description                       | Min | Max | Unit |
|------------------------------------|-------------------|-----------------------------------|-----|-----|------|
| Cypress Parameter                  | Alt Parameter     |                                   |     |     |      |
| <b>SRAM Read Cycle</b>             |                   |                                   |     |     |      |
| t <sub>CE</sub>                    | t <sub>ACE</sub>  | Chip enable access time           | –   | 70  | ns   |
| t <sub>CA</sub>                    | –                 | Chip enable active time           | 70  | –   | ns   |
| t <sub>RC</sub>                    | –                 | Read cycle time                   | 130 | –   | ns   |
| t <sub>PC</sub>                    | –                 | Pre-charge time                   | 60  | –   | ns   |
| t <sub>AS</sub>                    | t <sub>SA</sub>   | Address setup time                | 0   | –   | ns   |
| t <sub>AH</sub>                    | t <sub>HA</sub>   | Address hold time                 | 15  | –   | ns   |
| t <sub>OE</sub>                    | t <sub>DOE</sub>  | Output enable access time         | –   | 12  | ns   |
| t <sub>HZ</sub> <sup>[3, 4]</sup>  | t <sub>HZCE</sub> | Chip Enable to output HI-Z        | –   | 15  | ns   |
| t <sub>OHZ</sub> <sup>[3, 4]</sup> | t <sub>HZOE</sub> | Output enable HIGH to output HI-Z | –   | 15  | ns   |

### Notes

- Test conditions assume a signal transition time of 10 ns or less, timing reference levels of  $0.5 \times V_{DD}$ , input pulse levels of 0 to 3 V, output loading of the specified  $I_{OL}/I_{OH}$  and load capacitance shown in [AC Test Conditions on page 8](#).
- t<sub>HZ</sub> and t<sub>OHZ</sub> are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
- This parameter is characterized but not 100% tested.

**AC Switching Characteristics** (continued)

 Over the [Operating Range](#)

| Parameters <sup>[2]</sup> |               | Description                                    | Min | Max | Unit |
|---------------------------|---------------|--|-----|-----|------|
| Cypress Parameter         | Alt Parameter |  |     |     |      |
| <b>SRAM Write Cycle</b>   |               |  |     |     |      |
| $t_{WC}$                  | $t_{WC}$      | Write cycle time                               | 130 | –   | ns   |
| $t_{CA}$                  | –             | Chip enable active time                        | 70  | –   | ns   |
| $t_{CW}$                  | $t_{SCE}$     | Chip enable to write enable HIGH               | 70  | –   | ns   |
| $t_{PC}$                  | –             | Pre-charge time                                | 60  | –   | ns   |
| $t_{WP}$                  | $t_{PWE}$     | Write enable pulse width                       | 40  | –   | ns   |
| $t_{AS}$                  | $t_{SA}$      | Address setup time                             | 0   | –   | ns   |
| $t_{AH}$                  | $t_{HA}$      | Address hold time                              | 15  | –   | ns   |
| $t_{DS}$                  | $t_{SD}$      | Data input setup time                          | 30  | –   | ns   |
| $t_{DH}$                  | $t_{HD}$      | Data input hold time                           | 0   | –   | ns   |
| $t_{WZ}^{[5, 6]}$         | $t_{HZWE}$    | Write enable LOW to output HI-Z                | –   | 15  | ns   |
| $t_{WX}^{[6]}$            | –             | Write enable HIGH to output driven             | 10  | –   | ns   |
| $t_{HZ}^{[5]}$            | –             | Chip enable to output HI-Z                     | –   | 15  | ns   |
| $t_{WS}^{[7]}$            | –             | Write enable to $\overline{CE}$ LOW setup time | 0   | –   | ns   |
| $t_{WH}^{[7]}$            | –             | Write enable to $\overline{CE}$ HIGH hold time | 0   | –   | ns   |

**Notes**

5.  $t_{WZ}$  and  $t_{HZ}$  is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
6. This parameter is characterized but not 100% tested.
7. The relationship between  $\overline{CE}$  and  $\overline{WE}$  determines if a  $\overline{CE}$  or  $\overline{WE}$  controlled write occurs. There is no timing specification associated with this relationship.

Figure 6. Read Cycle Timing 1



Figure 7. Read Cycle Timing 2 ( $\overline{CE}$  Controlled)



Figure 8. Write Cycle Timing 1 ( $\overline{WE}$  Controlled)

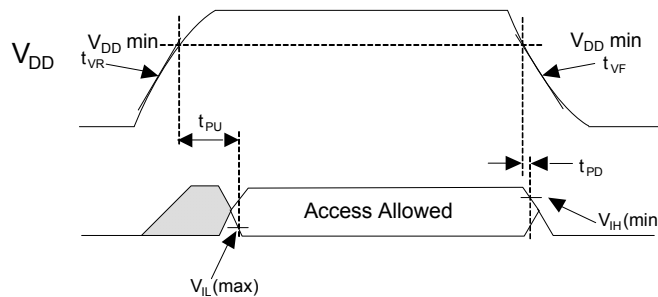


### Power Cycle Timing

Over the [Operating Range](#)

| Parameter      | Description  | Min | Max | Unit      |
|----------------|--|-----|-----|-----------|
| $t_{PU}$       | Power-up (after $V_{DD}$ min. is reached) to first access time | 10  | –   | ms        |
| $t_{PD}$       | Last write ( $\overline{WE}$ HIGH) to power down time          | 0   | –   | $\mu$ s   |
| $t_{VR}^{[8]}$ | $V_{DD}$ power-up ramp rate                                    | 30  | –   | $\mu$ s/V |
| $t_{VF}^{[8]}$ | $V_{DD}$ power-down ramp rate                                  | 30  | –   | $\mu$ s/V |

Figure 9. Power Cycle Timing



**Note**

8. Slope measured at any point on the  $V_{DD}$  waveform.

**Functional Truth Table**

| $\overline{CE}$ | $\overline{WE}$ | Operation <sup>[9, 10]</sup>                             |
|-----------------|-----------------|--|
| H               | X               | Standby/Pre-charge                                       |
| ↓               | X               | Latch Address (and begin write if $\overline{WE}$ = LOW) |
| L               | H               | Read   |
| L               | ↓               | Write  |

**Notes**

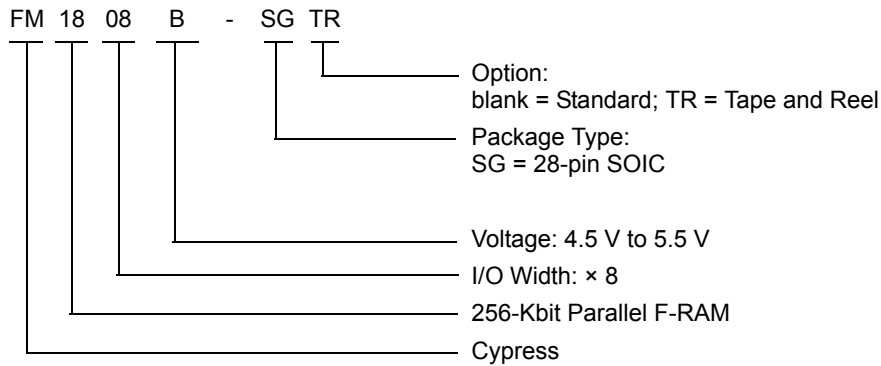
9. H = Logic HIGH, L = Logic LOW, V = Valid Data, X = Don't Care, ↓ = toggle LOW, ↑ = toggle HIGH.  
 10. The  $\overline{OE}$  pin controls only the DQ output buffers.

**Ordering Information**

| Ordering Code | Package Diagram | Package Type | Operating Range |
|---------------|-----------------|--------------|-----------------|
| FM1808B-SG    | 51-85026        | 28-pin SOIC  | Industrial      |
| FM1808B-SGTR  | 51-85026        | 28-pin SOIC  |                 |

All the above parts are Pb-free.

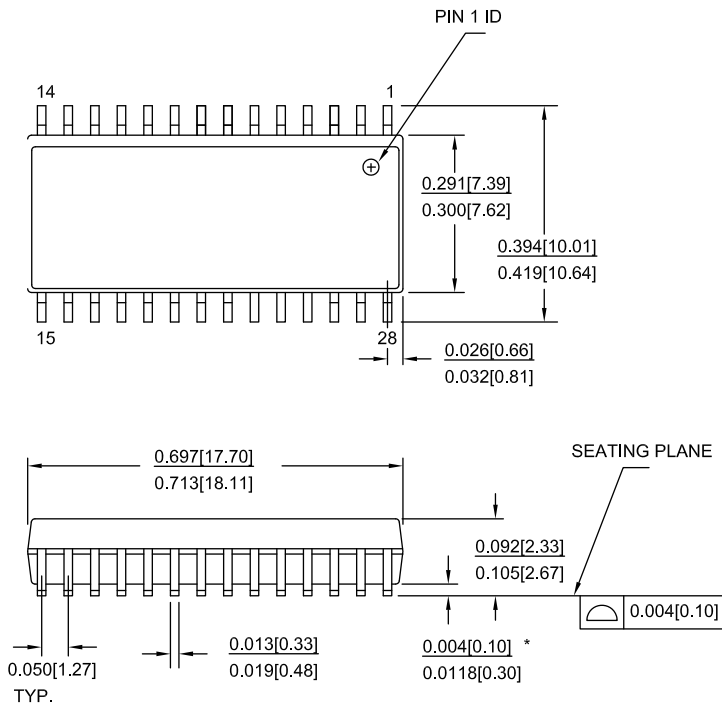
**Ordering Code Definitions**



Package Diagram

Figure 10. 28-pin SOIC Package Outline, 51-85026

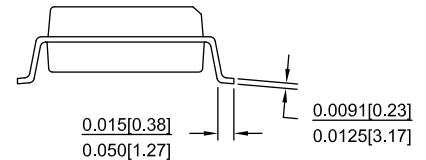
28 Lead (300 Mil) SOIC – S21



NOTE :

1. JEDEC STD REF MO-119
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.

| PART # |                |
|--------|----------------|
| S28.3  | STANDARD PKG.  |
| SZ28.3 | LEAD FREE PKG. |
| SX28.3 | LEAD FREE PKG. |



51-85026 \*H

### Acronyms

| Acronym | Description                                |
|---------|--|
| CPU     | Central Processing Unit                    |
| CMOS    | Complementary Metal Oxide Semiconductor    |
| JEDEC   | Joint Electron Devices Engineering Council |
| JESD    | JEDEC Standards                            |
| EIA     | Electronic Industries Alliance             |
| F-RAM   | Ferroelectric Random Access Memory         |
| I/O     | Input/Output                               |
| MCU     | Microcontroller Unit                       |
| MPU     | Microprocessor Unit                        |
| RoHS    | Restriction of Hazardous Substances        |
| R/W     | Read and Write                             |
| SOIC    | Small Outline Integrated Circuit           |
| SRAM    | Static Random Access Memory                |

### Document Conventions

#### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| Hz     | hertz           |
| kHz    | kilohertz       |
| kΩ     | kilohm          |
| MHz    | megahertz       |
| μA     | microampere     |
| μF     | microfarad      |
| μs     | microsecond     |
| mA     | milliampere     |
| ms     | millisecond     |
| MΩ     | megaohm         |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |



**Document History Page**

| Document Title: FM1808B, 256-Kbit (32 K x 8) Byte-wide F-RAM Memory |         |                 |                 |   |
|---|---------|-----------------|-----------------|---|
| Document Number: 001-86209  |         |                 |                 |   |
| Rev.  | ECN No. | Orig. of Change | Submission Date | Description of Change   |
| **  | 3912933 | GVCH            | 02/25/2013      | New spec  |
| *A  | 4000965 | GVCH            | 05/15/2013      | Added Appendix A - Errata for FM1808B   |
| *B  | 4045491 | GVCH            | 06/30/2013      | All errata items are fixed and the errata is removed.   |
| *C  | 4274813 | GVCH            | 03/10/2014      | Converted to Cypress standard format<br>Changed datasheet status from "Preliminary to Final"<br>Changed endurance value from $10^{12}$ to $10^{14}$ cycles<br>Updated <a href="#">Maximum Ratings</a> table<br>- Removed Moisture Sensitivity Level (MSL)<br>- Added junction temperature and latch up current<br>Updated <a href="#">Data Retention and Endurance</a> table<br>Added <a href="#">Thermal Resistance</a> table<br>Removed Package Marking Scheme (top mark) |
| *D  | 4562106 | GVCH            | 11/05/2014      | Added related documentation hyperlink in page 1.<br>Updated package diagram 51-85026 to current version.  |

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