5 V 18-Bit *nano*DAC® in a SOT-23

Data Sheet **AD5680**

FEATURES

- Single 18-bit *nano*DAC
- 18-bit monotonic
- 12-bit accuracy guaranteed
- Tiny 8-lead SOT-23 package
- Power-on reset to zero scale/midscale
- 4.5 V to 5.5 V power supply
- Serial interface
- Rail-to-rail operation
- $\overline{\text{SYNC}}$ interrupt facility
- Temperature range: −40°C to +105°C

APPLICATIONS

- Closed-loop process control
- Low bandwidth data acquisition systems
- Portable battery-powered instruments
- Gain and offset adjustment
- Precision setpoint control

FUNCTIONAL BLOCK DIAGRAM

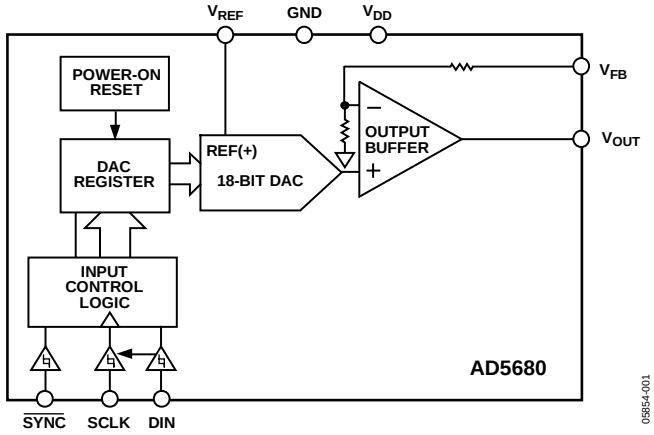

Figure 1.

GENERAL DESCRIPTION

The AD5680, a member of the *nano*DAC family, is a single, 18-bit buffered voltage-out digital-to-analog converter (DAC) that operates from a single 4.5 V to 5.5 V supply and is 18-bit monotonic.

The AD5680 requires an external reference voltage to set the output range of the DAC. The part incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V (AD5680-1) or to midscale (AD5680-2) and remains there until a valid write takes place.

The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The power consumption is 1.6 mW at 5 V.

The AD5680 on-chip precision output amplifier allows rail-to-rail output swing to be achieved. For remote sensing applications, the output amplifier's inverting input is available to the user.

The AD5680 uses a versatile 3-wire serial interface that operates at clock rates up to 30 MHz, and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

PRODUCT HIGHLIGHTS

1. 18 bits of resolution.
2. 12-bit accuracy guaranteed for 18-bit DAC.
3. Available in an 8-lead SOT-23.
4. Low power; typically consumes 1.6 mW at 5 V.
5. Power-on reset to zero scale or to midscale.

RELATED DEVICES

AD5662—16-bit DAC in SOT-23.

Rev. C Document Feedback
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REVISION HISTORY

7/2017—Rev. B to Rev. C

Changed ADSP-BF53x to ADSP-BF531 ... Throughout
Changed ADuM13x to ADuM130D ... Throughout
Added t_{UPDATE} Parameter, Table 2 ... 4
Change to Figure 28 ... 13
Changes to Figure 37 ... 16
Changes to Ordering Guide ... 19

2/2014—Rev. A to Rev. B

Added 8-Lead LFCSP ... Universal
Changes to Figure 3 Caption and Table 4 Caption ... 6
Added Figure 4; Renumbered Sequentially ... 6
Updated Outline Dimensions ... 17
Changes to Ordering Guide ... 17

3/2007—Rev. 0 to Rev. A

Changes to Input Shift Register Section ... 12
Changes to Figure 25 ... 12

6/2006—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; $V_{REF} = V_{DD}$; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	B Grade[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
STATIC PERFORMANCE[2]					
Resolution	18			Bits	
Relative Accuracy		±32	±64	LSB	
Differential Nonlinearity[3]			±1	LSB	Measured in 50 Hz system bandwidth
			±2	LSB	Measured in 300 Hz system bandwidth
Zero-Code Error		2	10	mV	All 0s loaded to DAC register
Full-Scale Error		−0.2	−1	% FSR	All 1s loaded to DAC register
Offset Error			±10	mV	
Gain Error			±1.5	% FSR	
Zero-Code Error Drift		±2		μV/°C	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−100		dB	DAC code = midscale; V_{DD} = 5 V ± 10%
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Output Voltage Settling Time		80	85	μs	¼ to ¾ scale change settling to ±8 LSB, R_L = 2 kΩ; 0 pF < C_L < 200 pF
Slew Rate		1.5		V/μs	¼ to ¾ scale
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	R_L = 2 kΩ
Output Noise Spectral Density[4]		80		nV/√Hz	DAC code = midscale, 10 kHz
Output Noise (0.1 Hz to 10 Hz)[4]		25		μV p-p	DAC code = midscale
Total Harmonic Distortion (THD)[4]		−80		dB	V_{REF} = 2 V ± 300 mV p-p, f = 200 Hz
Digital-to-Analog Glitch Impulse		5		nV-s	1 LSB change around major carry
Digital Feedthrough		0.2		nV-s	
DC Output Impedance		0.5		Ω	
Short-Circuit Current[4]		30		mA	V_{DD} = 5 V
REFERENCE INPUT					
Reference Current		40	75	μA	$V_{REF} = V_{DD}$ = 5 V
Reference Input Range[5]	0.75		V_{DD}	V	
Reference Input Impedance		125		kΩ	
LOGIC INPUTS[3]					
Input Current			±2	μA	All digital inputs
V_{INL}, Input Low Voltage			0.8	V	V_{DD} = 5 V
V_{INH}, Input High Voltage		2		V	V_{DD} = 5 V
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	4.5		5.5	V	All digital inputs at 0 V or V_{DD}
I_{DD} (Normal Mode)					DAC active and excluding load current
V_{DD} = 4.5 V to 5.5 V		325	450	μA	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY					
I_{OUT}/I_{DD}		85		%	I_{LOAD} = 2 mA, V_{DD} = 5 V

[1] Temperature range for B version is −40°C to +105°C, typical at +25°C.
[2] DC specifications tested with the outputs unloaded, unless otherwise stated. Linearity calculated using a reduced code range of 2048 to 260,096.
[3] Guaranteed by design and characterization; not production tested.
[4] Output unloaded.
[5] Reference input range at ambient where maximum DNL specification is achievable.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. V_{DD} = 4.5 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX} V_{DD} = 4.5 V to 5.5 V	Unit	Conditions/Comments
t_1[1]	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	4.5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8	33	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_9	13	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK fall ignore
t_{10}	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ fall ignore
t_{UPDATE}	250	µs min	Minimum update period

[1] Maximum SCLK frequency is 30 MHz at V_{DD} = 4.5 V to 5.5 V.

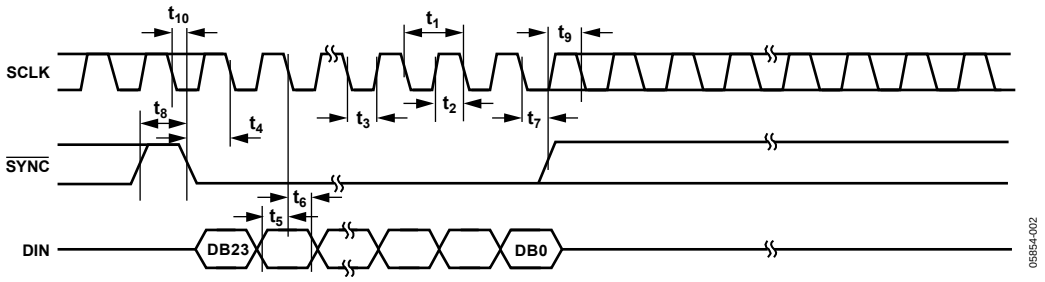


Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{FB} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	
SOT-23 Package (4-Layer Board)	119°C/W
Reflow Soldering Peak Temperature	
Pb-free	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

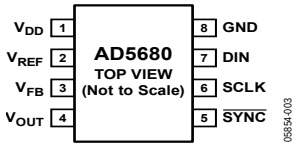


Figure 3. 8-Lead SOT-23 Pin Configuration

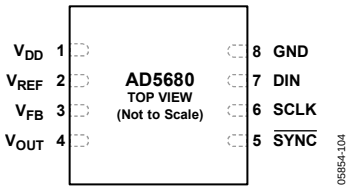


Figure 4. 8-Lead LFCSP Pin Configuration

Table 4. 8-Lead SOT-23 and 8-Lead LFSCP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The part can be operated from 4.5 V to 5.5 V. V_{DD} should be decoupled to GND.
2	V_{REF}	Reference Voltage Input.
3	V_{FB}	Feedback Connection for the Output Amplifier. V_{FB} should be connected to V_{OUT} for normal operation.
4	V_{OUT}	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{SYNC}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC. $\overline{SYNC}$
6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
7	DIN	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
8	GND	Ground. Ground reference point for all circuitry on the part.

TYPICAL PERFORMANCE CHARACTERISTICS

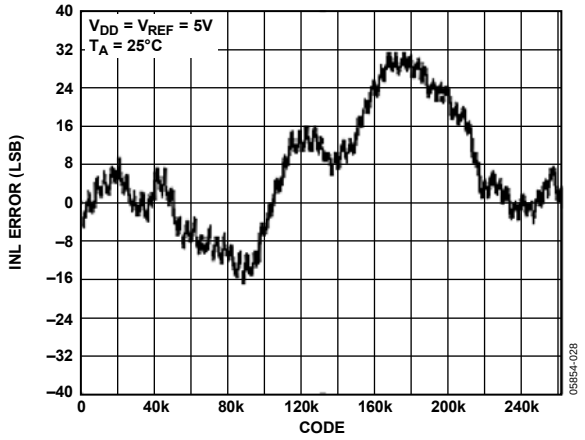


Figure 5. Typical INL Plot

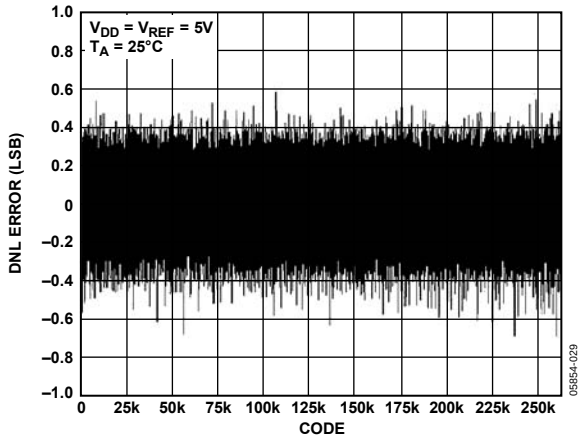


Figure 6. Typical DNL Plot in 50 Hz System Bandwidth

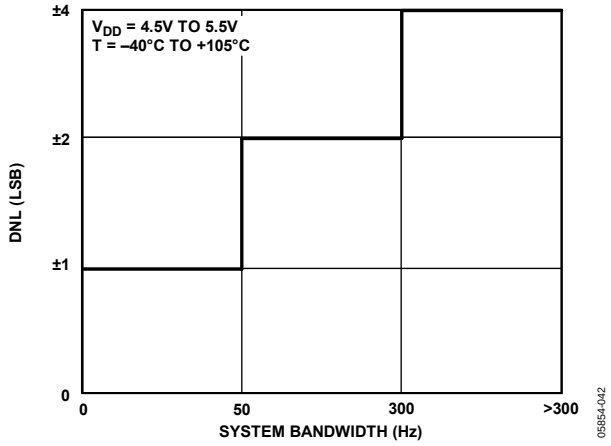


Figure 7. DNL Performance vs. System Bandwidth

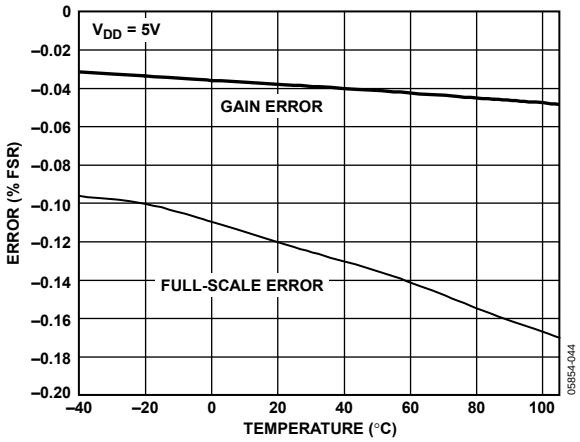


Figure 8. Gain Error and Full-Scale Error vs. Temperature

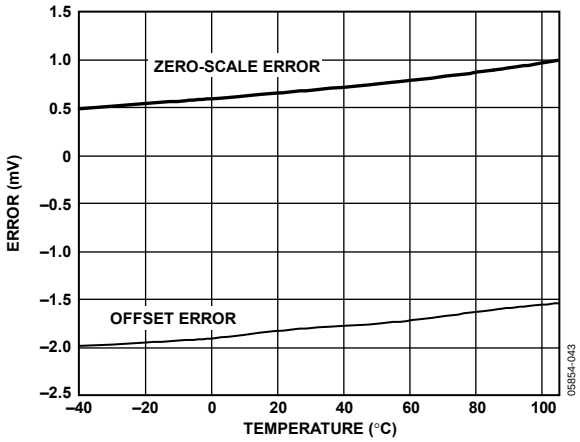


Figure 9. Zero-Scale Error and Offset Error vs. Temperature

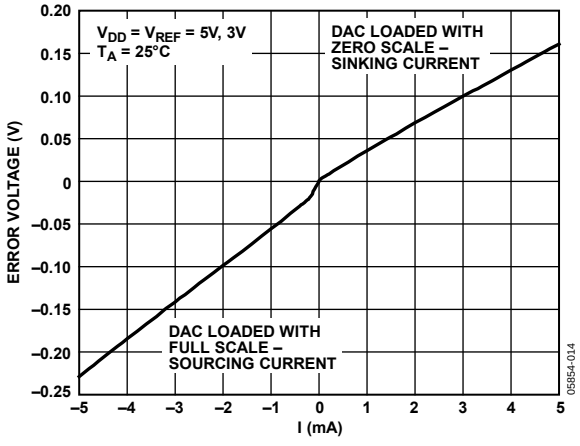


Figure 10. Headroom at Rails vs. Source and Sink Current

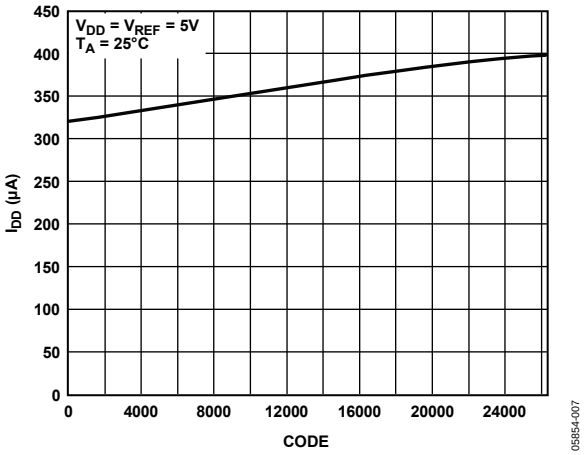


Figure 11. Supply Current vs. Code

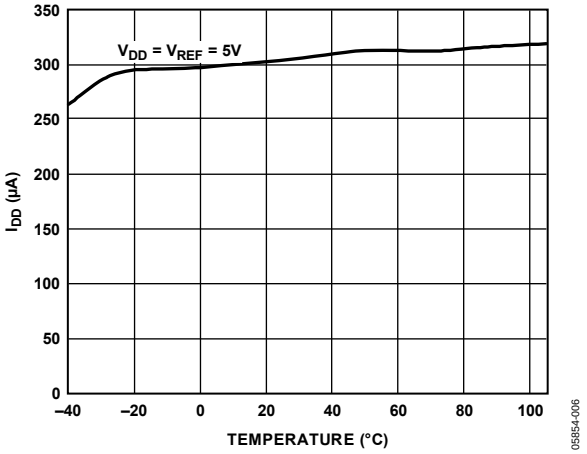


Figure 12. Supply Current vs. Temperature

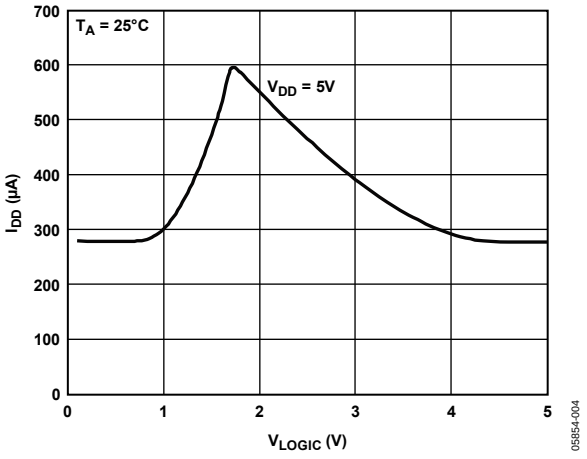


Figure 13. Supply Current vs. Logic Input Voltage

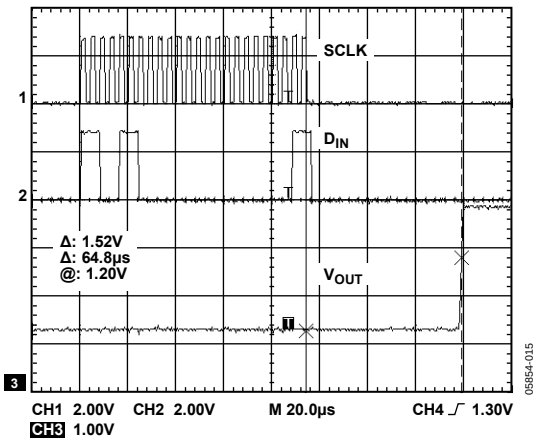


Figure 14. Full-Scale Settling Time, 5 V

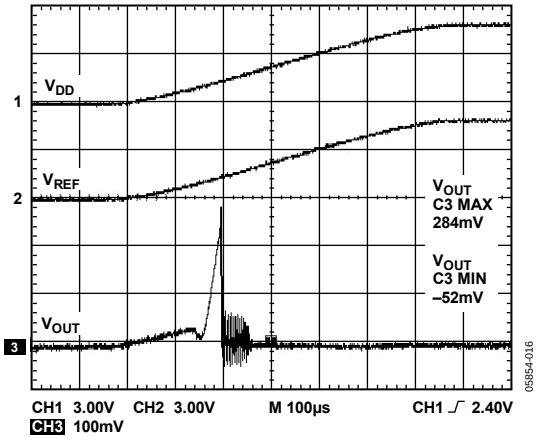


Figure 15. Power-On Reset to 0 V

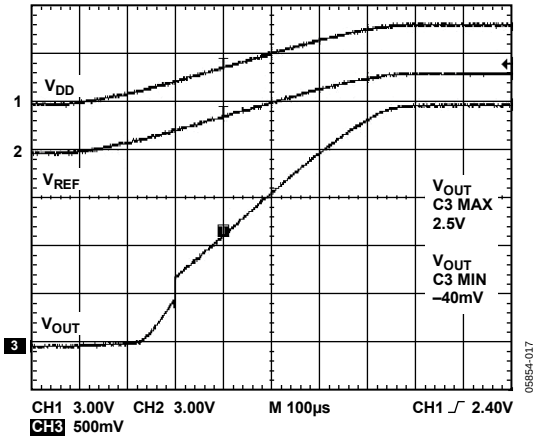


Figure 16. Power-On Reset to Midscale

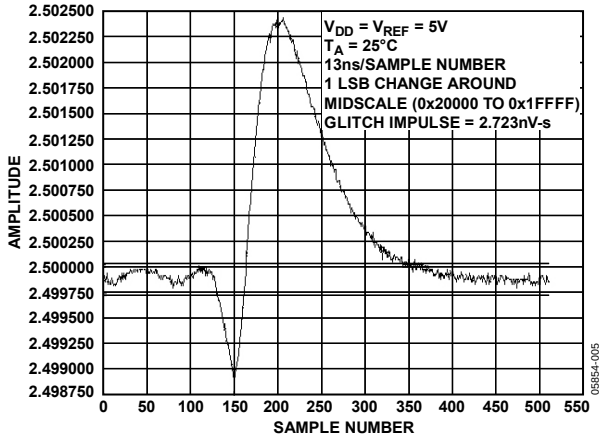


Figure 17. Digital-to-Analog Glitch Impulse (Negative)

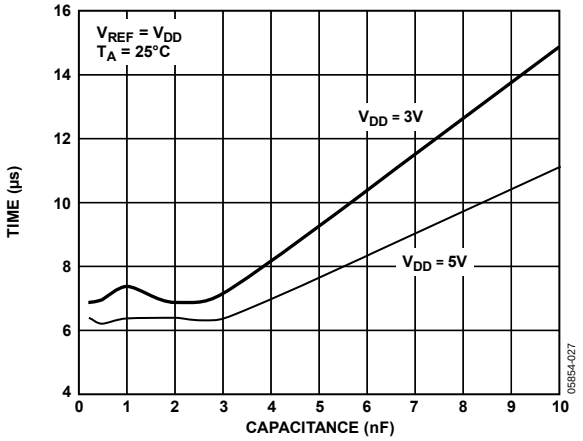


Figure 20. Settling Time vs. Capacitive Load

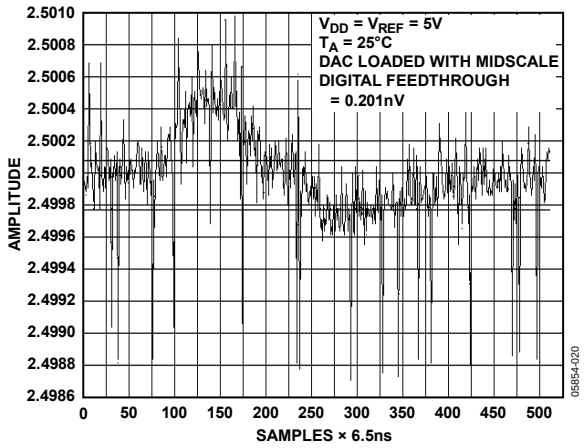


Figure 18. Digital Feedthrough

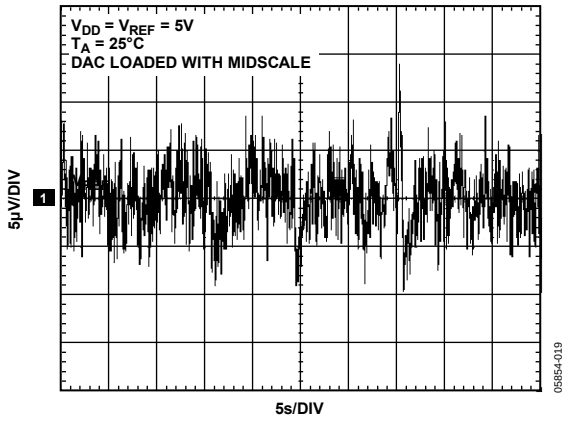


Figure 21. 0.1 Hz to 10 Hz Output Noise Plot

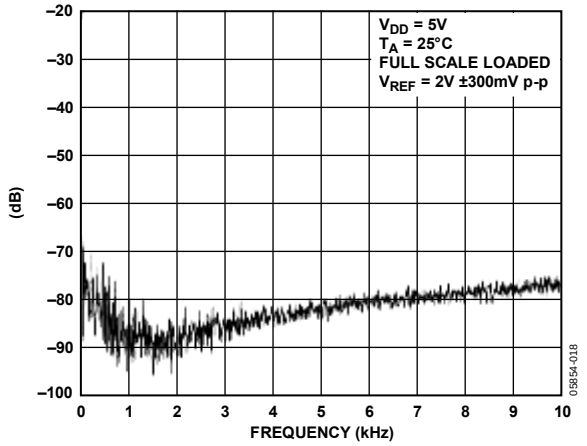


Figure 19. Total Harmonic Distortion

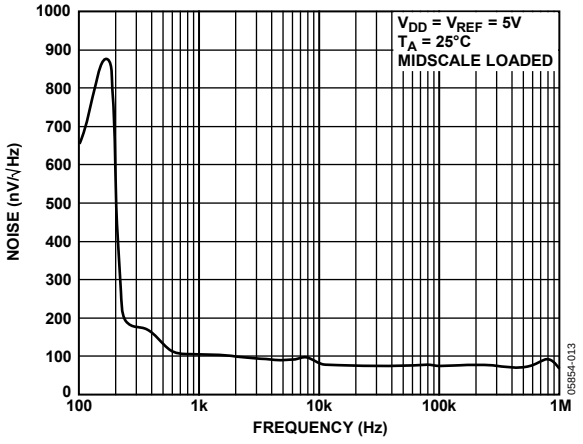


Figure 22. Noise Spectral Density

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Figure 5 shows a typical INL vs. code plot.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. Figure 6 shows a typical DNL vs. code plot.

Zero-Code Error
Zero-code error is a measurement of the output error when zero code (0x00000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5680 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 9.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0x3FFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percent of the full-scale range.

Zero-Code Error Drift
This is a measurement of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Temperature Coefficient
This is a measurement of the change in gain error with a change in temperature. It is expressed in (ppm of full-scale range)/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal), expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5680 with Code 2048 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
This is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the 24th falling edge of SCLK.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x1FFFF to 0x20000). See Figure 17.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Total Harmonic Distortion (THD)
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC. The THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Noise Spectral Density
This is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. Figure 22 shows a plot of noise spectral density.

THEORY OF OPERATION

DAC SECTION

The AD5680 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 23 shows a block diagram of the DAC architecture.

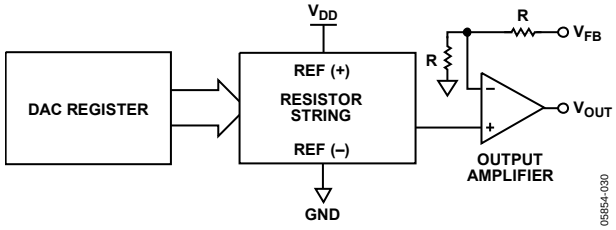


Figure 23. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{REF} \times \left(\frac{D}{262{,}144} \right)$$

where D is the decimal equivalent of the binary code that is loaded to the DAC register. It can range from 0 to 262,143.

RESISTOR STRING

The resistor string section is shown in Figure 24. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

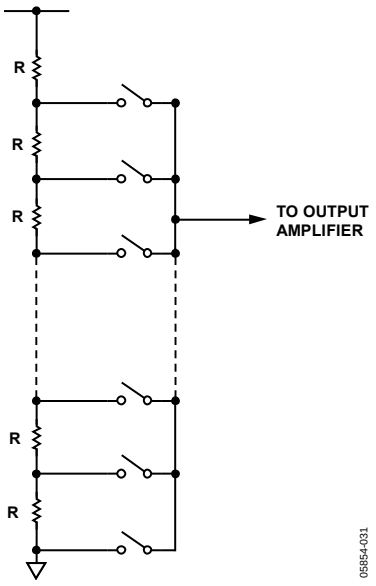


Figure 24. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. This output buffer amplifier has a gain of 2 derived from a 50 kΩ resistor divider network in the feedback path. The output amplifier's inverting input is available to the user, allowing for remote sensing. This V_{FB} pin must be connected to V_{OUT} for normal operation. It can drive a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 10. The slew rate is 1.5 V/µs with a ¼ to ¾ full-scale settling time of 10 µs.

INTERPOLATOR ARCHITECTURE

The AD5680 contains a 16-bit DAC with an internal clock generator and interpolator. The voltage levels generated by the 16-bit, 1 LSB step can be subdivided using the interpolator to increase the resolution to 18 bits.

The 18-bit input code can be divided into two segments: 16-bit DAC code (DB19 to DB4) and 2-bit interpolator code (DB3 and DB2). The input to the DAC is switched between a 16-bit code (for example, Code 1023) and a 16-bit code + 1 LSB (for example, Code 1024). The 2-bit interpolator code determines the duty cycle of the switching and hence the 18-bit code level. See Table 5 for an example.

Table 5.

18-Bit Code	16-Bit DAC Code	2-Bit Interpolator Code		Duty Cycle
DB19 to DB2	DB19 to DB4	DB3	DB2	
4092	1023	0	0	0
4093	1023	0	1	25%
4094	1023	1	0	50%
4095	1023	1	1	75%
4096	1024	0	0	0

The DAC output voltage is given by the average value of the waveform switching between 16-bit code (C) and 16-bit code + 1 (C + 1). The output voltage is a function of the duty cycle of the switching.

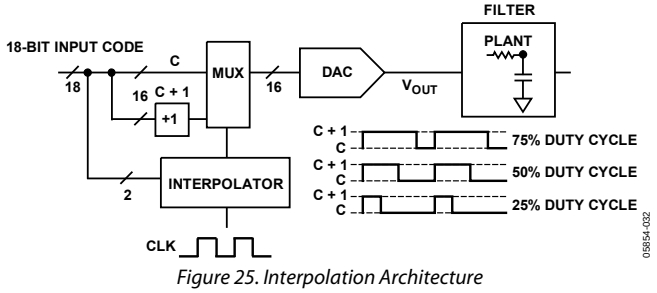


Figure 25. Interpolation Architecture

SERIAL INTERFACE

The AD5680 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as with most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5680 compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents occurs. At this stage, the $\overline{SYNC}$ line can be kept low or brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Because the $\overline{SYNC}$ buffer draws more current when V_{IN} = 2 V than it does when V_{IN} = 0.8 V, $\overline{SYNC}$ should be idled low between write sequences for even lower power operation. As mentioned previously, it must, however, be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide (see Figure 26). The first two bits are don't care bits. Bit DB21 and Bit DB20 are reserved bits and should be set to 0. The next 18 bits are the data bits followed by two don't care bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

$\overline{SYNC}$ INTERRUPT

In a normal write sequence, the $\overline{SYNC}$ line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However, if $\overline{SYNC}$ is brought high before the 24th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 27).

POWER-ON RESET

The AD5680 family contains a power-on reset circuit that controls the output voltage during power-up. The AD5680-1 DAC output powers up to 0 V, and the AD5680-2 DAC output powers up to midscale. The output remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the output state of the DAC while it is in the process of powering up.

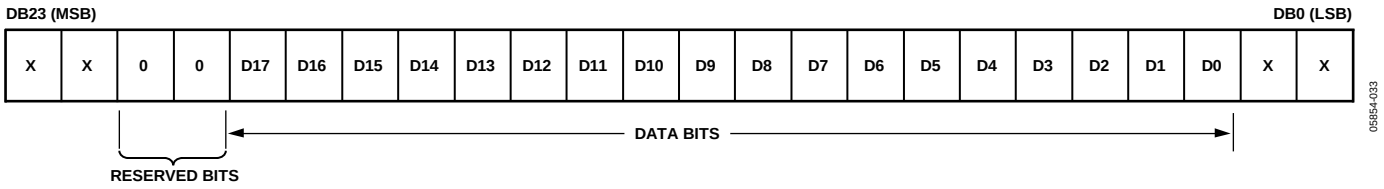


Figure 26. Input Register Contents

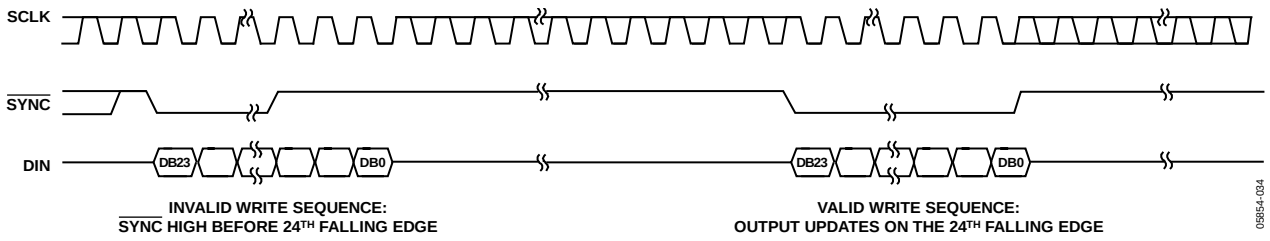
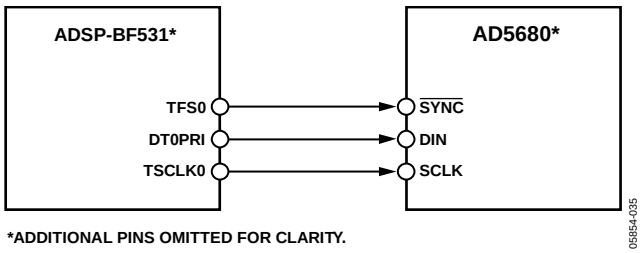


Figure 27. $\overline{SYNC}$ Interrupt Facility

MICROPROCESSOR INTERFACING

AD5680 to Blackfin® ADSP-BF531 Interface

Figure 28 shows a serial interface between the AD5680 and the Blackfin ADSP-BF531 microprocessor. The ADSP-BF531 processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5680, the setup for the interface is as follows. DT0PRI drives the DIN pin of the AD5680, while TSCLK0 drives the SCLK of the part. The $\overline{\text{SYNC}}$ is driven from TFS0.



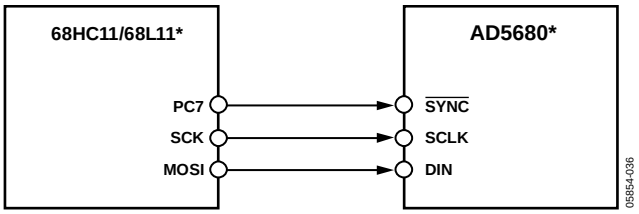
*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 28. AD5680 to Blackfin ADSP-BF531 Interface

AD5680 to 68HC11/68L11 Interface

Figure 29 shows a serial interface between the AD5680 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5680, while the MOSI output drives the serial data line of the DAC.

The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: The 68HC11/68L11 is configured with its CPOL bit as 0 and its CPHA bit as 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured this way, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5680, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.

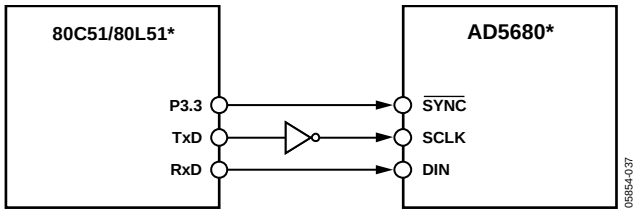


*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 29. AD5680 to 68HC11/68L11 Interface

AD5680 to 80C51/80L51 Interface

Figure 30 shows a serial interface between the AD5680 and the 80C51/80L51 microcontroller. The setup for the interface is as follows. TxD of the 80C51/80L51 drives SCLK of the AD5680, while RxD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the AD5680, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes only; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5680 must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

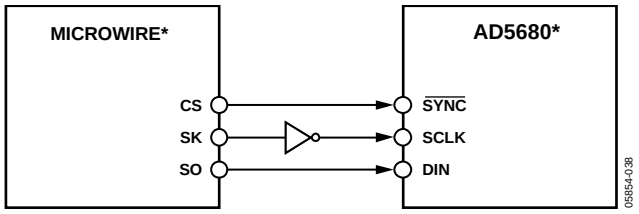


*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 30. AD5680 to 80C51/80L51 Interface

AD5680 to MICROWIRE Interface

Figure 31 shows an interface between the AD5680 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5680 on the rising edge of the SK.



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 31. AD5680 to MICROWIRE Interface

APPLICATIONS INFORMATION

CLOSED-LOOP APPLICATIONS

The AD5680 is suitable for closed-loop low bandwidth applications. Ideally, the system bandwidth acts as a filter on the DAC output. (See the Filter section for details of the DAC output prefiltering and postfiltering.) The DAC updates at the interpolation frequency of 10 kHz.

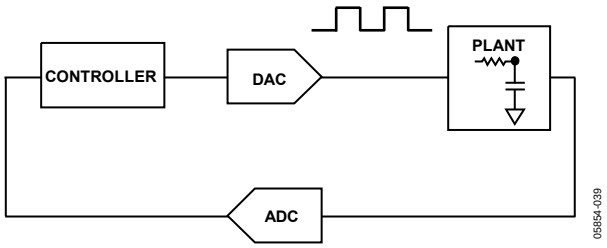


Figure 32. Typical Closed-Loop Application

FILTER

The DAC output voltage for code transition 4092 to 4094 can be seen in Figure 33. This is the DAC output unfiltered. Code 4092 does not have any interpolation but Code 4094 has interpolation with a 50% duty cycle (see Table 5). Figure 34 shows the DAC output with a 50 Hz passive RC filter and Figure 35 shows the output with a 300 Hz passive RC filter. An RC combination of 320 kΩ and 10 nF has been used to achieve the 50 Hz cutoff frequency, and an RC combination of 81 kΩ and 10 nF has been used to achieve the 300 Hz cutoff frequency.

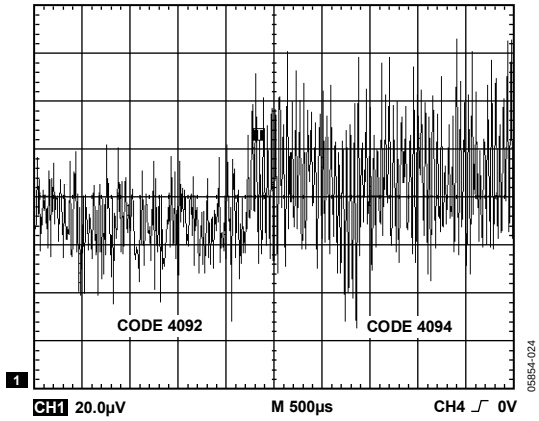


Figure 33. DAC Output Unfiltered

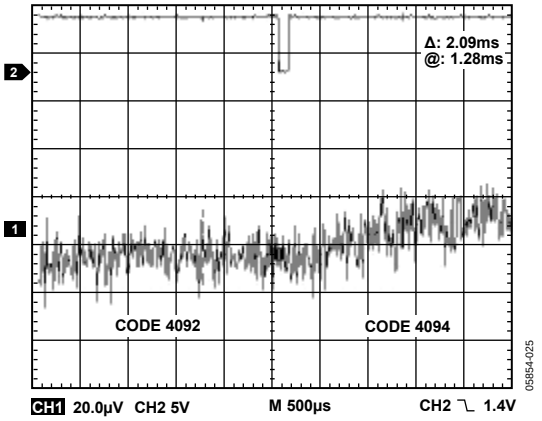


Figure 34. DAC Output with 50 Hz Filter on Output

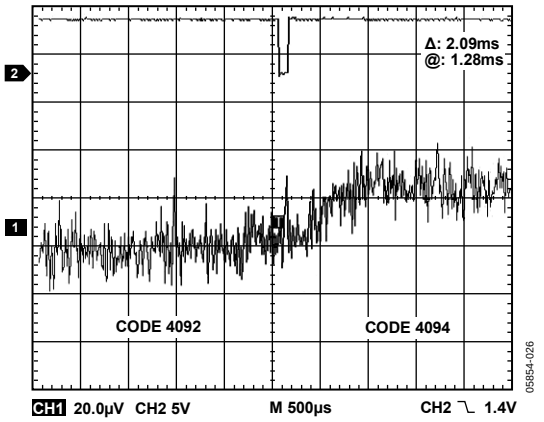


Figure 35. DAC Output with 300 Hz Filter on Output

CHOOSING A REFERENCE FOR THE AD5680

To achieve the optimum performance from the AD5680, choose a precision voltage reference carefully. The AD5680 has only one reference input, V_{REF}. The voltage on the reference input is used to supply the positive input to the DAC. Therefore, any error in the reference is reflected in the DAC.

When choosing a voltage reference for high accuracy applications, the sources of error are initial accuracy, ppm drift, long-term drift, and output voltage noise. Initial accuracy on the output voltage of the DAC leads to a full-scale error in the DAC. To minimize these errors, a reference with high initial accuracy is preferred. In addition, choosing a reference with an output trim adjustment, such as the ADR425, allows a system designer to trim out system errors by setting a reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Long-term drift is a measurement of how much the reference drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable during its entire lifetime.

The temperature coefficient of a reference's output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce temperature dependence of the DAC output voltage in ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. It is important to choose a reference with as low an output noise voltage as is practical for the system noise resolution required. Precision voltage references such as the ADR425 produce low output noise in the 0.1 Hz to 10 Hz range. Examples of recommended precision references for use as supply to the AD5680 are shown in the Table 6.

Table 6. Partial List of Precision References for Use with the AD5680

Part No.	Initial Accuracy (mV max)	Temperature Drift (ppm/°C max)	0.1 Hz to 10 Hz Noise (µV p-p typ)	V_{OUT} (V)
ADR425	±2	3	3.4	5
ADR395	±6	25	5	5
REF195	±2	5	50	5

USING A REFERENCE AS A POWER SUPPLY FOR THE AD5680

Because the supply current required by the AD5680 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the part (see Figure 36). This is especially useful if the power supply is quite noisy, or if the system supply voltages are at some value other than 5 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD5680; see Table 6 for a suitable reference. If the low dropout REF195 is used, it must supply 325 µA of current to the AD5680, with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

$$325\ \mu A + (5\ V/5\ k\Omega) = 1.33\ mA$$

The load regulation of the REF195 is typically 2 ppm/mA, which results in a 2.7 ppm (13.5 µV) error for the 1.33 mA current drawn from it. This corresponds to a 0.177 LSB error.

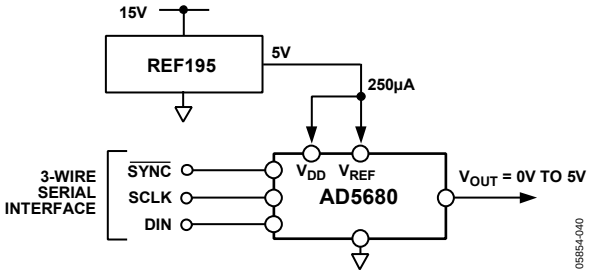


Figure 36. REF195 as Power Supply to the AD5680

USING THE AD5680 WITH A GALVANICALLY ISOLATED INTERFACE

In process-control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur in the area where the DAC is functioning. Isocouplers provide isolation in excess of 3 kV. The AD5680 uses a 3-wire serial logic interface, so the ADuM130D 3-channel digital isolator provides the required isolation (see Figure 37). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5680.

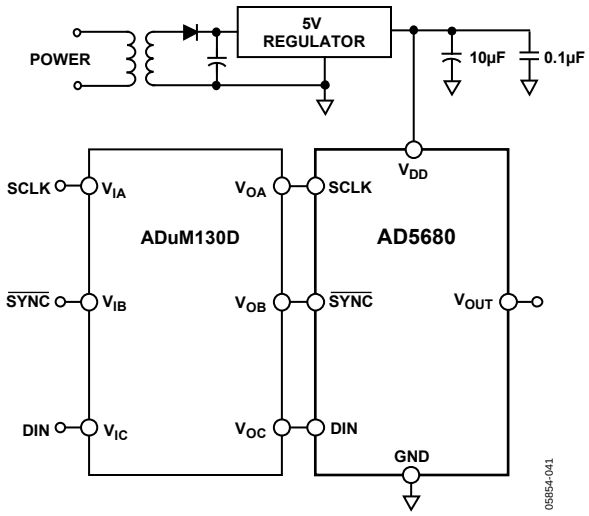


Figure 37. AD5680 with a Galvanically Isolated Interface

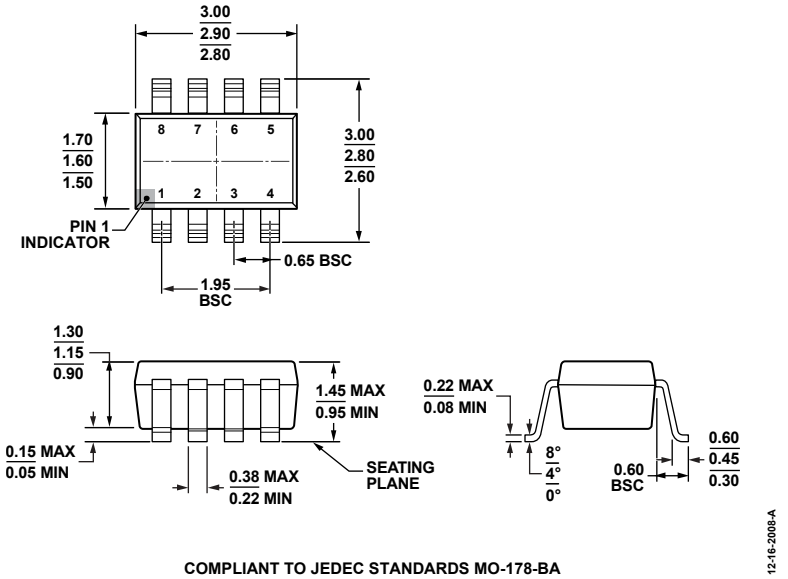
POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5680 should have separate analog and digital sections, each having its own area of the board. If the AD5680 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5680.

The power supply to the AD5680 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be located as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors should be the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), for example, common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

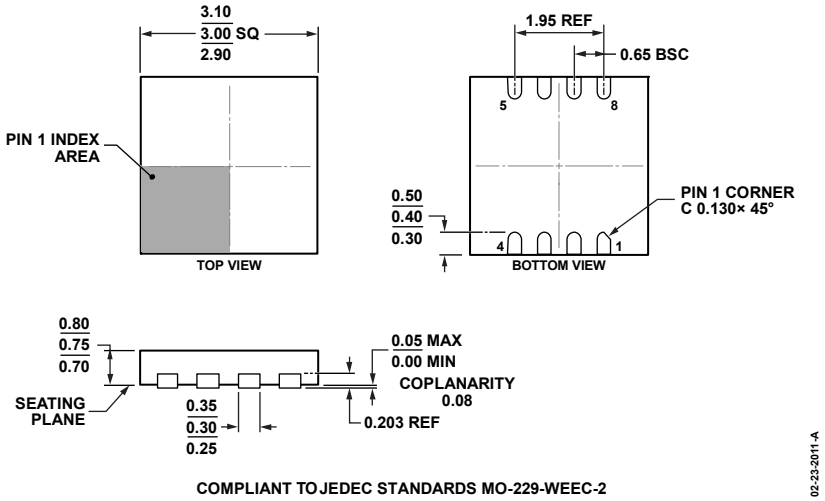
The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 38. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-229-WEEC-2

Figure 39. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Power-On Reset to Code	Accuracy	Temperature Range	Package Description	Package Option	Branding
AD5680BRJZ-1500RL7	Zero	±64 LSB INL	−40°C to +105°C	8-Lead SOT-23	RJ-8	D3C
AD5680BRJZ-1REEL7	Zero	±64 LSB INL	−40°C to +105°C	8-Lead SOT-23	RJ-8	D3C
AD5680BRJZ-2500RL7	Midscale	±64 LSB INL	−40°C to +105°C	8-Lead SOT-23	RJ-8	D3D
AD5680BRJZ-2REEL7	Midscale	±64 LSB INL	−40°C to +105°C	8-Lead SOT-23	RJ-8	D3D
AD5680BCPZ-1500RL7	Zero	±64 LSB INL	−40°C to +105°C	8-Lead LFCSP	CP-8-15	DLN
AD5680BCPZ-1RL7	Zero	±64 LSB INL	−40°C to +105°C	8-Lead LFCSP	CP-8-15	DLN
AD5680BCPZ-2500RL7	Midscale	±64 LSB INL	−40°C to +105°C	8-Lead LFCSP	CP-8-15	DLP
AD5680BCPZ-2RL7	Midscale	±64 LSB INL	−40°C to +105°C	8-Lead LFCSP	CP-8-15	DLP
EVAL-AD5680DBZ				Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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