Datasheet

Power Management IC for Cell phone・Smart Phone

Power Management IC for Near Field Communication LSI

BD7602GUL

Summary

BD7602GUL is a Power Management IC for mobile device with NFC IC.
Each LDO output is controlled by 2 line serial interface which supports I2C Bus protocol.
This helps to save space to integrate all PMIC for NFC IC.

Features

- Low current consumption 10μA (Typ)
- 2 Channel LDO
- 2.7V UVLO detection
- 1 Channel GPO
- Thermal Shut Down function
- 2 line serial interface which supports I2C bus protocol.

USE

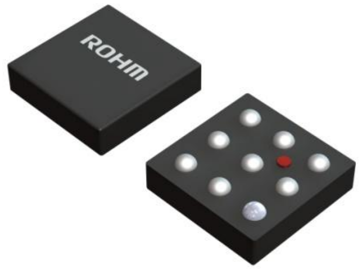
- Smart Phones
- Cell Phones
- Mobile device which has NFC IC

Key Parameters

- Input voltage range : 2.7V ～ 5.5V
- Output voltage(LDO1) : 3.0V(Typ)
- Output voltage range(LDO2) : 2.8V ～ 3.3V
- Output current(LDO1) : 100mA(Max)
- Output current(LDO2) : 150mA(Max)
- VBAT operating current : 10μA (Typ)
- Operating temperature range : -35°C ～ +85°C

PACKAGE

	W (Typ) x D (Typ) x H (Max)
VCSP50L1C	1.60mm x 1.60mm x 0.57mm



VCSP50L1C

Application Schematic

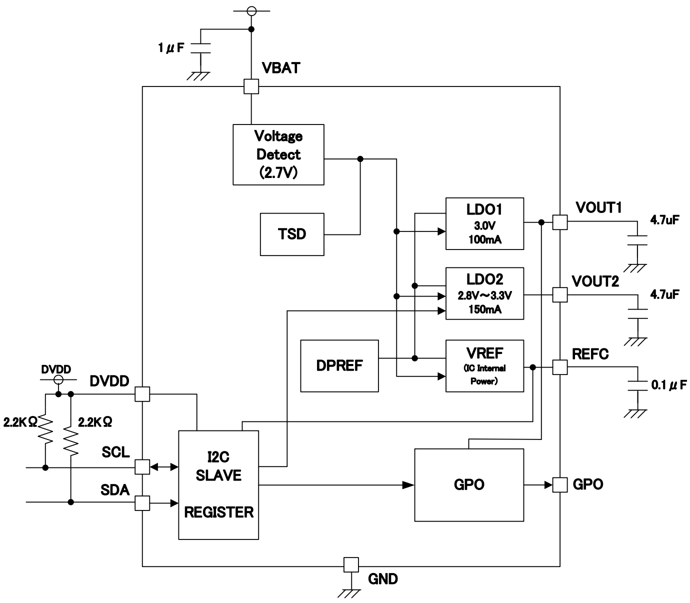


Figure 1. Application schematic.

○Product structure : Silicon monolithic integrated circuit. ○This product has no designed protection against radioactive rays.

Pinout Diagram

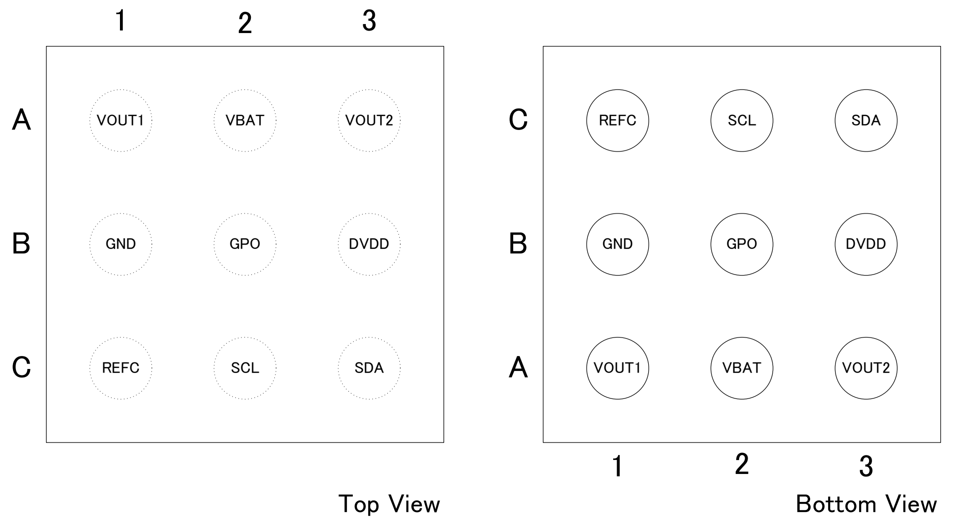


Figure 2. Pinout Diagram

Pin Descriptions

Terminal Number	Name	Function	Diode	
			+side	-side
SiA1	VOUT1	LDO1 OUTPUT	VBAT	GND
A2	VBAT	POWER Supply	-	GND
A3	VOUT2	LDO2 OUTPUT	VBAT	GND
B1	GND	Ground	VBAT	-
B2	GPO	GPO OUTPUT	-	GND
B3	DVDD	I2C Serial Interface I/O Power supply	-	GND
C1	REFC	Power for logic circuit.	VBAT	GND
C2	SCL	I2C serial interface CLK input	DVDD	GND
C3	SDA	I2C serial interface DATA inout	DVDD	GND

IC Block Diagram

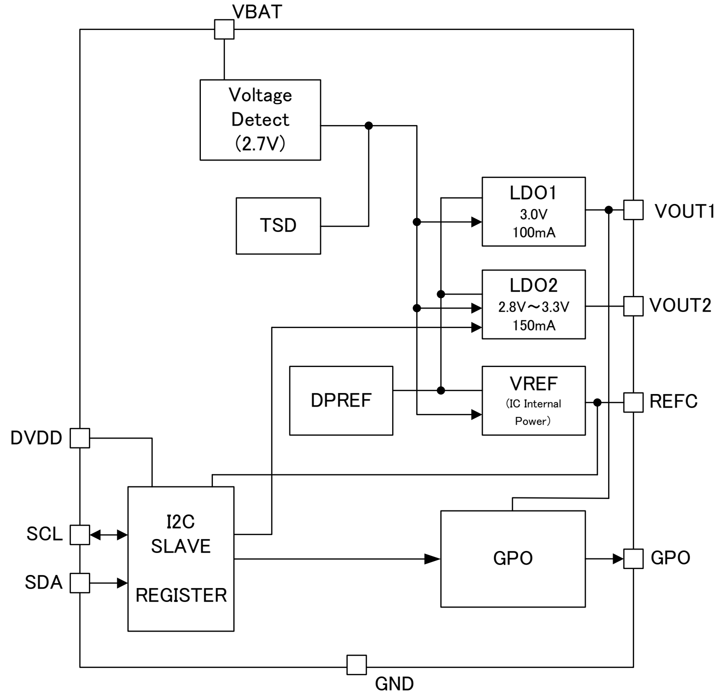


Figure 3. Block Diagram

Block Explanation

The output voltage for LDO1 is 3V (Typ) with an output current capability of 100mA (Max). UVLO Function is released when the IC starts by turning the power ON (VBAT).
LDO1 turns OFF when UVLO function is enabled.
I2C controller can also be used to turn off the IC. When LDO1 turns off, VOUT1 automatically connects with 100Ω discharge resistance.
VOUT1 needs 4.7uF external capacitor.

LDO2 has an adjustable output voltage from 2.8V to 3.3V.The initial value is 3V (Typ) with an output current capability of 150mA (Max). UVLO Function is released when the IC starts by turning the power ON (VBAT).
LDO2 turns OFF when UVLO function is enabled.
I2C Controller is used to adjust output voltage from 2.8V to 3.3V (8steps). It is also used to turn off the IC.
When LDO2 turns off, VOUT2 automatically connects with 100Ω discharge resistance.
VOUT2 needs 4.7uF external capacitor.

GPO is a logic output pin from register and could be used as enable or disable signal. The register can also set its output to CMOS type or NMOS type with an output current capability of 3mA.
Initial condition of GPO is disabled or in HI-Z state.
Maximum pull up voltage during NMOS output is equal to V_{BAT}

I2C SLAVE REGISTER is the function for I2C serial interface. Input voltage level is DVDD.

Voltage Detect for VBAT UVLO is 2.7V (Typ). When UVLO is detected, registers are reset.
Also at this time VREF, LDO1 and LDO2 outputs turn off.

VREF is equal to 2.5V (Typ). It powers the internal circuit and cannot be used externally. UVLO Function is released when the IC starts by turning power ON (VBAT). When UVLO function is detected, IC turns off.
REFC needs 0.1uF external capacitor.

DPREF is reference voltage for LDO VREF and Voltage Detect.

TSD is for thermal shut down function. This prevents damaging and breaking of IC. When IC‘s internal temperature rise up to a certain temperature, LDO1 and LDO2 are automatically turned off. When temperature goes down, LDO1 and LDO2 automatically return to its normal operation.
In this case, register doesn’t need to be reset.

Absolute Maximum Rating(s) (Ta = 25°C)

Parameter	Symbol	Value	Unit
Power Supply (VBAT)	V_{INVBAT}	-0.3 ～ +7.0	V
Power Supply (DVDD)	V_{INDVDD}	-0.3 ～ +7.0	V
Power Dissipation	Pd	0.66 (Note 1)	W
Operating Temperature Range	Topr	-35 ～ +85	°C
Storage Temperature	Tstg	-55 ～+150	°C
Junction Temperature	Tjmax	150	°C
Other Pin Voltage	V_{OTH}	-0.3 ～ +7.0	V

(Note 1) Derate by 5.2mW/℃when operating above Ta=25℃. (Mounted on a ROHM specification board.50mm x 58mm)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Condition (Ta= -35°C to +85°C)

Parameter	Symbol	MIN	TYP	MAC	UNIT
Power Supply(VBAT)	V_{BAT}	2.7	3.6	5.5	V
Power Supply(DVDD)	V_{DVDD}	1.70	1.80	3.50	V

Electrical Characteristic (Unless otherwise specified, V_{BAT}=3.6V, V_{DVDD}=1.8V, Ta=25°C)

Parameter	Symbol	MIN	TYP	MAX	UNIT	Condition
Circuit Current						
VBAT Circuit Current(VBAT=3.6V)	I_{CCBAT}	-	10	18	μA	LDO1,2: No Load
VBAT Circuit Current(VBAT=3.1V)	I_{CCBAT}		9.5	15	μA	LDO1,2: No Load
DVDD Circuit Current	I_{CCDVDD}	-	0	1	μA	
Voltage Detector						
Detect Voltage	V_{UVLO}	2.64	2.70	2.76	V	Down Sweep
Detect Voltage Hysteresis	$V_{UVLOHYS}$	50	100	150	mV	
VREF Output Voltage	V_{OREF}	2.45	2.50	2.55	V	
LDO1						
Output Voltage	V_{OUT1}	2.94	3.00	3.06	V	I_{OUT1}= 50mA
Output Max Current	$I_{OUT1MAX}$	100	-	-	mA	
Line Regulation	ΔV_{IS1}	-	2	-	mV	V_{BAT}=3.3～4.5V, I_{OUT1}= 50mA
Load Regulation	ΔV_{LS1}	-	20	-	mV	I_{OUT1}= 1～100mA
PSRR	PSRR1	-	45	-	dB	V_{BAT}=4.2V+0.2Vpp, I_{OUT1}= 50mA fr=120Hz,BW=20～20kHz
Discharge Resistance	R_{DIS1}	-	100	-	Ω	V_{BAT}=2.5V
LDO2						
Output Voltage	V_{OUT2}	2.94	3.00	3.06	V	I_{OUT1}= 50mA
Variable Output Voltage	V_{O2RNG}	2.80	-	3.30	V	
Output Max Current	$I_{OUT2MAX}$	150	-	-	mA	
Line Regulation	ΔV_{IS2}	-	2	-	mV	V_{BAT}=V_{OUT2}+0.3V～4.5V, I_{OUT2}= 50mA
Load Regulation	ΔV_{LS2}	-	20	-	mV	I_{OUT2}= 1～150mA
PSRR	PSRR2	-	45	-	dB	V_{BAT}=4.2V+0.2Vpp, I_{OUT2}= 50mA fr=120Hz,BW=20～20kHz
Discharge resistance	R_{DIS2}	-	100	-	Ω	V_{BAT}=2.5V
GPO						
Output H Level	V_{OHGPO}	0.8× V_{OUT1}	-	0.3+ V_{OUT1}	V	$I_{SINKGPO}$= 3mA
Output L Level	V_{OLGPO}	-0.3	-	0.4	V	$I_{SOURCEGPO}$= 3mA
NMOS output pulled up max voltage	V_{MXGPON}	-	-	V_{BAT}	V	
NMOS output L level	V_{OLGPON}	-0.3	-	0.4	V	$I_{SOURCEGPO}$= 3mA
NMOS output leak current	I_{LKGPON}	-1	0	1	μA	Terminal voltage=V_{OUT1}, 0V
I2Cserial interface						
Input H Level (SCL, SDA)	V_{IH}	0.75× V_{DVDD}	-	0.3+ V_{DVDD}	V	
Input L Level (SCL, SDA)	V_{IL}	-0.3	-	0.25× V_{DVDD}	V	
Input Leak Current (SCL, SDA)	I_{LK}	-1	0	1	μA	Terminal voltage=V_{DVDD}, 0V
Output L Level (SDA)	V_{OL}	-0.3	-	0.4	V	I_{SOURCE}= 6mA

Electrical Characteristic (Unless otherwise specified, V_{BAT}=3.6V, V_{DVDD}=1.8V, Ta=-35～85°C(Note2))

Parameter	Symbol	MIN	TYP	MAX	UNIT	Condition
Circuit Current						
VBAT Circuit Current(VBAT=3.6V)	I_{CCBAT}	-	10	18	µA	LDO1,2: No Load
VBAT Circuit Current(VBAT=3.1V)	I_{CCBAT}	-	9.5	15	µA	LDO1,2: No Load
DVDD Circuit Current	I_{CCDVDD}	-	0	1	µA	
Voltage Detector						
Detect Voltage	V_{UVLO}	2.6	2.7	2.8	V	Down Sweep
Detect Voltage Hysteresis	$V_{UVLOHYS}$	50	100	150	mV	
VREF Output Voltage	V_{OREF}	2.4	2.5	2.6	V	
LDO1						
Output Voltage	V_{OUT1}	2.88	3	3.12	V	I_{OUT1}= 50mA
Output Max Current	$I_{OUT1MAX}$	100	-	-	mA	
Line Regulation	ΔV_{IS1}	-	2	-	mV	V_{BAT}=3.3～4.5V, I_{OUT1}= 50mA
Load Regulation	ΔV_{LS1}	-	20	-	mV	I_{OUT1}= 1～100mA
PSRR	PSRR1	-	45	-	dB	V_{BAT}=4.2V+0.2Vpp, I_{OUT1}= 50mA fr=120Hz,BW=20～20kHz
Discharge Resistance	R_{DIS1}	-	100	-	Ω	V_{BAT}=2.5V
LDO2						
Output Voltage	V_{OUT2}	2.88	3	3.12	V	I_{OUT1}= 50mA
Variable Output Voltage	V_{O2RNG}	2.8	-	3.3	V	
Output Max Current	$I_{OUT2MAX}$	150	-	-	mA	
Line Regulation	ΔV_{IS2}	-	2	-	mV	V_{BAT}=V_{OUT2}+0.3V～4.5V, I_{OUT2}= 50mA
Load Regulation	ΔV_{LS2}	-	20	-	mV	I_{OUT2}= 1～150mA
PSRR	PSRR2	-	45	-	dB	V_{BAT}=4.2V+0.2Vpp, I_{OUT2}= 50mA fr=120Hz,BW=20～20kHz
Discharge resistance	R_{DIS2}	-	100	-	Ω	V_{BAT}=2.5V
GPO						
Output H Level	V_{OHGPO}	0.8× V_{OUT1}	-	0.3+ V_{OUT1}	V	$I_{SINKGPO}$= 3mA
Output L Level	V_{OLGPO}	-0.3	-	0.4	V	$I_{SOURCEGPO}$= 3mA
NMOS output pulled up max voltage	V_{MXGPON}	-	-	V_{BAT}	V	
NMOS output L level	V_{OLGPON}	-0.3	-	0.4	V	$I_{SOURCEGPO}$= 3mA
NMOS output leak current	I_{LKGPON}	-1	0	1	µA	Terminal voltage=V_{OUT1}, 0V
I2Cserial interface						
Input H Level (SCL, SDA)	V_{IH}	0.75× V_{DVDD}	-	0.3+ V_{DVDD}	V	
Input L Level (SCL, SDA)	V_{IL}	-0.3	-	0.25× V_{DVDD}	V	
Input Leak Current (SCL, SDA)	I_{LK}	-1	0	1	µA	Terminal voltage=V_{DVDD}, 0V
Output L Level (SDA)	V_{OL}	-0.3	-	0.4	V	I_{SOURCE}= 6mA

(Note2)：These are guaranteed by design engineering from -35℃ to 85℃.

Characteristic Data(Reference Data)

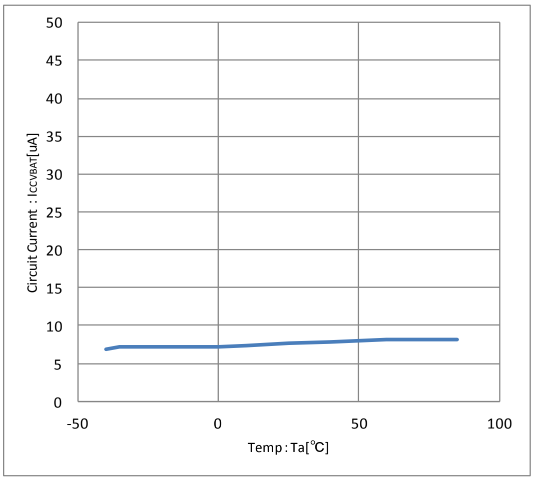


Figure 4. Circuit Current VS temperature
(VBAT=3.6V,Ta=-35℃~85℃)

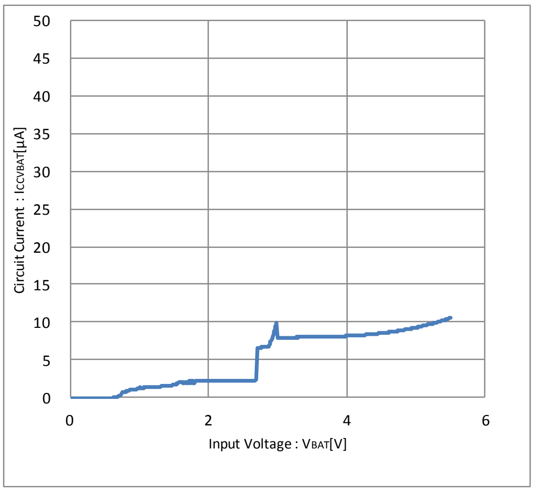


Figure 5. Input Current VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃)

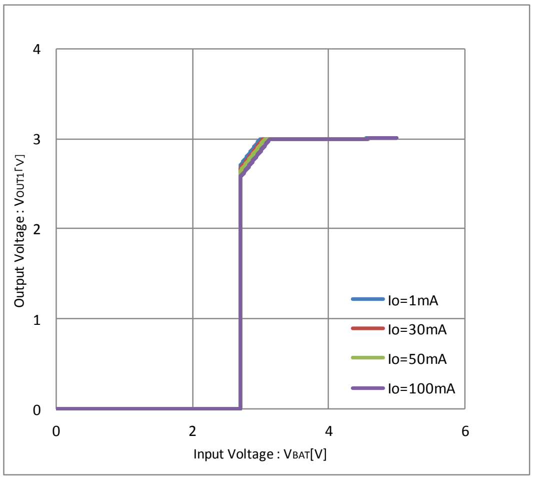


Figure 6. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃)

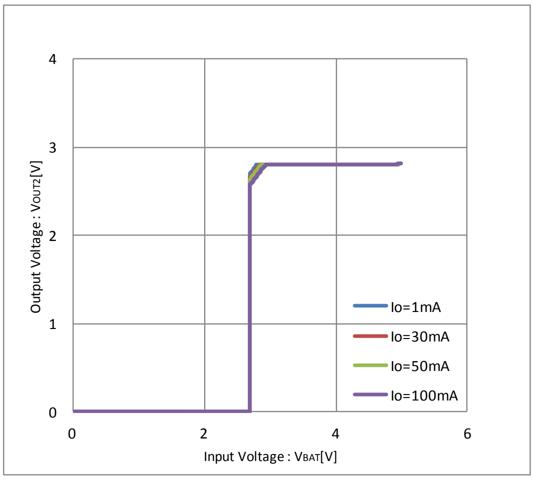


Figure 7. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃,Vout=2.8V)

Characteristic Data(Reference Data) -continuance

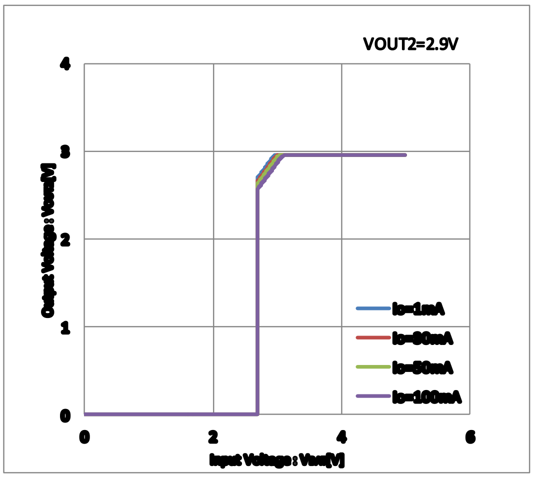


Figure 8. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃,Vout=2.9V)

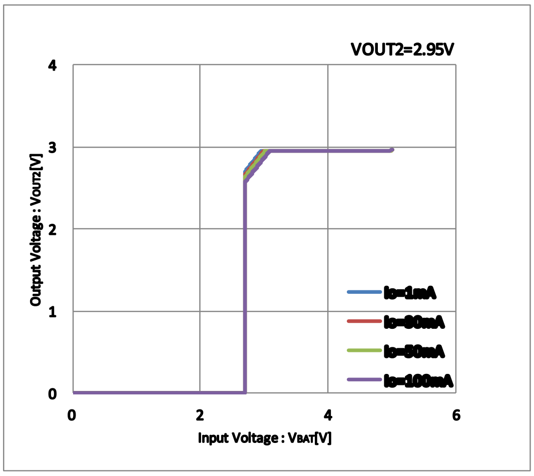


Figure 9. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃,Vout=2.95V)

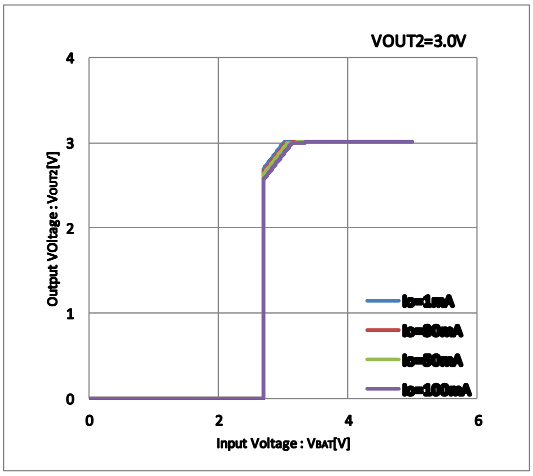


Figure 10. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃,Vout=3.0V)

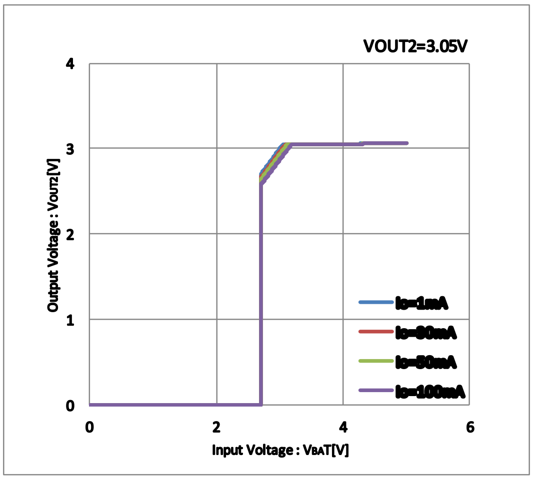


Figure 11. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃,Vout=3.05V)

Characteristic Data(Reference Data) -continuance

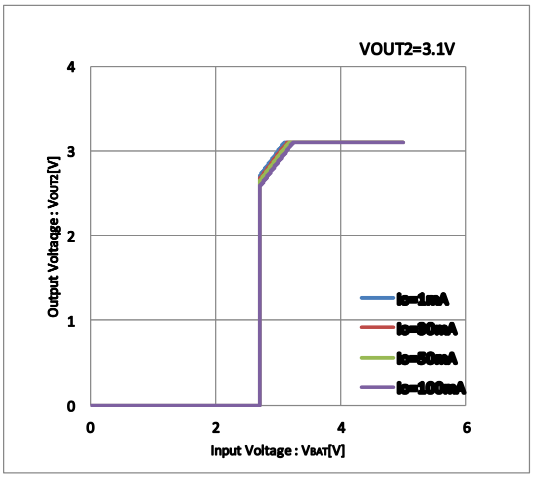


Figure 12. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃,Vout=3.1V)

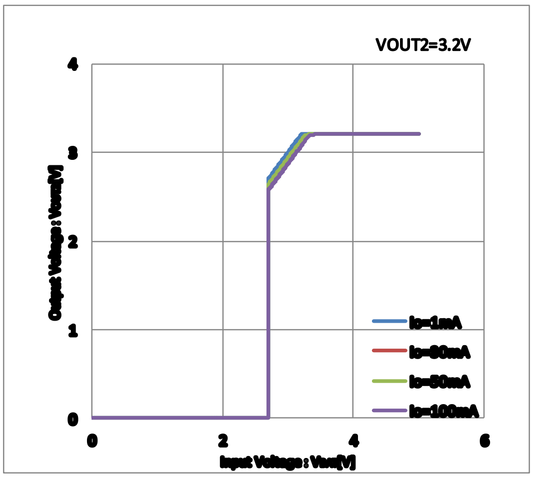


Figure 13. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃,Vout=3.2V)

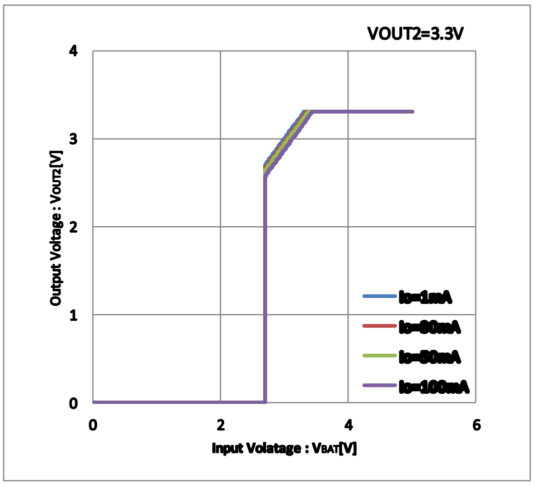


Figure 14. Output Voltage VS Input Voltage
(VBAT=0V~5.5V,Ta=25℃,Vout=3.3V)

Characteristic Data(Reference Data) -continuance

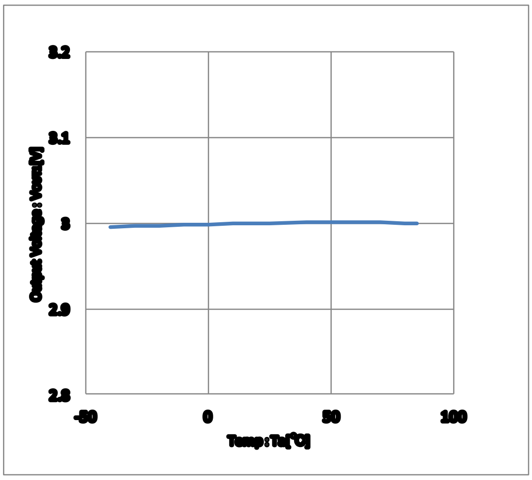


Figure 15. Output Voltage VS Temperature
(VBAT=3.6V,Ta=25℃,Io=1mA)

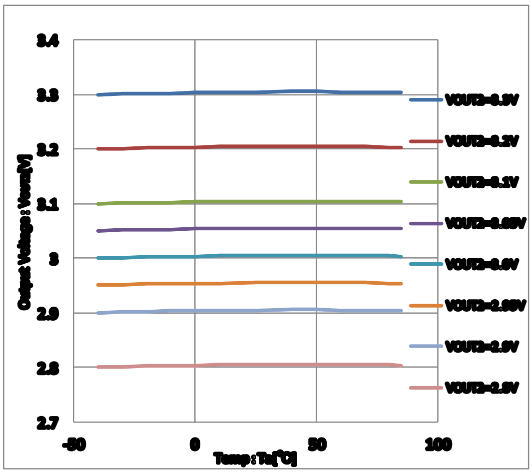


Figure 16. Output Voltage VS Temperature
(VBAT=3.6V,Ta=25℃,Io=1mA)

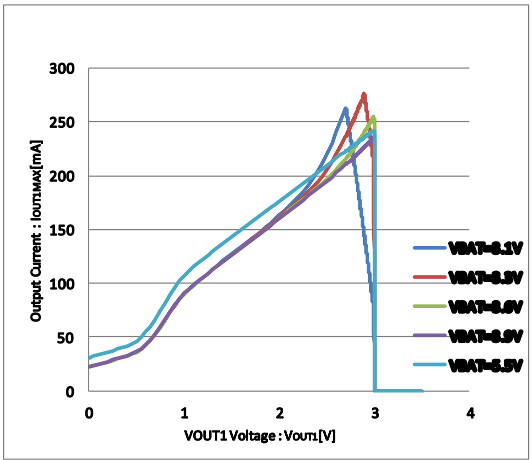


Figure 17. Output Current VS VOUT1 Voltage
(VBAT=3.6V,Ta=25℃)

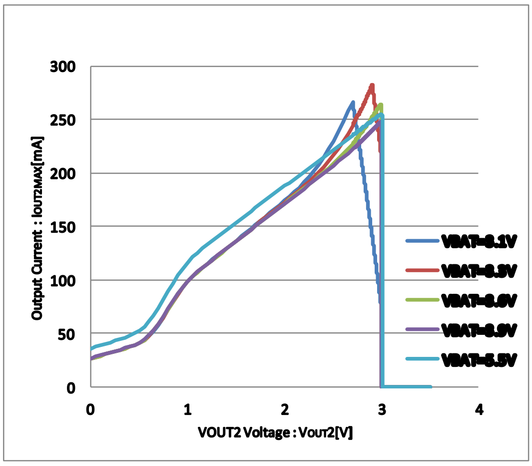


Figure 18. Output Current VS VOUT2 Voltage
(VBAT=3.6V,Ta=25℃,VOUT2=3.0V)

Characteristic Data(Reference Data) -continuance

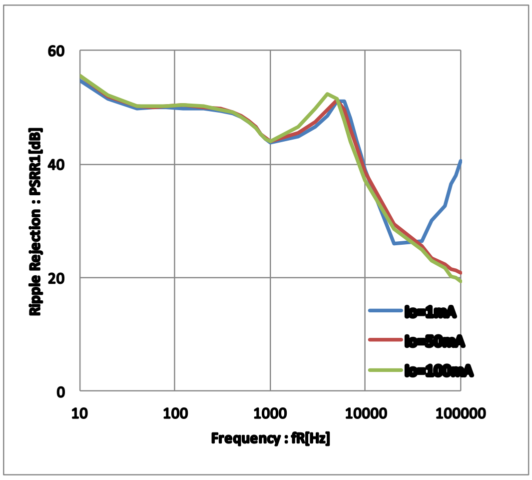


Figure 19. Ripple Rejection VS Frequency
(VBAT=4.2V+0.2Vpp,Cout=4.7μF,fR=120Hz,Ta=25℃)

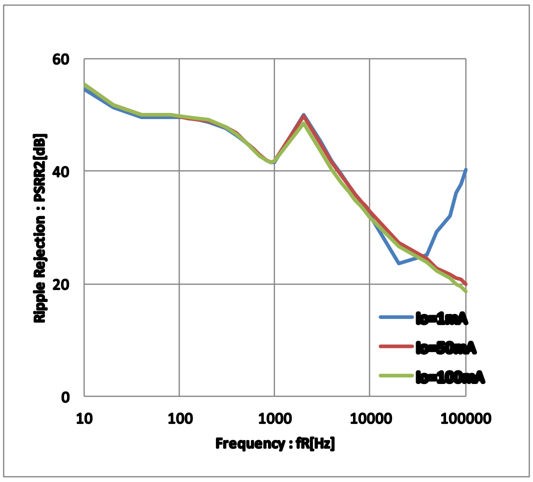


Figure 20. Ripple Rejection VS Frequency
(VBAT=4.2V+0.2Vpp,Cout=4.7μF,fR=120Hz,Ta=25℃)

Characteristic Data(Reference Data) -continuance

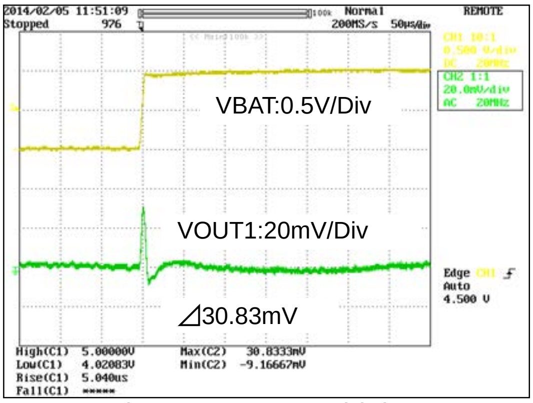


Figure 21. VBAT Response(Rise)
(VBAT=4V→5V,Cout=4.7μF,Ta=25℃,Tf=0.5μs)

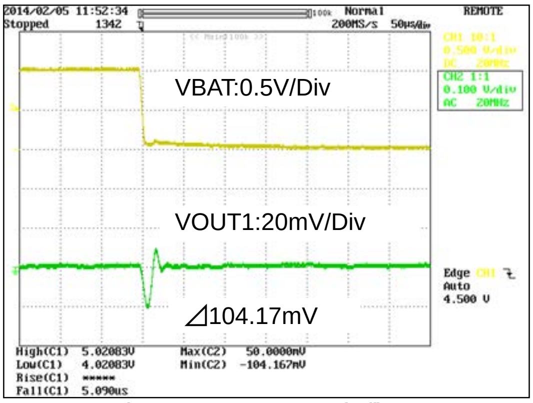


Figure 22. VBAT Response(Fall)
(VBAT=5V→4V,Cout=4.7μF,Ta=25℃,Tf=0.5μs)

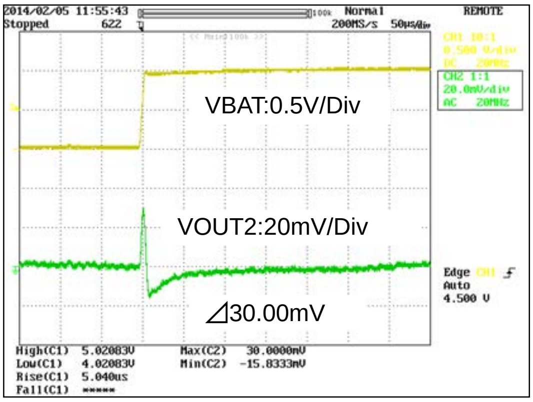


Figure 23. VBAT Response(Rise)
(VBAT=4V→5V,Cout=4.7μF,Ta=25℃,Tf=0.5μs)

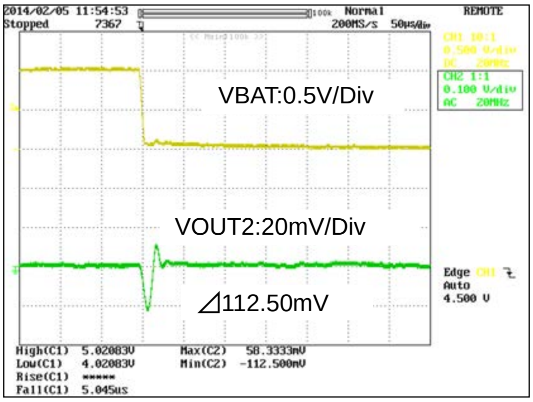


Figure 24. VBAT Response(Fall)
(VBAT=5V→4V,Cout=4.7μF,Ta=25℃,Tf=0.5μs)

Characteristic Data(Reference Data) -continuance

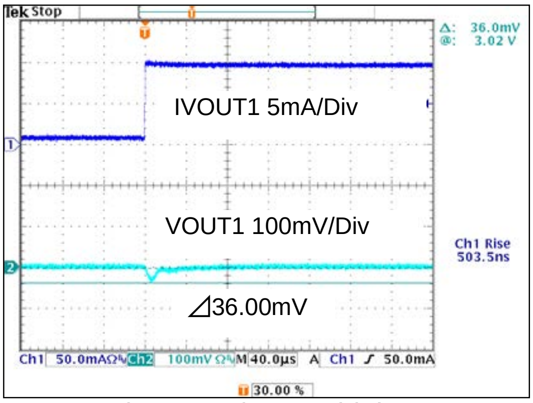


Figure 25. Load Response(Rise)
(VBAT=3.6V,Cout=4.7μF,Ta=25℃,Iout=1mA→10mA,Tr=0.5μs)

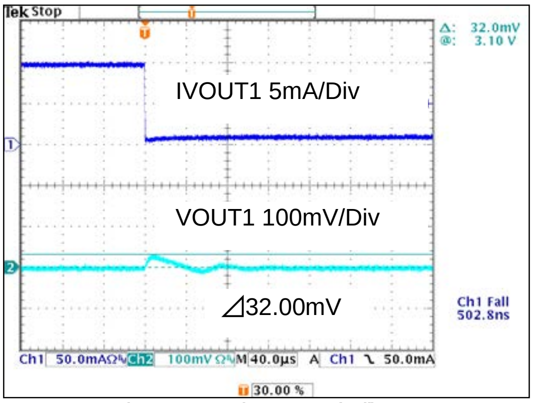


Figure 26. Load Response(Fall)
(VBAT=3.6V,Cout=4.7μF,Ta=25℃,Iout=10mA→1mA,Tf=0.5μs)

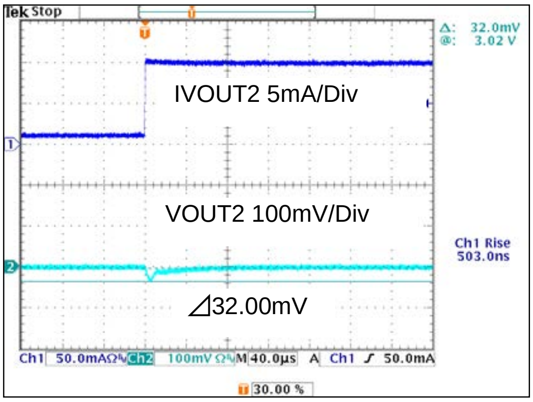


Figure 27. Load Response(Rise)
(VBAT=3.6V,Cout=4.7μF,Ta=25℃,Iout=1mA→10mA,Tr=0.5μs)

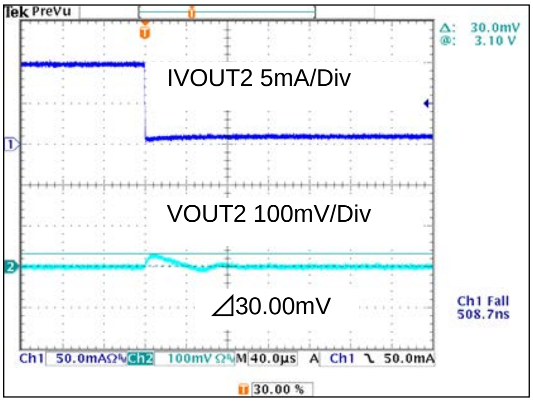


Figure 28. Load Response(Fall)
(VBAT=3.6V,Cout=4.7μF,Ta=25℃,Iout=10mA→1mA,Tf=0.5μs)

Characteristic Data(Reference Data) -continuance

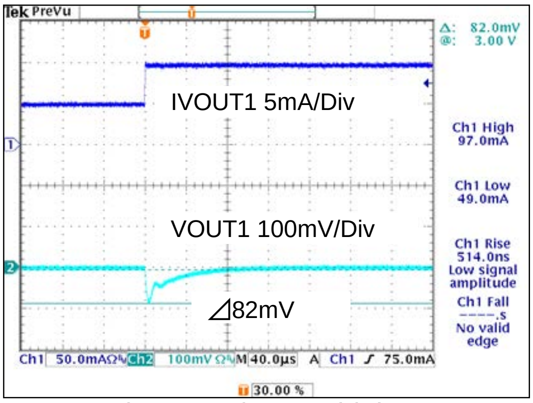


Figure 29. Load Response(Rise)
(VBAT=3.6V,Cout=4.7 μ Ta=25℃,F,Iout=50mA→100mA,Tr=0.5 μ s)

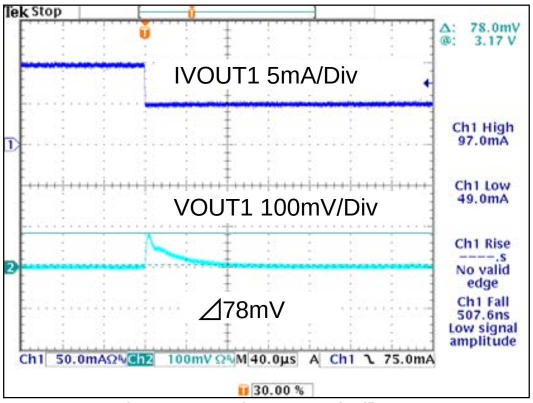


Figure 30. Load Response(Fall)
(VBAT=3.6V,Cout=4.7 μ F,Ta=25℃,Iout=100mA→50mA,Tf=0.5 μ s)

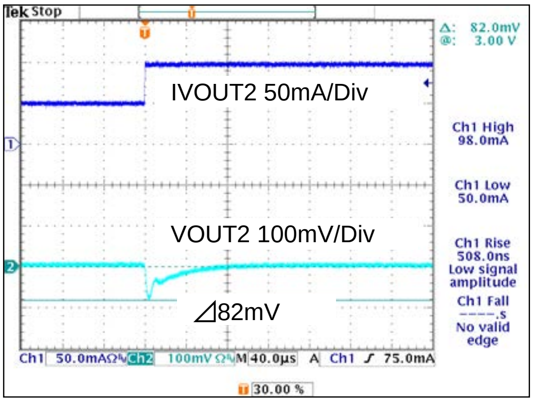


Figure 31. Load Response(Rise)
(VBAT=3.6V,Cout=4.7 μ F,Ta=25℃,Iout=50mA→100mA,Tr=0.5 μ s)

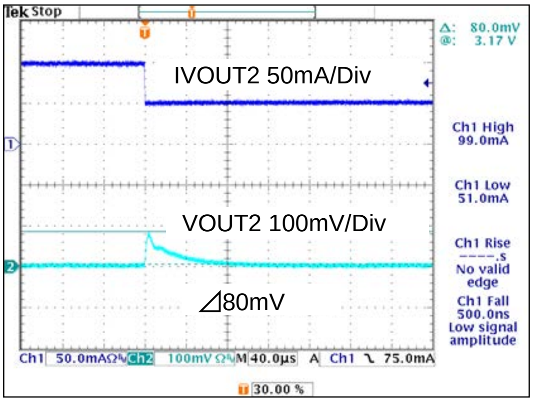


Figure 32. Load Response(Fall)
(VBAT=3.6V,Cout=4.7 μ F,Ta=25℃,Iout=100mA→50mA,Tf=0.5 μ s)

Characteristic Data(Reference Data) -continuance

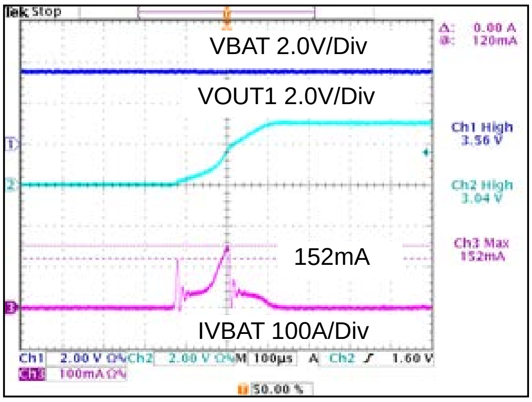


Figure 33. Rush Current
(VBAT=3.6V, LDO_EN=L→H ,Cout=4.7 μ F,Ta=25℃)

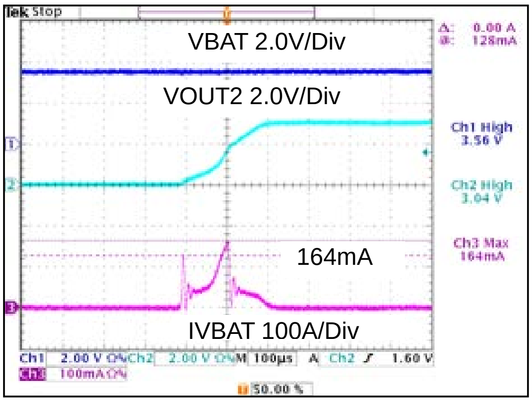


Figure 34. Rush Current
(VBAT=3.6V,LDO_EN=L→H Cout=4.7 μ F,Ta=25℃)

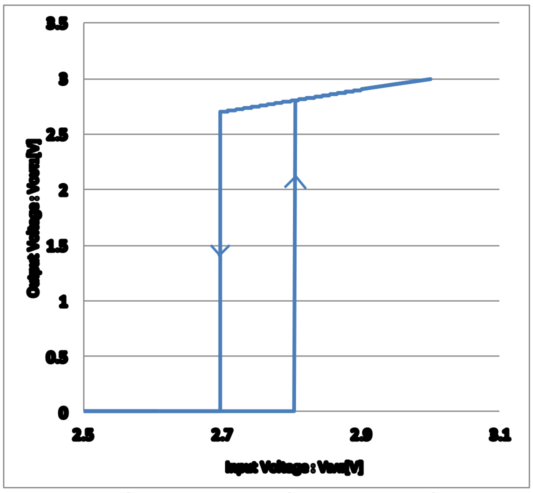


Figure 35. Output Voltage VS Input Voltage
(VBAT=3.6V,Ta=25℃)

Characteristic Data(Reference Data) -continuance

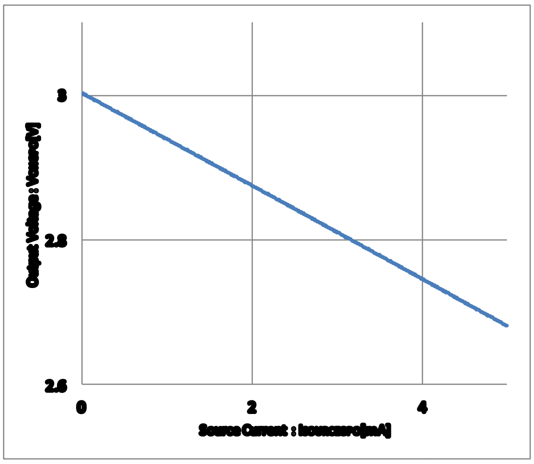


Figure 36. Output Voltage VS Source Current(CMOS Output)
(VBAT=3.6V,Ta=25℃)

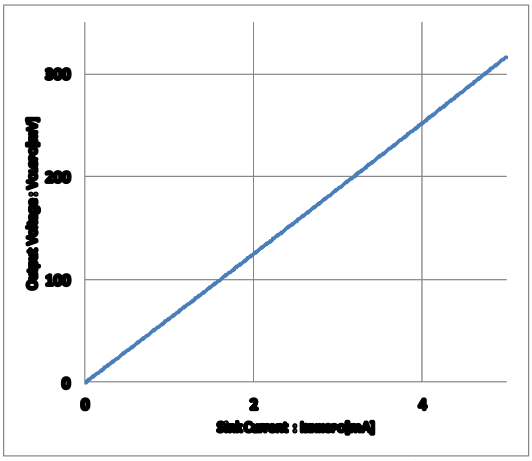


Figure 37. Output Voltage VS Sink Current(CMOS Output)
(VBAT=3.6V,Ta=25℃)

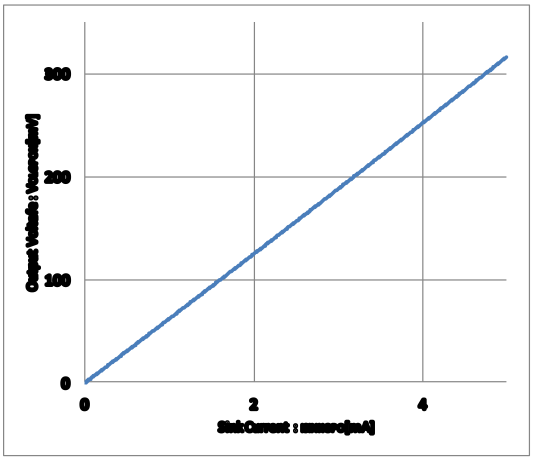


Figure 38. Output Voltage VS Sink Current(NMOS Output)
(VBAT=3.6V,Ta=25℃)

I2C Interface Timing Specification

BD7602GUL has 2 line serial interface which supports I2C Bus protocol.

Table 1. I2C slave address

A7	A6	A5	A4	A3	A2	A1	R/W
0	0	1	1	1	1	0	1/0

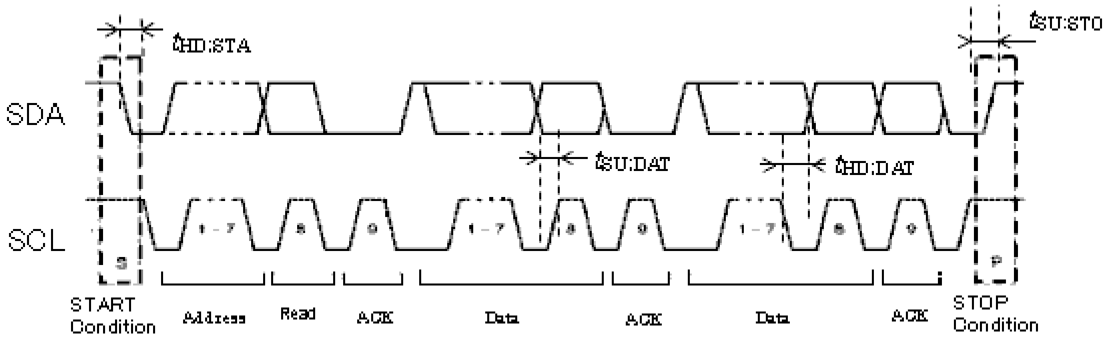


Figure 39. I2C interface Timing

(Unless otherwise specified, V_{BAT}=3.6V, V_{DVDD}=1.8V, Ta=25°C)

Parameter	Symbol	MIN	TYP	MAX	UNIT	Condition
SCL Clock Frequency	f_{SCL}	-	-	400	kHz	
START Hold time	$t_{HD:STA}$	0.6	-	-	µs	
SCL of "L" time	t_{LOW}	1.3	-	-	µs	
SCL of "H" time	t_{HIGH}	0.6	-	-	µs	
Data input hold time	$t_{HD:DAT}$	0.0	-	-	ns	
Data input setup time	$t_{SU:DAT}$	100	-	-	ns	
STOP condition setup time	$t_{SU:STO}$	0.6	-	-	µs	

Register Map

Table 2.Register Map

Address	Register name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0
00h	ICREV	R	09h	-	-	DEVICE [2:0]			CHIPREV [2:0]		
01h	LDOCNT	R/W	03h	-	-	-		-	-	LDO2_EN	LDO1_EN
02h	LDO2ADJ	R/W	03h	-	-	-	-	-	LDO2_VOUT [2:0]		
03h	GPOCNT	R/W	00h	-	-	-	-	-	-	GPO_EN	REG_GPO
04h	GPOMODE	R/W	00h	-	-	-	-	-	-	Reserved	GPO_SEL

Register Detail

Address	Register name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0
00h	ICREV	R	09h	-	-	DEVICE [2:0]			CHIPREV [2:0]		

Bit[5:3]: DEVICE [2:0] DEVICE Name Notification
001: BD7602GUL (Initial Value)
Bit[2:0]: CHIPREV [2:0] CHIP Revision Notification
001: DS1 (Initial Value)

Address	Register name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0
01h	LDOCNT	R/W	03h	-	-	-	-	-	-	LDO2_EN	LDO1_EN

Bit[1]: LDO2_EN LDO2 Output ON/OFF Control
0: OFF
1: ON (Initial Value)
Bit[0]: LDO1_EN LDO1 Output ON/OFF Control
0: OFF
1: ON (Initial Value)

Address	Register name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0
02h	LDO2ADJ	R/W	03h	-	-	-	-	-	LDO2_VOUT [2:0]		

Bit[2:0]: LDO2_VOUT [2:0] LDO2 Output Voltage set “
000: 2.80V
001: 2.90V
010: 2.95V
011: 3.00V (Initial Value)
100: 3.05V
101: 3.10V
110: 3.20V
111: 3.30V

Address	Register name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0
03h	GPOCNT	R/W	00h	-	-	-	-	-	-	GPO_EN	REG_GPO

Bit[1]: GPO_EN GPO Enable/Disable Control
0: Disable (Hi-Z) (Initial Value)
1: Enable (Output Type and Output Voltage follow data of address 04h)
Bit[0]: REG_GPO GPO Output Control
0: Low Output (Initial Value)
1: High Output (CMOS Output), Hi-Z (NMOS Output)

Address	Register name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0
04h	GPOMODE	R/W	00h	-	-	-	-	-	-	Reserved	GPO_SEL

Bit[1]: Reserved Reserved Register （no any function）
In case of writing address 04h, note to set this bit to “0”.

Bit[0]: GPO_SEL GPO Output Type
0: CMOS Output (Initial Value)
1: NMOS Output

Timing Chart

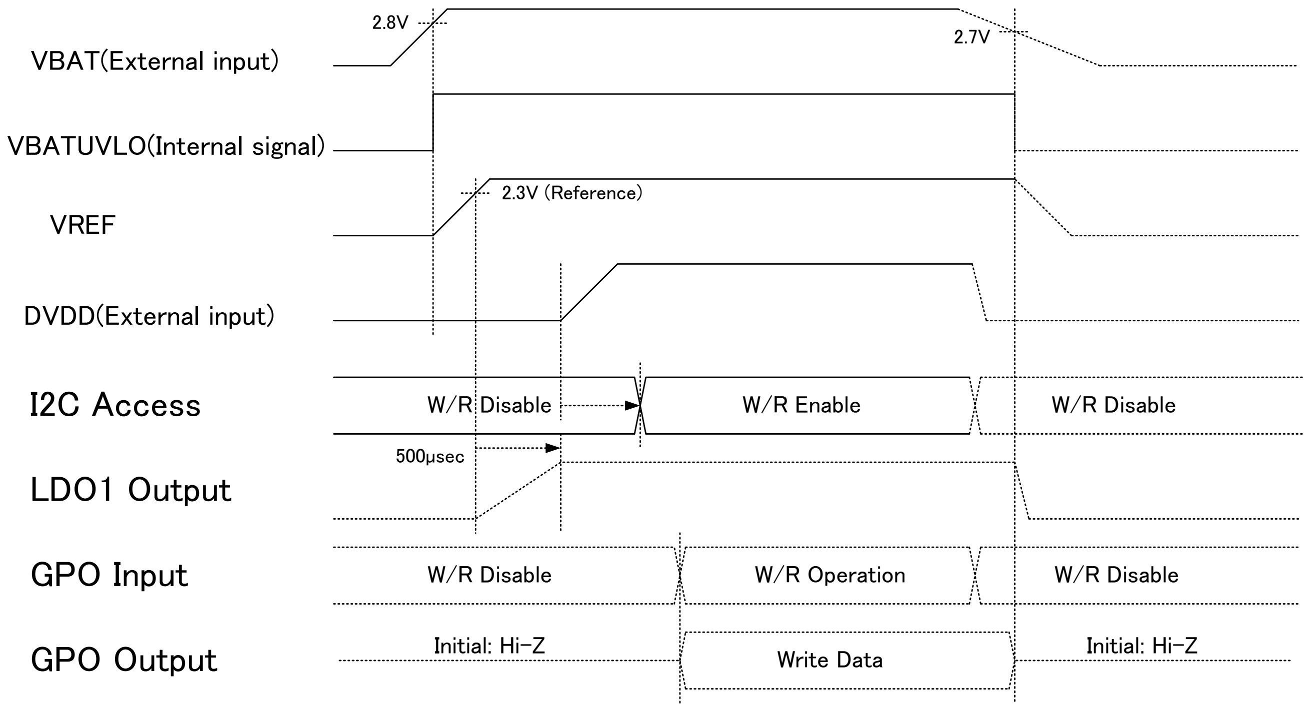


Figure 40. Timing Chart

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Thermal Consideration**
   Should by any chance the power dissipation (Pd) rating be exceeded, the rise in temperature of the chip may result in deterioration of its properties. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 1.64mm x 1.64mm x 0.57mm glass epoxy board. In case the absolute maximum rating has been exceeded, increase the board size and copper area to prevent exceeding the Pd rating.

5. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

6. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

10. Unused Input Terminals
Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

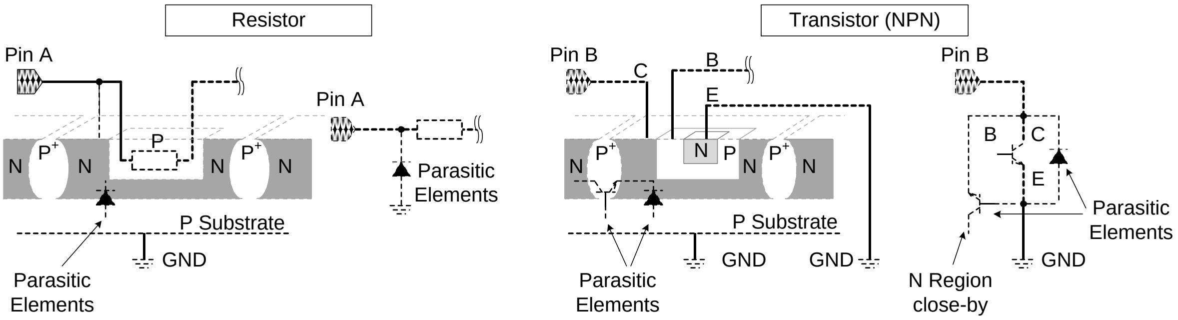


Figure 41.Example of monolithic IC structure

12. Ceramic Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Save Operating Range
When using this IC, set output transistor not to exceed absolute maximum range or ASO.

14. Thermal Shutdown Circuit(TSD)
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn off all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage

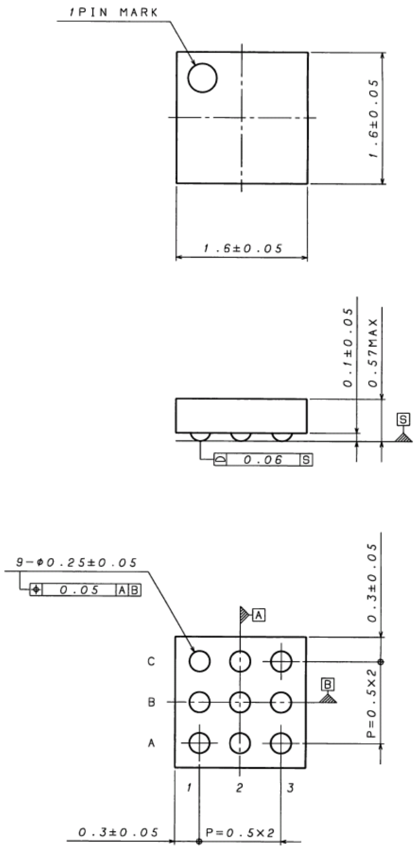
15. Over Current Protection circuit
Because output has an Over Current Protection (OCP) circuit that operates in accordance with the rated output capacity, IC is protected from breakage or possible damage when the load becomes shorted. This protection circuit is also effective in preventing damage to the IC in case of sudden and unexpected current surges only and not for its continuous protection.

Ordering Name information

B D 7 6 0 2 G U L - E 2

- Name of Product
- Package: GUL: VCSP50L1C
- Packing、forming specification: E2: reel type emboss taping

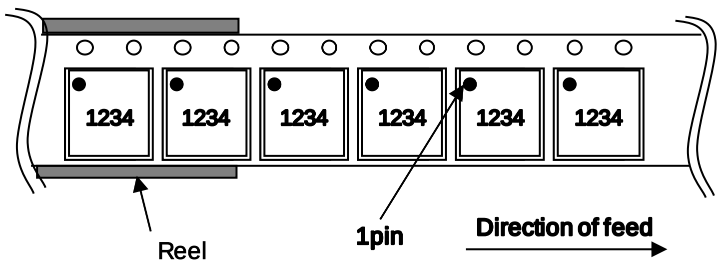
Package Dimensions



Unit: mm

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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