

DESCRIPTION

The MP44014 is a boundary conduction mode PFC controller that provides simple, high-performance, active power factor correction using minimal external components.

The output voltage is regulated accurately by a high-performance voltage mode amplifier with an accurate internal voltage reference.

The precise, adjustable output over-voltage protection greatly enhances system reliability.

The on-chip R/C filter on the current sense pin can potentially eliminate the external R/C filter.

The extremely low start-up current, quiescent current, and disable function reduces power consumption, resulting in excellent efficiency performance.

The MP44014 is available in a SOIC-8 package.

FEATURES

- Boundary Conduction Mode PFC Controller for Pre-Regulator
- Zero-Crossing Compensation to Minimum THD of the AC Input Current
- Precise Adjustable Output Over-Voltage Protection
- Ultra-Low (15 μ A) Start-Up Current
- Low Quiescent Current (0.46 μ A) at OVP Condition
- On-Chip Filter on Current Sense Pin
- Disable Function on ZCS Pin
- -750mA/+800mA Peak Gate Drive Current
- Available in SOIC-8 Packages

APPLICATIONS

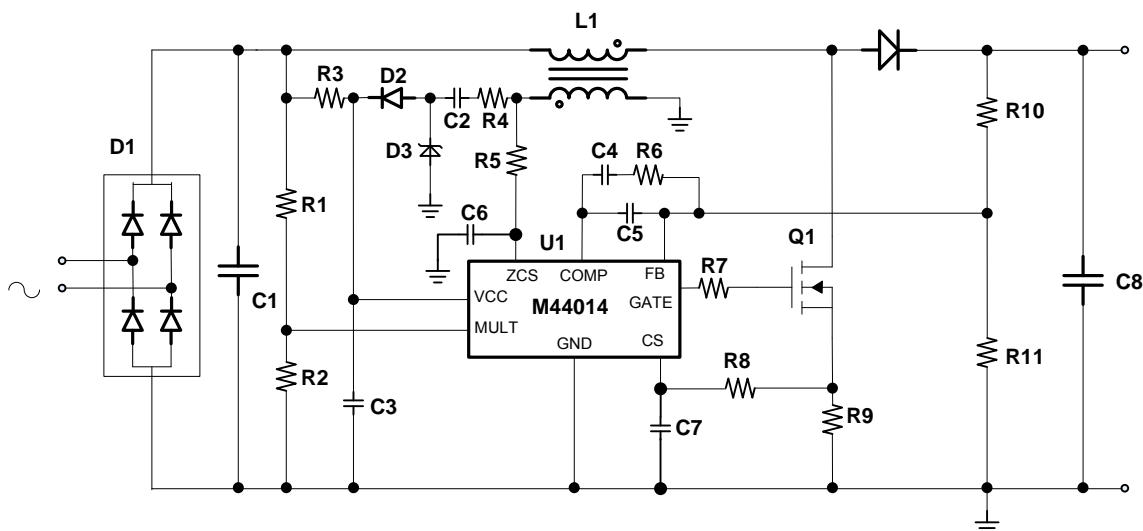
- Offline Adaptors
- Electronic Ballast
- LLC Front End
- Other PFC Pre-Regulators

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Other patents pending.

TYPICAL APPLICATION



ORDERING INFORMATION

| Part Number | Package | Top Marking |
|-------------|---------|-------------|
| MP44014GS* | SOIC-8 | See Below |

* For Tape & Reel, add suffix -Z (e.g. MP44014GS-Z)

TOP MARKING

MP44014
LLLLLLLLL
MPSYWW

MP44014: Part number
 LLLLLLLL: Lot number
 MPS: MPS prefix
 Y: Year code
 WW: Week code

PACKAGE REFERENCE



Absolute Maximum Ratings ⁽¹⁾

Supply voltage (VCC) -0.5V to self limit
 Analog inputs and outputs ⁽²⁾ -0.3V to 6.5V
 ZCS max. current -2.5mA to 10mA
 Continuous power dissipation (T_A = +25°C) ⁽³⁾
 SOIC-8 1.4W
 Junction temperature 150°C
 Lead temperature (solder) 260°C
 Storage temperature -55°C to +150°C

Recommended Operating Conditions ⁽⁴⁾

Supply voltage (VCC) 13.4V to 22V
 Analog inputs and outputs -0.3V to 6.5V
 Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance ⁽⁵⁾ **θ_{JA}** **θ_{JC}**
 SOIC-8 90 45 ... °C/W

NOTES:

- Exceeding these ratings may damage the device.
- Except ZCS pin, which is self limited.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 15V$, $C_{GATE} = 1nF$, $T_J = -40^{\circ}C \sim +125^{\circ}C$, unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|----------------------------------|---------------------------------|--|-------|------|-------|---------|
| Supply Voltage | | | | | | |
| Operating range | V_{CC} | After turn on | 10.7 | | 21 | V |
| Turn-on threshold | V_{CC_on} | | 11 | 12.3 | 13.8 | V |
| Turn-off threshold | V_{CC_off} | | 8.7 | 9.8 | 10.8 | V |
| Hysteresis | V_{CC_hys} | | 2.1 | | 3 | V |
| Zener voltage | V_Z | $I_{IN} = 20mA$ | 22 | 25 | 29 | V |
| Supply Current | | | | | | |
| Start-up current | $I_{startup}$ | $V_{CC} = 11V$ | | 15 | 30 | μA |
| Quiescent current | I_q | No switch | | 2.5 | 3.2 | mA |
| Operating current | I_{cc} | $F_s = 70kHz$, $C_{LOAD} = 1nF$ | | 3.5 | 4.5 | mA |
| Quiescent current | I_q | During OVP (either static or dynamic) or $V_{FB} \leq 150mV$ | | 0.46 | 0.7 | mA |
| Multiplier | | | | | | |
| Input bias current | I_{MULT} | | | | -1 | μA |
| Linear operation range | V_{MULT} | | 0 | | 3 | V |
| Output max. slope | $\Delta V_{CS}/\Delta V_{MULT}$ | $V_{MULT} = 0 \sim 0.6V$ $V_{COMP} = \text{upper clamp}$ | 1.60 | 1.90 | | V/V |
| Gain ⁽⁶⁾ | K | $V_{MULT} = 1V$, $V_{COMP} = 4V$, $T_J = 25^{\circ}C$ | 0.5 | 0.6 | 0.7 | 1/V |
| Error Amplifier | | | | | | |
| Feedback voltage | V_{FB} | $T_J = 25^{\circ}C$ | 2.465 | 2.5 | 2.535 | V |
| Feedback voltage line regulation | V_{FB_LR} | $V_{CC} = 10.7V \text{ to } 22V$ | | 2 | 5 | mV |
| Feedback bias current | I_{FB} | $V_{FB} = 2.6V$ | | | 1 | μA |
| Source current | I_{COMP_source} | $V_{COMP} = 4V$, $V_{FB} = 2.4V$, $T_J = 25^{\circ}C$ | -2.7 | -4.7 | -6.9 | mA |
| Sink current | I_{COMP_sink} | $V_{COMP} = 4V$, $V_{FB} = 2.6V$, $T_J = 25^{\circ}C$ | 3 | 5 | | mA |
| Upper clamp voltage | V_{COMP_H} | $V_{FB} = 2V$, $I_{comp} = -0.5mA$ | 5.5 | 6.1 | 6.5 | V |
| Lower clamp voltage | V_{COMP_L} | $V_{FB} = 2V$, $I_{comp} = -0.5mA$ | 2.0 | 2.15 | 2.3 | V |
| Current Sense Comparator | | | | | | |
| Input bias current | I_{CS} | CS = 0 | | | -1 | μA |
| Turn-off delay | T_{DT} | MULT = 0.2V | | 190 | | ns |
| LEB time | T_{LEB} | MULT = 0.2V | 45 | 70 | 95 | ns |
| Current sense clamp voltage | V_{CS_Clamp} | | 1.6 | 1.72 | 1.83 | V |
| Current sense offset | V_{CS_Offset} | $V_{MULT} = 0V$ | | 26 | | mV |
| | | $V_{MULT} = 2.5V$ | | 8 | | mV |
| Zero Current Sensor | | | | | | |
| Upper clamp voltage | $V_{ZCSclamp_H}$ | $I_{ZCS} = 2.5mA$ | 7.1 | 7.8 | 8.6 | V |

ELECTRICAL CHARACTERISTICS (continued)
 $V_{CC} = 15V$, $C_{GATE} = 1nF$, $T_J = -40^{\circ}C \sim +125^{\circ}C$, unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|--------------------------------|----------------------|---|------|------|------|---------|
| Lower clamp voltage | $V_{ZCS_{clamp_L}}$ | $I_{ZCS} = -2.5mA$ | 0.2 | 0.5 | 0.7 | V |
| Zero current sensing threshold | V_{ZCS_H} | V_{ZCS} rising | | 2.1 | 2.21 | V |
| | V_{ZCS_L} | V_{ZCS} falling | 1.45 | 1.56 | 1.66 | V |
| ZCS_DISABLE threshold | $V_{ZCS_DISABLE_}$ | | 140 | 185 | 230 | mV |
| ZCS_EN threshold | V_{ZCS_EN} | | 260 | 320 | 380 | mV |
| Source current capability | I_{ZCS_source} | | -1.8 | | | mA |
| Restart current after disable | I_{ZCS_res} | | 55 | 85 | | μA |
| Re-Starter | | | | | | |
| Re-start time | T_{start} | | 80 | 175 | 280 | μs |
| Over Voltage | | | | | | |
| Dynamic OVP current | I_{OVP} | | 35 | 40 | 45 | μA |
| Hysteresis | I_{OVP_Hys} | | | 30 | | μA |
| Static OVP threshold | V_{OVP} | | 2.15 | 2.25 | 2.35 | V |
| Gate Driver | | | | | | |
| Dropout voltage | V_{OH} | $I_{GD_{source}} = 20mA$ | | 2.4 | 3.1 | V |
| | | $I_{GD_{source}} = 200mA$ | | 3.9 | 5.0 | V |
| | V_{OL} | $I_{GD_{sink}} = 200mA$ | | 0.9 | 1.9 | V |
| Voltage fall time | T_f | | | 30 | 70 | ns |
| Voltage rise time | T_r | | | 40 | 80 | ns |
| Max. output drive voltage | V_{D_max} | | 12 | 13.5 | 15.5 | V |
| Source current capability | I_{Gate_source} | | | -750 | | mA |
| Sink current capability | I_{Gate_sink} | | | 800 | | mA |
| UVLO saturation voltage | $V_{Saturation}$ | $V_{CC} = 0$ to V_{CC_ON} , $I_{Gate_sink} = 10mA$ | | | 0.3 | V |

NOTES:

- 6) The multiplier output is given by: $V_{cs} = K \cdot V_{MUTL} \cdot (V_{COMP} - 2.5)$.
 7) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs. Supply Voltage



Supply Current vs. T_J



Start-Up & UVLO vs. T_J



VCC Zener Voltage vs. T_J



Feedback Reference vs. T_J



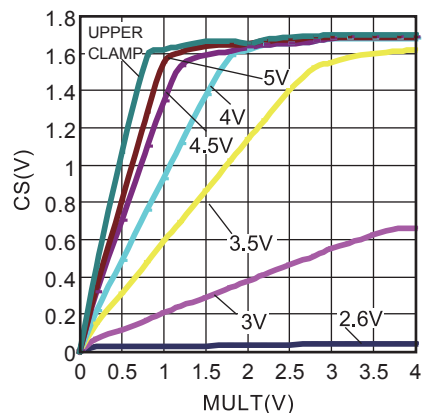
Delay-to-Output vs. T_J



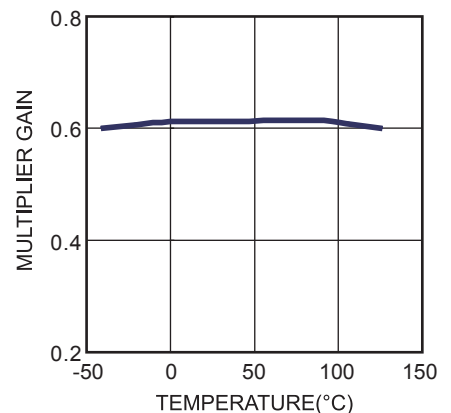
OVP Current vs. T_J



Multiplier Characteristic



Multiplier Gain vs. T_J



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

ZCS Clamp Levels vs. T_J



Gate-Drive Output High Saturation



Gate-Drive Output Low Saturation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

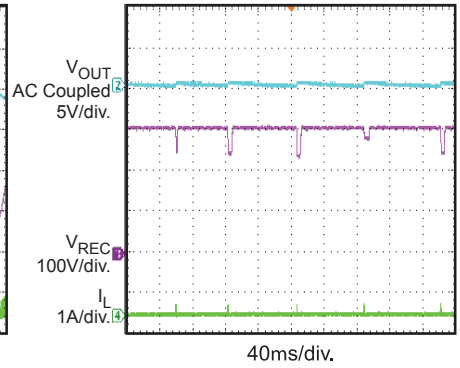
Steady State
P_{OUT} = 100W



Steady State
P_{OUT} = 50W



Steady State
P_{OUT} = 0W



Start-Up



Shutdown



Zero-Current Sensing



Zero-Crossing Compensation Harmonics
V_{AC} = 85V



PIN FUNCTIONS

| Pin # | Name | Description |
|-------|------|---|
| 1 | FB | Feedback. The output voltage is fed into FB through a resistor divider. |
| 2 | COMP | Output of the error amplifier. A compensation network is connected between COMP and FB. |
| 3 | MULT | Input of the multiplier. Connect MULT to the rectified main voltage via a resistor divider to provide the sinusoidal reference for the current control loop. |
| 4 | CS | Current sense. The current through the MOSFET is fed into CS via a resistor. The resulting voltage on CS is compared with the output of the internal multiplier to get an internal sinusoidal-shaped reference to determine the MOSFET's turn-off. The on-chip R/C filter can reduce high frequency noise on CS. Also, suggest to add a RC filter on the CS pin in case of switching noise is too large. |
| 5 | ZCS | Inductor's zero-crossing current sensing input. A negative transition edge triggers the MOSFET's turn-on. Suggest to connect a 22pF cap from this ZCS to GND to tune ZVS point. |
| 6 | GND | Ground. |
| 7 | GATE | Gate driver output. The high output current of the gate driver is able to drive a low-cost power MOSFET. The high-level voltage of GATE is clamped to 12V in case GATE is supplied with a high VCC. |
| 8 | VCC | Supply voltage for both the signal path of the IC and the gate driver. A bypass capacitor from VCC to ground is needed to reduce noise. |

FUNCTIONAL BLOCK DIAGRAM



Figure 1: Functional Block Diagram

OPERATION

The MP44014 is a boundary conduction mode PFC controller optimized for the PFC pre-regulator up to 300W and fully complies with IEC1000-3-2 specification.

Output Voltage Regulation

The output voltage is sensed at FB through a resistor divider from the output voltage to ground. The accurate on-chip reference voltage and the high performance error amplifier regulate the output voltage accurately.

Over-Voltage Protection (OVP)

The MP44014 offers two stages of over-voltage protection: dynamic over-voltage protection and static over-voltage protection. With two-stage protection, the circuit operates reliably.

The MP44014 achieves OVP by monitoring the current flow through COMP.

During steady-state operation, the current flow through the high-side feedback resistor (R9) and the low-side feedback resistor (R10) is calculated with Equation (1):

$$I_{R9} = \frac{V_O - V_{FB}}{R9} = I_{R10} = \frac{V_{FB}}{R10} \quad (1)$$

If there is an abrupt rise on the output (ΔV_O) and the compensation network connected between FB and COMP takes time to achieve high power factor (PF) due to the long RC time constant, the voltage on FB will still be kept at the reference value. The current through R10 remains equal to $V_{FB}/R10$. However, the current through R9 is calculated with Equation (2):

$$I'_{R9} = \frac{V_O + \Delta V_O - V_{FB}}{R9} \quad (2)$$

This current has to flow into COMP. Simultaneously, this current is monitored inside the chip. If the current rises to $35\mu A$, the output voltage of the multiplier will be forced to decrease, and the energy delivered to the output will be reduced. If this current continues to rise to about $40\mu A$, the dynamic OVP can be triggered. Consequently, the gate driver is blocked to turn off the external power MOSFET, and the device enters an idle state. This state is maintained until the current falls below $10\mu A$, the point at which the internal starter will be re-enabled and allow the switching to restart.

When the load is very light, the output voltage tends to stay steadily above the nominal value. In this condition, the error amplifier output will saturate low. When the error amplifier output is lower than 2.25V, static OVP will be triggered. Consequently, the gate driver will be blocked to turn off the external power MOSFET, and the device will enter an idle state. Normal operation resumes once the error amplifier output returns to the regulated region (see Figure 2).



Figure 2: OVP Detector Block

Disable Function

The MP44014 can be disabled by pulling the zero-current sensing (ZCS) pin lower than 190mV. This helps to further reduce quiescent current when the PFC pre-regulator needs to be shut down. After releasing ZCS, it will stay at a lower clamp voltage when there is no external voltage from the auxiliary winding (see Figure 3).

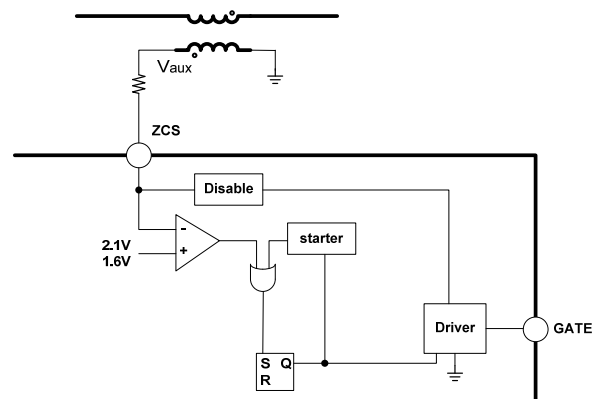


Figure 3: ZCS Triggering and Disable Block

Boundary Conduction Mode

When the current of the boost inductor reaches zero, the voltage on the inductor is reversed. ZCS then generates the turn-on signal of the MOSFET by sensing the falling edge of the voltage on the auxiliary winding coupled with the inductor. If the ZCS voltage rises above 2.1V, the comparator waits until the voltage falls below 1.6V. Once the voltage falls below 1.6V, the MP44014 turns on the MOSFET. The 7.8V high clamp and 0.55V low clamp protect ZCS. The internal 175µs timer generates a signal to turn on the MOSFET if the driver signal has been low for more than 175µs. This also allows the MOSFET to turn on during the start-up period since no signal is generated from ZCD during start-up.

Zero-Crossing Compensation

The MP44014 offers 30mV voltage offset for the multiplier output near the zero crossing of the line voltage (which can force the circuit to process more energy at the bottom of the line voltage). With this function, the THD of the current is reduced.

To prevent redundant energy, this offset is reduced as the instantaneous line voltage increases. Therefore the offset will be negligible near the top of the line voltage.

Power Factor Correction

The MP44014 senses the inductor current through the current sense pin and compares it

to the sinusoidal-shaped signal, which is generated from the output of the multiplier. When the external power MOSFET turns on, the inductor current rises linearly. When the peak current hits the sinusoidal-shaped signal, the external power MOSFET begins to turn off, and the diode turns on. Also, the inductor current begins to fall. When the inductor current reaches zero, the power MOSFET begins to turn on again, which causes the inductor current to start rising again. The power circuit works in boundary conduction mode, and the envelope of the inductor current is sinusoidal shaped. The average input current is half of the peak current, so the average input current is also sinusoidal shaped. A high power factor can be achieved through this control method (see Figure 4).



Figure 4: Inductor Current Waveform

The control flow chart of the MP44014 is shown in Figure 5.

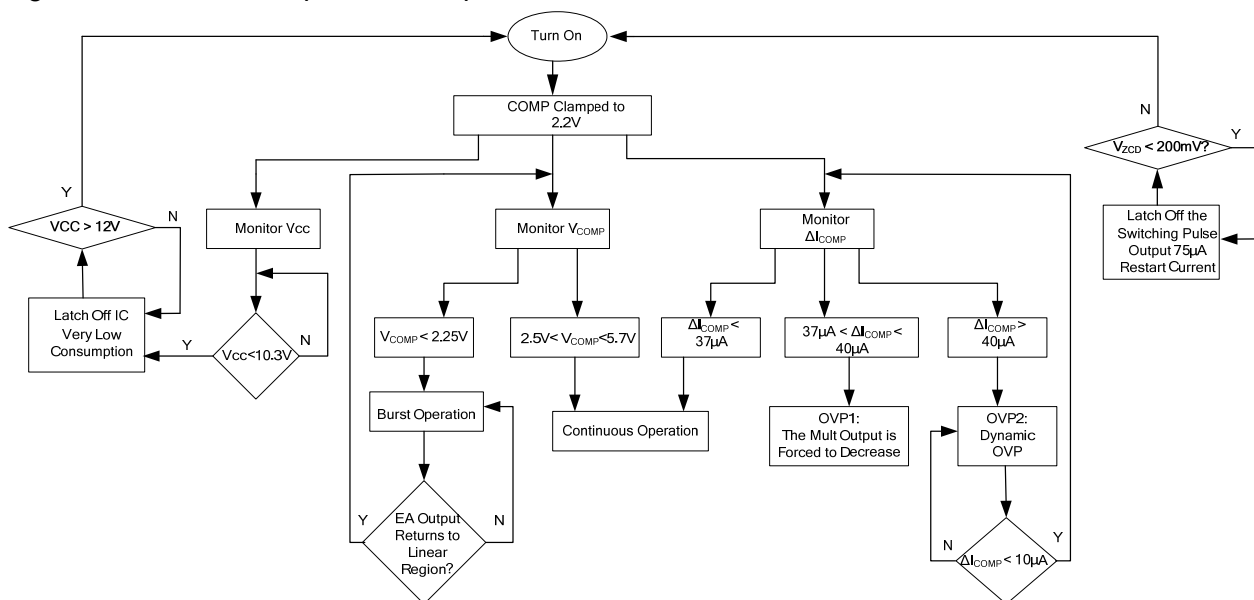


Figure 5: Control Flow Chart

PACKAGE INFORMATION

SOIC-8



TOP VIEW



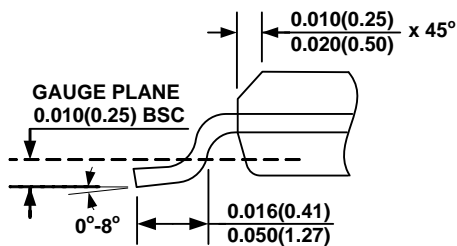
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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