MK1491-09

AMD Geode™ GX2 Clock Source

Description

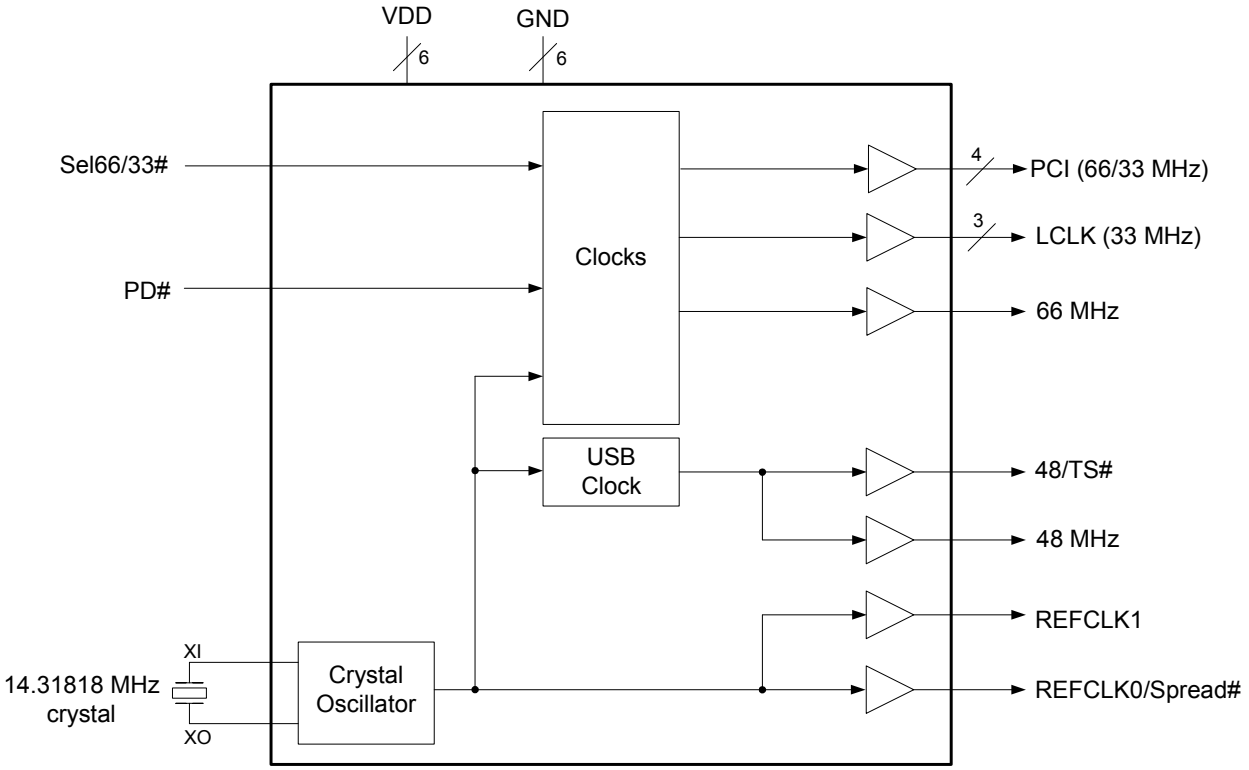
The MK1491-09 is a low-cost, low-jitter, high-performance clock synthesizer for AMD's Geode-based computer and portable appliance applications. Using patented analog Phased-Locked Loop (PLL) techniques, the device accepts a 14.318 MHz crystal input to produce multiple output clocks. It provides selectable PCI local bus clocks, 48 MHz clocks for Super I/O and USB, as well as multiple Reference outputs.

The device has multiple power-down modes to reduce power consumption.

Features

- Packaged in 28-pin SSOP (209 mil body)
- Available in Pb (lead) free packaged
- Provides all critical timing for the AMD Geode companion chip
- Four selectable PCI clocks
- Three LPC interface clocks
- One Fixed 66 MHz clock
- 2 Reference clocks
- 48 MHz USB and 48 MHz IO support
- Power down mode
- Low EMI Enable pin reduces EMI radiation on PCI clocks, LCLKS, and 66 MHz clock
- Operating voltage of 3.3 V ±5%

Block Diagram



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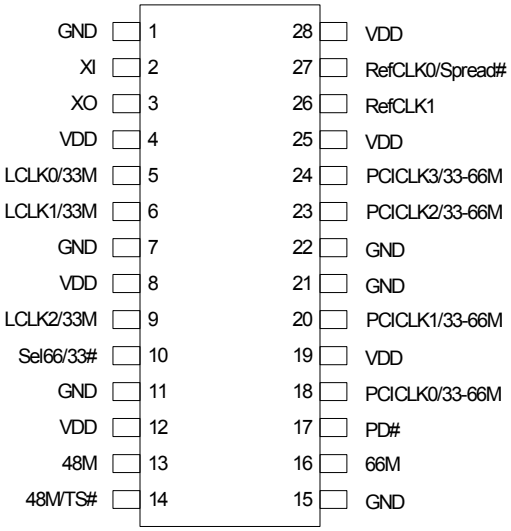
Pin Assignment



PCI Frequency Select Table

Sel66/33#	PCI Frequency
0	33 MHz
1	66 MHz

EMI Control

Spread#	PCI Low EMI
0	ON
1	OFF

Spread direction is DOWN.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1, 7, 11, 15, 21, 22	GND	P	Connect to Ground.
2	XI	I	Crystal connection. Connect to a 14.31818 MHz crystal or input clock.
3	XO	O	Crystal connection. Connect to a 14.31818 MHz crystal, or leave unconnected.
4, 8, 12, 19, 25, 28	VDD	P	Connect to 3.3 V.
5, 6, 9	LCLK	O	33 MHz low skew clock outputs.
10	Sel66/33#	I	Selects frequency on PCICLK.
13	48M	O	48 MHz clock output.
14	48M/TS#	I/O	48 MHz clock output. TS# is high at power-up.
16	66M	O	66 MHz clock output.
17	PD#	I	Power-down input (see table on page 3).
18, 20, 23, 24	PCICLK	O	33 to 66 MHz PCI synchronous clock outputs with low skew.
26	RefCLK1	O	Buffered reference output of 14.31818 MHz.
27	RefCLK0/ Spread#	I/O	Buffered reference output of 14.31818 MHz. Spread select at power-up. For Spread#, see table above.

KEY: I = Input, TI = Tri-level, O = Output, P = Power supply connection, (T)I/O = Input on power up, becomes an Output after 10 ms, Weak internal pull-up resistors are present on TS#, Spread#, PD#, and Sel66/33.

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Power Down Control Table

PD#	Functions
0	All clocks are stopped low.
1	All clocks are running.

Power-on Default Conditions

Pin #	Function	Default	Condition
14	TS#	H	All outputs enabled.
27	Spread#	H	Spread disabled.
17	PD#	H	PCI clocks set to 33.3 MHz. Refer to Power Down Control Table above.
10	Sel66/33	H	PCI frequency = 66 MHz.

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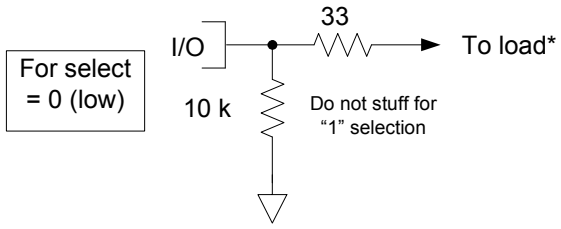
External Components

The MK1491-09 requires some inexpensive external components for proper operation. Decoupling capacitors of 0.1µF should be connected on each VDD pin to ground, as close to the MK1491-09 as possible. A series termination resistor of 33Ω may be used for each clock output. See the discussion below for other external resistors required for proper I/O operation. The 14.318 MHz oscillator has internal caps that provide the proper load for a parallel resonant crystal with CL=18 pF. For tuning with other values of C_L, the formula 2*(C_L-18) gives the value of each capacitor that should be connected between X1 and ground and X2 and ground.

I/O Structure

The MK1491-09 provides more functionality in a 28-pin package by using a unique I/O technique. The device checks the status of all I/O pins during power-up. This status (pulled high or low) then determines the frequency selections and power down modes (see the tables on pages 2 and 3). Within 10ms after power up, the inputs change to outputs and the clocks start up. In the diagrams below, the 33Ω resistors are the normal output termination resistors. The 10kΩ resistor pulls low to generate a logic zero when needed. Weak internal pull-up resistors are present on TS#, Spread#, PD#, and Sel66/33 to pull the pin to high when left floating.



*Note: Do not use a TTL load. This will overcome the 10 kΩ pull-down and force the input to a logic 1.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1491-09. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referenced to VSS)	4.6 V
All Inputs and Outputs (referenced to VSS)	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature (10 seconds max)	260°C
Spread Spectrum Enabled for PCI and LPC Clocks	30 kHz min., 33 kHz max.

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13	3.3	3.46	V
Input High Voltage	V_{IH}		2		VDD	V
Input Low Voltage	V_{IL}		VSS		0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Operating Supply Current	IDD	VDD = 3.3 V			60	mA
Clock Disable Mode Supply Current					0.5	mA
Internal Pull-up Resistor		All inputs except XI				kΩ
Input Capacitance	C_{IN}	All inputs except XI		5		pF

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AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}			14.31818		MHz
Output Clock Skew Rate (PCI and LPC), load = 30 pF		Between 0.4 V and 2.4 V			4	V/ns
Output Clock Rise and Fall Time (all but PCI and LPC), load=pF	t_{OR}, t_{OF}	Between 0.4 V and 2.4 V	0.5		2	ns
Output Clock Duty Cycle, all MHz Clocks	t_{OD}	At 1.5 V	40		60	%
PCI Output to Output Skew, at 33 MHz		Rising edges at 1.5 V			500	ps
PCI Output to Output Skew, at 66 MHz		Rising edges at 1.5 V			250	ps
LPC Output to Output Skew		Rising edges at 1.5 V			500	ps
PCI to LPC Output to Output Skew (note 1)		Rising edge at 1.5 V			500	ns
Cycle-to-Cycle Jitter, PCICLK					300	ps
Cycle-to-Cycle Jitter, LPCCLK					500	ps
Cycle-to-Cycle Jitter, USBCLK and 48 MHz					500	ps
Cycle-to-Cycle Jitter, REFCLKs					1400	ps
Power-on Time, applied VDD to all Clocks Stable					5	ms
Load Capacitance Crystal				18		pF

Note 1: Only valid when PCI is at 33 MHz.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		100		°C/W
	θ_{JA}	1 m/s air flow		80		°C/W
	θ_{JA}	3 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

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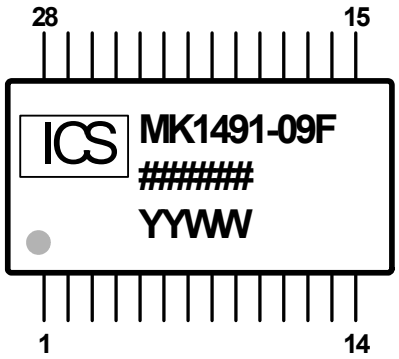
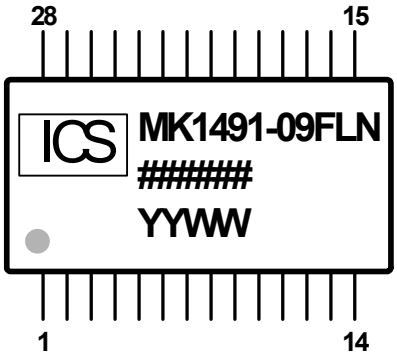
Marking Diagram



Marking Diagram (for Pb free)



Notes:

1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. “LN” designates Pb (lead) free.

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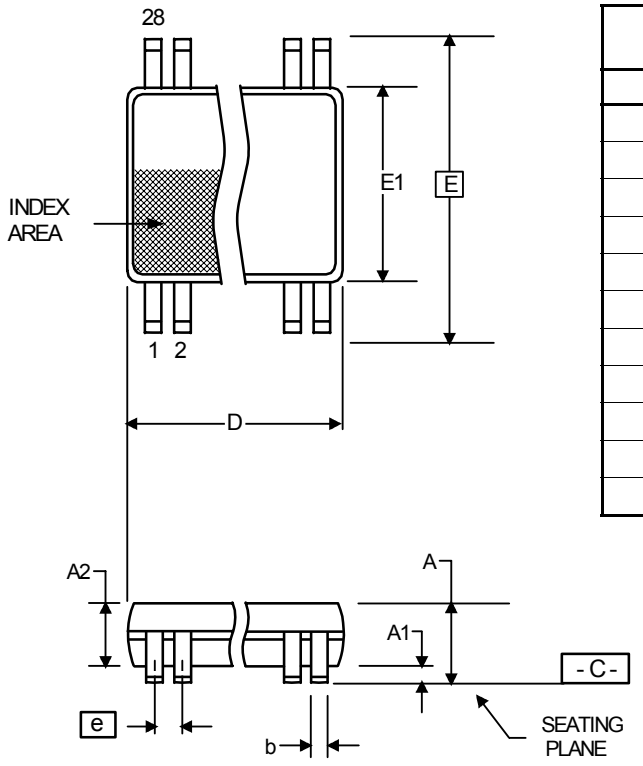
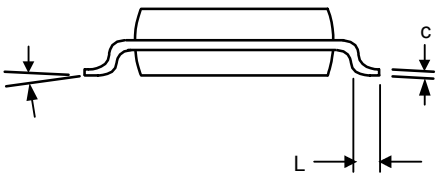
Package Outline and Package Dimensions (28-pin SSOP, 209 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95, MO-150



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	—	2.00	—	0.079
A1	0.05	—	0.002	—
A2	1.65	1.85	0.065	0.073
b	0.22	0.38	0.009	0.015
c	0.09	0.25	0.0035	0.010
D	9.90	10.50	0.390	0.413
E	7.40	8.20	0.291	0.323
E1	5.00	5.60	0.197	0.220
e	0.65 Basic		0.0256 Basic	
L	0.55	0.95	0.022	0.037
α	0°	8°	0°	8°

The controlling dimensions is inches



Ordering Information

Part / Order Number	Marking (see note 1)	Low EMI Feature	Shipping Packaging	Package	Temperature
MK1491-09F	MK1491-09F	Yes	Tubes	28-pin SSOP	0 to +70°C
MK1491-09FTR	MK1491-09F	Yes	Tape and Reel	28-pin SSOP	0 to +70°C
MK1491-09FLN	MK1491-09FLN	Yes	Tubes	28-pin SSOP	0 to +70°C
MK1491-09FLNTR	MK1491-09FLN	Yes	Tape and Reel	28-pin SSOP	0 to +70°C

Note:

1. “L” designates Pb (lead) free.

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