



N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
20	0.017 at V _{GS} = 4.5 V	6	12.5 nC
	0.022 at V _{GS} = 2.5 V	6	

FEATURES

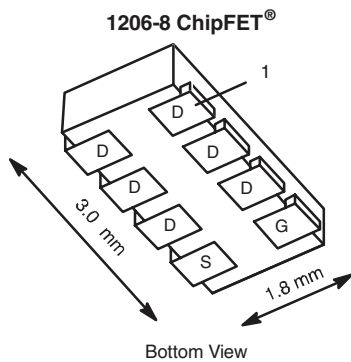
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

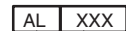
APPLICATIONS

- Load Switches
- Notebook System Power



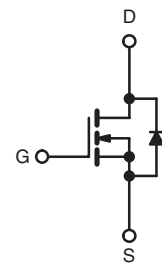
Bottom View

Marking Code



Part #
Code

Lot Traceability
and Date Code



N-Channel MOSFET

Ordering Information: Si5414DC-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	20	V	
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	6 ^a	A
		T _C = 70 °C	6 ^a	
		T _A = 25 °C	6 ^{a, b, c}	
		T _A = 70 °C	6 ^{a, b, c}	
Pulsed Drain Current	I _{DM}	30		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	5.2	
		T _A = 25 °C	2.1 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C	6.3	W
		T _C = 70 °C	4	
		T _A = 25 °C	2.5 ^{b, c}	
		T _A = 70 °C	1.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{e, f}		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c, d}	R _{thJA}	40	50	°C/W	
Maximum Junction-to-Foot (Drain)	R _{thJF}	15	20		

Notes:

- Package limited, T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 95 °C/W.
- The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		19		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 9.9\text{ A}$		0.014	0.017	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 8.7\text{ A}$		0.017	0.022	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 9.9\text{ A}$		41		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1500		pF
Output Capacitance	C_{oss}			280		
Reverse Transfer Capacitance	C_{rss}			125		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 9.9\text{ A}$		27	41	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9.9\text{ A}$		12.5	19	
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}		2.1			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.46	2.3	4.6	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1.3\text{ }\Omega$ $I_D \cong 7.9\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		14	25	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			36	55	
Fall Time	t_f			14	25	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1.3\text{ }\Omega$ $I_D \cong 7.9\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		10	15	
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			5.2	A
Pulse Diode Forward Current	I_{SM}				30	
Body Diode Voltage	V_{SD}	$I_S = 7.9\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 7.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		20	40	ns
Body Diode Reverse Recovery Charge	Q_{rr}			10	20	nC
Reverse Recovery Fall Time	t_a			8		ns
Reverse Recovery Rise Time	t_b			12		

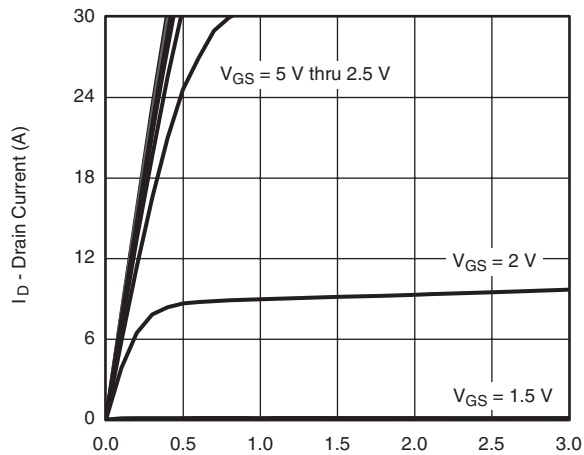
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

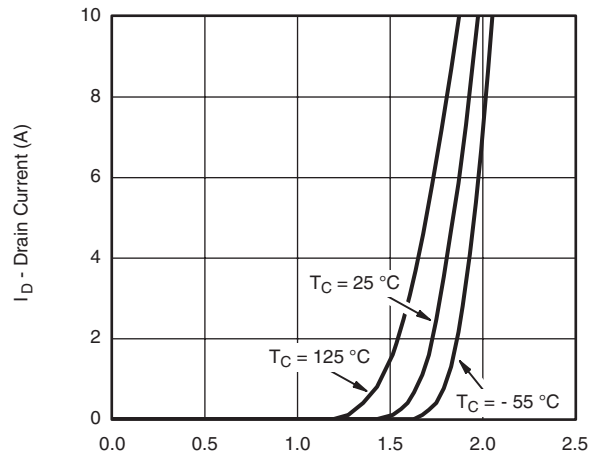
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



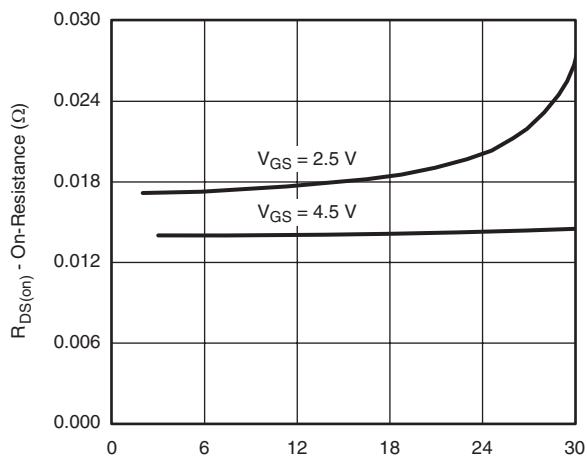
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



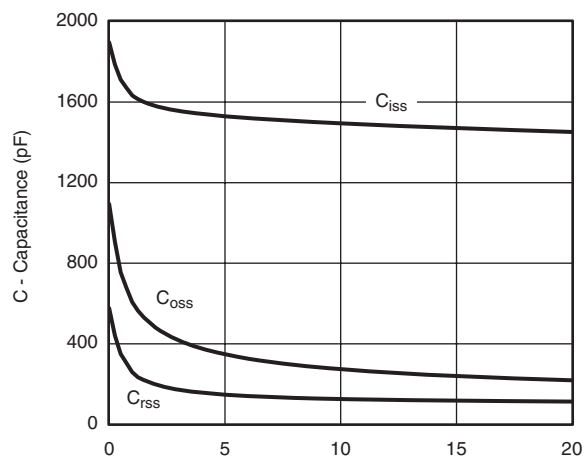
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



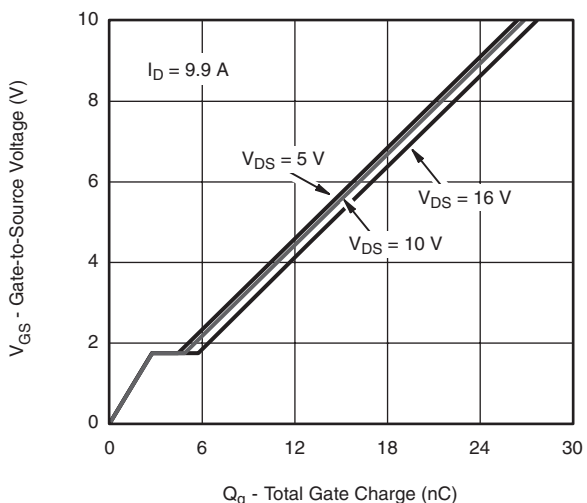
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



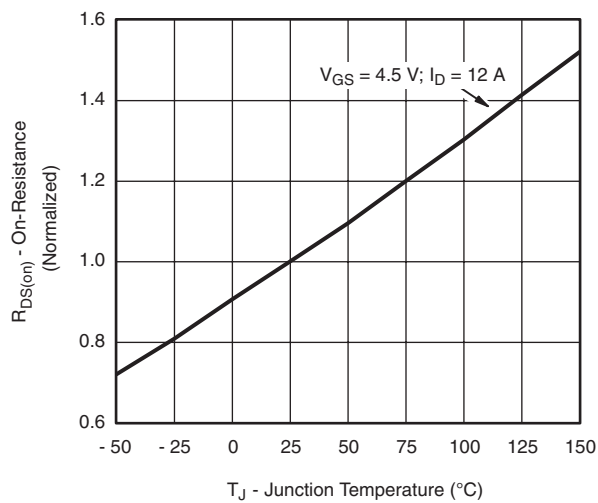
I_D - Drain Current (A)
On-Resistance vs. Drain Current



V_{DS} - Drain-to-Source Voltage (V)
Capacitance



Q_g - Total Gate Charge (nC)
Gate Charge



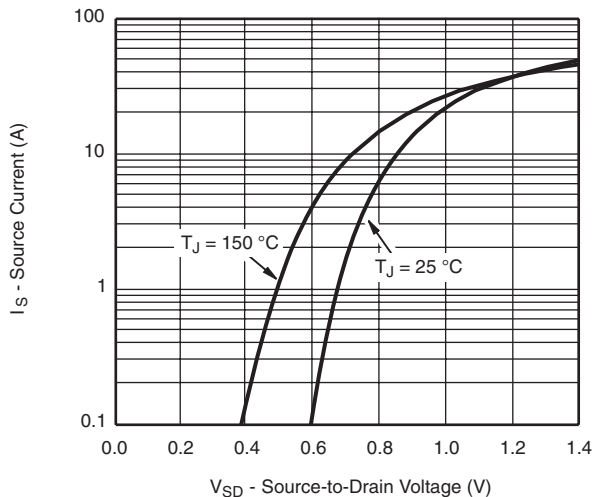
T_J - Junction Temperature (°C)
On-Resistance vs. Junction Temperature

Si5414DC

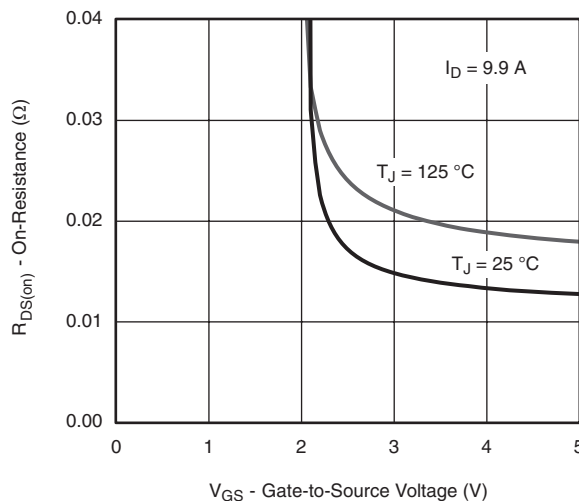
Vishay Siliconix



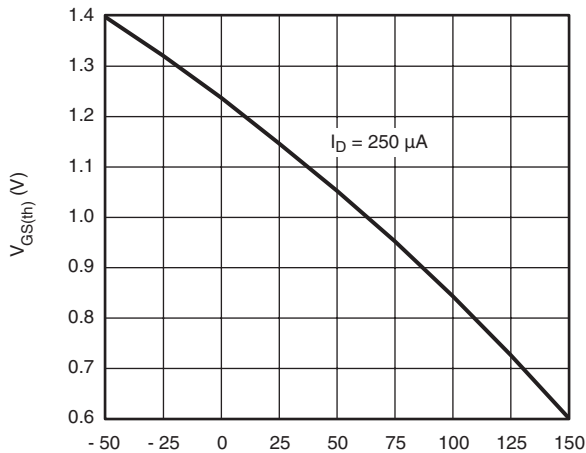
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



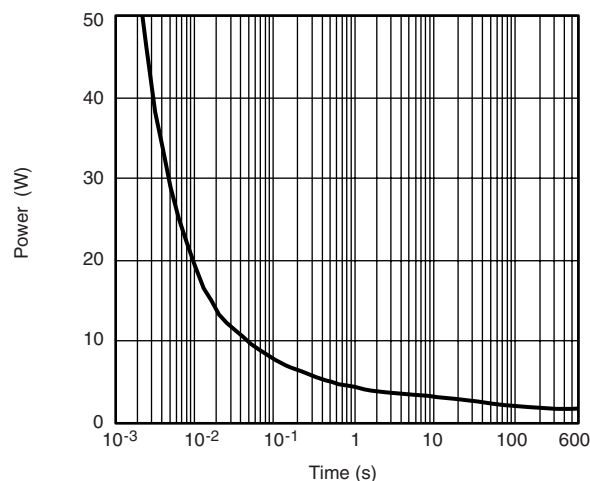
Source-Drain Diode Forward Voltage



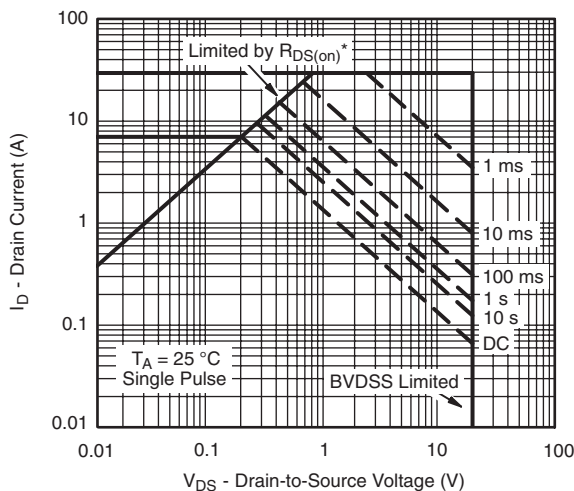
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power

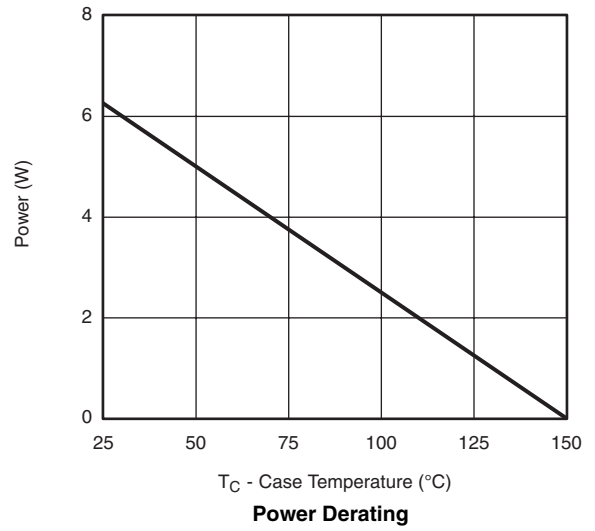
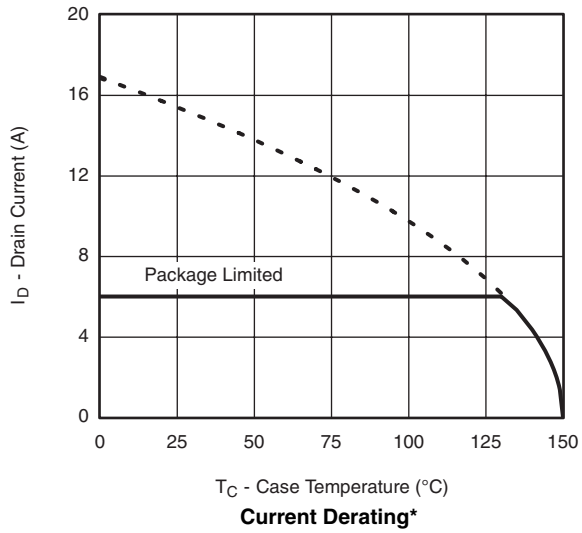


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



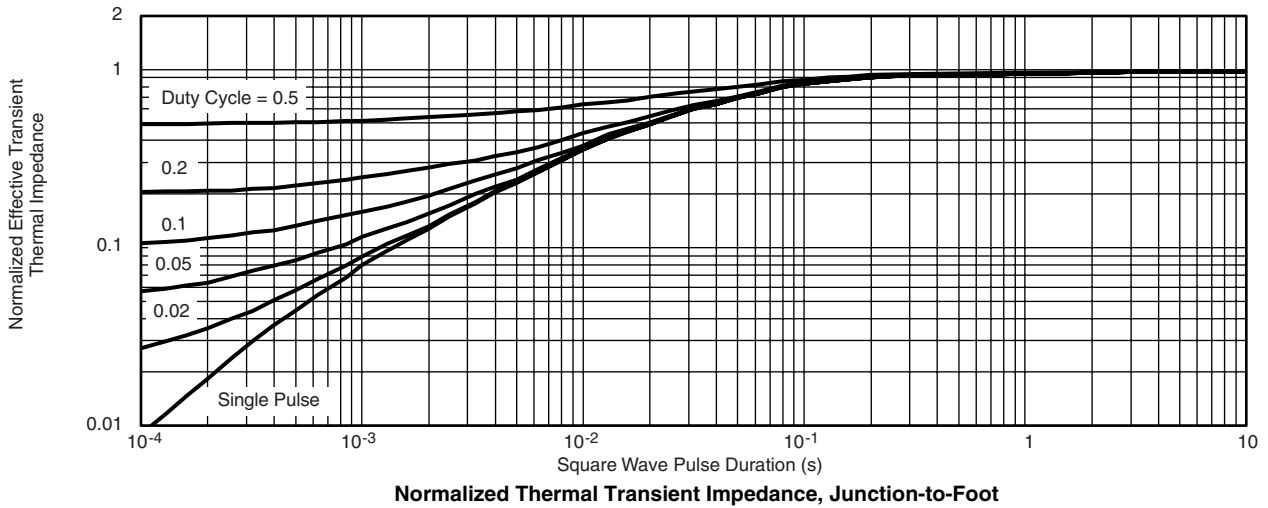
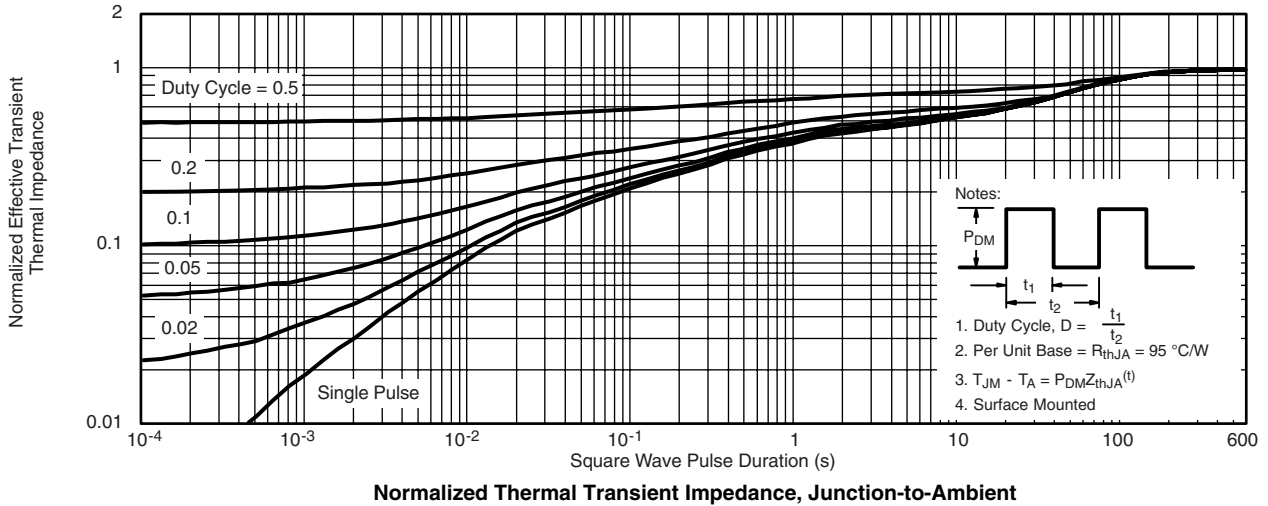
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si5414DC

Vishay Siliconix



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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