300MHz to 4GHz 3.3V Dual Active Downconverting Mixer

FEATURES

- **High IIP3: 26.8dBm at 1950MHz**
- **2dB Conversion Gain**
- **Low Noise Figure: 11.7dB at 1950MHz**
- **17dB NF Under 5dBm Blocking**
- **44dB Channel Isolation**
- **Low Power: 3.3V/600mW Total**
- **Very Small Solution Size**
- **Enable Pins for Each Mixer**
- **Wide IF Frequency Range**
- LO Input 50Ω Matched in All Modes
- –40°C to 105°C Operation
- 16-Lead (4mm × 4mm) QFN package

APPLICATIONS

- Wireless Infrastructure Diversity Receivers
- MIMO Infrastructure Receivers
- Remote Radio Units

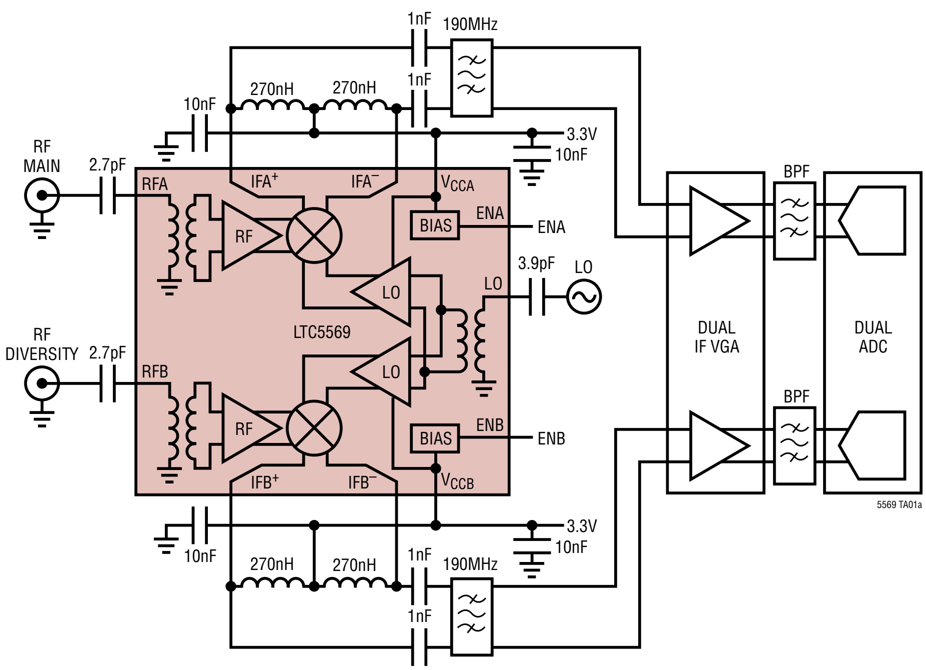
DESCRIPTION

The LTC®5569 dual active downconverting mixer is optimized for diversity and MIMO receiver applications that require low power and small size. Each mixer includes an independent LO buffer amplifier, active mixer core, and bias circuit with enable pin. The symmetry of the IC assures that a phase and amplitude coherent LO is applied to each mixer.

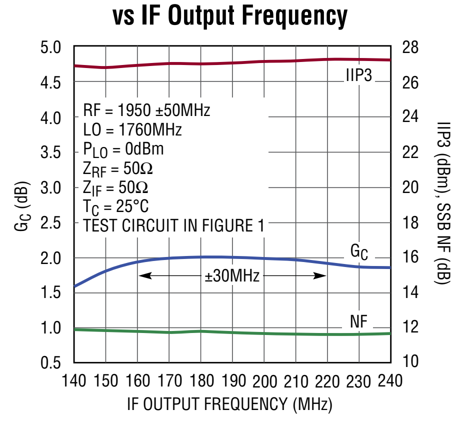
The RF inputs are 50Ω matched from 1.4GHz to 3.3GHz, and easily matched for higher or lower RF frequencies with simple external matching. The LO input is 50Ω matched from 1GHz to 3.5GHz, even when one or both mixers are disabled. The LO input is easily matched for higher or lower frequencies, as low as 350MHz, with simple external matching. The low capacitance differential IF outputs are usable up to 1.6GHz.

TYPICAL APPLICATION

Diversity Receiver with 190MHz Bandpass IF Matching



Mixer Conversion Gain, IIP3 and NF vs IF Output Frequency



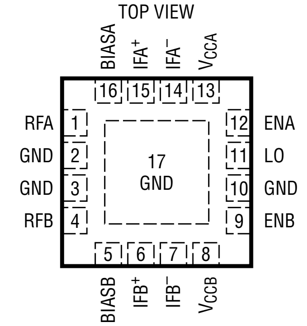
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
V_{CCA}, V_{CCB}, IFA^+, IFA^-, IFB^+, IFB^- 4.0V
Enable Input Voltage (ENA, ENB) .....–0.3V to V_{CC} + 0.3V
Mixer Bias Voltage (BIASA, BIASB)..–0.3V to V_{CC} + 0.3V
LO Input Power (350MHz to 4.5GHz)...................10dBm
LO Input DC Voltage... ±0.1V
RFA, RFB Input Power (300MHz to 4GHz) 20dBm
RFA, RFB Input DC Voltage................................... ±0.1V
Operating Temperature Range (T_C)........–40°C to 105°C
Junction Temperature (T_J) .... 150°C
Storage Temperature Range ....–65°C to 150°C

PIN CONFIGURATION

TOP VIEW



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5569IUF#PBF	LTC5569IUF#TRPBF	5569	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AC ELECTRICAL CHARACTERISTICS V_{CC} = 3.3V, ENA, ENB = High. Test circuit shown in Figure 1.

(Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Input Frequency Range			300 to 4000		MHz
LO Input Frequency Range			350 to 4500		MHz
IF Output Frequency Range	External Matching Required		LF to 1600		MHz
RF Input Return Loss	Z_0 = 50Ω, 1400MHz to 3300MHz		>12		dB
LO Input Return Loss	Z_0 = 50Ω, 1000MHz to 3500MHz		>12		dB
IF Output Impedance	Differential at 190MHz		530Ω‖1.3pF		R‖C
LO Input Power		–6	0	6	dBm

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, ENA, ENB = High. T_C = 25°C, P_{LO} = 0dBm, IF = 190MHz, P_{RF} = –6dBm (–6dBm/tone for 2-tone tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Conversion Gain	RF = 450MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2550MHz, Low Side LO RF = 3500MHz, Low Side LO	 0.5	1.5 2.0 2.0 1.8 1.4		dB dB dB dB dB
Conversion Gain Flatness	RF = 1950 ±30MHz, LO = 1760MHz, IF = 190 ±30MHz		±0.05		dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, RF = 1950MHz, Low Side LO		–0.014		dB/°C
2-Tone Input 3rd Order Intercept (Δf = 2MHz)	RF = 450MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2550MHz, Low Side LO RF = 3500MHz, Low Side LO	 24.0	26.0 27.1 26.8 26.0 25.2		dBm dBm dBm dBm dBm
2-Tone Input 2nd Order Intercept (Δf = 190MHz, $f_{SPUR} = f_{RF1} – f_{RF2}$)	f_{RF1} = 945MHz, f_{RF2} = 755MHz, f_{LO} = 1040MHz f_{RF1} = 2045MHz, f_{RF2} = 1855MHz, f_{LO} = 1760MHz		62.3 63.1		dBm dBm
SSB Noise Figure	RF = 450MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2550MHz, Low Side LO RF = 3500MHz, Low Side LO		11.9 11.7 11.7 12.1 14.3		dB dB dB dB dB
SSB Noise Figure Under Blocking	RF = 850MHz, High Side LO, 750MHz Blocker at 5dBm RF = 1950MHz, Low Side LO, 2050MHz Blocker at 5dBm		17.5 17.0		dB dB
LO to RF Leakage	LO = 350MHz to 1000MHz LO = 1000MHz to 2900MHz LO = 2900MHz to 4500MHz		<–58 <–50 <–42		dBm dBm dBm
LO to IF Leakage	LO = 350MHz to 1000MHz LO = 1000MHz to 2900MHz LO = 2900MHz to 4500MHz		<–38 <–35 <–33		dBm dBm dBm
RF to LO Isolation	RF = 300MHz to 2500MHz RF = 2500MHz to 4000MHz		>57 >50		dB dB
RF to IF Isolation	RF = 300MHz to 1400MHz RF = 1400MHz to 3000MHz RF = 3000MHz to 4000MHz		>28 >30 >31		dB dB dB
1/2IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 190MHz)	850MHz: f_{RF} = 945MHz at –10dBm, f_{LO} = 1040MHz 1950MHz: f_{RF} = 1855MHz at –10dBm, f_{LO} = 1760MHz		–75 –71		dBc dBc
1/3IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 190MHz)	850MHz: f_{RF} = 976.67MHz at –10dBm, f_{LO} = 1040MHz 1950MHz: f_{RF} = 1823.33MHz at –10dBm, f_{LO} = 1760MHz		–88 –84		dBc dBc
Input 1dB Compression	RF = 450MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2550MHz, Low Side LO RF = 3500MHz, Low Side LO		11.1 10.4 10.2 10.4 10.2		dBm dBm dBm dBm dBm
Channel-to-Channel Isolation	RF = 300MHz to 1000MHz RF = 1000MHz to 2700MHz RF = 2700MHz to 3000MHz RF = 3000MHz to 3300MHz RF = 3300MHz to 3800MHz		>44 >44 >42 >36 >34		dB dB dB dB dB

DC ELECTRICAL CHARACTERISTICS V_{CC} = 3.3V, T_C = 25°C. Test circuit shown in Figure 1. (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})			3.0	3.3	3.6	V
Supply Current	One Mixer Enabled Both Mixers Enabled	ENA or ENB = High ENA and ENB = High		90 180	106 212	mA mA
Shutdown Current—Both Mixers Disabled		ENA and ENB = Low			200	µA
Enable Logic Inputs (ENA, ENB)						
ENA, ENB Input High Voltage (On)			2.5			V
ENA, ENB Input Low Voltage (Off)					0.3	V
ENA, ENB Input Current		–0.3V to V_{CC} + 0.3V			100	µA
Turn-On Time				0.6		µs
Turn-Off Time				0.5		µs
Mixer DC Bias Adjust (BIASA, BIASB)						
Open-Circuit DC Voltage				2.2		V
Short-Circuit DC Current		Pin Shorted to Ground		1.8		mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

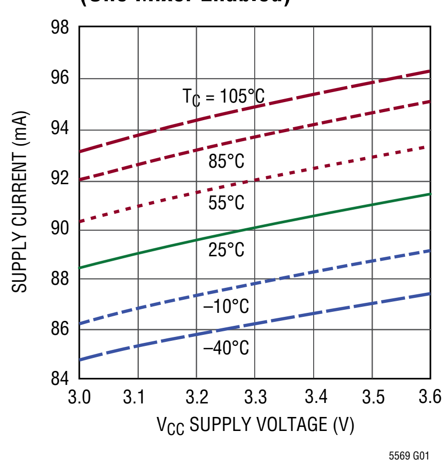
Note 2: The LTC5569 is guaranteed functional over the –40°C to 105°C case temperature range (θ_{JC} = 8°C/W).

Note 3: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 2dB matching pad on RF input, and bandpass filter on the LO input.

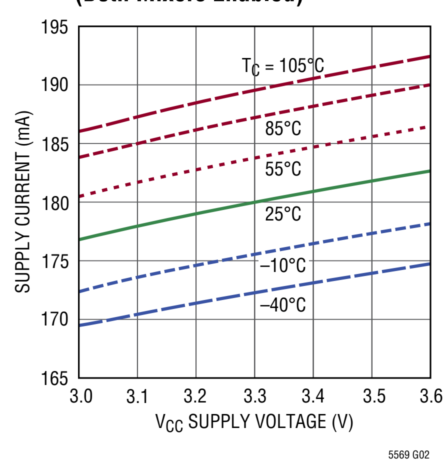
Note 4: Channel A to channel B isolation is measured as the relative IF output power of channel B to channel A, with the RF input signal applied to channel A. The RF input of channel B is 50Ω terminated, and both mixers are enabled.

TYPICAL DC PERFORMANCE CHARACTERISTICS Test circuit shown in Figure 1.

Supply Current vs Supply Voltage (One Mixer Enabled)



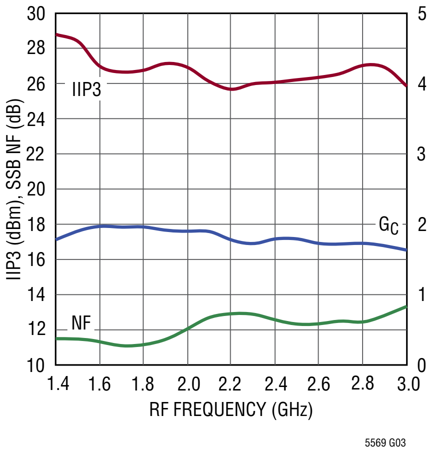
Supply Current vs Supply Voltage (Both Mixers Enabled)



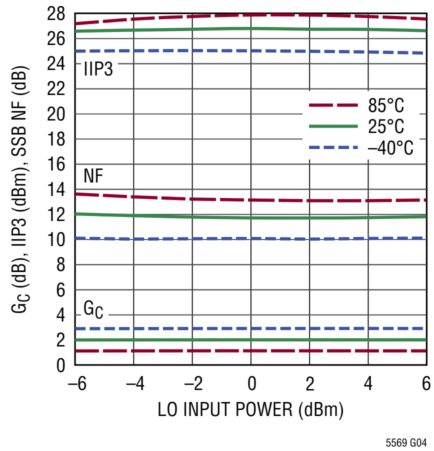
TYPICAL PERFORMANCE CHARACTERISTICS

1400MHz to 3000MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, ∆f = 2MHz), IF = 190MHz unless otherwise noted.

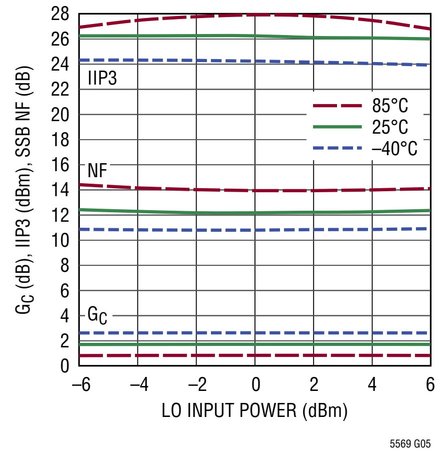
Conversion Gain, IIP3 and NF vs RF Frequency (Low Side LO)



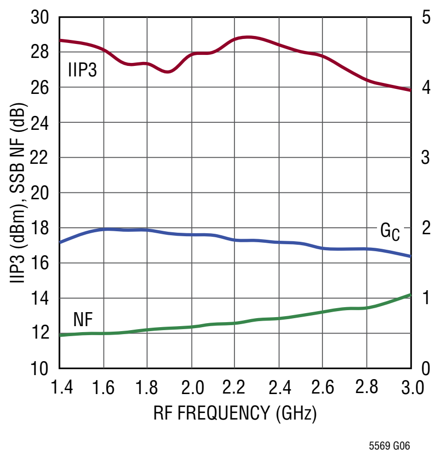
1950MHz Conversion Gain, IIP3 and NF vs LO Power (Low Side LO)



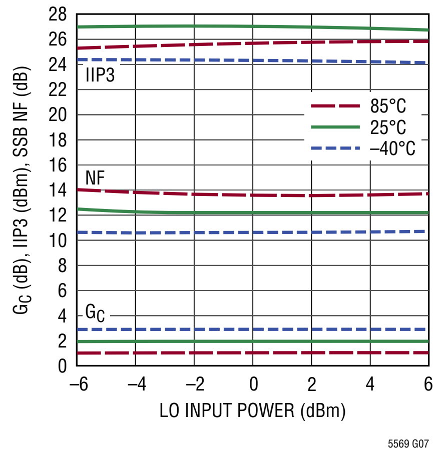
2550MHz Conversion Gain, IIP3 and NF vs LO Power (Low Side LO)



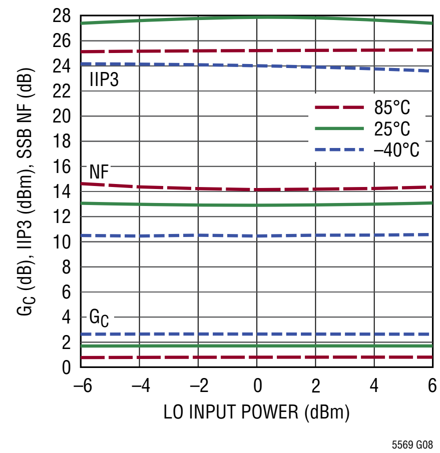
Conversion Gain, IIP3 and NF vs RF Frequency (High Side LO)



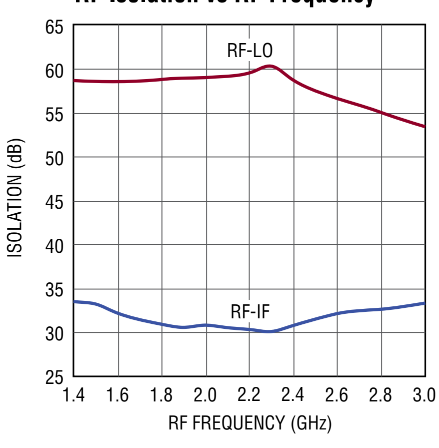
1950MHz Conversion Gain, IIP3 and NF vs LO Power (High Side LO)



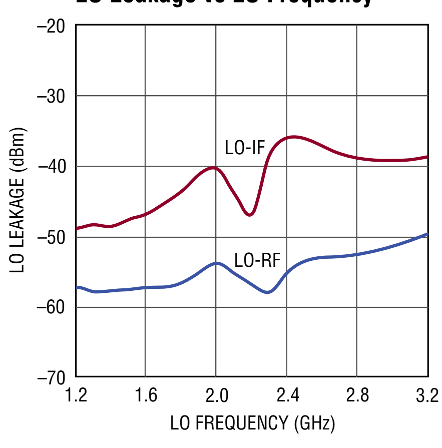
2550MHz Conversion Gain, IIP3 and NF vs LO Power (High Side LO)



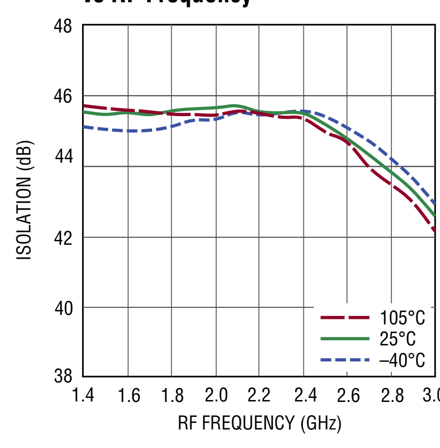
RF Isolation vs RF Frequency



LO Leakage vs LO Frequency



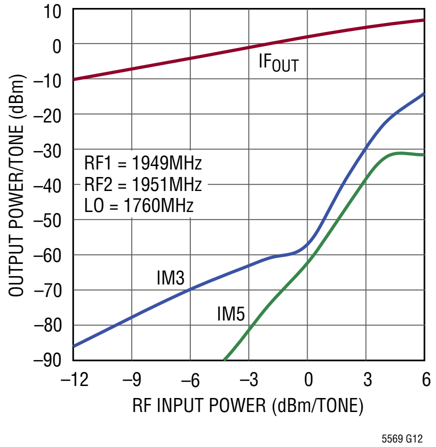
Channel Isolation vs RF Frequency



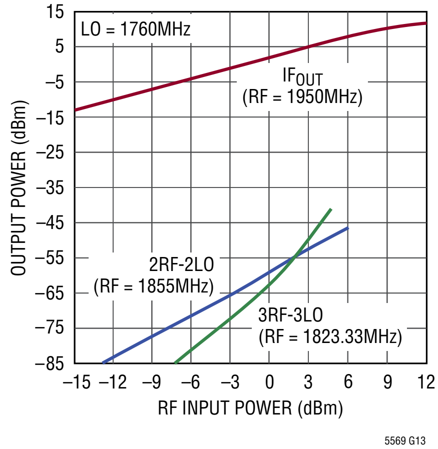
TYPICAL PERFORMANCE CHARACTERISTICS

1400MHz to 3000MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 190MHz unless otherwise noted.

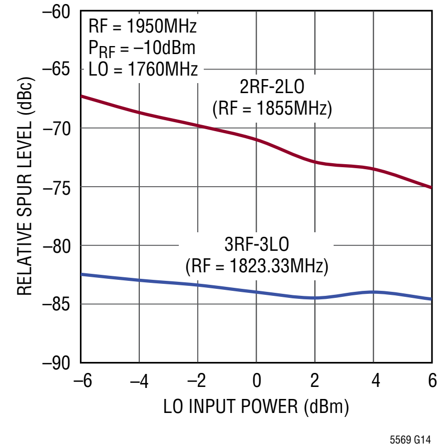
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



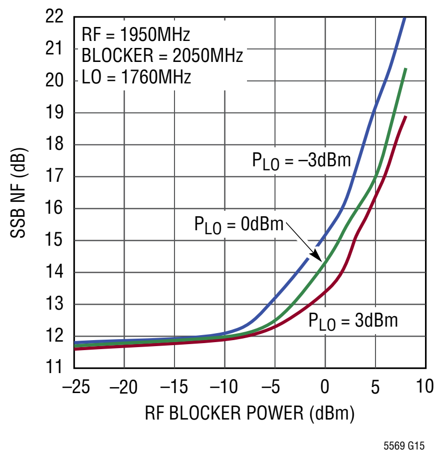
Single Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



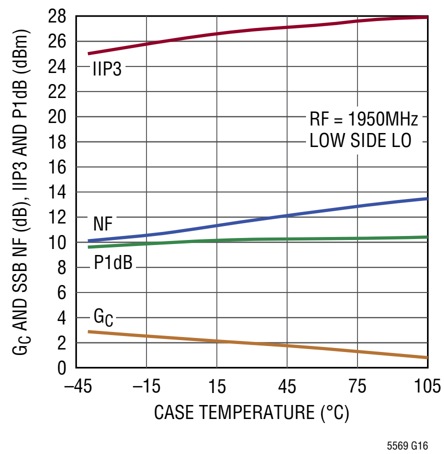
2 × 2 and 3 × 3 Spur Suppression vs LO Power



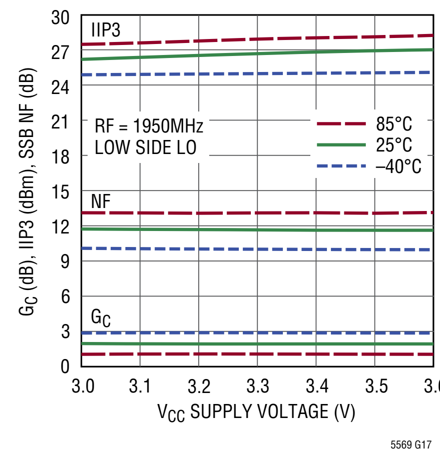
SSB Noise Figure vs RF Blocker Level



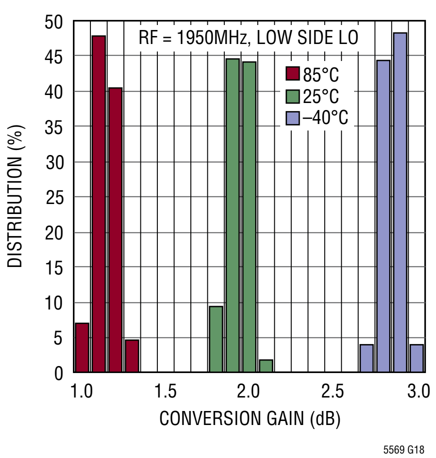
Conversion Gain, IIP3, NF and RF Input P1dB vs Temperature



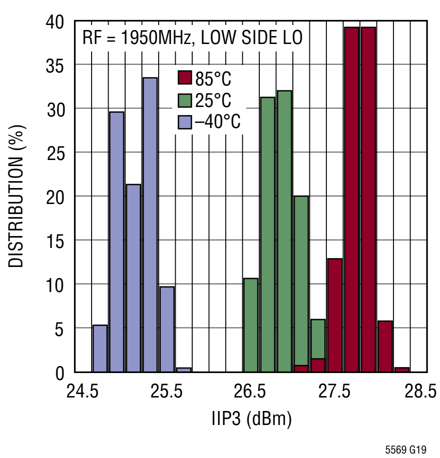
Conversion Gain, IIP3 and NF vs Supply Voltage



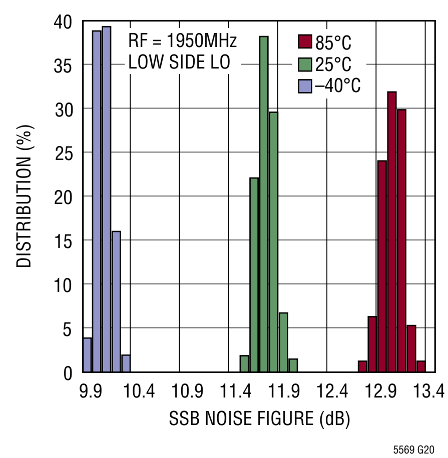
1950MHz Conversion Gain Histogram



1950MHz IIP3 Histogram



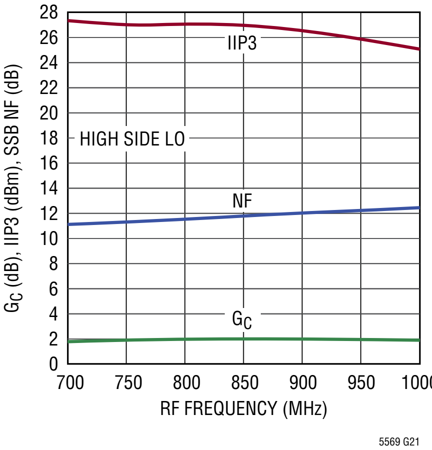
1950MHz SSB NF Histogram



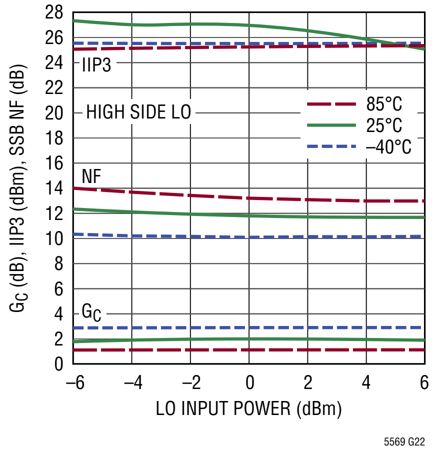
TYPICAL PERFORMANCE CHARACTERISTICS

700MHz to 1000MHz application. Test circuit shown in Figure 1. $V_{CC} = 3.3V$, $T_C = 25°C$, $P_{LO} = 0dBm$, $P_{RF} = -6dBm$ (–6dBm/tone for 2-tone IIP3 tests, $\Delta f = 2MHz$), IF = 190MHz unless otherwise noted.

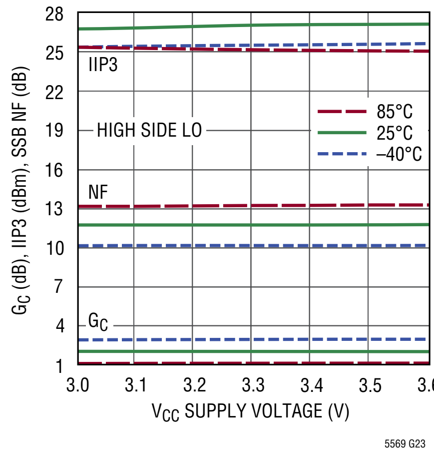
Conversion Gain, IIP3 and NF vs RF Frequency



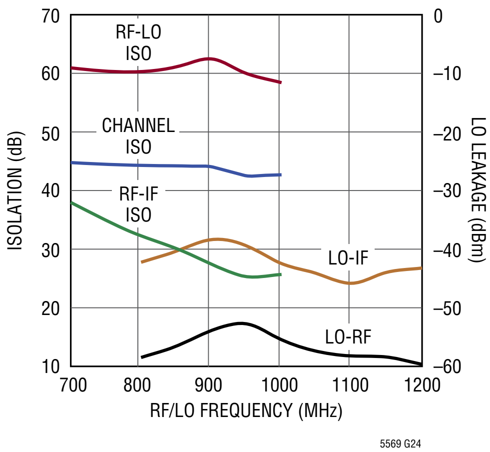
850MHz Conversion Gain, IIP3 and NF vs LO Power



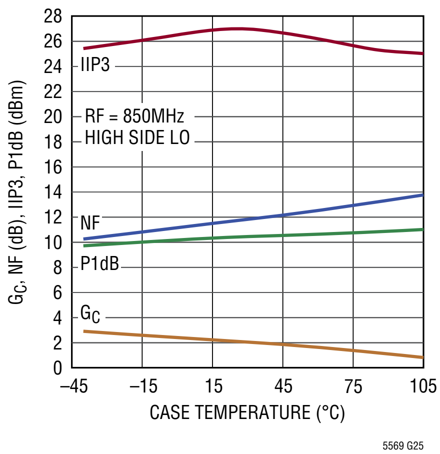
850MHz Conversion Gain, IIP3 and NF vs Supply Voltage



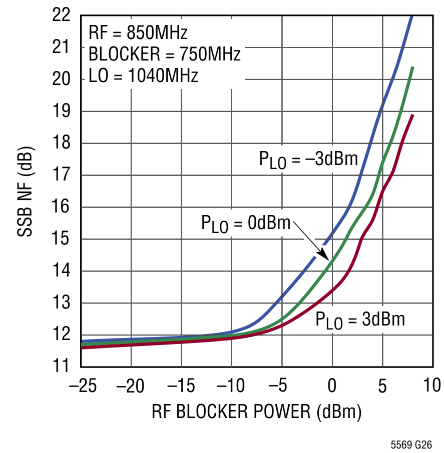
Channel Isolation, RF Isolation and LO Leakage vs Frequency



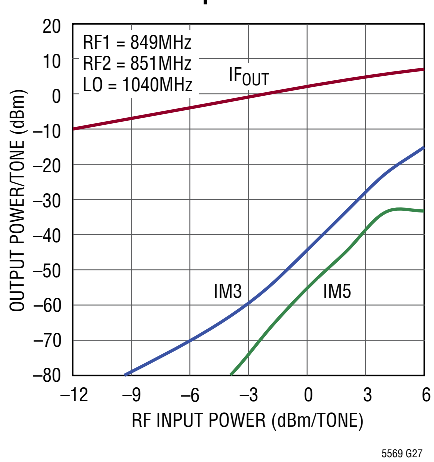
Conversion Gain, IIP3, NF and RF Input P1dB vs Temperature



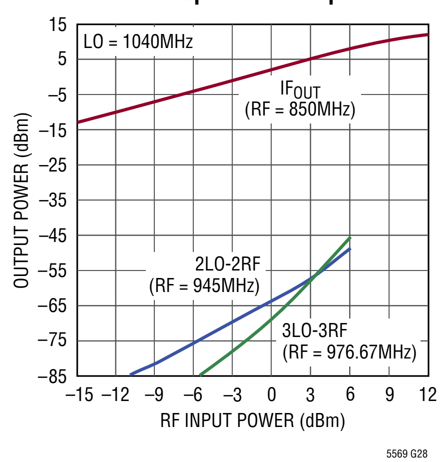
SSB Noise Figure vs RF Blocker Level



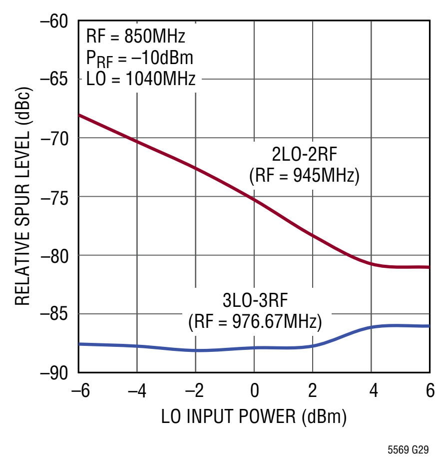
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



Single Tone IF Output Power 2 × 2 and 3 × 3 Spurs vs RF Input Power



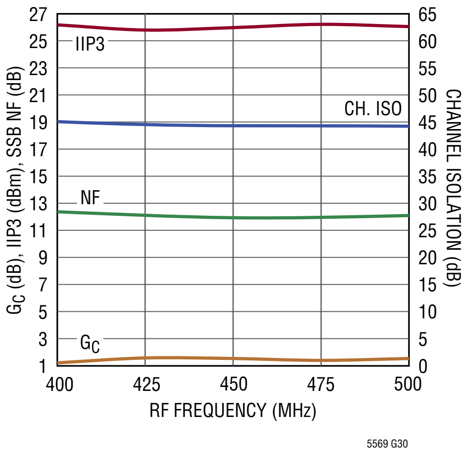
2 × 2 and 3 × 3 Spur Suppression vs LO Power



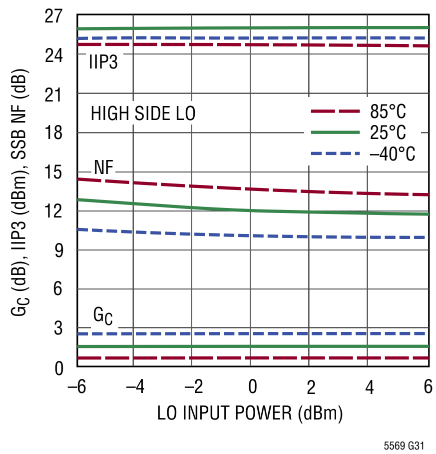
TYPICAL PERFORMANCE CHARACTERISTICS

400MHz to 500MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 190MHz unless otherwise noted.

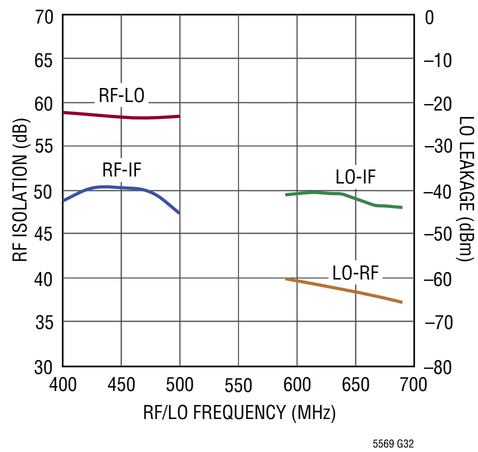
Conversion Gain, IIP3, NF and Channel Isolation vs RF Frequency



450MHz Conversion Gain, IIP3 and NF vs LO Power

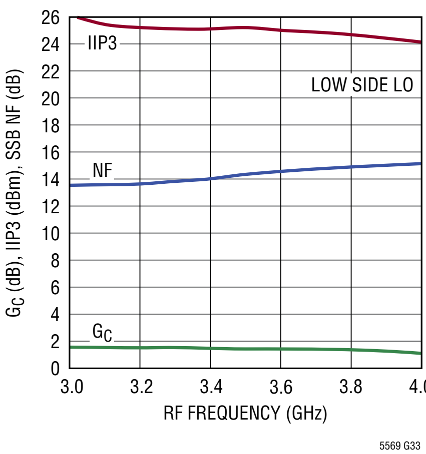


RF Isolation and LO Leakage vs RF and LO Frequency

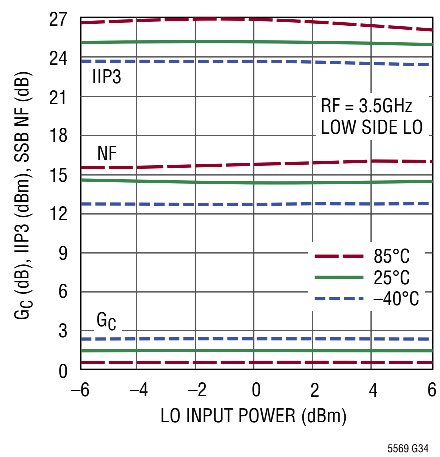


3GHz to 4GHz application. Test circuit shown in Figure 1.

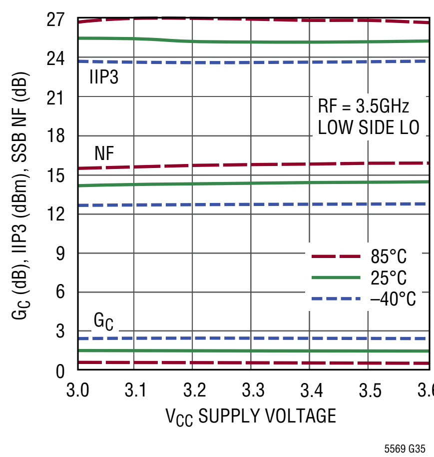
Conversion Gain, IIP3 and NF vs RF Frequency



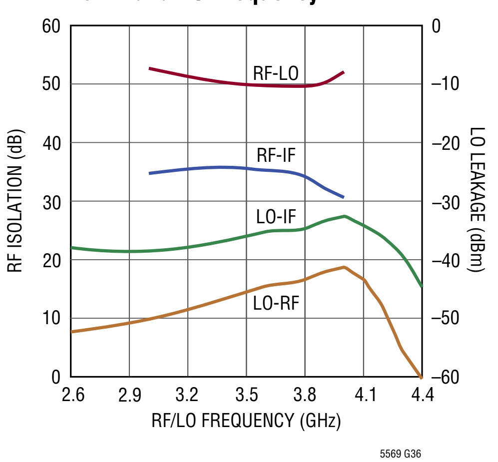
3500MHz Conversion Gain, IIP3 and NF vs LO Power



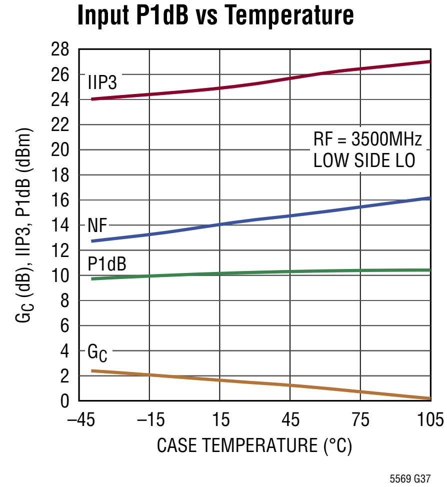
3500MHz Conversion Gain, IIP3 and NF vs Supply Voltage



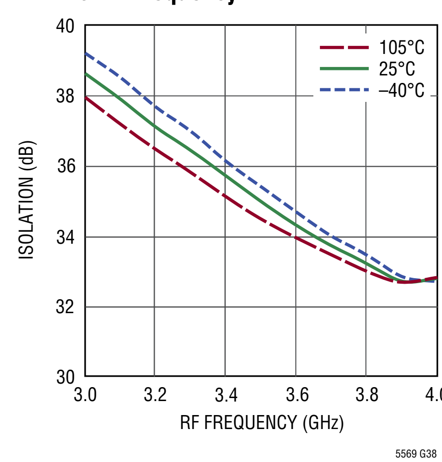
RF Isolation and LO leakage vs RF and LO Frequency



Conversion Gain, IIP3 and RF Input P1dB vs Temperature



Channel Isolation vs RF Frequency



PIN FUNCTIONS

RFA/RFB (Pin 1/Pin 4): Single-Ended RF Inputs for the A and B Mixers, Respectively. These pins are internally connected to the primary winding of the integrated RF transformers, which have low DC resistance to ground. **Series DC-blocking capacitors must be used if the RF sources have DC voltage present.** The RF inputs are 50Ω impedance matched from 1.4GHz to 3.3GHz, as long as the mixer is enabled. Operation down to 300MHz or up to 4GHz is possible with external matching.

GND (Pins 2, 3, 10, Exposed Pad Pin 17): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

LO (Pin 11): Single-Ended Local Oscillator Input. This pin is internally connected to the primary winding of an integrated transformer, which has low DC resistance to ground. **A series DC-blocking capacitor must be used to avoid damage to the internal transformer.** This input is 50Ω impedance matched from 1GHz to 3.5GHz, even when one or both mixers are disabled. Operation down to 350MHz or up to 4500MHz is possible with external matching.

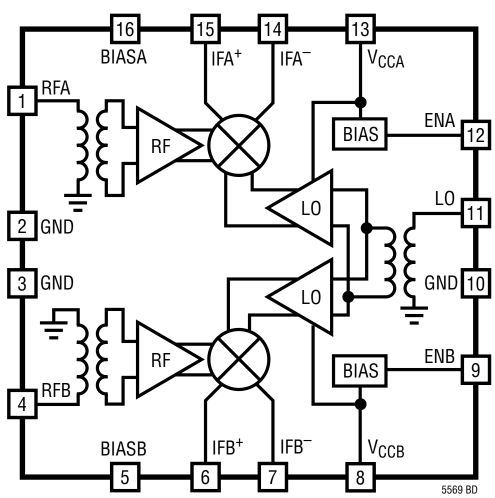
ENA/ENB (Pin 12/Pin 9): Enable Pins for the A and B Mixers, Respectively. When the input voltage is greater than 2.5V, the mixer is enabled. When the input voltage is less than 0.3V, the mixer is disabled. Typical input current is less than 30µA. These pins have internal pull-down resistors.

V_{CCA}/V_{CCB} (Pin 13/Pin 8): Power Supply Pins for the A and B Mixers, Respectively. These pins must be connected to a regulated 3.3V supply, with bypass capacitors located close to the pins. Typical DC current consumption is 34mA, each.

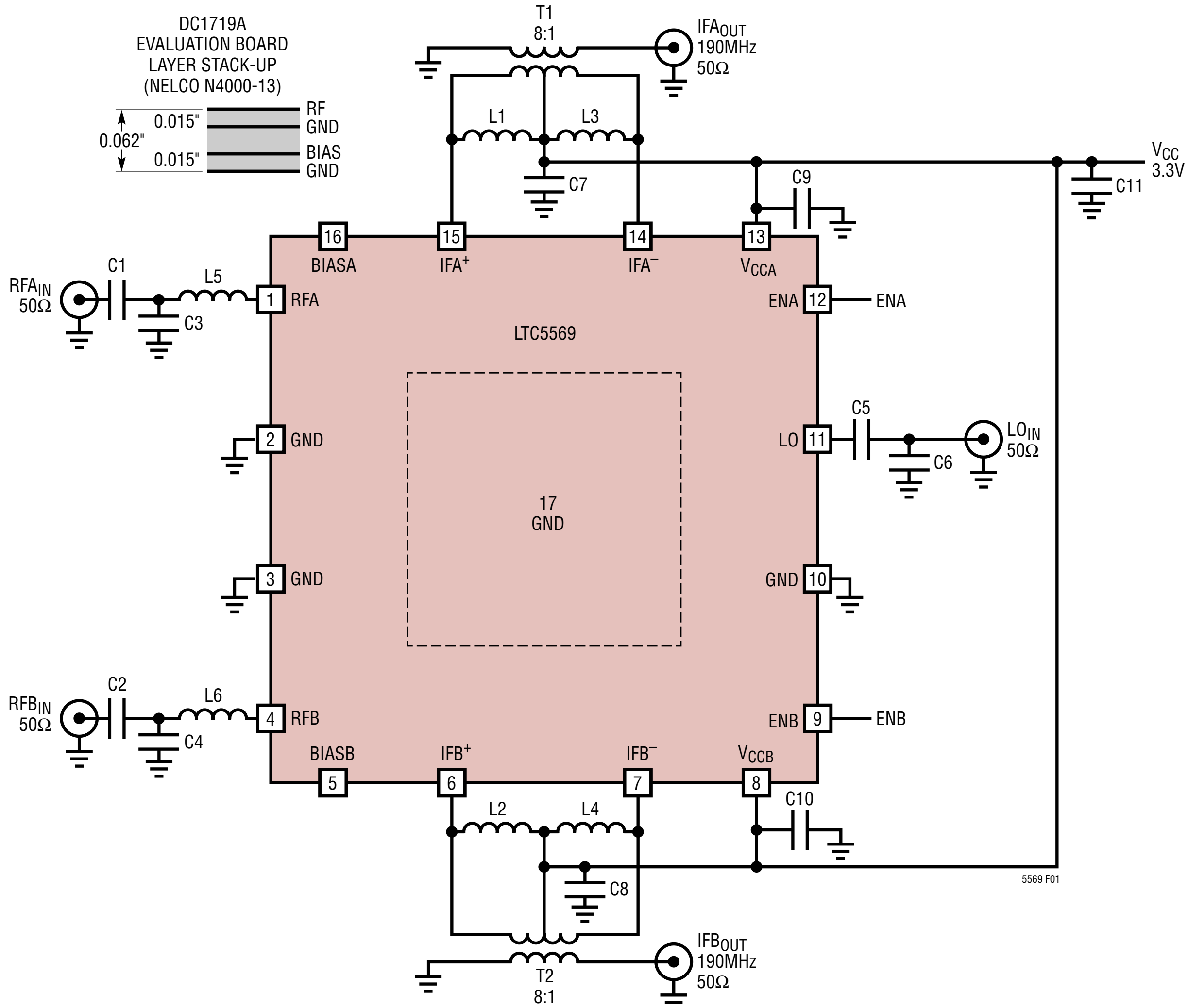
IFA^+/IFA^- (Pin 15/Pin 14), IFB^+/IFB^- (Pin 6/Pin 7): Open-Collector Differential IF Outputs for the A and B Mixers, Respectively. These pins must be connected to the V_{CC} supply through impedance-matching inductors or a transformer center tap. Typical DC current consumption is 28mA into each pin.

BIASA/BIASB (Pin 16/Pin 5): These pins allow adjustment of the mixer DC supply currents for mixers A and B, respectively. Typical, open-circuit DC voltage is 2.2V. These pins should be left open circuited for optimum performance.

BLOCK DIAGRAM



TEST CIRCUIT



APPLICATION		RF MATCH			LO MATCH	
RF (MHz)	**LO**	**C1, C2**	**C3, C4**	**L5, L6**	**C5**	**C6**
300 to 400	HS	120pF	18pF	3.3nH	1nF	10pF
400 to 500	HS	120pF	12pF	2nH	27pF	6.8pF
700 to 1000	HS	68pF	4.7pF	—	6.8pF	2.2pF
1400 to 3000	LS, HS	2.7pF	—	—	3.9pF	—
3000 to 4000	LS	3.9pF	0.7pF	—	3.9pF	0.3pF

LS = Low side, HS = High side

REF DES	VALUE	SIZE	VENDOR	REF DES	VALUE	SIZE	VENDOR
C1, C2	See Table	0402	AVX	C11	2.2µF	0603	AVX
C3, C4	See Table	0402	AVX	T1, T2	8:1	—	Mini-Circuits TC8-1-10LN+
C5	See Table	0402	AVX	L1- L4	180nH	0603	Coilcraft 0603HP
C6	See Table	0402	AVX	L5, L6	See Table	0402	Coilcraft 0402HP
C7-C10	10nF	0402	AVX				

Figure 1. Standard Downmixer Test Circuit Schematic (190MHz Bandpass IF Matching)

APPLICATIONS INFORMATION

Introduction

The LTC5569 incorporates two identical, symmetric double-balanced active mixers with a common LO input, separate RF inputs and separate IF outputs. See the Pin Functions and Block Diagram sections for a description of each pin. A test circuit schematic showing all external components required for the data sheet specified performance is shown in Figure 1. A few additional components may be used to modify the DC supply current or frequency response, which will be discussed in the following sections.

The LO and RF inputs are single ended. The IF outputs are differential. Low side or high side LO injection may be used. The test circuit, shown in Figure 1, utilizes bandpass IF output matching and 8:1 IF transformers to realize 50Ω single-ended IF outputs. The evaluation board layout is shown in Figure 2.

RF Inputs

A simplified schematic of the A-channel mixer's RF input is shown in Figure 3. The B-channel is identical, and not shown for clarity. As shown, one terminal of the integrated RF transformer's primary winding is connected to Pin 1, while the other terminal is DC-grounded internally. For this reason, a series DC-blocking capacitor (C1) is needed if the RF source has DC voltage present. The DC resistance of the primary winding is approximately 4Ω. The secondary winding of the RF transformer is internally connected to the RF buffer amplifier.

The RF inputs are 50Ω matched from 1400MHz to 3300MHz with a single 2.7pF series capacitor on each input. Matching to RF frequencies above or below this frequency range is easily accomplished by adding shunt capacitor C3, shown in Figure 3. For RF frequencies below 500MHz, series

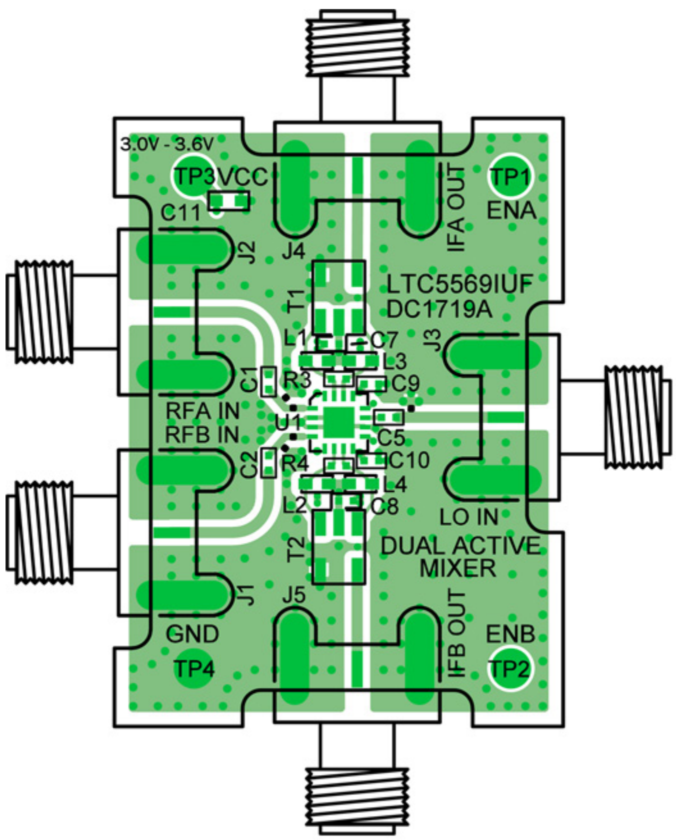


Figure 2. Evaluation Board Layout

APPLICATIONS INFORMATION

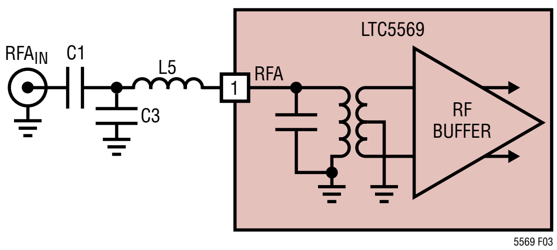


Figure 3. RF Input Schematic

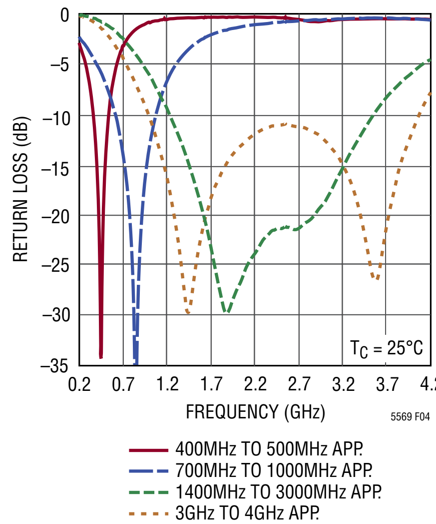


Figure 4. RF Input Return Loss

inductor L5 is also needed. The evaluation board does not include pads for the series inductors, so the 50Ω RF input traces need to be cut to install these in series. The RF input matching element values for each application are tabulated in Figure 1. Measured RF input return losses are shown in Figure 4. The RF input impedance and input reflection coefficient, versus frequency are listed in Table 1.

Table 1. RF Input Impedance and S11 (At Pin 1, No External Matching, Mixer Enabled)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
350	9.0 + j11.9	0.71	152.5
450	11.0 + j13.8	0.66	147.7
575	13.1 + j15.7	0.62	143.0
700	15.2 + j17.3	0.58	138.6
900	18.1 + j20.0	0.53	131.6
1100	21.3 + j22.4	0.49	124.6
1400	27.0 + j25.3	0.42	114.1
1700	33.4 + j26.8	0.36	103.9
1950	39.1 + j25.6	0.30	97.1
2200	43.4 + j21.5	0.23	94.2
2450	44.3 + j15.9	0.18	100.2
2700	40.8 + j9.9	0.15	126.5
3000	33.1 + j6.4	0.22	154.7
3300	24.3 + j6.8	0.36	159.9
3600	17.6 + j9.6	0.49	155.4
3900	12.9 + j12.7	0.61	149.6

LO Input

A simplified schematic of the LO input, with external components is shown in Figure 5. Similar to the RF inputs, the integrated LO transformer's primary winding is DC-grounded internally, and therefore requires an external

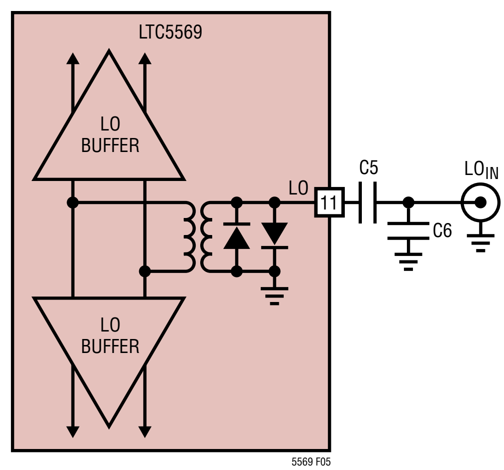


Figure 5. LO Input Schematic

DC-blocking capacitor. Capacitor C5 provides the necessary DC-blocking, and optimizes the LO input match over the 1GHz to 3.5GHz frequency range. The nominal LO input level is 0dBm although the limiting amplifiers will deliver excellent performance over a ±5dB input power range. LO input power greater than +6dBm may cause conduction of the internal ESD diodes.

To optimize the LO input match for frequencies below 1GHz, the value of C5 is increased and shunt capacitor C6 is added. A summary of values for C5 and C6, versus LO frequency range is listed in Table 2. Measured LO input

APPLICATIONS INFORMATION

return losses are shown in Figure 6. Finally, LO input impedance and input reflection coefficient, versus frequency is shown in Table 3.

Table 2. LO Input Matching Values vs LO Frequency Range

FREQUENCY (MHz)	C5 (pF)	C6 (pF)
350 to 430	390	22
480 to 630	68	12
576 to 722	27	6.8
720 to 980	15	4.7
814 to 1155	6.8	2.2
1000 to 3500	3.9	—
2200 to 4000	3.9	0.3

The LO buffers have been designed such that the LO input

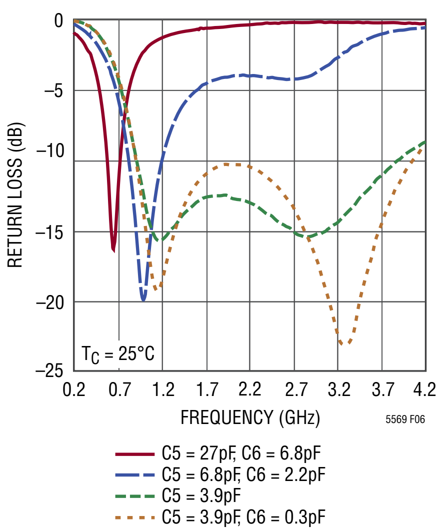


Figure 6. LO Input Return Loss

impedance does not change significantly when one or both mixers are disabled. This feature only requires that supply voltage is applied to both mixers. The actual performance of this feature is shown in Figure 7, where LO input return loss versus frequency is shown for the following three operating conditions: both mixers enabled, one mixer enabled, and both mixers disabled. As shown, the LO input return loss is better than 12dB over the 1000MHz to 3500MHz frequency range for all three operating states.

Table 3. LO Input Impedance and S11 (At Pin 11, No External Matching, Both Mixers Enabled)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
350	5.5 + j15.1	0.82	146.1
400	6.0 + j17.3	0.81	141.3
450	6.9 + j19.5	0.79	136.7
500	8.0 + j21.8	0.77	131.9
600	10.3 + j26.5	0.73	122.6
800	17.6 + j35.7	0.63	104.5
1000	29.5 + j43.6	0.53	86.5
1500	70.8 + j28.3	0.28	40.5
2000	60.1 – j4.2	0.10	–20.2
2500	41.8 – j3.2	0.10	–156.6
3000	33.1 + j7.4	0.22	151.3
3500	29.8 + j19.2	0.34	122.9
4000	29.5 + j29.9	0.43	103.7
4500	32.0 + j37.6	0.46	90.9

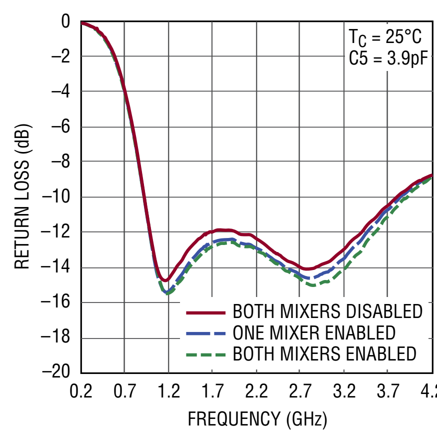


Figure 7. LO Input Return Loss for Three Operating States

IF Outputs

The A-channel IF output schematic with external matching components is shown in Figure 8. The B-channel is identical, and not shown for clarity. As shown, the outputs are differential open collector. Each IF output pin must

APPLICATIONS INFORMATION

be biased at the supply voltage (V_{CC}), which is applied through the external matching inductors (L1 and L3) shown in Figure 8. Alternatively, the IF outputs can be biased through the center tap of the IF transformer. Each IF output pin on the IC draws approximately 28mA of DC supply current (56mA total per mixer).

The differential IF output impedance can be modeled as a parallel R-C circuit. These R-C values are listed in Table 4, versus IF frequency. This data is referenced to the package pins (with no external components) and includes the effects of the IC and package parasitics. The values of L1 and L3 are calculated to resonate with the internal capacitance (C_{IF}) at the desired IF center frequency, using the following equation:

$$L1, L3 = \frac{1}{(2 \cdot \pi \cdot f_{IF})^2 \cdot 2 \cdot C_{IF}}$$

For IF frequencies below 130MHz, the matching inductors are not needed due to the low IF output capacitance. The evaluation board has the transformer center tap connected to the matching inductor center node, thus allowing the circuit to be used without matching inductors. The measured IF output return loss for this case is shown in Figure 9.

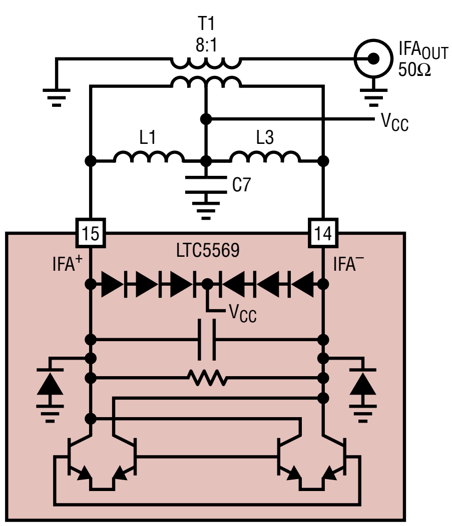


Figure 8. IF Output Schematic with Bandpass Matching and 8:1 Transformer

Table 4 summarizes the optimum IF matching inductor values, versus IF center frequency, to be used in the standard downmixer test circuit shown in Figure 1. The inductor values listed are less than the ideal calculated values due to the additional capacitance of the 8:1 transformer. For differential IF output applications where the 8:1 transformer is eliminated, the ideal calculated values should be used. Measured IF output return losses are shown in Figure 9.

Table 4. IF Output Impedance and Bandpass Matching Element Values vs IF Frequency.

IF FREQUENCY (MHz)	DIFFERENTIAL IF OUTPUT IMPEDANCE (R_{IF}‖C_{IF})	BANDPASS MATCHING L1, L3 (A) L2, L4 (B)
50	540Ω‖1.3pF	Open
140	532Ω‖1.3pF	330nH
190	530Ω‖1.3pF	180nH
240	525Ω‖1.3pF	110nH
300	519Ω‖1.3pF	72nH
380	511Ω‖1.3pF	43nH
456	502Ω‖1.3pF	30nH
580	490Ω‖1.33pF	
810	477Ω‖1.35pF	
1000	450Ω‖1.4pF	

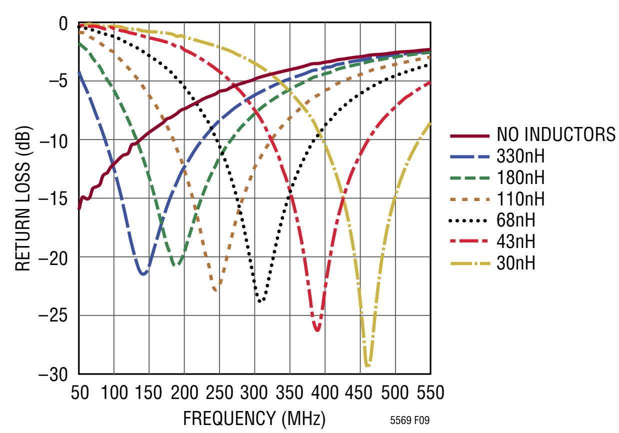


Figure 9. IF Output Return Loss—Bandpass Matching with 8:1 Transformer

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Wideband IF Using Load Resistor and 4:1 Transformer

Wide IF bandwidth and high input 1dB compression can be obtained by reducing the IF output resistance with a shunt resistor (R3), as shown in Figure 10. This will reduce the mixer's conversion gain, but will not degrade the IIP3 or noise figure. The evaluation board includes pads for R3 (and R4 for the B-channel). To accommodate the lower total IF resistance, transformer T1 should be changed from an 8:1 impedance ratio to a 4:1 ratio. The value of the external matching inductors L1 and L3 needs to be adjusted to account for the differences in the IF transformer parasitics.

Table 5 summarizes the measured conversion gain, IIP3, noise figure, RF input P1dB and IF bandwidth for three values of load resistor. Inductors L1 and L3 have been increased from 180nH to 270nH to keep the IF match centered at 190MHz (the 8:1 transformer has higher capacitance). Also shown, for comparison, is the measured performance using an 8:1 IF transformer and no load resistor. Measured conversion gain and IF output return loss versus IF frequency are shown for each case in Figure 11.

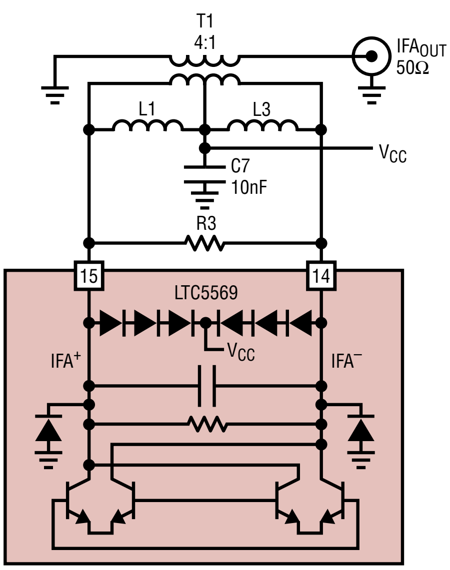

Figure 10. IF Output Schematic with Wideband Matching and 4:1 Transformer

Table 5. Measured Performance Using IF Load Resistor (R3) and 4:1 Transformer (RF = 1950MHz, Low-Side LO, IF = 190MHz, V_{CC} = 3.3V, T_C = 25°C)

IF XFMR	R3 (Ω)	G_C (dB)	IIP3 (dBm)	SSB NF (dB)	INPUT P1dB (dBm)	0.5dB IF BANDWIDTH (MHz)
8:1	—	2.0	26.8	11.7	10.2	–55/+85
4:1	1210	0.9	26.8	11.7	12.8	–90/+110
	604	0.0	26.8	11.7	13.0	–100/+120
	374	-1.1	26.8	11.8	13.3	–115/+120

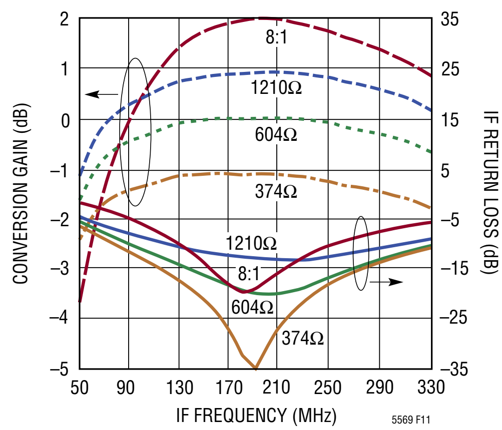

Figure 11. Conversion Gain and IF Output Return Loss vs IF Frequency—Wideband Matching with 4:1 Transformer

Discrete IF Balun Matching

For narrowband IF applications, it is possible to replace the IF transformer with the discrete IF balun shown in Figure 12 (only the A-channel is shown for clarity). The values of L3, L7, C13 and C15 are calculated to realize a 180° phase shift at the desired IF frequency, and provide a 50Ω single-ended output, using the equations listed below. Inductor L1 is calculated to cancel the internal IF capacitance (C_{IF} from Table 4). L1 and L3 also supply DC bias to the IF output pins. R5 and R7 are used to reduce the differential output resistance (R_S), which increases

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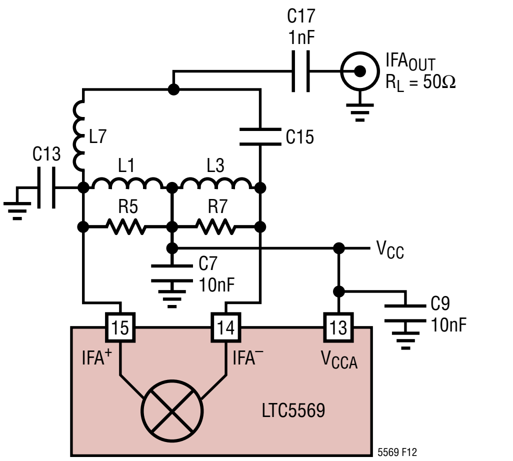


Figure 12. Discrete IF Balun Matching

the IF bandwidth, but reduces the conversion gain. C17 is a DC-blocking capacitor.

$$R_S = \frac{2 \cdot R5 \cdot R_{IF}}{2 \cdot R5 + R_{IF}} \qquad (R5 = R7)$$

$$L1 = \frac{1}{2 \cdot C_{IF} \cdot (\omega_{IF})^2}$$

$$L7 = \frac{\sqrt{R_S \cdot R_L}}{\omega_{IF}}$$

$$L3 = \frac{L1 \cdot L7}{L1 + L7}$$

$$C13, C15 = \frac{1}{\omega_{IF}\sqrt{R_S \cdot R_L}}$$

These equations give a good starting point, but it is usually necessary to adjust the component values after building and testing the circuit. The final solution can be achieved with less iteration by considering the parasitics of L1 and L3 in the above calculations. Specifically, the effective parallel resistance of L1 and L3 (calculated from the manufacturers Q data) will reduce the value of R_S, which in turn influences the calculated values of L7, C13 and C15. Also, the effective parallel capacitance of L1 and L3 (taken from the manufacturers SRF data) must be considered, since it is in parallel with C_{IF}. Frequently, the calculated value for L7 does not fall on a standard value for the desired IF. In this case, a simple solution is to vary the value of R5 (R7), which changes the value of R_S, until L7 is a standard value.

Discrete IF balun element values for five common IF frequencies are listed in Table 6. Measured IF output return losses are shown in Figure 13. Measured conversion gain, IIP3 and noise figure versus IF output frequency is shown in Figure 14.

Compared to the transformer-based IF matching technique, the most significant performance difference, as shown in Figure 14, is the limited IF bandwidth. For low IF frequencies, the passband bandwidth is small, whereas higher IF frequencies offer wider bandwidth.

Table 6. Discrete IF Balun Element Values (R_L = 50Ω) (Values Shown for the A Channel and B Channel

IF (MHz)	R5, R7 (A) R6, R8 (B) (Ω)	L1 (A) L2 (B) (nH)	L3 (A) L4 (B) (nH)	L7 (A) L8 (B) (nH)	C13, C15 (A) C14, C16 (B) (pF)
170	475	330	91	120	7
190	750	270	82	120	6
240	332	180	56	82	5.6
300	604	110	43	72	3.9
380	475	68	30	56	3.3

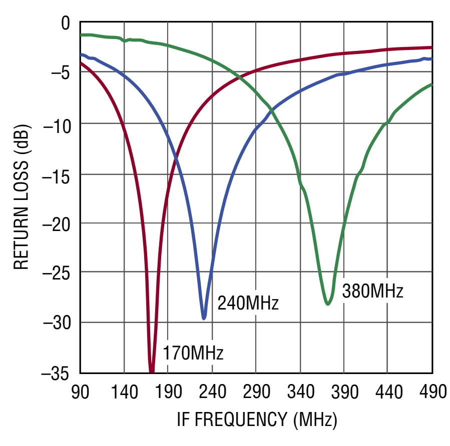


Figure 13. IF Output Return Losses with Discrete IF Balun Matching

APPLICATIONS INFORMATION

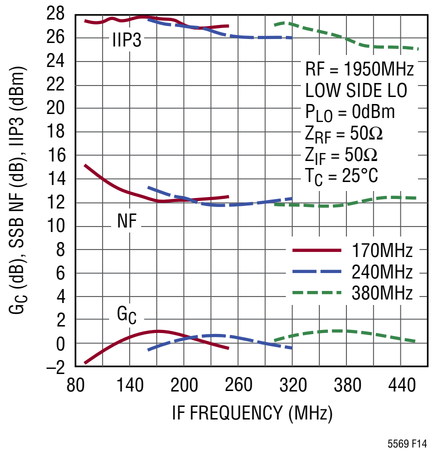


Figure 14. Conversion Gain, IIP3 and SSB NF vs IF Output Frequency Using Discrete IF Balun Matching

Mixer Bias Current Reduction

The BIASA and BIASB pins (Pins 16 and 5) are available for reducing the mixer core DC current consumption, of the A- and B-channels, respectively, at the expense of linearity and P1dB. For the highest performance, these pins should be left open circuit. As shown in Figure 15, an internal bias circuit produces a 3mA reference current for each mixer core. If a resistor is connected to Pin 16, as shown in Figure 15, a portion of the reference current can be shunted to ground, resulting in reduced mixer core current. For example, R1 = 1k will shunt away 1mA from Pin 16 and reduce the mixer core current by 33%. The nominal, open-circuit DC voltage at the BIASA and BIASB pins is 2.2V. Table 7 lists DC supply current and RF performance at 1950MHz for various values of R1.

Table 7. Mixer Performance with Reduced Current (RF = 1950MHz, Low Side LO, IF = 190MHz)

R1 (Ω)	I_{CC} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
Open	90.0	2.0	26.8	10.2	11.7
10k	85.2	1.9	25.6	10.2	11.4
1k	71.0	1.6	21.4	10.1	10.4
100	58.6	1.1	17.9	8.9	10.0

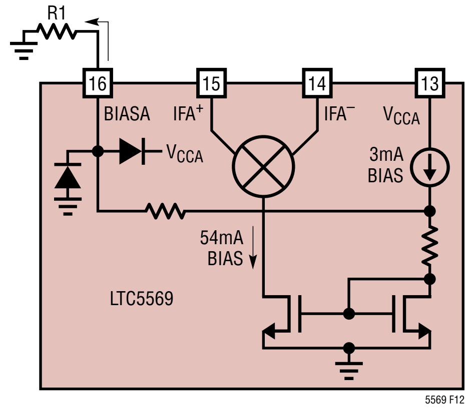


Figure 15. BIASA Interface (BIASB is Identical)

Enable Interfaces

Figure 16 shows a simplified schematic of the A-channel enable interface. The B-channel is identical, and not shown for clarity. To enable the A-channel mixer, the ENA voltage must be higher than 2.5V. If the enable function is not required, the pin should be connected directly to V_{CC}. The voltage at the ENA pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

The ENA and ENB pins have internal 300k pull-down resistors. Therefore, an unused mixer will be disabled with its corresponding enable pin left floating.

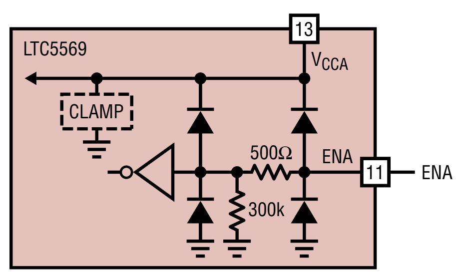


Figure 16. Enable Input Circuit

APPLICATIONS INFORMATION

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD clamp circuits connected to the V_{CCA} and V_{CCB} pins. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the 4.0V maximum rating. A supply voltage ramp time greater than 1ms is recommended.

Spurious Output Levels

Mixer spurious output levels versus harmonics of the RF and LO are tabulated in Table 8. The spur levels were measured on a standard evaluation board using the test circuit shown in Figure 1. The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) - (N \bullet f_{LO})$$

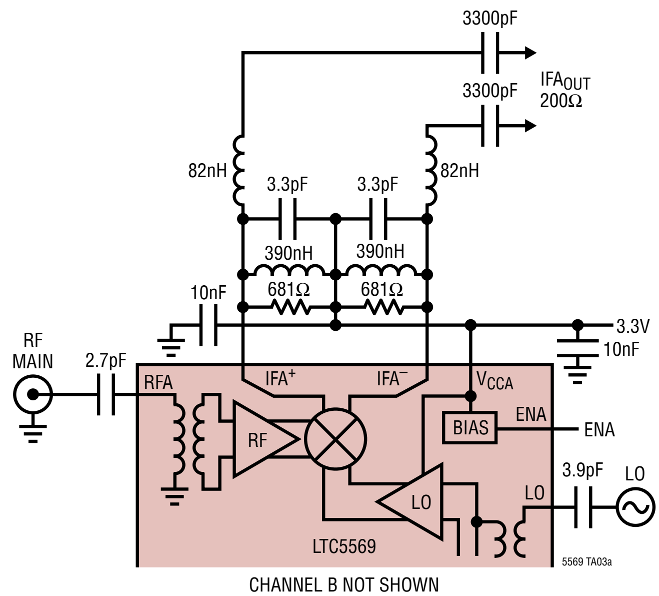
Table 8. IF Output Spur Levels (dBm)
(RF = 1950MHz, P_{RF} = –2dBm, P_{IF} = 0dBm at 190MHz, Low Side LO, P_{LO} = 0dBm, V_{CC} = 3.3V, T_C = 25°C)

		N									
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
	0		–56	–24	–58	–36	–51	–44	–58	–49	–80
	1	–32	0	–56	–57	–68	–41	–69	–52	–75	–58
	2	–59	–56	–67	–65	–76	–85	–71	–85	–80	*
M	3	*	–88	–89	–74	*	*	*	*	–89	*
	4	*	*	–85	*	*	*	*	*	–85	*
	5	*	*	*	*	*	*	*	*	*	*
	6		*	*	*	*	*	*	*	*	*
	7				*	*				*	

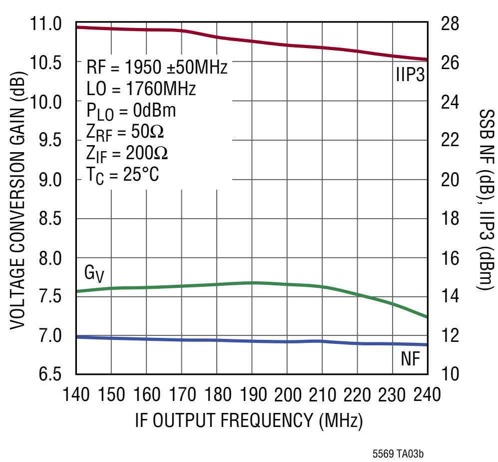
*Less than –90dBc

TYPICAL APPLICATION

200Ω Differential Lowpass IF Output Matching (Element Values Shown for 190MHz IF)



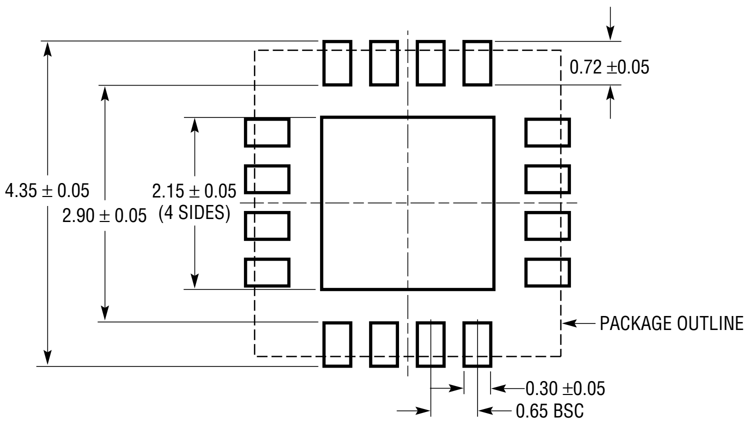
Voltage Conversion Gain, IIP3 and NF vs IF Frequency



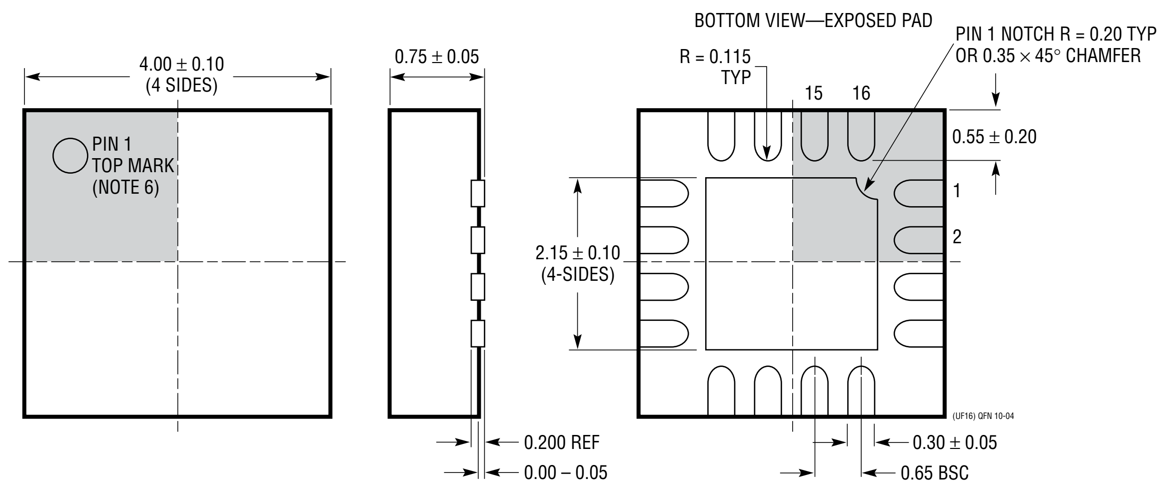
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



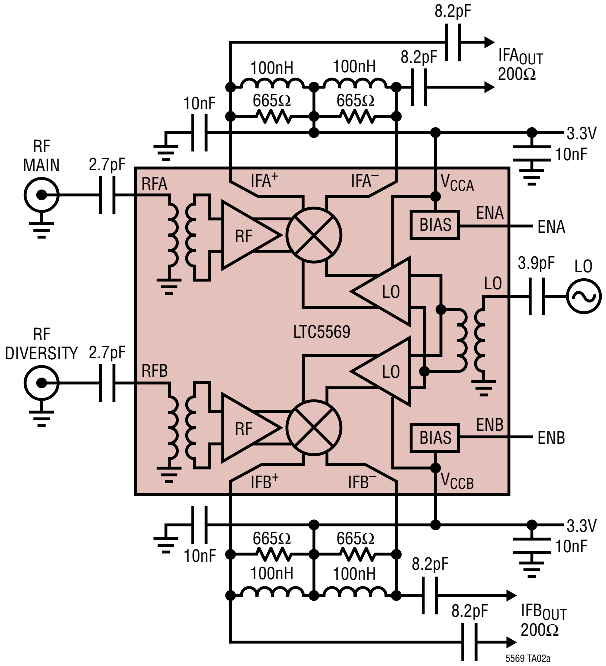
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

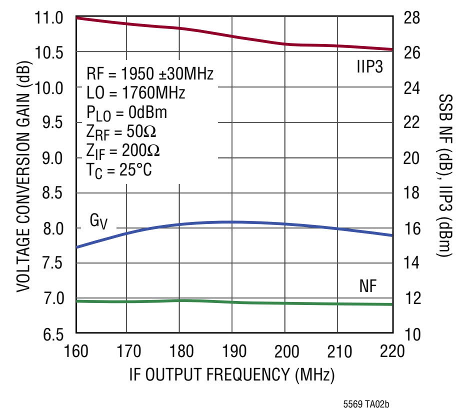
REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/11	Revised Turn-On Time and Turn-Off Time Typical values in DC Electrical Characteristics	4
B	11/14	Increase RF Input Absolute Maximum power rating	2
		Correct (increase) LO Input Power Absolute Maximum Frequency range	2
		Clarify Case Temperature range in Order Information	2
		Extend IF Output Frequency range down to low frequency	2
		Clarify Case Temperature on Supply Current graphs	4
		Correct x-axis label on graph G25	7

TYPICAL APPLICATION

200Ω Differential Highpass IF Output Matching (Element Values Shown for 190MHz IF)



Voltage Conversion Gain, IIP3 and NF vs IF Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LTC559x	600MHz to 4.5GHz Dual Downconverting Mixer Family	8.5dB Gain, 26.5dBm IIP3, 9.9dB NF, 3.3V/380mA Supply
LT5527	400MHz to 3.7GHz, 5V Downconverting Mixer	2.3dB Gain, 23.5dBm IIP3 and 12.5dB NF at 1900MHz, 5V/78mA Supply
LT5557	400MHz to 3.8GHz, 3.3V Downconverting Mixer	2.9dB Gain, 24.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/82mA Supply
LTC6400-X	300MHz Low Distortion IF Amp/ADC Driver	Fixed Gain of 8dB, 14dB, 20dB and 26dB; >36dBm OIP3 at 300MHz, Differential I/O
LTC6416	2GHz 16-Bit ADC Buffer	40dBm OIP3 to 300MHz, Programmable Fast Recovery Output Clamping
LTC6412	31dB Linear Analog VGA	35dBm OIP3 at 240MHz, Continuous Gain Range –14dB to 17dB
LT5554	Ultralow Distort IF Digital VGA	48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps
LT5575	700MHz to 2.7GHz I/Q Demodulator	28dBm IIP3, 13dBm P1dB, 0.03dB I/Q Amplitude Match, 0.4° Phase Match
LT5578	400MHz to 2.7GHz Upconverting Mixer	27dBm OIP3 at 900MHz, 24.2dBm at 1.95GHz, Integrated RF Transformer
LT5579	1.5GHz to 3.8GHz Upconverting Mixer	27.3dBm OIP3 at 2.14GHz, NF = 9.9dB, 3.3V Supply, Single-Ended LO and RF Ports
LTC5588-1	200MHz to 6GHz I/Q Modulator	31dBm OIP3 at 2.14GHz, –160.6dBm/Hz Noise Floor
RF Power Detectors		
LT5538	40MHz to 3.8GHz Log Detector	±0.8dB Accuracy Over Temperature, –72dBm Sensitivity, 75dB Dynamic Range
LT5581	6GHz Low Power RMS Detector	40dB Dynamic Range, ±1dB Accuracy Over Temperature, 1.5mA Supply Current
LTC5582	40MHz to 10GHz RMS Detector	±0.5dB Accuracy Over Temperature, ±0.2dB Linearity Error, 57dB Dynamic
LTC5583	Dual 6GHz RMS Power Detector	Up to 60dB Dynamic Range, ±0.5dB Accuracy Over Temperature, >50dB Isolation
ADCs		
LTC2208	16-Bit, 130Msps ADC	78dBFS Noise Floor, >83dB SFDR at 250MHz
LTC2285	Dual 14-Bit, 125Msps Low Power ADC	72.4dB SNR, 88dB SFDR, 790mW Power Consumption
LTC2268-14	Dual 14-Bit, 125Msps Serial Output ADC	73.1dB SNR, 88dB SFDR, 299mW Power Consumption

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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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