



MIC23163/4

4MHz, 2A, 100% Duty Cycle Buck Regulator
with HyperLight Load[®] and Power Good

General Description

The MIC23163/4 is a high-efficiency, 4MHz, 2A, synchronous buck regulator with HyperLight Load[®] (HLL) mode and maximum 100% duty cycle. HLL provides very-high efficiency at light loads and ultra-fast transient response which makes the MIC23163/4 perfectly suited for supplying processor core voltages. An additional benefit of this proprietary architecture is very low output ripple voltage throughout the entire load range with the use of small output capacitors. The tiny 2.0mm × 2.0mm DFN package saves precious board space and requires only three external components.

The MIC23163/4 is designed for use with a very small 0.47μH inductor and 10μF output capacitor that enables a total solution size, less than 1mm height.

The MIC23163/4 has a very low quiescent current of 33μA and achieves as high as 85% efficiency at 1mA. At higher loads, the MIC23163/4 provides a constant switching frequency around 4MHz while achieving peak efficiencies up to 93%. The MIC23164 incorporates an active discharge feature that switches an 180Ω FET to ground to discharge the output when the part is disabled.

The MIC23163/4 is available in 10-pin 2.0mm × 2.0mm DFN package with an operating junction temperature range from -40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

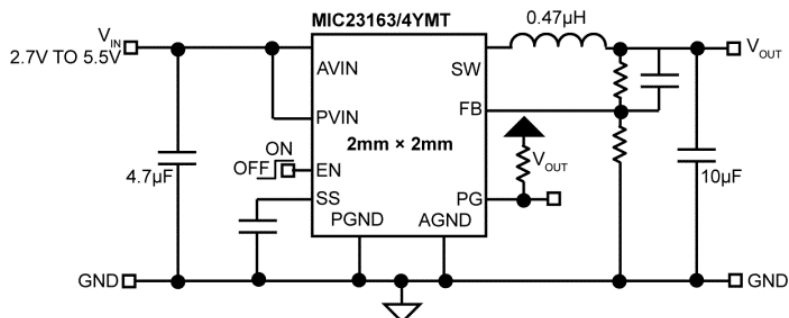
Features

- Input voltage: 2.7V to 5.5V
- 100% duty cycle
- 2A output current
- Up to 93% peak efficiency
- 85% typical efficiency at 1mA
- Programmable soft-start with pre-bias start-up capability
- Power Good (PG) Indicator
- 4MHz PWM operation in continuous mode
- Ultra-fast transient response
- Low ripple output voltage
- Fully-integrated MOSFET switches
- 0.1μA shutdown current
- Thermal shutdown and current-limit protection
- 10-pin 2.0mm × 2.0mm Thin DFN
- -40°C to +125°C junction temperature range
- Disable pull down 180Ω (MIC23164 only)

Applications

- Cellular modems
- Mobile handsets
- Portable media/MP3 players
- Portable navigation devices (GPS)
- WiFi/WiMax/WiBro modules
- Digital cameras
- Wireless LAN cards

Typical Application



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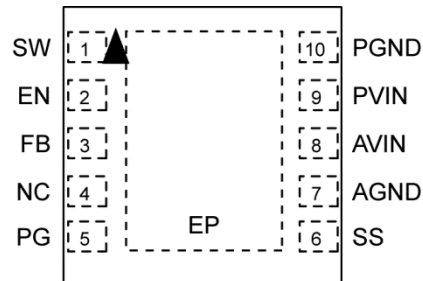
Ordering Information

Part Number	Marking Code	Output Voltage	Auto Discharge	Junction Temperature Range	Package ^(1, 2)
MIC23163YMT	QAQ	ADJ	No	-40°C to +125°C	10-Pin 2mm × 2mm Thin DFN
MIC23164YMT	KQA	ADJ	Yes	-40°C to +125°C	10-Pin 2mm × 2mm Thin DFN

Note:

- DFN is a GREEN, RoHS-compliant package. Mold compound is Halogen Free.
- DFN ▲ = Pin 1 identifier.

Pin Configuration



**2mm × 2mm DFN (MT)
Adjustable Output Voltage
(Top View)**

Pin Description

Pin Number	Pin Name	Pin Function
1	SW	Switch (Output): Internal power MOSFET output switches. Disable pull down 180Ω (MIC23164 only).
2	EN	Enable (Input): Logic high enables operation of the regulator. Logic low will shut down the device. Do not leave floating.
3	FB	Feedback: Connect a resistor divider from the output to ground to set the output voltage.
4	NC	Not Internally Connected.
5	PG	Power Good: Open drain output for the power good indicator. Use a pull-up resistor from this pin to a voltage source to detect a power good condition.
6	SS	Soft Start: Place a capacitor from this pin to ground to program the soft start time. Do not leave floating, 100pF minimum C _{SS} is required.
7	AGND	Analog Ground: Connect to central ground point where all high-current paths meet (C _{IN} , C _{OUT} , PGND) for best operation.
8	AVIN	Analog Input Voltage: Connect a capacitor to ground to decouple the noise.
9	PVIN	Power Input Voltage: Connect a capacitor to PGND to decouple the noise.
10	PGND	Power Ground.
EP	ePad	Exposed Pad. Connect to GND.

Absolute Maximum Ratings⁽³⁾

Supply Voltage (V_{AVIN} , V_{PVIN})	-0.3V to 6V
Power Good Voltage (V_{PG})	-0.3V to 6V
Output Switch Voltage (V_{SW})	-0.3V to 6V
Enable Input Voltage (V_{EN})	-0.3V to V_{IN}
Junction Temperature (T_J)	+150°C
Storage Temperature Range (T_S)	-65°C to +150°C
Lead Temperature (soldering, 10s)	260°C
ESD Rating ⁽⁵⁾	ESD Sensitive

Operating Ratings⁽⁴⁾

Supply Voltage (V_{AVIN} , V_{PVIN})	2.7V to 5.5V
Enable Input Voltage (V_{EN})	0V to V_{IN}
Feedback Voltage (V_{FB})	0.7V to V_{IN}
Junction Temperature Range (T_J)	-40°C ≤ T_J ≤ +125°C
Thermal Resistance	
2mm x 2mm Thin DFN -10 (θ_{JA})	90°C/W
2mm x 2mm Thin DFN -10 (θ_{JC})	45°C/W

Electrical Characteristics⁽⁶⁾

$T_A = 25^\circ\text{C}$; $V_{IN} = V_{EN} = 3.6\text{V}$; $L = 0.47\mu\text{H}$; $C_{OUT} = 10\mu\text{F}$ unless otherwise specified. **Bold** values indicate $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, unless otherwise noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage Range		2.7		5.5	V
Undervoltage Lockout Threshold	(Turn-On)	2.40	2.53	2.65	V
Undervoltage Lockout Hysteresis			75		mV
Quiescent Current	$I_{OUT} = 0\text{mA}$, $V_{SNS} > 1.2 \times V_{OUT}$ Nominal		33	55	μA
Shutdown Current	$V_{EN} = 0\text{V}$; $V_{IN} = 5.5\text{V}$		0.1	5	μA
Output Voltage Accuracy	$V_{IN} = 3.6\text{V}$ if $V_{OUTNOM} < 2.5\text{V}$, $I_{LOAD} = 20\text{mA}$	-2.5		+2.5	%
	$V_{IN} = 4.5\text{V}$ if $V_{OUTNOM} \geq 2.5\text{V}$, $I_{LOAD} = 20\text{mA}$				
Feedback Regulation Voltage		0.68	0.7	0.72	V
Current Limit	$V_{SNS} = 0.9 \times V_{OUTNOM}$	2.5	3.3		A
Output Voltage Line Regulation	$V_{IN} = 3.6\text{V}$ to 5.5V if $V_{OUTNOM} < 2.5\text{V}$, $I_{LOAD} = 20\text{mA}$		0.3		%/V
	$V_{IN} = 4.5\text{V}$ to 5.5V if $V_{OUTNOM} \geq 2.5\text{V}$, $I_{LOAD} = 20\text{mA}$				
Output Voltage Load Regulation	$20\text{mA} < I_{LOAD} < 500\text{mA}$, $V_{IN} = 3.6\text{V}$ if $V_{OUTNOM} < 2.5\text{V}$		0.3		%
	$20\text{mA} < I_{LOAD} < 500\text{mA}$, $V_{IN} = 5.0\text{V}$ if $V_{OUTNOM} \geq 2.5\text{V}$				
	$20\text{mA} < I_{LOAD} < 1\text{A}$, $V_{IN} = 3.6\text{V}$ if $V_{OUTNOM} < 2.5\text{V}$				
	$20\text{mA} < I_{LOAD} < 1\text{A}$, $V_{IN} = 5.0\text{V}$ if $V_{OUTNOM} \geq 2.5\text{V}$				
PWM Switch ON-Resistance	$I_{SW} = 100\text{mA}$ PMOS		0.13		Ω
	$I_{SW} = -100\text{mA}$ NMOS		0.13		
Switching Frequency	$I_{OUT} = 120\text{mA}$		4		MHz
Soft-Start Time	$V_{OUT} = 90\%$, $C_{SS} = 1\text{nF}$		1000		μs
Soft-Start Current	$V_{SS} = 0\text{V}$		2.2		μA
Power Good Threshold (Rising)	% of V_{NOM}	85	90	95	%

Notes:

- Exceeding the absolute maximum ratings may damage the device.
- The device is not guaranteed to function outside its operating ratings.
- Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5k Ω in series with 100pF.
- Specification for packaged product only.

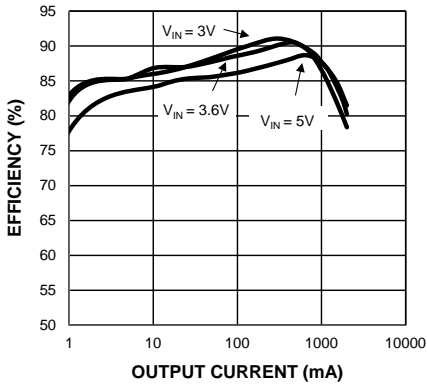
Electrical Characteristics⁽⁶⁾ (Continued)

$T_A = 25^\circ\text{C}$; $V_{IN} = V_{EN} = 3.6\text{V}$; $L = 0.47\mu\text{H}$; $C_{OUT} = 10\mu\text{F}$ unless otherwise specified. **Bold** values indicate $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, unless otherwise noted.

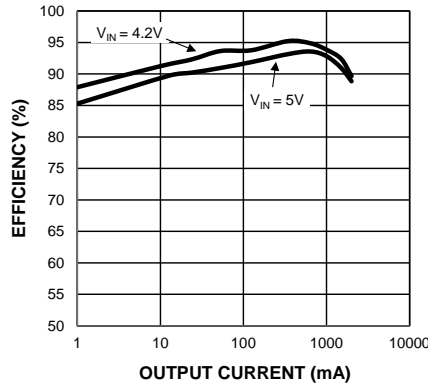
Parameter	Condition	Min.	Typ.	Max.	Units
Power Good Threshold Hysteresis			7		%
Power Good Pull-Down	$V_{SNS} = 90\% V_{NOMINAL}$, $I_{PG} = 1\text{mA}$			200	mV
Enable Threshold	Turn-On	0.5	0.8	1.2	V
Enable Input Current			0.1	2	μA
Overtemperature Shutdown			160		$^\circ\text{C}$
Overtemperature Shutdown Hysteresis			20		$^\circ\text{C}$
SW Pull-Down Resistance (MIC23164 only)	$V_{EN} = 0\text{V}$		180		Ω

Typical Characteristics

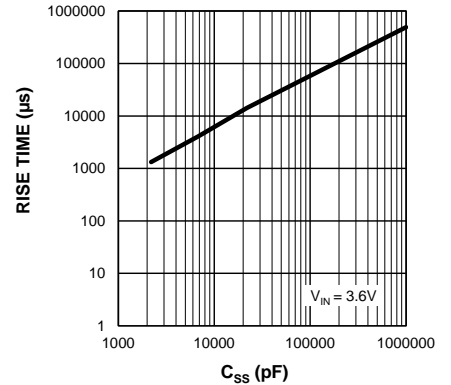
Efficiency vs. Output Current
 $V_{OUT} = 1.8V @ 25^{\circ}C$



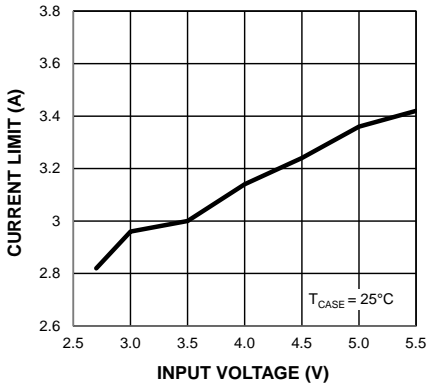
Efficiency vs. Output Current
 $V_{OUT} = 3.3V @ 25^{\circ}C$



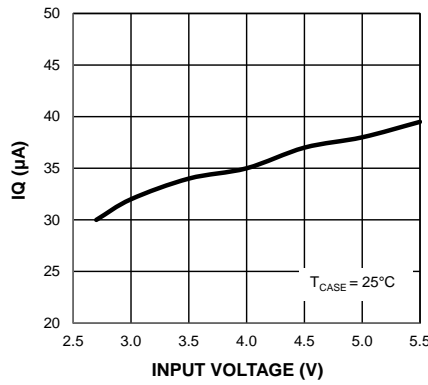
V_{OUT} Rise Time vs. C_{SS}



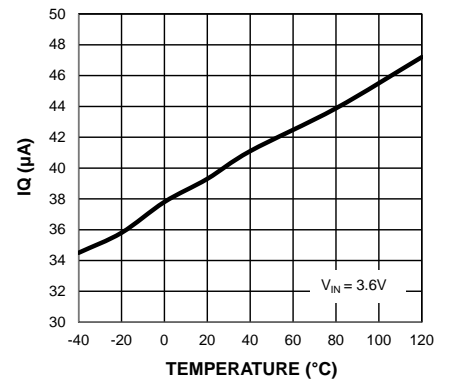
Current Limit vs. Input Voltage



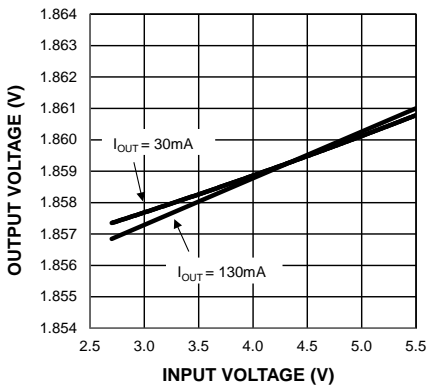
Quiscent Current vs. Input Voltage



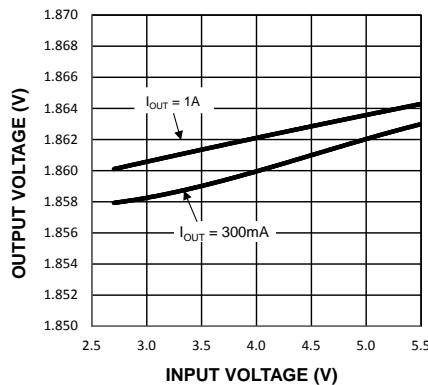
IQ vs. Temperature



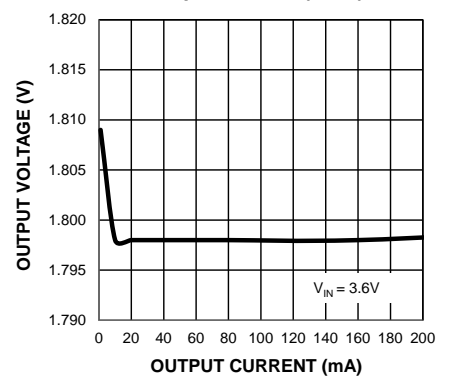
Line Regulation (Light Loads)



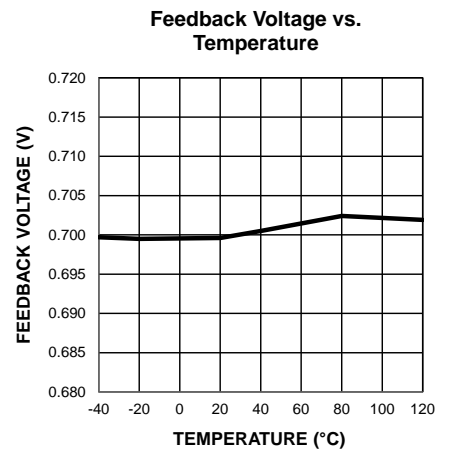
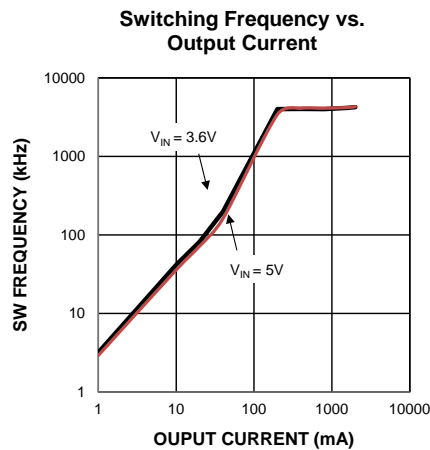
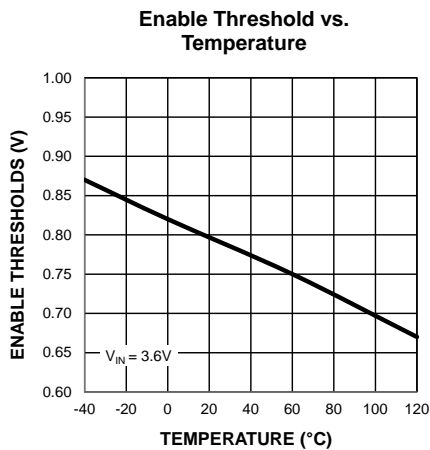
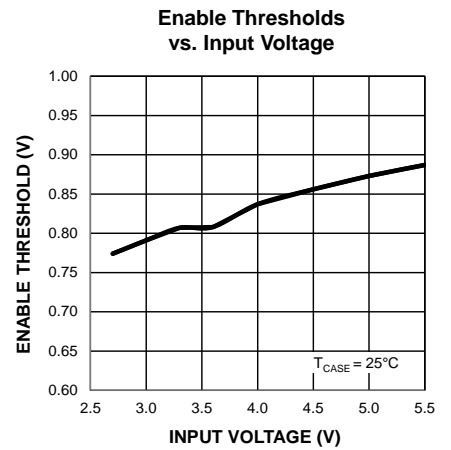
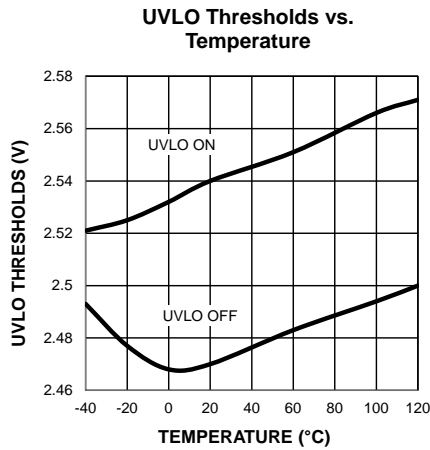
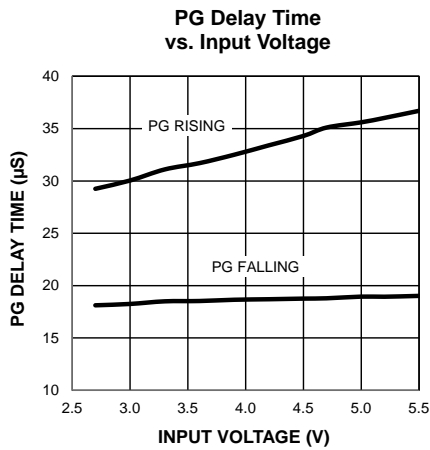
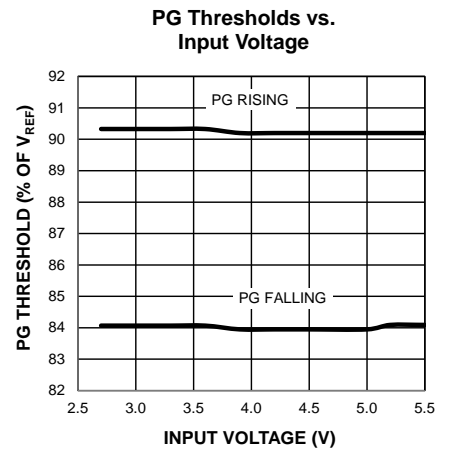
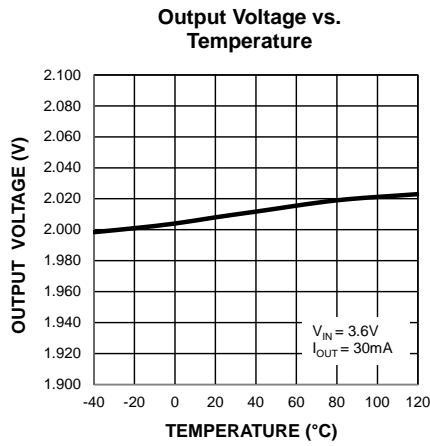
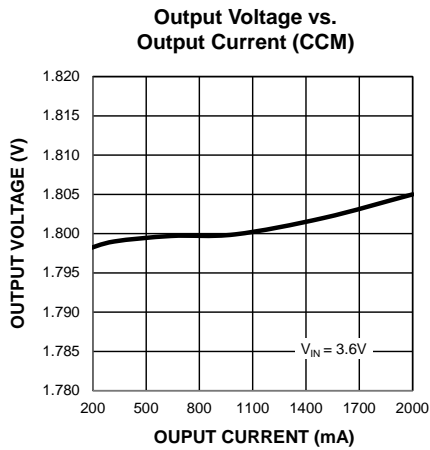
Line Regulation (High Loads)



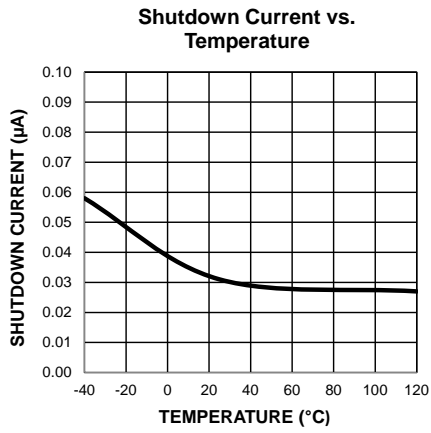
Output Voltage vs. Output Current (DCM)



Typical Characteristics (Continued)

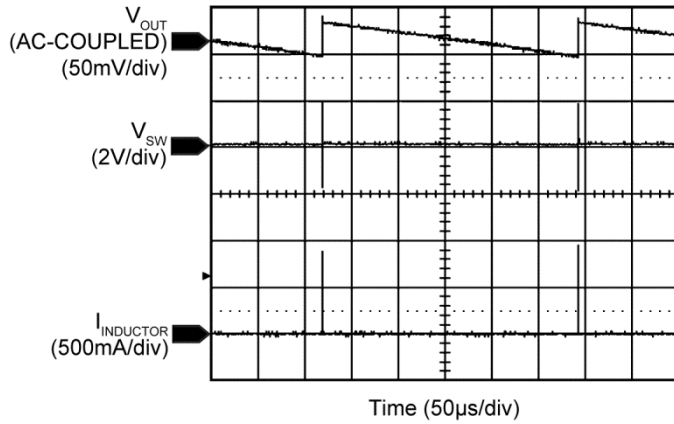


Typical Characteristics (Continued)

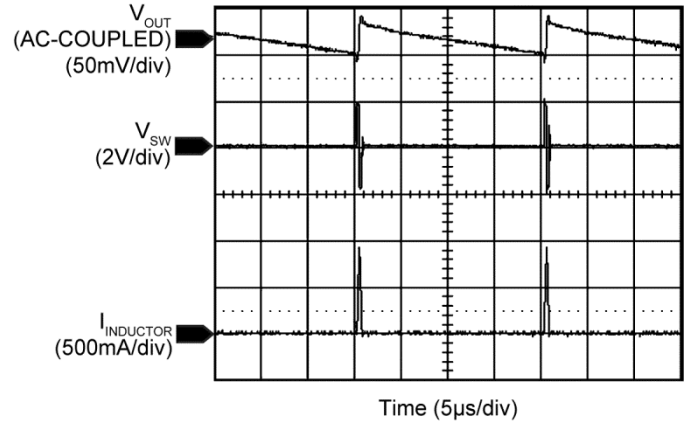


Functional Characteristics

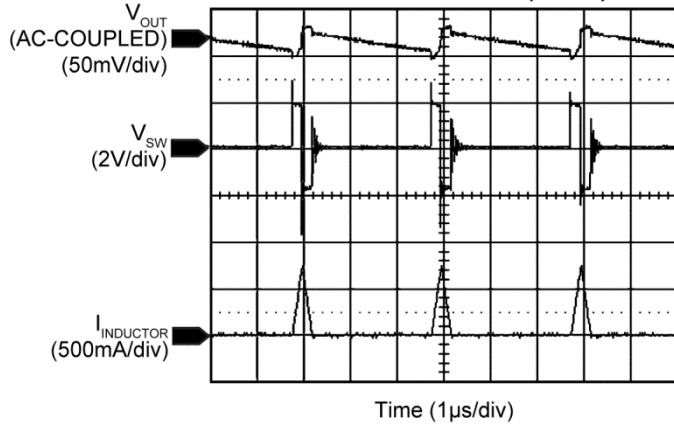
**Switching Waveform
Discontinuous Mode (1mA)**



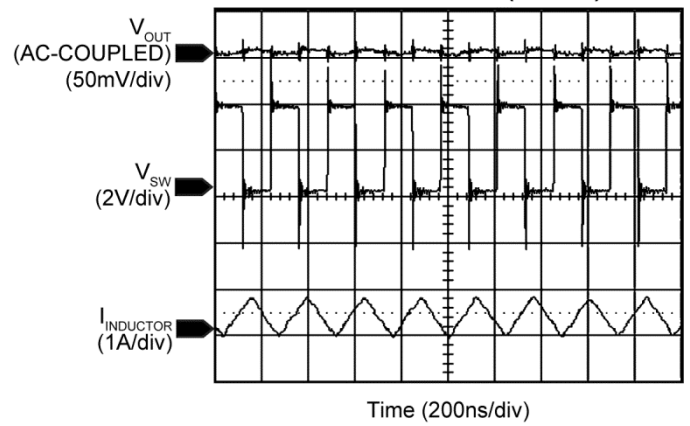
**Switching Waveform
Discontinuous Mode (10mA)**



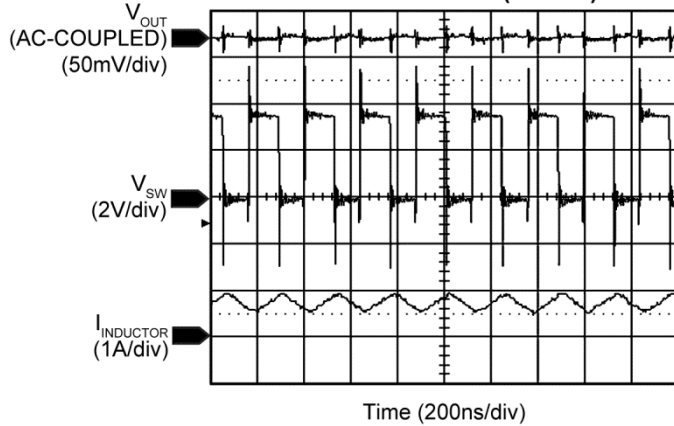
**Switching Waveform
Discontinuous Mode (50mA)**



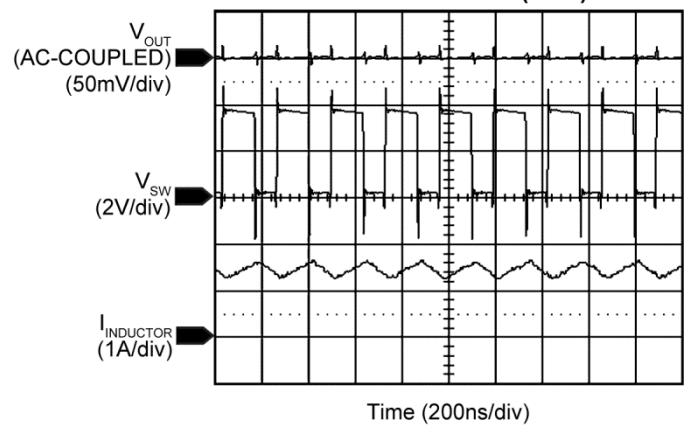
**Switching Waveform
Continuous Mode (200mA)**



**Switching Waveform
Continuous Mode (800mA)**

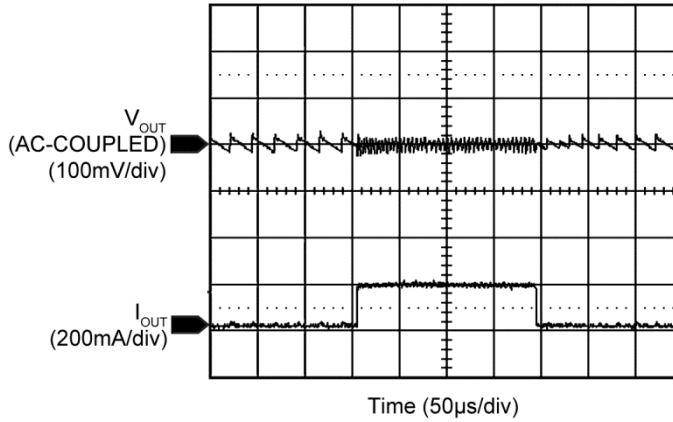


**Switching Waveform
Continuous Mode (1.5A)**

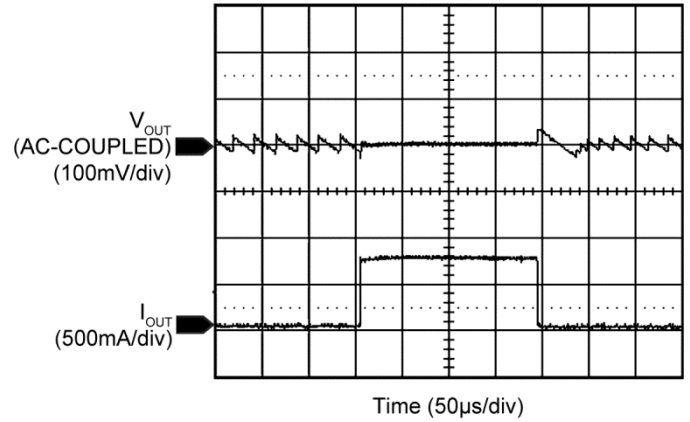


Functional Characteristics (Continued)

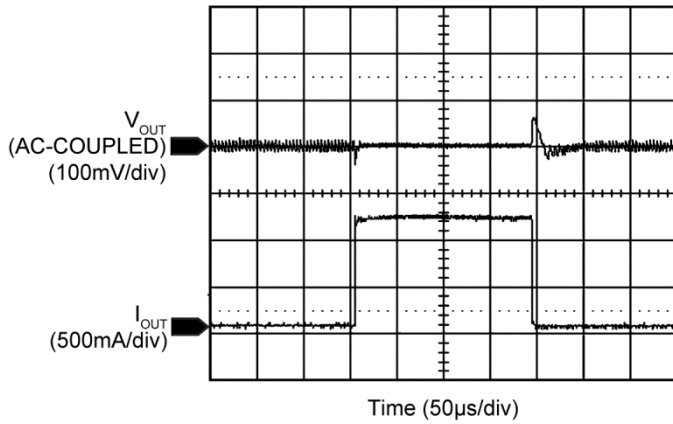
**Load Transient
(10mA to 200mA)**



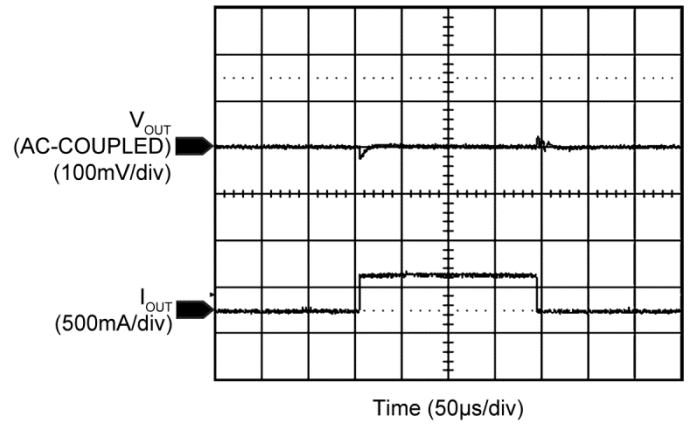
**Load Transient
(10mA to 750mA)**



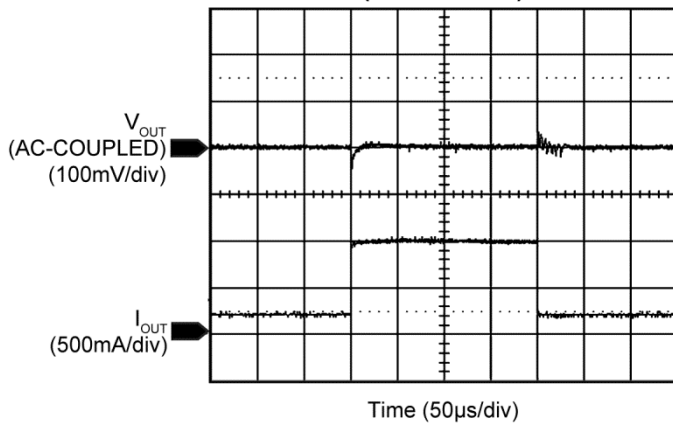
**Load Transient
(50mA to 1.5A)**



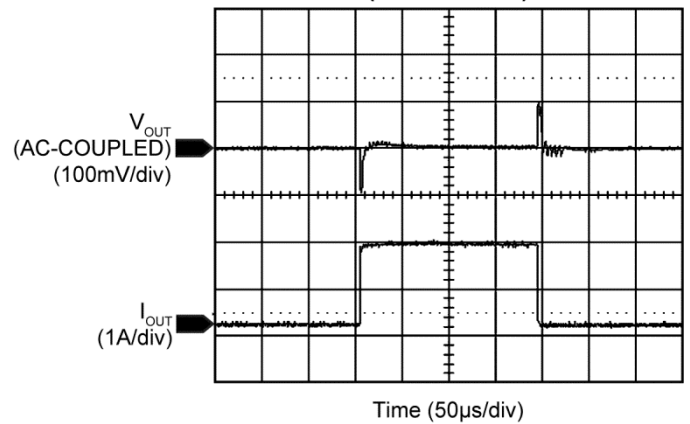
**Load Transient
(200mA to 600mA)**



**Load Transient
(200mA to 1A)**

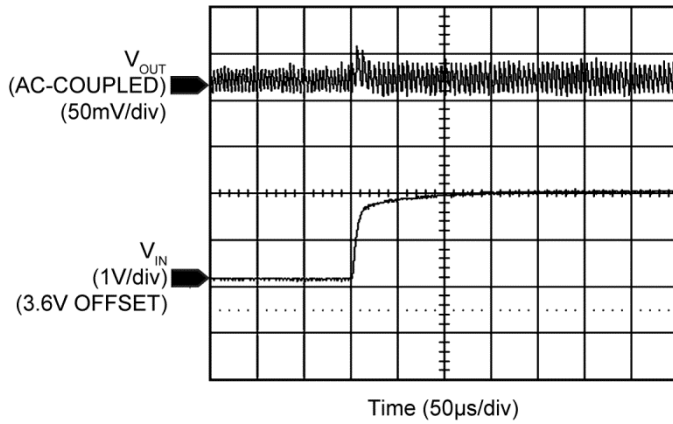


**Load Transient
(200mA to 2A)**

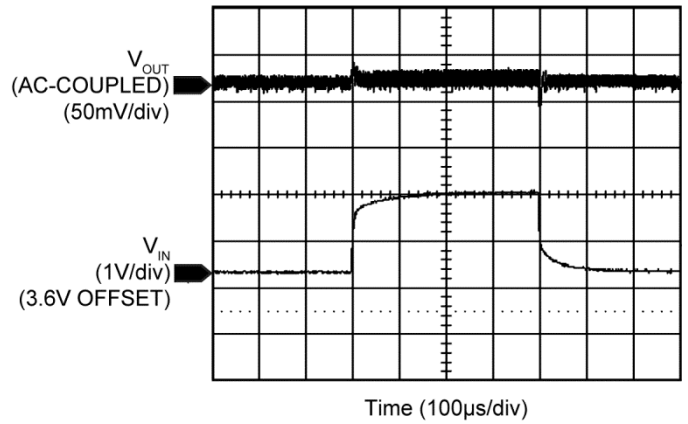


Functional Characteristics (Continued)

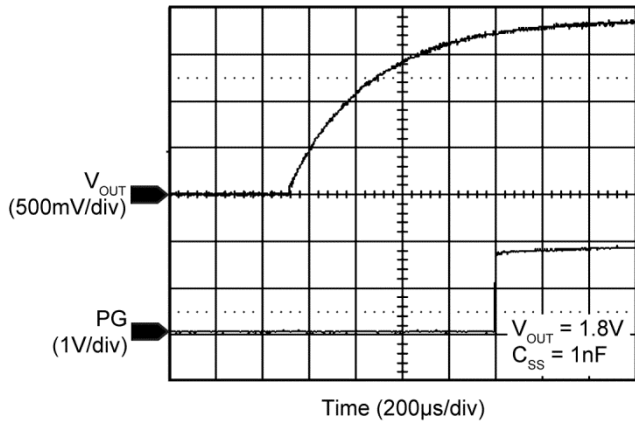
Line Transient
(3.6V to 5.5V @ 30mA)



Line Transient
(3.6V to 5.5V @ 2A)



Start-Up and PG
Waveform



Functional Diagram

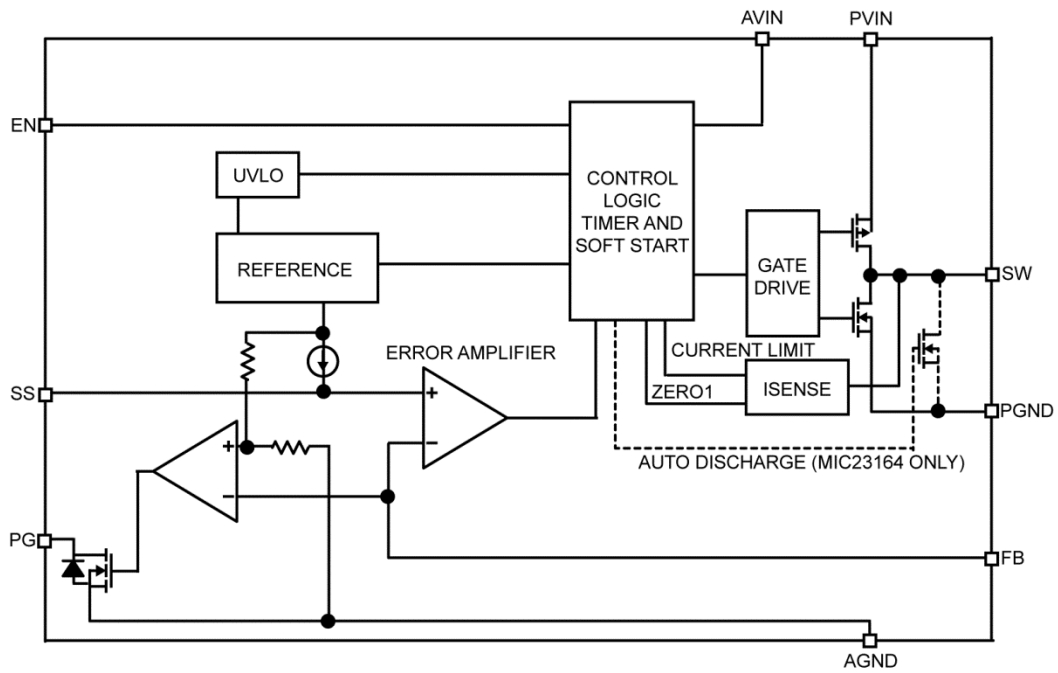


Figure 1. Simplified MIC23163/4 Functional Block Diagram – Adjustable Output Voltage

Functional Description

VIN

The input supply (VIN) provides power to the internal MOSFETs for the switch-mode regulator along with the internal control circuitry. The VIN operating range is 2.7V to 5.5V so an input capacitor, with a minimum voltage rating of 6.3V, is recommended. Due to the high switching speed, a minimum 2.2μF bypass capacitor placed close to VIN and the power ground (PGND) pin is required. Refer to the “[PCB Layout Recommendations](#)” section for details.

EN/Shutdown

A logic high signal on the enable pin activates the output voltage of the device. A logic low signal on the enable pin deactivates the output and reduces supply current to 0.1μA. When disabled the MIC23164 switches an internal load of 180Ω on the regulators switch node to discharge the output. The MIC23163/4 features external soft-start circuitry via the soft start (SS) pin that reduces in-rush current and prevents the output voltage from overshooting at start up. Do not leave the EN pin floating.

SW

The switch (SW) connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load, SNS pin and output capacitor. Due to the high-speed switching on this pin, the switch node should be routed away from sensitive nodes whenever possible.

AGND

The analog ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the “[PCB Layout Recommendations](#)” section for details.

PGND

The power ground pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND) loop as applicable. Refer to the “[PCB Layout Recommendations](#)” section for details.

PG

The power good (PG) pin is an open drain output which indicates logic high when the output voltage is typically above 90% of its steady state voltage. A pull-up resistor of more than 5kΩ should be connected from PG to V_{OUT}.

SS

The soft start (SS) pin is used to control the output voltage ramp up time. The approximate equation for the ramp time in seconds is $270 \times 10^3 \times \ln(10) \times C_{SS}$. For example, for a $C_{SS} = 1\text{nF}$, $T_{RISE} \sim 600\mu\text{s}$. The minimum recommended value for C_{SS} is 1nF.

FB

The feedback (FB) pin is provided for the adjustable voltage option (no internal connection for fixed options). This is the control input for programming the output voltage. A resistor divider network is connected to this pin from the output and is compared to the internal 0.7V reference within the regulation loop.

The output voltage can be programmed between 0.7V and V_{IN} using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad \text{Eq. 1}$$

where:

R1 is the top resistor, R2 is the bottom resistor.

Table 1. Example Feedback Resistor Values

V _{OUT}	R1	R2
1.2V	215k	301k
1.5V	301k	261k
1.8V	340k	215k
2.5V	274k	107k
3.3V	383k	102k
3.6V	422k	102k

Application Information

The MIC23163/4 is a high-performance DC/DC step-down regulator offering a small solution size. Supporting an output current up to 2A inside a tiny 2mm x 2mm DFN package, the IC requires only three external components while meeting today's miniature portable electronic device needs. Using the HyperLight Load (HLL) switching scheme, the MIC23163/4 is able to maintain high efficiency throughout the entire load range while providing ultra-fast load transient response. The following sections provide additional device application information.

Input Capacitor

A 2.2µF ceramic capacitor or greater should be placed close to the VIN pin and PGND pin for bypassing. A Murata GRM188R60J475ME84D, size 0603, 4.7µF ceramic capacitor is recommended based on performance, size, and cost. A X5R or X7R temperature rating is recommended for the input capacitor. Y5V temperature rating capacitors, aside from losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high-frequency noise.

Output Capacitor

The MIC23163/4 is designed for use with a 10µF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response but could also increase solution size or cost. A low equivalent series resistance (ESR) ceramic output capacitor such as the Murata GRM188R60J106ME84D, size 0603, 10µF ceramic capacitor is recommended based upon performance, size and cost. Both the X7R or X5R temperature rating capacitors are recommended. The Y5V and Z5U temperature rating capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies.

Inductor Selection

When selecting an inductor, it is important to consider the following factors (not necessarily in the order of importance):

- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23163/4 is designed for use with a 0.47µH inductor. This allows for rapid output voltage recovery during line and load transients.

Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current does not cause the inductor to saturate. Peak current can be calculated as illustrated in Equation 2:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right] \quad \text{Eq. 2}$$

As shown by Equation 2, the peak inductor current is inversely proportional to the switching frequency and the inductance; the lower the switching frequency or the inductance the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the “[Typical Application Circuit](#)” and “[Bill of Materials](#)” sections for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the “[Efficiency Considerations](#)” section for more details.

The transition between high loads (CCM) to HLL mode is determined by the inductor ripple current and the load current.

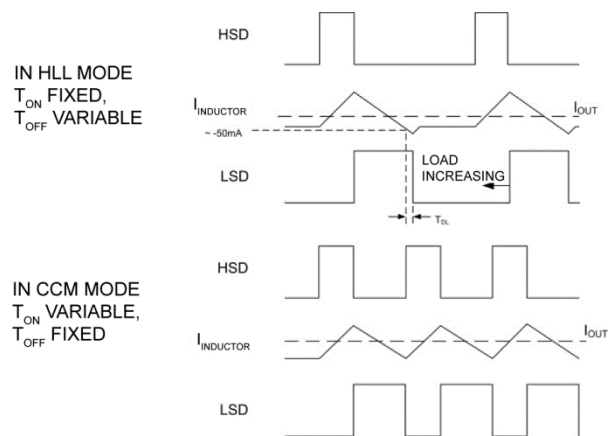


Figure 2. Signals for High-Side Switch Drive (HSD) for T_{ON} Control, Inductor Current, and Low-Side Switch Drive (LSD) for T_{OFF} Control

In HLL mode, the inductor is charged with a fixed T_{on} pulse on the high-side switch (HSD). After this, the LSD is switched on and current falls at a rate V_{OUT}/L . The controller remains in HLL mode while the inductor falling current is detected to cross approximately -50mA . When the LSD (or T_{OFF}) time reaches its minimum and the inductor falling current is no longer able to reach this -50mA threshold, the part is in CCM mode and switching at a virtually constant frequency.

Once in CCM mode, the T_{OFF} time will not vary.

Compensation

The MIC23163/4 is designed to be stable with a $0.47\mu\text{H}$ inductor with a $10\mu\text{F}$ ceramic (X5R) output capacitor. A feed-forward capacitor in the range of 15pF to 68pF is essential across the top feedback resistor.

Duty Cycle

The maximum duty cycle of the MIC23163/4 is 100%, allowing operation in dropout to extend battery life.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied, as shown in Equation 3:

$$\text{Efficiency \%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100 \quad \text{Eq. 3}$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery-powered applications. Reduced current draw from a battery increases the device's operating time and is critical in handheld devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R . Power is dissipated in the high side MOSFET during the on cycle. Power loss is equal to the high side MOSFET $R_{DS(ON)}$ multiplied by the switch current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at a constant 4MHz frequency and the switching transitions make up the switching losses.

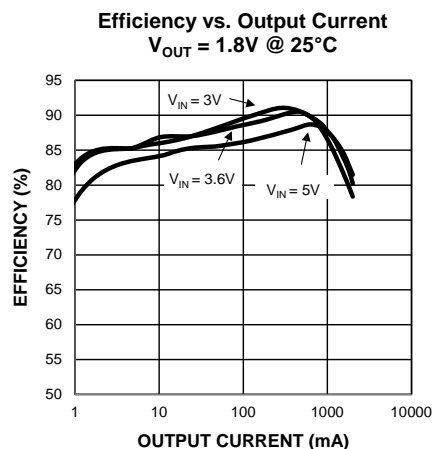


Figure 3. Efficiency under Load

Figure 3 shows an efficiency curve. From no load to 100mA , efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HLL mode, the MIC23163/4 is able to maintain high efficiency at low output currents.

Over 100mA , efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, thereby reducing the internal $R_{DS(ON)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as in Equation 4:

$$P_{DCR} = I_{OUT}^2 \times DCR \quad \text{Eq. 4}$$

From that, the loss in efficiency due to inductor resistance can be calculated as in Equation 5:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{DCR}} \right) \right] \times 100 \quad \text{Eq. 5}$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

HyperLight Load Mode

MIC23163/4 uses a minimum on and off time proprietary control loop (PCL) patented by Micrel called HyperLight Load (HLL). When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23163/4 works in pulse frequency modulation (PFM) to regulate the output. As the output current increases, the off-time decreases, thus provides more energy to the output. This switching scheme improves the efficiency of MIC23163/4 during light load currents by only switching when it is needed. As the load current increases, the MIC23163/4 goes into continuous conduction mode (CCM) and switches at a frequency centered at 4MHz. The equation to calculate the load when the MIC23163/4 goes into continuous conduction mode may be approximated by Equation 6:

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2L \times f} \right) \quad \text{Eq. 6}$$

As shown in Equation 6, the load at which the MIC23163/4 transitions from HLL mode to PWM mode is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), duty cycle (D), inductance (L) and frequency (f). As shown in Figure 4, as the output current increases, the switching frequency also increases until the MIC23163/4 goes from HLL mode to PWM mode at approximately 120mA. The MIC23163/4 will switch at a relatively constant frequency around 4MHz once the output current is over 120mA.

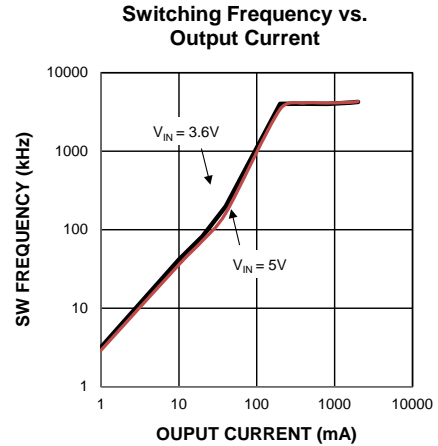
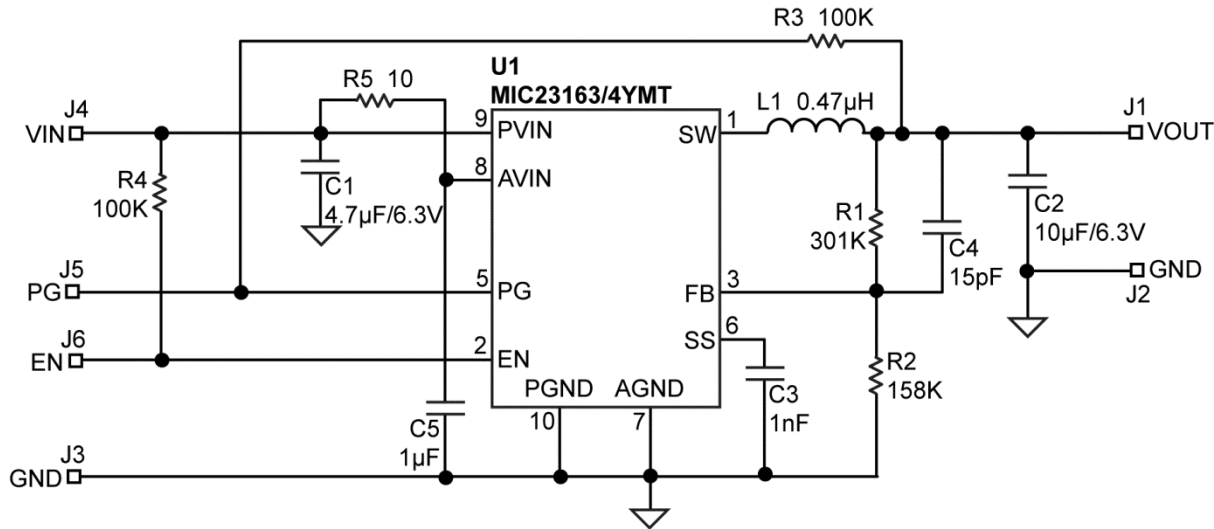


Figure 4. SW Frequency vs. Output Current

Typical Application Circuit



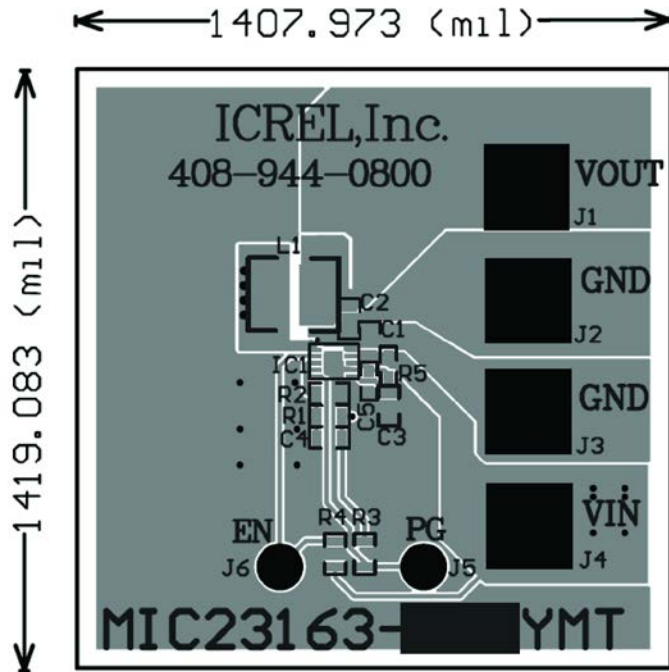
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	C1608X5R0J475K	TDK ⁽⁷⁾	4.7μF, 6.3V, X5R, Size 0603	1
	GRM188R60J475KE19D	Murata ⁽⁸⁾		
C2	C1608X5R0J106K080AB	TDK	10μF, 6.3V, X5R, Size 0603	1
	GRM188R60J106ME84D	Murata		
C3	GRM188R71H102MA01D	Murata	1nF/50V, X7R, 0603	1
	06035C102KAT2A	AVX ⁽⁹⁾		
C4	06035A150KAT2A	AVX	15pF, 50V, 0603	1
	GRM1885C1H150JA01D	Murata		
L1	FLF3215T-R47N	TDK	0.47μH, 2.8A, 21mΩ, L3.2mm x W2.5mm x H1.55mm	1
	LQH32PNR47NNC	Murata		
R1	CRCW0603301KFKEA	Vishay ⁽¹⁰⁾	301kΩ, 1%, 1/10W, Size 0603	1
R2	CRCW0603158KFKEA	Vishay	158kΩ, 1%, 1/10W, Size 0603	1
R3, R4	CRCW0603100KFKEA	Vishay	100kΩ, 1%, 1/10W, Size 0603	1
R5	CRCW060310R0FKEA	Vishay	10Ω, 1%, 1/10W, Size 0603	1
U1	MIC23163YMT	Micrel, Inc. ⁽¹¹⁾	4MHz, 2A, 100% Duty Cycle Buck Regulator with HyperLight Load [®] and Power Good	1
	MIC23164YMT			

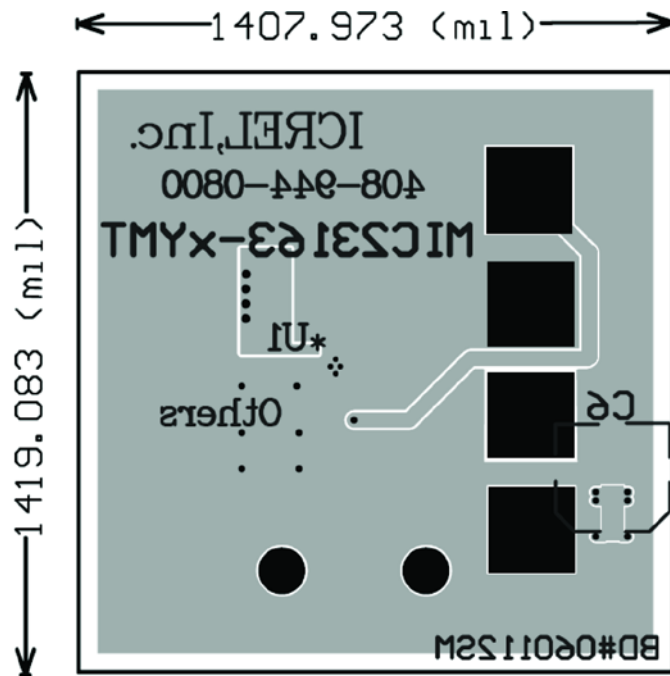
Notes:

7. TDK: www.tdk.com.
8. Murata: www.murata.com.
9. AVX: www.avx.com.
10. Vishay: www.vishay.com.
11. Micrel, Inc.: www.micrel.com.

PCB Layout Recommendations

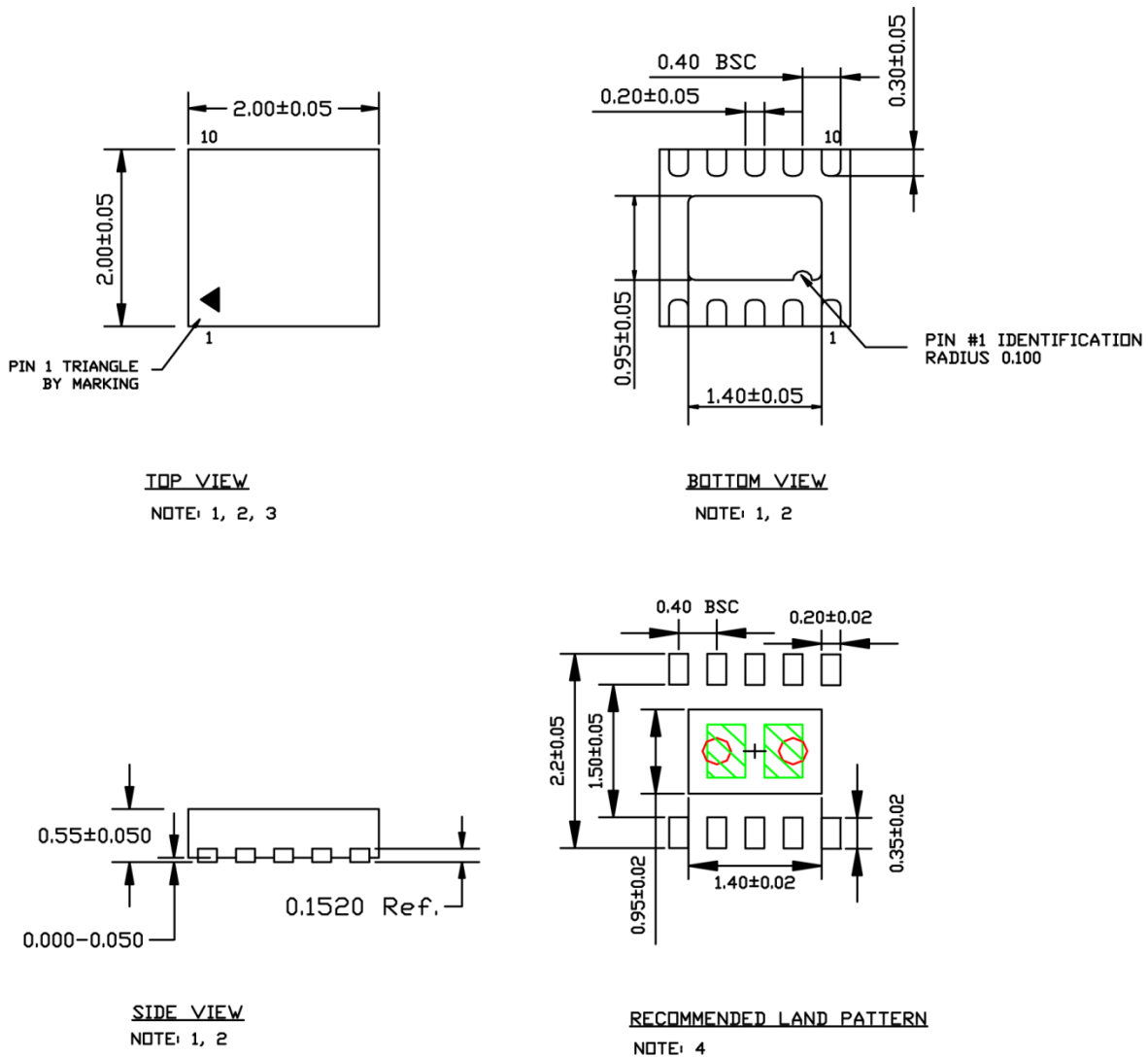


Top Layer



Bottom Layer

Package Information⁽¹²⁾ and Recommended Landing Pattern



NOTE:

1. MAX PACKAGE WARPAGE IS 0.05MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. GREEN RECTANGLES (SHADED AREA) INDICATE STENCIL OPENING ON EXPOSED AREA. SIZE IS 0.6X0.4MM, SPACING IS 0.2MM.
5. RED CIRCLES REPRESENT THERMAL VIAS AND SHOULD BE CONNECTED TO GND FOR MAX PERFORMANCE. 0.30 - 0.35 MM RECOMMENDED DIAMETER, 0.80 MM PITCH.

10-Pin 2mm x 2mm DFN (MT)

Note:

12. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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