Datasheet

Power Management LSI for Mobile Phone

BD71801GWL

General Description

The BD71801GWL is an integrated Power Management LSI available in a small 80-pins 0.4mm-pitch 3.8mm-by-3.8mm Wafer-level CSP package, which is designed to meet demands for space-constrained Smart phones.

The device provides 5-Buck Converters.
The device also includes 12 general-purpose LDOs providing a wide range of voltage and current capabilities.

All Buck Converters and LDOs are fully controllable by the I2C interface. The BD71801GWL is very easy to use in any mobile platforms.

Features

- 5-Channel High Efficiency Step-down Converters. (Adjustable Voltage Options by I2C) (Switching frequency 2MHz(TYP))
- All Buck Converters Support PFM/PWM Auto Mode.
- 12-Channel LDOs are Programmable to Voltage Options by I2C.
- LDOs and all Buck Converters Power ON/OFF Control Enabled by I2C Interface or External pin.
- 2ch NMOS output LDOs (LDO11, 12) for Optimized Efficiency.
- Power ON/OFF Sequence.
- Support TCXO Buffer (26MHz) and 32KHz crystal oscillator.
- I2C Compatible Interface. (I2C Clock Support : Full Speed Mode 400kHz) (Device Address is “1001011”,”1001100”)

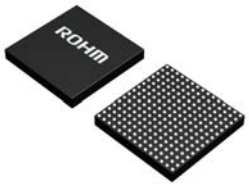
Applications

- Smart Phones
- Tablets
- Mobile Router
- Data Transmitter

Key Specifications

- Input Voltage Range: 2.6V to 5.5V
- Output Voltage Range: 1.0V to 3.4V
- Switching Frequency: 2.0MHz(Typ)
- OFF Current: 0.3μA (Typ)
- Operating Temperature Range: -35℃ to +85℃

Package	W(Typ) x D(Typ) x H(Max)
UCSP50L3C	3.80mm x 3.80mm x 0.57mm



Absolute Maximum Ratings（Ta=25°C）

Parameter	Symbol	Rating	Unit
Maximum Supply Voltage 1 (VBATREF,VBAT, VIN1)	VBATMAX	7.0	V
Maximum Supply Voltage 2 (PBAT1,2,3,4,5)	VPBATMAX	7.0	V
Maximum Supply Voltage 3 (VIN2)	VIN2MAX	4.2	V
Maximum Input Voltage 1 (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8, OUT9, OUT10, LX1, LX2, LX3, LX4, LX5, PSET, ADRS, EN_O7, PWRON, PWRHOLD, POR, TCXO_IN, OSC_IN, DVDD(Note 1), OSC_OUT, SIMRSTIN, SIMCLKIN, SIMIODBB, SIMIO)	VINMAX1	7.0	V
Maximum Input Voltage 2 (SDA, SCL)	VINMAX2	DVDD + 0.3	V
Maximum Input Voltage 3 (OUT11,12, REFC)	VINMAX3	VIN2MAX+ 0.3	V
Power Dissipation	Pd	1.38(Note 2)	W
Operating Temperature Range	Topr	-35 ~ +85	°C
Storage Temperature Range	Tstg	-55 ~ +125	°C

(Note 1) The DVDD Voltage must be under the Battery voltage VBAT, PBAT anytimes.
(Note 2) Derate by 13.8mW/ when operation above Ta=25 (when mounted in ROHM's standard board(54mm × 62mm)).
Caution: Operation the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, likes adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Range	Unit
VBAT Voltage	VBAT	2.70 ～ 5.50 (Note3)	V
PBAT Voltage	VPBAT	2.70 ～ 5.50 (Note3)	V
VIN1 Voltage	VIN1	2.70 ～ 5.50 (Note4)	V
VIN2 Voltage	VIN2	1.40 ～ 1.80 (Note5)	V

(Note 3) Whenever the VBAT or PBAT or VIN1 or VIN2 voltage is under the LDO, SWREG output voltage, or under certain levels, the LDO and SWREG output is not guaranteed to meet its published specifications. It is necessary to supply the same voltage to PBAT and VBAT.
(Note 4) To achieve the best efficiency performance, SWREG5 output is recommended to be connected to VIN1 externally.
(Note 5) To achieve the best efficiency performance, SWREG4 output is recommended to be connected to VIN2 externally.

Block Diagram

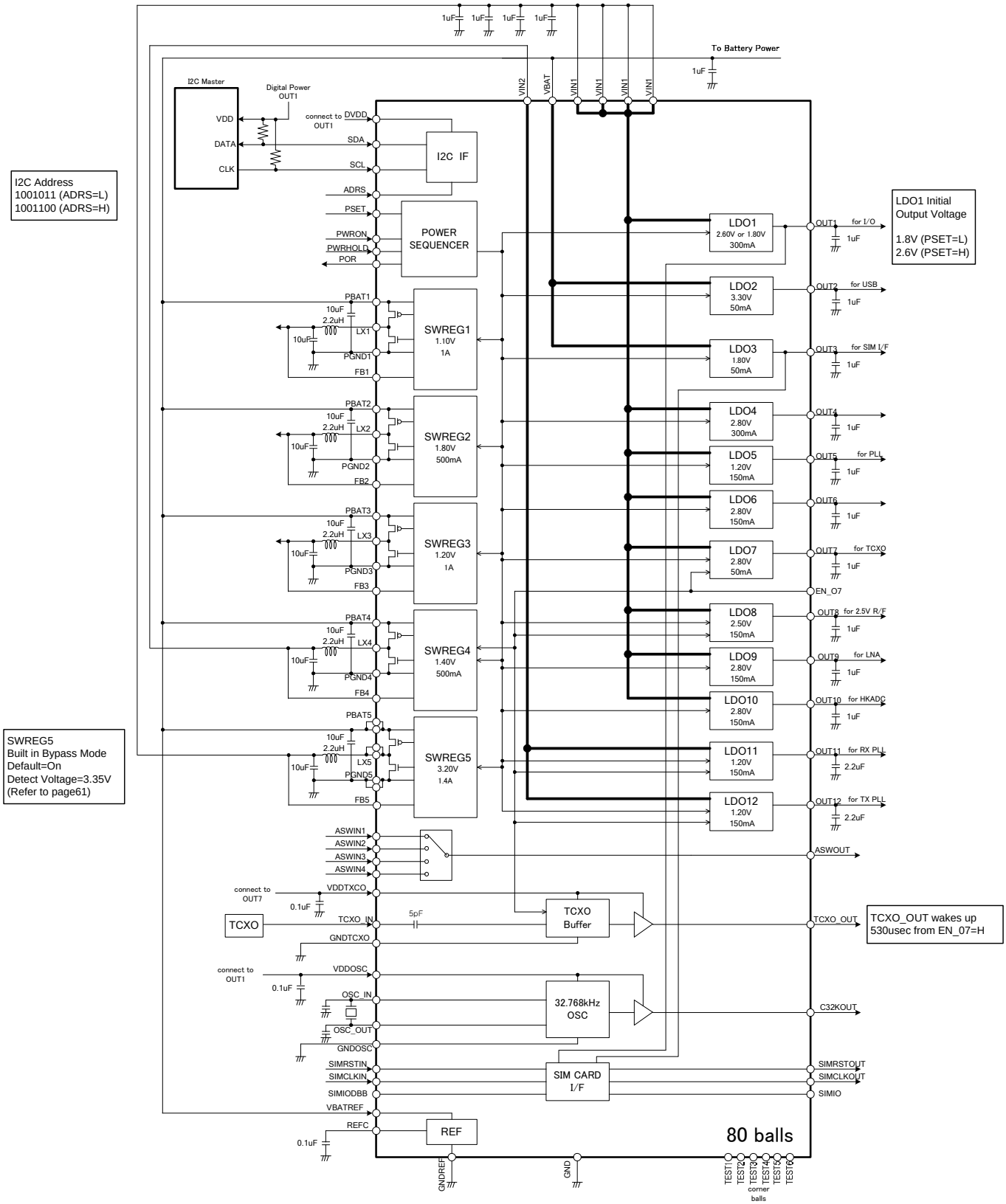
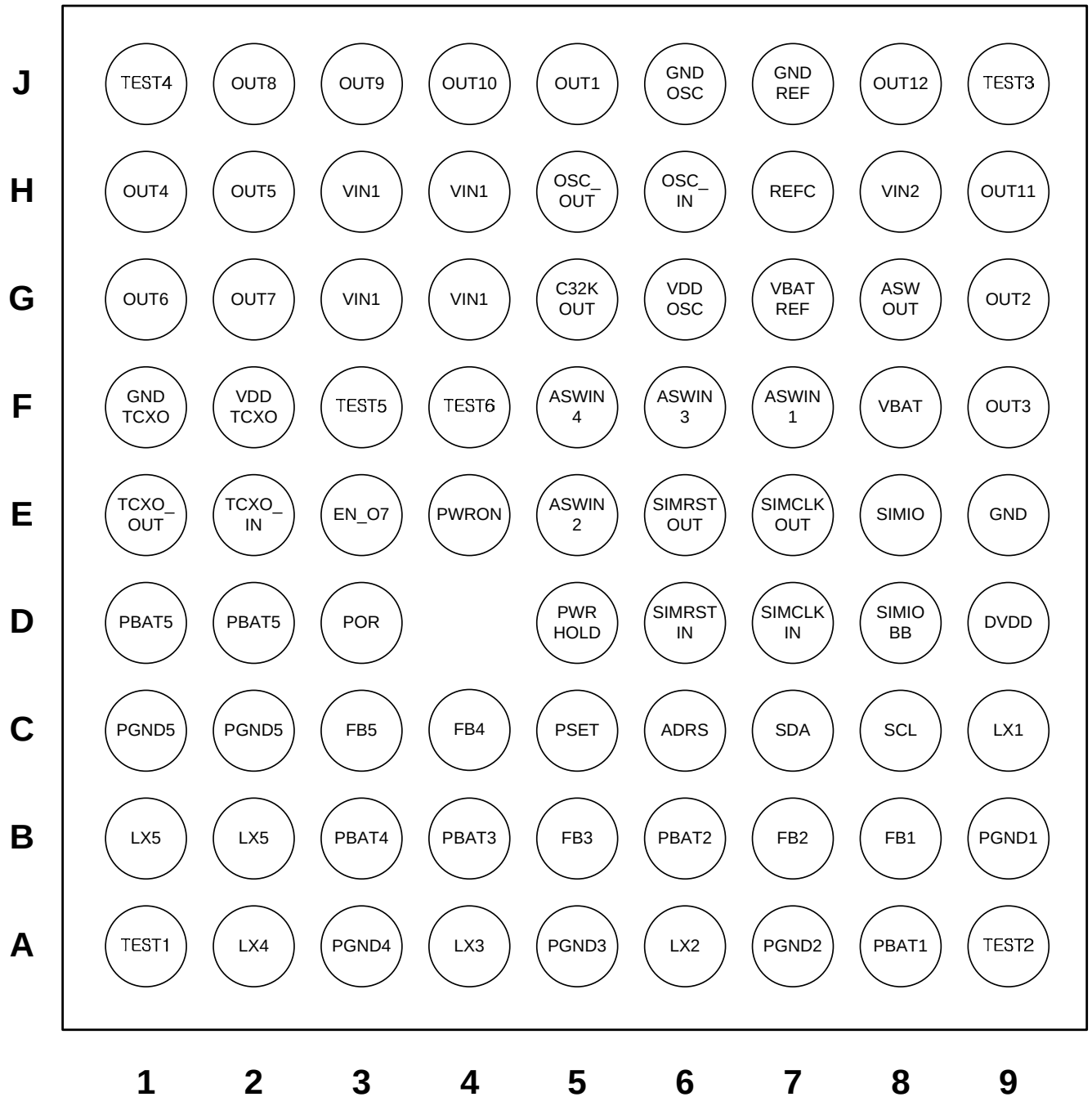


Figure 1. Block Diagram

(Note1) Recommend Parts

1. Coil : SWREG2, SWREG4 → DFE201612R-H-2R2N (TOKO)
   SWREG1, SWREG3, SWREG5 → DFE252012R-H-2R2N (TOKO)
2. X'tal : FC135 (EPSON TOYOCOM)
   CM7V-T1A (MICRO CRYSTAL SWITZERLAND)

Pin Configurations



Bottom View

Figure 2. Pin Configuration

Pin Descriptions

Ball No.	Pin Name	A/D	I/O	Equivalent Circuit Eiqure	Function	Diode		Initial Condition	Function
						+ side	- side		
A1	TEST1	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)
A2	LX4	A	O	A	Inductor Connection for SWREG4	PBAT4	PGND4	HiZ	
A3	PGND4	-	-	-	Ground for SWREG4	PBAT4	GND	-	
A4	LX3	A	O	A	Inductor Connection for SWREG3	PBAT3	PGND3	HiZ	
A5	PGND3	-	-	-	Ground for SWREG3	PBAT3	GND	-	
A6	LX2	A	O	A	Inductor Connection for SWREG2	PBAT2	PGND	HiZ	
A7	PGND2	-	-	-	Ground for SWREG2	PBAT2	GND	-	
A8	PBAT1	-	-	-	Power Supply for SWREG1	-	PGND1	-	
A9	TEST2	-	-	-	Non connect pin (Open or connected to GND)	VBAT	GND	-	(Note1)
B1	LX5	A	O	A	Inductor Connection for SWREG5	PBAT5	PGND5	HiZ	
B2	LX5	A	O	A	Inductor Connection for SWREG5	PBAT5	PGND5	HiZ	
B3	PBAT4	-	-	-	Power Supply for SWREG4	-	PGND4	-	
B4	PBAT3	-	-	-	Power Supply for SWREG3	-	PGND3	-	
B5	FB3	A	I/O	B	Voltage Feed back pin for SWREG3	PBAT3	GND	-	
B6	PBAT2	-	-	-	Power Supply for SWREG2	-	PGND2	-	
B7	FB2	A	I/O	B	Voltage Feed back pin for SWREG2	PBAT2	GND	-	
B8	FB1	A	I/O	B	Voltage Feed back pin for SWREG1	PBAT1	GND	-	
B9	PGND1	-	-	-	Ground for SWREG1	PBAT1	GND	-	
C1	PGND5	-	-	-	Ground for SWREG5	PBAT5	GND	-	
C2	PGND5	-	-	-	Ground for SWREG5	PBAT5	GND	-	
C3	FB5	A	I/O	B	Voltage Feed back pin for SWREG5	PBAT5	GND	-	
C4	FB4	A	I/O	B	Voltage Feed back pin for SWREG4	PBAT4	GND	-	
C5	PSET	D	I	C	LDO1 Initial voltage set pin (L=1.8V, H=2.6V)	PBAT3	GND	-	Connect to GND
C6	ADRS	D	I	C	Logic Selector	PBAT4	GND	-	I2C Address 1001011 (ADRS=L) 1001100 (ADRS=H)
C7	SDA	D	I	D	I2C data input	VBAT	GND	-	
C8	SCL	D	I	E	I2C clock input	VBAT	GND	-	
C9	LX1	A	O	A	Inductor Connection for SWREG1	PBAT1	PGND1	HiZ	

(Note 1) The TEST1, 2, 3, 4, 5, 6 pin are used for factory test mode. Please keep these pin “OPEN” or GND at all times.

Ball No.	Pin Name	A/D	I/O	Equivalent Circuit Eiqure	Function	Diode		Initial Condition	Function
						+ side	- side		
D1	PBAT5	-	-	-	Power Supply for SWREG5	-	PGND5	-	
D2	PBAT5	-	-	-	Power Supply for SWREG5	-	PGND5	-	
D3	POR	D	O	F	Power on reset signal output	VBAT	GND	L	(Note2)
D5	PWRHOLD	D	I	G	Power enable signal	VBAT	GND	-	
D6	SIMRSTIN	D	I	H	SIM clock input from DBB	VBAT	GND	-	
D7	SIMCLKIN	D	I	H	SIM reset input from DBB	VBAT	GND	-	
D8	SIMIOBB	D	I/O	I	SIM data input / output from DBB	VBAT	GND	-	Pull up 20KΩ to OUT1
D9	DVDD	-	-	-	VDD for I2C block	VBAT	GND	-	
E1	TCXO_OUT	D	O	K	TCXO_Buffer input frequency	VDDTCXO	GND	L	
E2	TCXO_IN	A	I	J	TCXO_Buffer output frequency	VBAT	GND	-	
E3	EN_07	D	I	L	TCXO Buffer,SWREG4, LDO7,8,11,12 control	VBAT	GND	Pull Down	Pull down 1.5MΩ
E4	PWRON	D	I	L	Start up signal input	VBAT	GND	Pull Down	Pull down 1.5MΩ
E5	ASWIN2	A	I	M	Analog SW input selector2	VBAT	GND	-	
E6	SIMRSTOUT	D	O	N	SIM CARD side reset output	VBAT OUT3	GND	L	
E7	SIMCLKOUT	D	O	N	SIM CARD side clock output	VBAT OUT3	GND	L	
E8	SIMIO	D	I/O	I	SIM CARD side data input/output	VBAT	GND	Pull Up	Pull up 10KΩ to OUT3
E9	GND	-	-	-	Ground Pin	VBAT	-	-	
F1	GNDTCXO	-	-	-	Ground for TCXO Buffer	VBAT	GND	-	
F2	VDDTCXO	-	-	-	Power Supply for TCXO Buffer	-	GND	-	
F3	TEST5	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)
F4	TEST6	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)
F5	ASWIN4	A	I	M	Analog SW input selector4	VBAT	GND	-	
F6	ASWIN3	A	I	M	Analog SW input selector3	VBAT	GND	-	
F7	ASWIN1	A	I	M	Analog SW input selector1	VBAT	GND	-	
F8	VBAT	-	-	-	Power Supply for IC	-	GND	-	
F9	OUT3	A	O	O	LDO3 output	VBAT	GND		

(Note 1) The TEST1, 2, 3, 4, 5, 6 pin are used for ROHM factory test mode. Please keep these pin “OPEN” or tied to GND at all times.

(Note 2) POR pin needs a pull up resistor in PCB layout.

Ball No.	PIN名	A/D	I/O	Equivalent Circuit Eiqure	Function	Diode		Initial Condition	Function
						+ side	- side		
G1	OUT6	A	O	P	LDO6 output	VIN1	GND	-	
G2	OUT7	A	O	P	LDO7 output	VIN1	GND	-	
G3	VIN1	-	-	-	Power Supply input for LDO	-	GND	-	
G4	VIN1	-	-	-	Power Supply input for LDO	VBAT	GND	-	
G5	C32KOUT	A	O	Q	32.768kHz output	VBAT	GND	-	
G6	VDDOSC	-	-	-	Power Supply for RTC Block	-	GND	-	
G7	VBATREF	-	-	-	Power Supply for Reference Block	-	GND	-	
G8	ASWOUT	A	O	M	Analog SW selector Output	VBAT	GND	-	
G9	OUT2	A	O	O	LDO2 output	VBAT	GND	-	
H1	OUT4	A	O	P	LDO4 output	VIN1	GND	-	
H2	OUT5	A	O	P	LDO5 output	VIN1	GND	-	
H3	VIN1	-	-	-	Power Supply input for LDO	VBAT	GND	-	
H4	VIN1	-	-	-	Power Supply input for LDO	VBAT	GND	-	
H5	OSC_OUT	A	I/O	R	32.768kHz crystal connect terminal	-	GND	-	
H6	OSC_IN	A	I/O	R	32.768kHz crystal connect terminal	-	GND	-	
H7	REFC	A	O	S	Reference Voltage output	VBAT	GND	-	
H8	VIN2	-	-	-	Power Supply input for LDO	VBAT	GND	-	
H9	OUT11	A	O	T	LDO11 output	VIN2	GND	-	
J1	TEST4	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)
J2	OUT8	A	O	P	LDO8 output	VIN1	GND	-	
J3	OUT9	A	O	P	LDO9 output	VIN1	GND	-	
J4	OUT10	A	O	P	LDO10 output	VIN1	GND	-	
J5	OUT1	A	O	P	LDO1 output	VIN1	GND	-	
J6	GNDOSC	-	-	-	GND for RTC block	VBAT	-	-	
J7	GNDREF	-	-	-	Ground for Reference Block	VBAT	-	-	
J8	OUT12	A	O	T	LDO12 output	VIN2	GND	-	
J9	TEST3	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)

(Note 1) The TEST1, 2, 3, 4, 5, 6 pin are used for factory test mode. Please keep these pin “OPEN” or tied to GND at all times.

I/O Equivalence Circuits

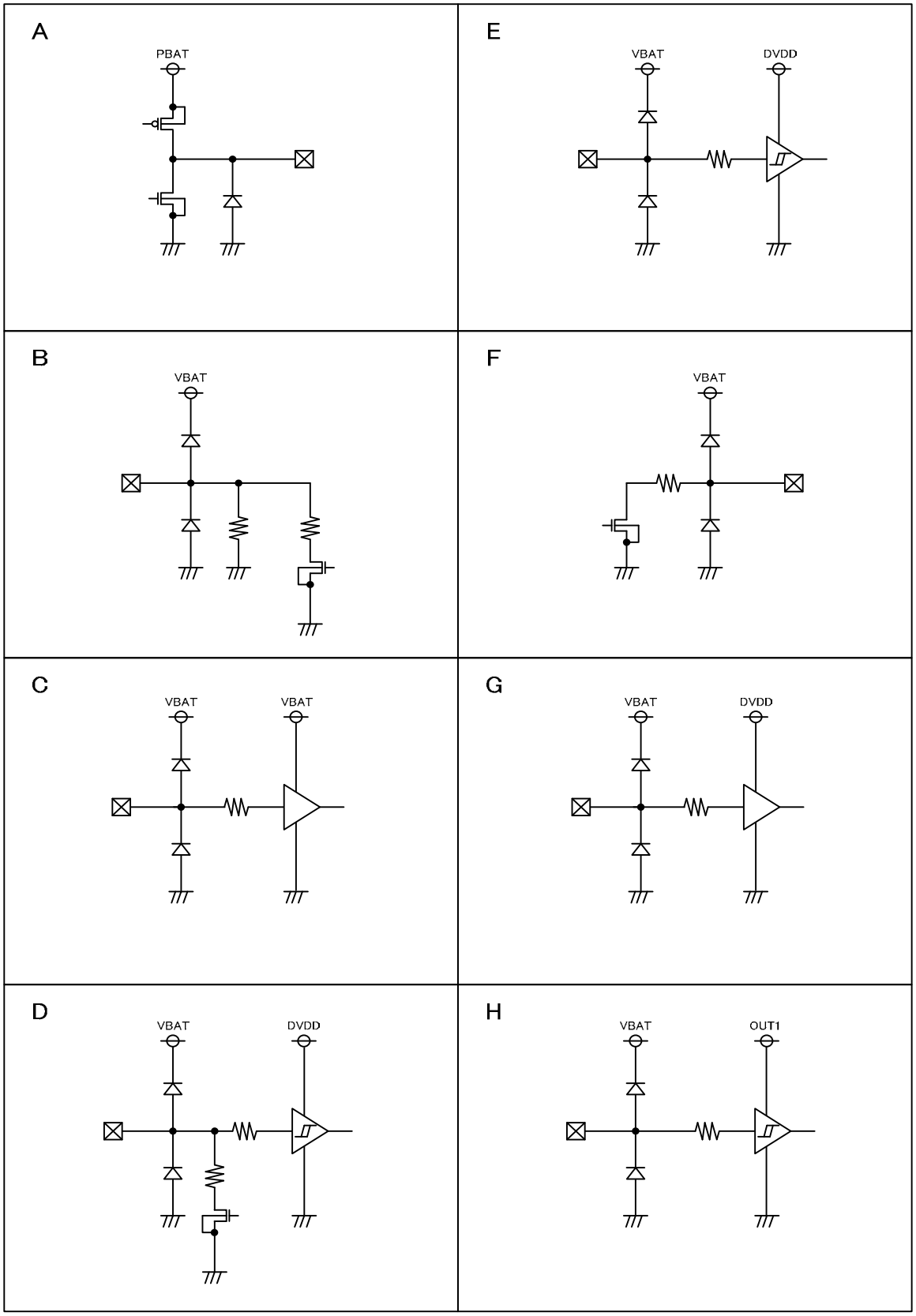


Figure 3. I/O Equivalence Circuits

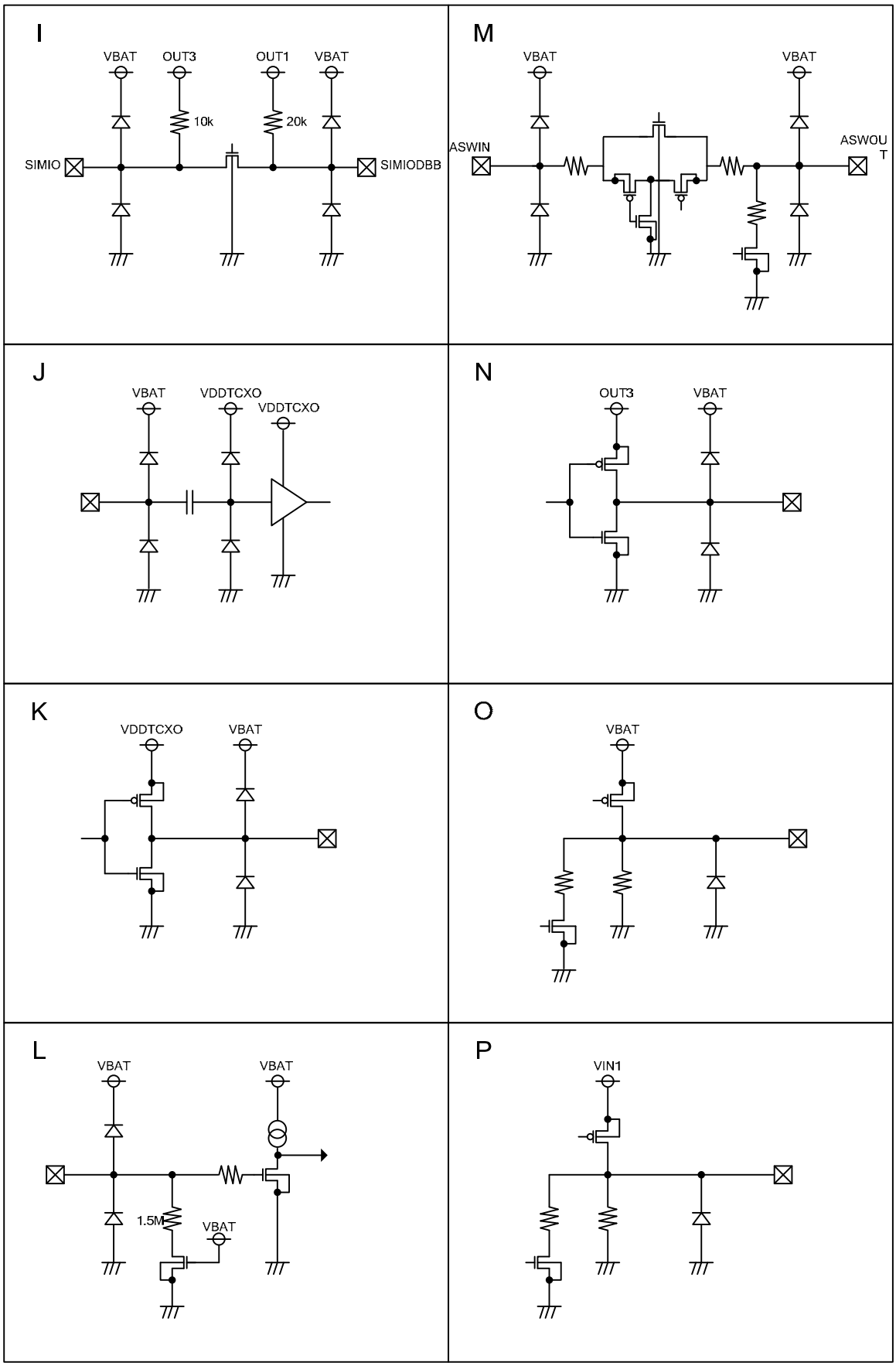


Figure 4. I/O Equivalence Circuits

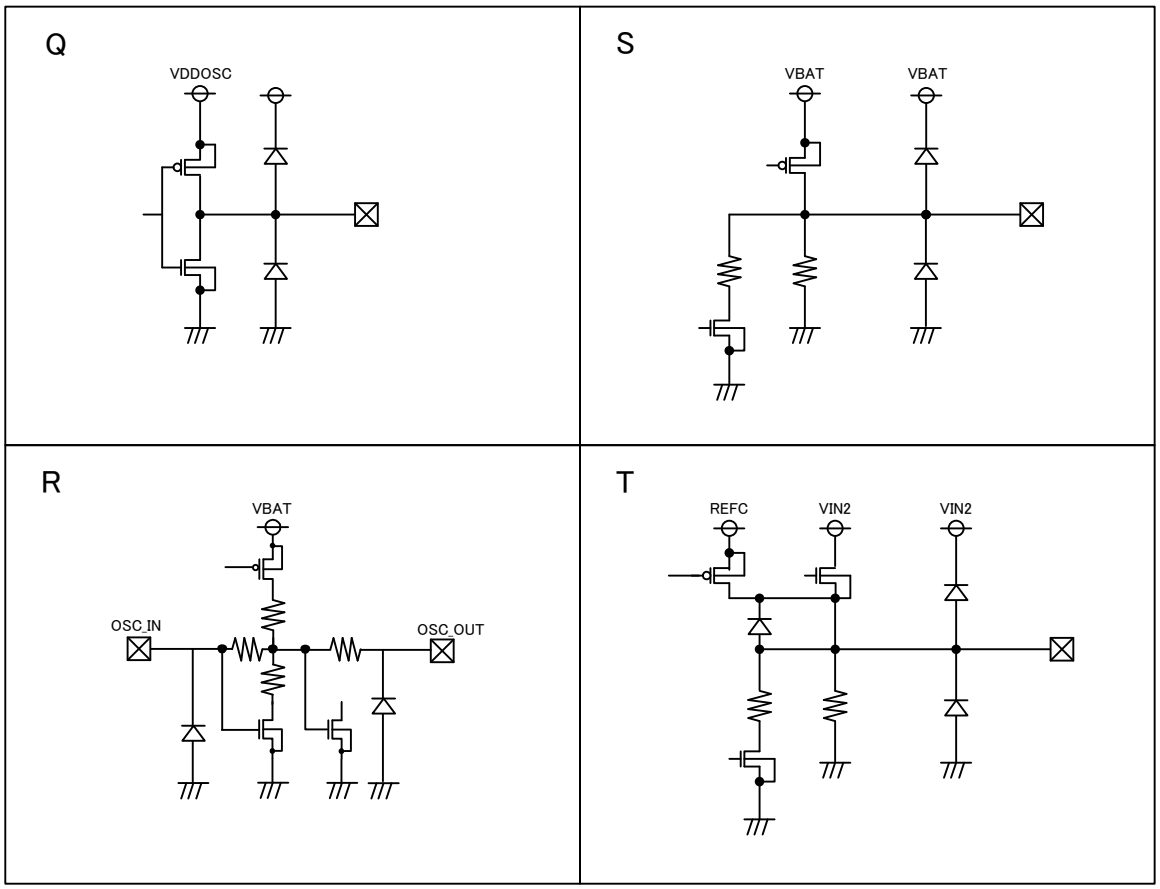


Figure 5. I/O Equivalence Circuits

Initial Output Voltage Summary

	Usage example	Power Supply	Initial Output Voltage	Load max	Adjustable range
SWREG1	CORE	PBAT1	1.10V	1.0A	±50,100mV
SWREG2	MEMORY	PBAT2	1.80V	0.5A	±50,100mV
SWREG3	ANALOG	PBAT3	1.20V	1.0A	±50,100mV
SWREG4	For VIN2 power supply (efficiency improvement)	PBAT4	1.40V	0.5A	±50,100mV
SWREG5	For VIN1 power supply (efficiency improvement)	PBAT5	3.20V	1.4A	±50,100mV
LDO1	I/O	VIN1	2.60V / 1.80V (Note 1)	300mA	±50,100mV
LDO2	USB	VBAT	3.30V	50mA	±50,100mV
LDO3	SIM I/F	VBAT	1.80V	50mA	±50,100mV
LDO4	Reserved	VIN1	2.80V	300mA	±50,100mV
LDO5	SYS PLL	VIN1	1.20V	150mA	±50,100mV
LDO6	Reserved	VIN1	2.80V	150mA	±50,100mV
LDO7	TCXO	VIN1	2.80V	50mA	±50,100mV
LDO8	2.5V R/F	VIN1	2.50V	150mA	±50,100mV
LDO9	LNA	VIN1	2.80V	150mA	±50,100mV
LDO10	HKADC	VIN1	2.80V	150mA	±50,100mV
LDO11	RX PLL	VIN2	1.20V	150mA	±50,100mV
LDO12	TX PLL	VIN2	1.20V	150mA	±50,100mV

(Note1) Depend on PSET pin setting.

SWREG Output Voltage Step Table

	SWREG1	SWREG2	SWREG3	SWREG4	SWREG5
Voltage step [V]	1.00	1.00	1.00	1.00	1.20
	1.05	1.05	1.05	1.05	1.40
	1.10	1.10	1.10	1.10	1.70
	1.15	1.15	1.15	1.15	1.75
	1.20	1.20	1.20	1.20	1.80
	1.25	1.25	1.25	1.25	1.85
	1.30	1.30	1.30	1.30	1.90
	1.35	1.35	1.35	1.35	3.00
	1.40	1.40	1.40	1.40	3.05
	1.45	1.45	1.45	1.45	3.10
	1.50	1.50	1.50	1.50	3.15
	1.70	1.70	1.70	1.70	3.20
	1.75	1.75	1.75	1.75	3.25
	1.80	1.80	1.80	1.80	3.30
	1.85	1.85	1.85	1.85	3.35
	1.90	1.90	1.90	1.90	3.40

	LDO1	LDO2	LDO3	LDO4	LDO5	LDO6	LDO7	LDO8	LDO9	LDO10	LDO11	LDO12
Voltage step [V]	1.70	2.55	1.70	1.10	1.00	1.10	1.10	1.20	1.10	1.10	1.00	1.00
	1.75	2.60	1.75	1.20	1.05	1.20	1.20	1.30	1.20	1.20	1.05	1.05
	1.80	2.65	1.80	1.30	1.10	1.30	1.30	1.70	1.30	1.30	1.10	1.10
	1.85	2.75	1.85	1.70	1.15	1.70	1.70	1.80	1.70	1.70	1.15	1.15
	1.90	2.80	1.90	1.80	1.20	1.80	1.80	2.40	1.80	1.80	1.20	1.20
	2.50	2.85	2.50	1.90	1.25	1.90	1.90	2.45	1.90	1.90	1.25	1.25
	2.55	2.90	2.60	2.50	1.30	2.50	2.50	2.50	2.50	2.50	1.30	1.30
	2.60	2.95	2.70	2.55	1.70	2.55	2.55	2.55	2.55	2.55	1.35	1.35
	2.65	3.00	2.80	2.60	1.80	2.60	2.60	2.60	2.60	2.60		
	2.70	3.05	2.90	2.65	1.90	2.65	2.65	2.65	2.65	2.65		
	2.80	3.10	2.95	2.70	2.60	2.70	2.70	2.70	2.70	2.70		
	2.90	3.20	3.00	2.75	2.70	2.75	2.75	2.75	2.75	2.75		
	2.95	3.25	3.05	2.80	2.80	2.80	2.80	2.80	2.80	2.80		
	3.00	3.30	3.10	2.85	2.90	2.85	2.85	2.85	2.85	2.85		
	3.05	3.35	3.20	2.90	3.00	2.90	2.90	2.90	2.90	2.90		
	3.10	3.40	3.30	3.00	3.10	3.00	3.00	3.00	3.00	3.00		

Power On Sequence

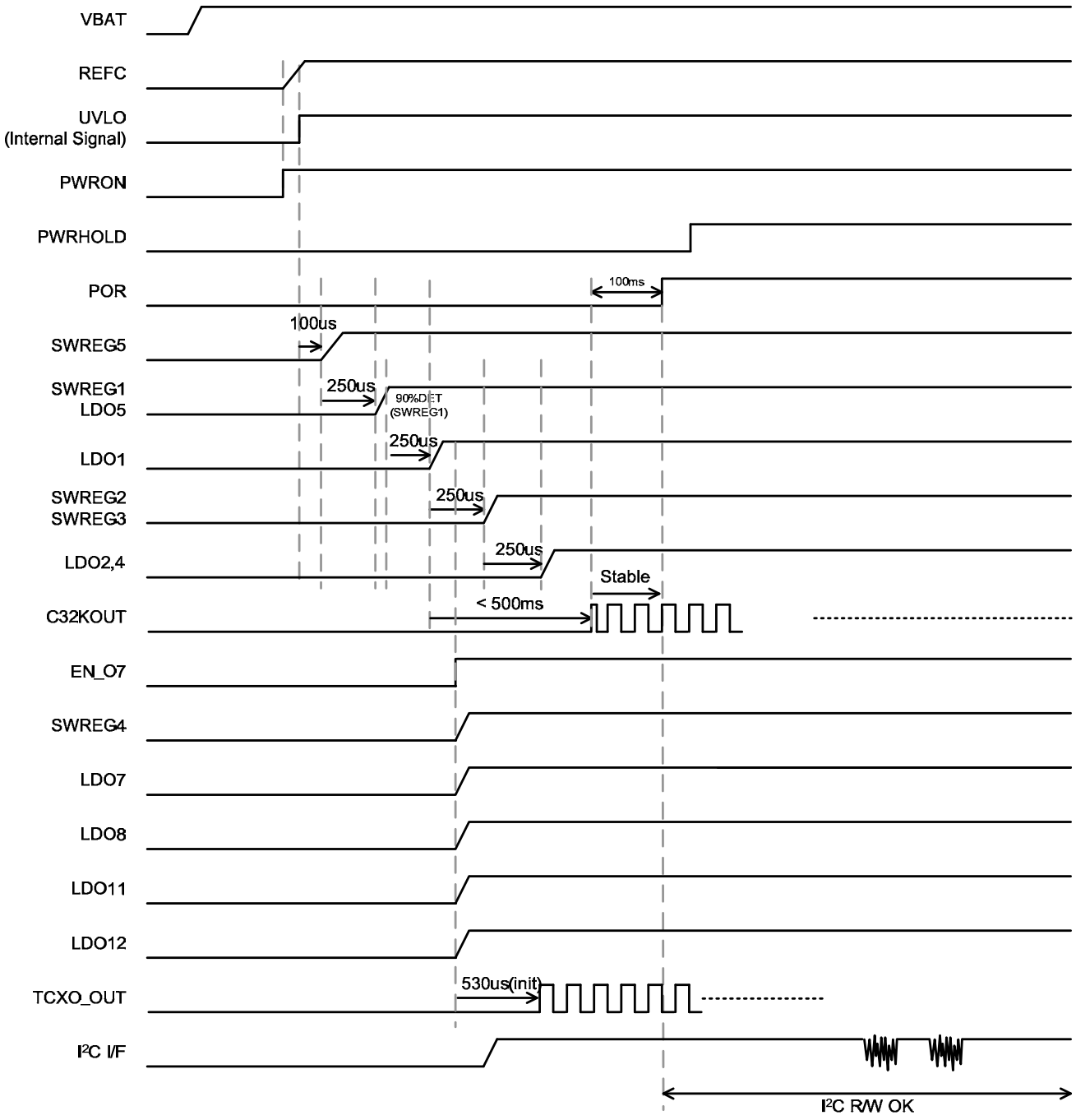


Figure 6. Power ON sequence (Start factor is PWRON)

The short detection circuit is built in the SWREG1,2,3,4 and 5 outputs.
When the output shorted state continued more than 100ms, the all LDO and SWREG will be OFF.
If the LDO and SWREG are turned off by the external pin (EN_O7) or I2C command, the short detection circuit is not detected.

The SWREG1, 2, 3, and 4 must be used external parts when not used SWREG's output voltage.
If it is not used the external parts in these SWREG, the short detector will detect when running the start up sequence.
(It is possible when these SWREG turn off by the I2C command after start up sequence.)

Power Off Sequence

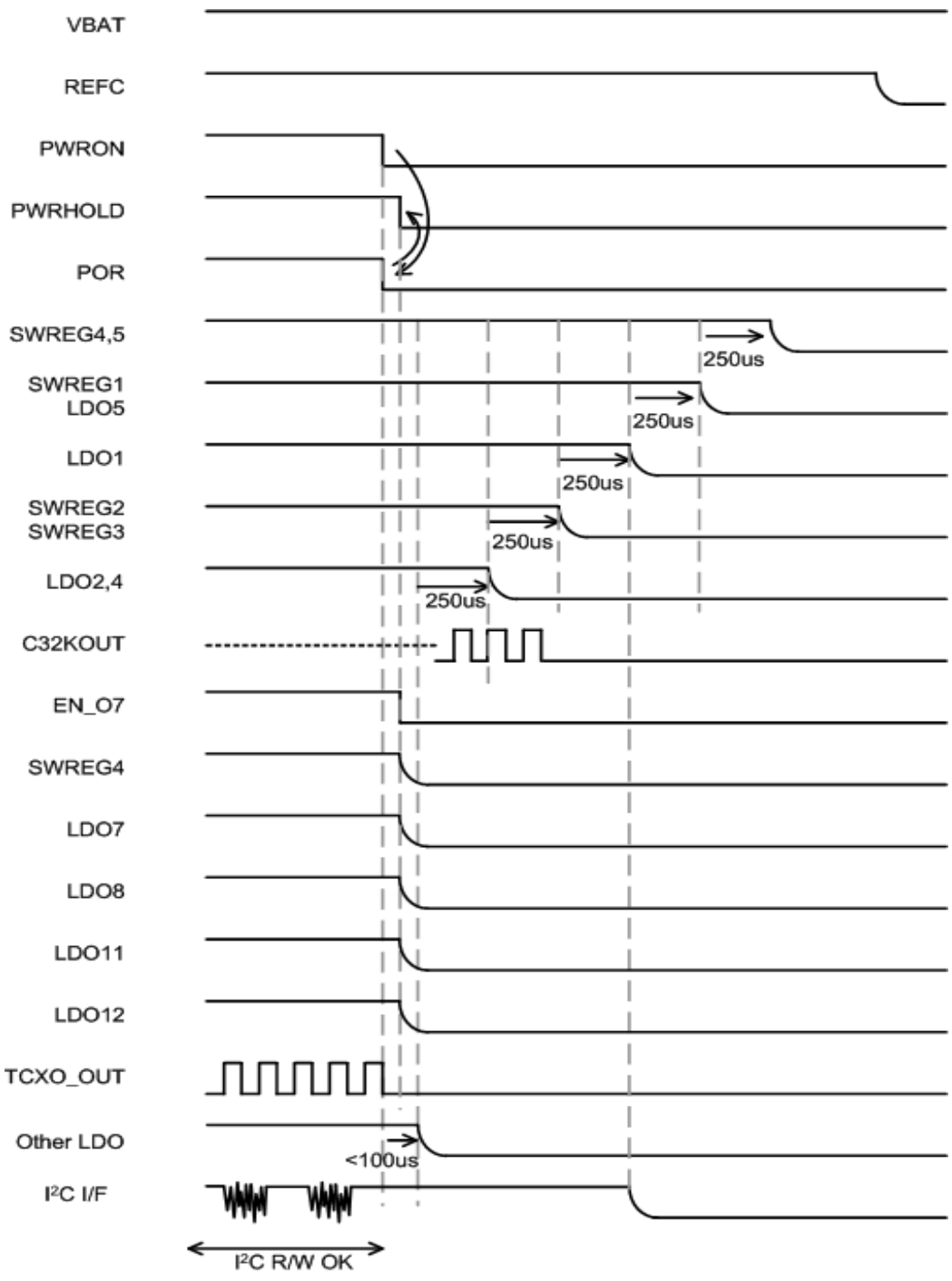


Figure 7. Power OFF sequence

Electrical Characteristics (Current Consumption)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT1, 2, 3, 4, 5=VIN1=VIN2=3.6V, DVDD=VDDOSC=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Circuit Current						
VBAT Circuit Current 1 (OFF)	IQVB1	-	0.3	1.0	µA	All LDO=OFF All SWREG=OFF DVDD=0V PWRON=L PWRHOLD=L EN_O7=L
VBAT Circuit Current 2 (Sleep)	IQVB2	-	280	475	µA	PWRON=H PWRHOLD=H LDO1,2,4,5=ON SWREG1,2,3,5=ON POR=H All SWREG=PFM/PWM auto mode All LDO,SWREG=No load 32kHz Buffer=ON EN_O7=L
VBAT Circuit Current 3 (All on)	IQVB3	-	580	1160	µA	PWRON=H PWRHOLD=H LDO1,2,3,4,5,6,7,8,9,10,11,12=ON SWREG1,2,3,4,5=ON POR=H All SWREG=PFM/PWM auto mode All LDO, SWREG=No load EN_O7=H

Electrical Characteristics (Logic Interface)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT1, 2, 3, 4, 5=VIN1=VIN2=3.6V, DVDD=OUT1)

Parameter	Symbol	Rating			Unit	Conditions
		Min	Typ	Max		
Digital characteristics (Digital Pins: EN_O7, PWRON as NMOS input) (Note1)						
Input "H" level	VIH1	1.44	-	-	V	
Input "L" level	VIL1	-	-	0.4	V	
Pull Down Resistance	RPD1	-	1.5	-	MΩ	PWRON, EN_O7
Digital characteristics (Digital Pins: SCL, SDA, PWRHOLD) (Note1)						
Input "H" level	VIH2	0.7× DVDD	-	DVDD+0.3	V	
Input "L" level	VIL2	-0.3	-	0.3× DVDD	V	
Input leak current	IIC2	-1	0	1	μA	
Digital characteristics (Digital Pins: PSET, ADRS)						
Input "H" level	VIH3	0.7× VBAT	-	VBAT+0.3	V	
Input "L" level	VIL3	-0.3	-	0.3× VBAT	V	
Input leak current	IIC3	-1	0	1	μA	
Digital characteristics (Digital Pins: SDA, POR)						
SDA output "L" level voltage	VOL1	-	-	0.4	V	IOL = 6mA
POR output "L" level voltage	VOL2	-	-	0.4	V	IOL = 1mA

(Note 1) The EN_07, PWRON, PWRHOLD and POR pin can be use under the Max VBAT+0.3V.

Electrical Characteristics (32 kHz Buffer)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT1, 2, 3, 4, 5=VIN1=VIN2=3.6V, DVDD=VDDOSC=OUT1)

Parameter	Symbol	Rating			Unit	Conditions
		Min	Typ	Max		
Digital characteristics (Digital Pins: C32KOUT)						
C32KOUT Output High Level	VOH_32K	0.8× OUT1	-	-	V	IO= -2mA
C32KOUT Output Low Level	VOL_32K	-	-	0.2× OUT1	V	IO= 2mA
32.768kHz Duty	DUTY	30	50	70	%	

Electrical Characteristics (SWREG1)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG1						
Output Voltage	VOSW1	1.067	1.100	1.133	V	initial value Io=100mA
Programmable Output Voltage	VOSW10 VOSW11 VOSW12 VOSW13	-3%	1.00 1.05 1.15 1.20	+3%	V	Io=100mA
Output Current	IOSW1	-	-	1000	mA	
Efficiency	ηSW1	-	86	-	%	Io=400mA, Vo=1.20V, VBAT=3.6V
Oscillating Frequency	FOSC1	-	2.0	-	MHz	Vo=1.10V (PWM mode, Io=100mA)
Output Inductance	LSWREG1	1.5	2.2	-	µH	Ta= -35～85°C
Output Capacitance	CSWREG1	4.7	10	-	µF	Ta= -35～85°C, with SWREG's DC bias

Electrical Characteristics (SWREG2)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG2						
Output Voltage	VOSW2	1.746	1.800	1.854	V	initial value Io=100mA
Programmable Output Voltage	VOSW20 VOSW21 VOSW22 VOSW23	-3%	1.70 1.75 1.85 1.90	+3%	V	Io=100mA
Output Current	IOSW2	-	-	500	mA	
Efficiency	ηSW2	-	86	-	%	Io= 200mA, Vo=1.80V, VBAT=3.6V
Oscillating Frequency	FOSC2	-	2.0	-	MHz	Vo=1.80V (PWM mode, Io=100mA)
Output Inductance	LSWREG2	1.5	2.2	-	µH	Ta= -35～85°C
Output Capacitance	CSWREG2	4.7	10	-	µF	Ta= -35～85°C, with SWREG's DC bias

Electrical Characteristics (SWREG3)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG3						
Output Voltage	VOSW3	1.164	1.200	1.236	V	initial value Io=100mA
Programmable Output Voltage	VOSW30 VOSW31 VOSW32 VOSW33	-3%	1.10 1.15 1.25 1.30	+3%	V	Io=100mA
Output Current	IOSW3	-	-	1000	mA	
Efficiency	ηSW3	-	86	-	%	Io=200mA, Vo=1.20V, VBAT=3.6V
Oscillating Frequency	FOSC3	-	2.0	-	MHz	Vo=1.20V (PWM mode, Io=100mA)
Output Inductance	LSWREG3	1.5	2.2	-	µH	Ta= -35～85°C
Output Capacitance	CSWREG3	4.7	10	-	µF	Ta= -35～85°C, with SWREG's DC bias

Electrical Characteristics (SWREG4)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG4						
Output Voltage	VOSW4	1.358	1.400	1.442	V	initial value Io=100mA
Programmable Output Voltage	VOSW40 VOSW41 VOSW42 VOSW43	-3%	1.50 1.45 1.35 1.30	+3%	V	Io=100mA
Output Current	IOSW4	-	-	500	mA	
Efficiency	ηSW4	-	87	-	%	Io=200mA, Vo=1.40V, VBAT=3.6V
Oscillating Frequency	FOSC4	-	2.0	-	MHz	Vo=1.40V (PWM mode, Io=100mA)
Output Inductance	LSWREG4	1.5	2.2	-	µH	Ta= -35～85°C
Output Capacitance	CSWREG4	4.7	10	-	µF	Ta= -35～85°C, with SWREG's DC bias

Electrical Characteristics (SWREG5)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG5						
Output Voltage	VOSW5	3.104	3.200	3.296	V	initial value Io=100mA
Programmable Output Voltage	VOSW50 VOSW51 VOSW52 VOSW53	-3%	3.300 3.250 3.150 3.100	+3%	V	Io=100mA
Output Current	IOSW5	-	-	1400	mA	
Efficiency	ηSW5	-	92	-	%	Io=400mA, Vo=3.20V, VBAT=3.6V
Oscillating Frequency	FOSC5	-	2.0	-	MHz	Vo=3.20V (PWM mode, Io=100mA)
Output Inductance	LSWREG5	1.5	2.2	-	µH	Ta= -35～85°C
Output Capacitance	CSWREG5	4.7	10	-	µF	Ta= -35～85°C, with SWREG's DC bias

Electrical Characteristics (LDO1)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO1						
Output Voltage A	VOM1A0	2.548	2.600	2.652	V	Initial setting, PSET=H Io=50mA
Output Voltage B	VOM1B0	1.764	1.800	1.836	V	Initial setting, PSET=L Io=50mA
Output Current	VOM1C	-	-	300	mA	
Dropout Voltage	VOM1DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.1V setting)
Input Voltage Stability	ΔVIM1	-	2	-	mV	VIN1=3~4.5V, Io=50mA
Load Stability	ΔVLM1	-	20	-	mV	Io=1mA ~ 300mA
Programmable Output Voltage A	VOM1A1 VOM1A2 VOM1A3 VOM1A4	-2%	2.70 2.65 2.55 2.50	+2%	V	Io=50mA
Programmable Output Voltage B	VOM1B1 VOM1B2 VOM1B3 VOM1B4	-2%	1.90 1.85 1.75 1.70	+2%	V	Io=50mA
Discharge Resistance	RDCHG1	-	100	-	ohm	
Ripple Rejection Ratio	RRM1	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=120Hz Io=50mA, Vo=2.60V BW=20Hz～20kHz
Output Capacitor	COUT1	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO2)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO2						
Output Voltage	VOM20	3.234	3.300	3.366	V	Io=50mA
Output Current	VOM2C	-	-	50	mA	
Dropout Voltage	VOM2DP	-	0.05	-	V	Io=50mA VBAT=2.8V(Vo=3.4V setting)
Input Voltage Stability	ΔVIM2	-	2	-	mV	VBAT=3.6~4.5V, Io=50mA
Load Stability	ΔVLM2	-	20	-	mV	Io=1mA ~ 50mA
Programmable Output Voltage	VOM21 VOM22 VOM23 VOM24	-2%	3.40 3.35 3.25 3.20	+2%	V	Io=50mA
Discharge Resistance	RDCHG2	-	100	-	ohm	
Ripple Rejection Ratio	RRM2	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=120Hz Io=50mA, Vo=3.3V BW=20Hz～20kHz
Output Capacitor	COUT2	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO3)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO3						
Output Voltage	VOM30	1.764	1.800	1.836	V	Io=50mA
Output Current	VOM3C	-	-	50	mA	
Dropout Voltage	VOM3DP	-	0.05	-	V	Io=50mA VBAT=2.8V(Vo=3.3V setting)
Input Voltage Stability	ΔVIM3	-	2	-	mV	VBAT=3.3~4.5V, Io=50mA
Load Stability	ΔVLM3	-	20	-	mV	Io=1mA ~ 50mA
Programmable Output Voltage B	VOM31 VOM32 VOM33 VOM34	-2%	1.90 1.85 1.75 1.70	+2%	V	Io=50mA
Discharge Resistance	RDCHG3	-	100	-	ohm	
Ripple Rejection Ratio	RRM3	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=120Hz Io=50mA, Vo=3.0V BW=20Hz～20kHz
Output Capacitor	COUT3	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO4)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO4						
Output Voltage	VOM40	2.744	2.800	2.856	V	Io=50mA
Output Current	VOM4C	-	-	300	mA	
Dropout Voltage	VOM4DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	ΔVIM4	-	2	-	mV	VBAT=3.2~4.5V, Io=50mA
Load Stability	ΔVLM4	-	20	-	mV	Io=1mA ~ 300mA
Programmable Output Voltage	VOM41 VOM42 VOM43 VOM44	-2%	2.90 2.85 2.75 2.70	+2%	V	Io=50mA
Discharge Resistance	RDCHG4	-	100	-	ohm	
Ripple Rejection Ratio	RRM4	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=120Hz Io=50mA, Vo=2.80V BW=20Hz～20kHz
Output Capacitor	COUT4	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO5)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO5						
Output Voltage	VOM50	1.176	1.200	1.224	V	Io=50mA
Output Current	VOM5C	-	-	150	mA	
Dropout Voltage	VOM5DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.1V setting)
Input Voltage Stability	ΔVIM5	-	2	-	mV	VIN1=3.0~4.5V, Io=50mA
Load Stability	ΔVLM5	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM51 VOM52 VOM53 VOM54	-2%	1.30 1.25 1.15 1.10	+2%	V	Io=50mA
Discharge Resistance	RDCHG5	-	100	-	ohm	
Ripple Rejection Ratio	RRM5	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Noise Level	VON5	-	60	-	μVrms	Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Capacitor	COUT5	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO6)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO6						
Output Voltage	VOM60	2.744	2.800	2.856	V	Io=50mA
Output Current	VOM6C	-	-	150	mA	
Dropout Voltage	VOM6DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	ΔVIM6	-	2	-	mV	VIN1=3.2~4.5V, Io=50mA
Load Stability	ΔVLM6	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM61 VOM62 VOM63 VOM64	-2%	2.90 2.85 2.75 2.70	+2%	V	Io=50mA
Discharge Resistance	RDCHG6	-	100	-	ohm	
Ripple Rejection Ratio	RRM6	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Noise Level	VON6	-	60	-	μVrms	Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Capacitor	COUT6	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO7)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO7						
Output Voltage	VOM70	2.744	2.800	2.856	V	Io=50mA
Output Current	VOM7C	-	-	50	mA	
Dropout Voltage	VOM7DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	ΔVIM7	-	2	-	mV	VIN1=3.2~4.5V, Io=50mA
Load Stability	ΔVLM7	-	20	-	mV	Io=1mA ~ 50mA
Programmable Output Voltage	VOM71 VOM72 VOM73 VOM74	-2%	2.90 2.85 2.75 2.70	+2%	V	Io=50mA
Discharge Resistance	RDCHG7	-	100	-	ohm	
Ripple Rejection Ratio	RRM7	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Noise Level	VON7	-	60	-	μVrms	Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Capacitor	COUT7	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO8)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO8						
Output Voltage	VOM80	2.45	2.50	2.55	V	Io=50mA
Output Current	VOM8C	-	-	150	mA	
Dropout Voltage	VOM8DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	ΔVIM8	-	2	-	mV	VIN1=3.0~4.5V, Io=50mA
Load Stability	ΔVLM8	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM81 VOM82 VOM83 VOM84	-2%	2.60 2.55 2.45 2.40	+2%	V	Io=50mA
Discharge Resistance	RDCHG8	-	100	-	ohm	
Ripple Rejection Ratio	RRM8	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Noise Level	VON8	-	60	-	μVrms	Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Capacitor	COUT8	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO9)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO9						
Output Voltage	VOM90	2.744	2.800	2.856	V	Io=50mA
Output Current	VOM9C	-	-	150	mA	
Dropout Voltage	VOM9DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	ΔVIM9	-	2	-	mV	VIN1=3.2~4.5V, Io=50mA
Load Stability	ΔVLM9	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM91 VOM92 VOM93 VOM94	-2%	2.90 2.85 2.75 2.70	+2%	V	Io=50mA
Discharge Resistance	RDCHG9	-	100	-	ohm	
Ripple Rejection Ratio	RRM9	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Noise Level	VON9	-	60	-	μVrms	Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Capacitor	COUT9	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO10)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO10						
Output Voltage	VOM100	2.744	2.800	2.856	V	Io=50mA
Output Current	VOM10C	-	-	150	mA	
Dropout Voltage	VOM10DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	ΔVIM10	-	2	-	mV	VIN1=3.2~4.5V, Io=50mA
Load Stability	ΔVLM10	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM101 VOM102 VOM103 VOM104	-2%	2.90 2.85 2.75 2.70	+2%	V	Io=50mA
Discharge Resistance	RDCHG10	-	100	-	ohm	
Ripple Rejection Ratio	RRM10	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Noise Level	VON10	-	60	-	μVrms	Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Capacitor	COUT10	0.47	1.0	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO11)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO11						
Output Voltage	VOM110	1.176	1.200	1.224	V	Io=50mA
Output Current	VOM11C	-	-	150	mA	
Dropout Voltage	VOM11DP	-	0.03	-	V	Io=50mA VIN2=1.2V(Vo=1.2V setting)
Input Voltage Stability	ΔVIM11	-	2	-	mV	VBAT=3.2~4.5V, Io=50mA
Load Stability	ΔVLM11	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM111 VOM112 VOM113 VOM114	-2%	1.30 1.25 1.15 1.10	+2%	V	Io=50mA
Discharge Resistance	RDCHG11	-	100	-	ohm	
Ripple Rejection Ratio	RRM11	-	70	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Noise Level	VON11	-	60	-	μVrms	Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Capacitor	COUT11	1.0	2.2	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (LDO12)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO12						
Output Voltage	VOM120	1.176	1.200	1.224	V	Io=50mA
Output Current	VOM12C	-	-	150	mA	
Dropout Voltage	VOM12DP	-	0.03	-	V	Io=50mA VIN2=1.2V(Vo=1.2V setting)
Input Voltage Stability	ΔVIM12	-	2	-	mV	VBAT=3.2~4.5V, Io=50mA
Load Stability	ΔVLM12	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM121 VOM122 VOM123 VOM124	-2%	1.30 1.25 1.15 1.10	+2%	V	Io=50mA
Discharge Resistance	RDCHG12	-	100	-	ohm	
Ripple Rejection Ratio	RRM12	-	70	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Noise Level	VON12	-	60	-	μVrms	Io=50mA, Vo=1.20V BW=20Hz～20kHz
Output Capacitor	COUT12	1.0	2.2	-	μF	Ta=-35～85°C, with LDO's DC bias

Electrical Characteristics (SIMCARD interface)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V (FB5), VIN2=1.4V (FB4), DVDD=OUT1)

Parameter	Symbol	SPEC			Unit	Condition
		Min	Typ	Max		
Digital Characteristics (SIMRSTIN pin)						
Input H Level	VIHURST	0.7*OUT1	-	-	V	
Input L Level	VILURST	-	-	0.2*OUT1	V	
Digital Characteristics (SIMCLKIN pin)						
Input H Level	VIHUCLK	0.7*OUT1	-	-	V	
Input L Level	VILUCLK	-	-	0.2*OUT1	V	
MAX Clock Frequency	FSIMMAX	-	-	20	MHz	
Digital Characteristics (SIMIODBB pin)						
Pull-Up Resistor	RPUSIM	13	20	28	kΩ	
Input H Level	VIHUDBB	OUT1-0.6	-	-	V	(Note1)
Input L Level	VILUDBB	-	-	0.3	V	(Note2)
Input H Current	LINHSIM	-	-	20	µA	SIMIODBB=OUT1
Input L Current	LINLSIM	-	-	1	mA	SIMIODBB=0.3V SIMIO=OPEN
Output H Level	VOHUDBB	0.7*OUT1	-	-	V	I_O=20µA
Output L Level	VOLUDBB	-	-	0.4	V	I_{IN}=200µA, SIMIO=0V
Timing Parameter (Cout=30pF, LDO1=LDO3=1.8V)						
SIMRSTOUT Rise/Fall Time	TIMRST	-	-	18	nsec	
SIMCLKOUT Rise/Fall Time	TIMCLK	-	-	18	nsec	
SIMIO Rise/Fall Time	TIMIO	-	-	1.0	µsec	
SIMIODBB Rise/Fall Time	TIMIODB	-	-	1.2	µsec	

(Note1) Input H Level is defined as the Voltage at which the Output SIMIODBB Voltage Equals 0.5V.

(Note2) Input L Level is defined as the Voltage at which the Output SIMIODBB Voltage Exceeds the Input SIMIO Voltage by 100mV.

SIMCARD Interface Electrical Characteristics

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V (FB5), VIN2=1.4V (FB4), DVDD=OUT1)

Parameter	Symbol	SPEC			Unit	Condition
		Min	Typ	Max		
Digital Characteristics (SIMRSTOUT pin)						
Output H Level	VOHURSTOUT	0.8*OUT3	-	-	V	I_O=200µA
Output L Level	VOLURSTOUT	-	-	0.4	V	I_{IN}=200µA
Digital Characteristics (SIMCLKOUT pin)						
Output H Level	VOHUCLKOUT	0.8*OUT3	-	-	V	I_O=200µA
Output L Level	VOLUCLKOUT	-	-	0.4	V	I_{IN}=200µA
Digital Characteristics (SIMIO pin)						
Pull-Up Resistor	RPUIO	6.5	10	14	kΩ	
Input H Level	VIHUIMIO	0.7*OUT3	-	-	V	(Note1)
Input L Level	VILUIMIO	0	-	0.3	V	(Note2)
Input H Current	LINHIO	-	-	20	µA	SIMIO = OUT3
Input L Current	LINLIO	-	-	1	mA	SIMIO = 0.3V
Output H Level	VOHUIMIO	0.8*OUT3	-	-	V	I_O=20µA
Output L Level	VOLUIMIO	-	-	0.4	V	I_{IN}=200µA, SIMIODBB=0V

(Note1) Input H Level is defined as the Voltage at which the Output SIMIO Voltage Equals 0.5V.

(Note2) Input L Level is defined as the Voltage at which the Output SIMIO Voltage Exceeds the Input SIMIODBB Voltage by 100mV.

Electrical Characteristics (4ch Analog SW)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	SPEC			Unit	Condition
		Min	Typ	Max		
4ch-Analog SW Input Selector						
Input Range	VINSW	0	-	2.2	V	
ASWIN1 ASWIN2 ASWIN3 ASWIN4 Input Leak Current when OFF or Non-Selected	IINSW	-	-	1	µA	
Between ASWIN1 ASWIN2 ASWIN3 ASWIN4 and ASWOUT ON Resistance when Selected	RONSW	-	100	200	Ω	ANASW_EN='1' VINSW=1.0V

Electrical Characteristics (CLOCK DRIVER)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1, VDDTCXO=OUT7)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
CLOCK DRIVER						
TCXO_IN Input Frequency 1	FTHRU1	-	19.2	-	MHz	
TCXO_IN Input Frequency 2	FTHRU2	-	26.0	-	MHz	
TCXO_IN Input Range	VPPCD	0.6	-	1.2	Vpp	
TCXO_OUT Output Frequency 1	FOUT1	18.2	19.2	20.2	MHz	Used 19.2MHz clock
TCXO_OUT Output Frequency 2	FOUT2	25.0	26.0	27.0	MHz	Used 26MHz clock
Output Pulse Width 1	TLWCD1	20	-	-	ns	Low Level CL=10pF
	THWCD1	20	-	-	ns	High Level CL=10pF
Output Pulse Width 2	TLWCD2	13	-	-	ns	Low Level CL=10pF
	THWCD2	13	-	-	ns	High Level CL=10pF
Output Rise Time	TRCD	-	-	6	ns	Tr CL=10pF
Output Fall Time	TFCD	-	-	6	ns	Tf CL=10pF

Electrical Characteristics (I2C AC Characteristics)

AC Characteristics On I2C bus.

Characteristics	Symbol	Min	Max	Unit
CLK Clock Frequency	f_{CLK}	0	400	kHz
CLK Clock "LOW" Time	t_{LOW}	1.3	-	µs
CLK Clock "HIGH" Time	t_{HIGH}	0.6	-	µs
Bus Free Time	t_{BUF}	1.3	-	µs
Start Condition Hold Time	$t_{HD.STA}$	0.6	-	µs
Start Condition Setup Time	$t_{SU.STA}$	0.6	-	µs
Data Input Hold Time	$t_{HD.DAT}$	0	-	ns
Data Input Setup Time	$t_{SU.DAT}$	100	-	ns
Stop Condition Setup Time	$t_{SU.STO}$	0.6	-	µs

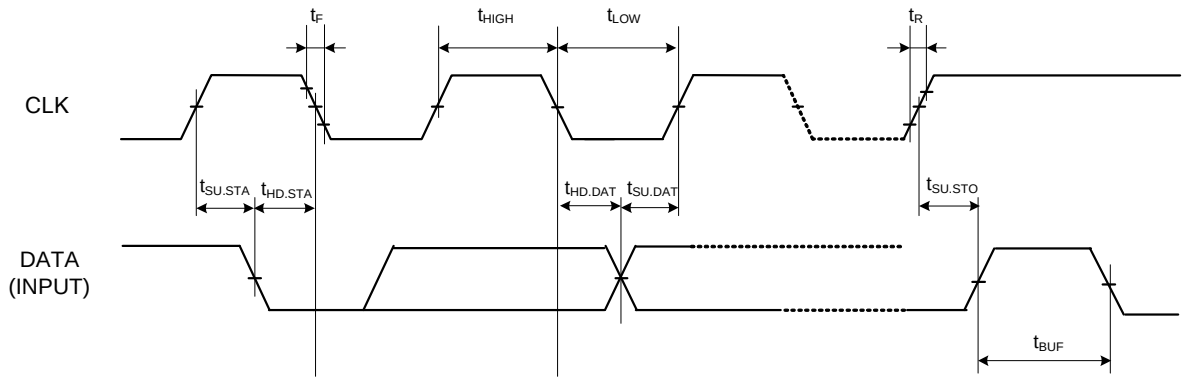


Figure 8. Bus Timing 1

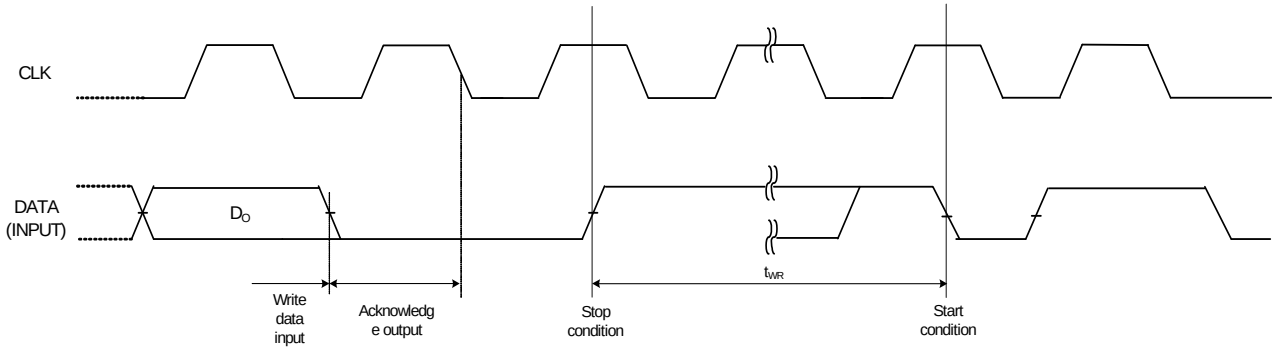


Figure. 9 Bus Timing 2

I2C Bus Interface

The I2C compatible synchronous serial interface provides access to programmable functions and register on the device.
This protocol uses a two-wire interface for bi-directional communications between the LSI's connected to the bus.
The two interface lines are the Serial Data Line (DATA), and the Serial Clock Line (CLK). These lines should be connected to the power supply DVDD by a pull-up resistor, and remain high even when the bus is idle.

1. Start and Stop Conditions

When CLK is high, pulling DATA low produces a start condition and pulling DATA high produces a stop condition. Every instruction is started when a start condition occurs and terminated when a stop condition occurs.
During read, a stop condition causes the read to terminate and the chip enters the standby state.
During write, a stop condition causes the fetching of write data to terminate, after which writing starts automatically. Upon the completion of writing, the chip enters the standby state.
Two or more start conditions cannot be entered consecutively.

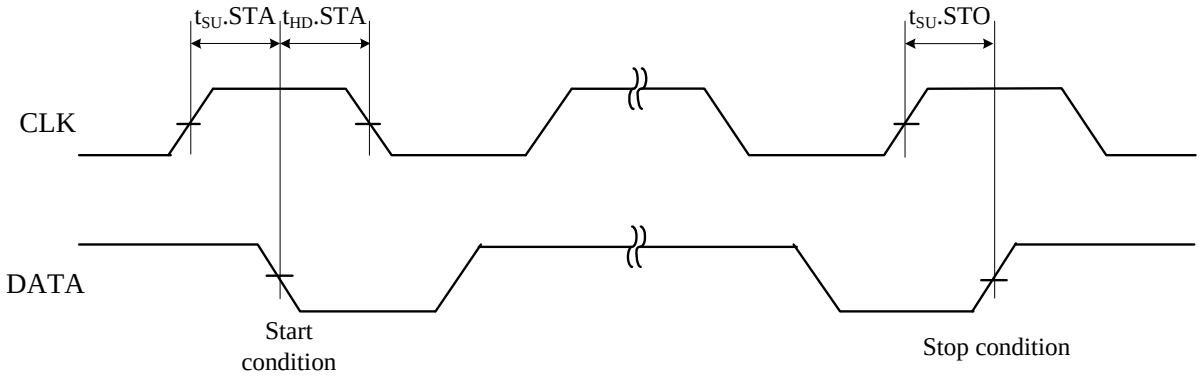


Figure. 10. Start and Stop Conditions

2. Modifying Data

Data on the DATA input can be modified while CLK is low. When CLK is high, modifying the DATA input means a start or stop condition.

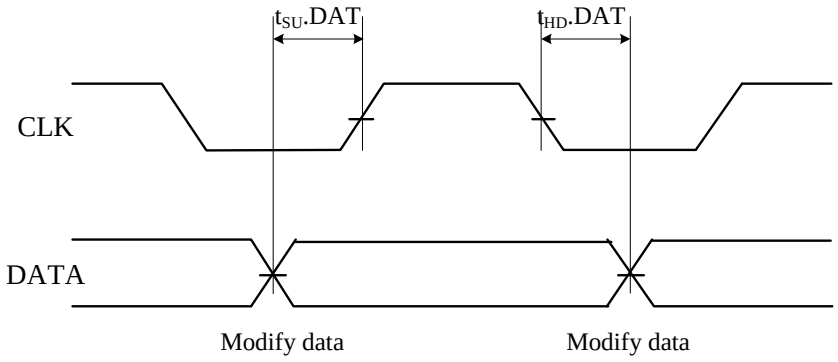


Figure 11. Modifying Data

3. Acknowledge

Data is transmitted and received in 8-bit units. The receiver sends an acknowledge signal by outputting a low on DATA in the 9th clock cycle, indicating that it has received data normally. The transmitter releases the bus in the 9th clock cycle to receive an acknowledge signal.

During write, the chip is always the receiver so that it outputs an acknowledge signal each time it has received eight bits of data.

During read, the chip outputs an acknowledge signal after it receives an address following a start condition. Then, it outputs read data and releases the bus to wait for an acknowledge signal from the master. When it detects an acknowledge signal, it outputs data at the next address if it does not detect a stop condition. If the chip does not detect an acknowledge signal, it stops read operation, and enters the standby state when a stop condition occurs subsequently.

If the chip does not detect an acknowledge signal nor a stop condition, it keeps the bus released.

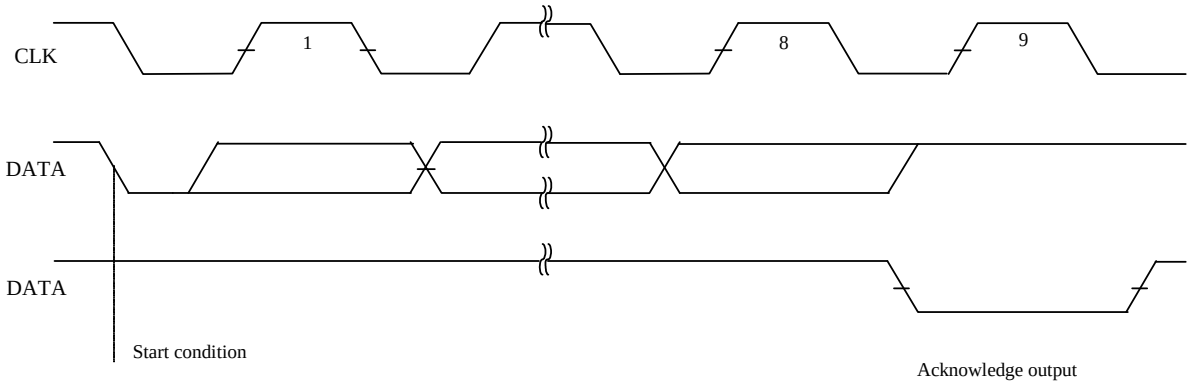


Figure 12. Acknowledge

4. Device Addressing

After a start condition occurs, a 7-bit device address and a 1-bit read/write instruction code are inputted into the chip.

The upper seven bits are called device address, which must always be “1001011” (ADRS=L) or “1001100” (ADRS=H).

The least significant bit *(R / W : READ / WRITE)* indicates a read instruction when set to 1 and a write instruction when set to 0.

An instruction is not executed if the device address does not match the specified value.

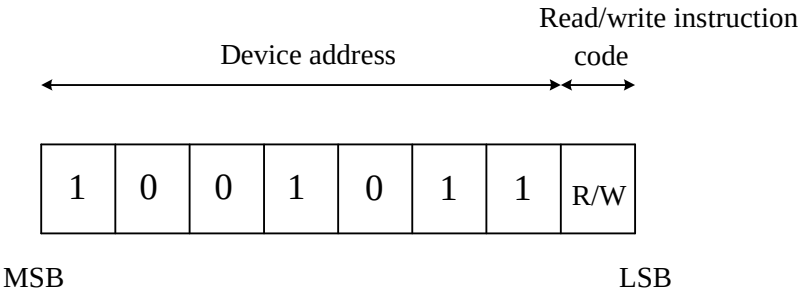


Figure 13. Device Addressing (Device address is “ 1001011” or "1001100".)

5. Write Operation

In order to write a specified address, after a start condition, input a device address, *R/W(=0)*, a word address, and write data.
When a stop condition is entered, the chip automatically enters standby state.
Address increment is acknowledged only whenever INC bit is'0'.

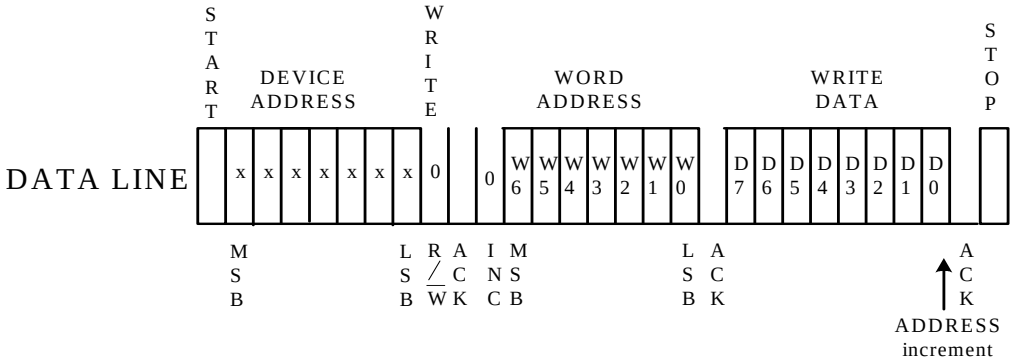


Figure 14. Write Operation

<Address Increment ON>

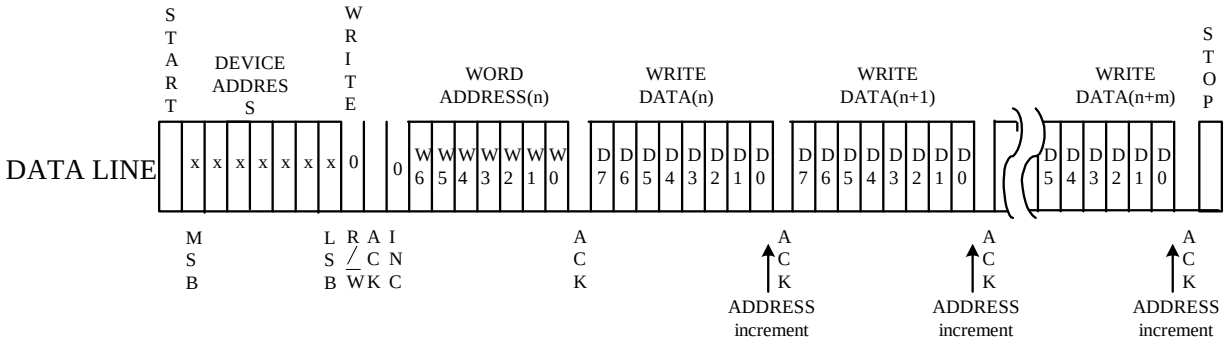


Figure 15. Address Increment ON

<Address Increment OFF>

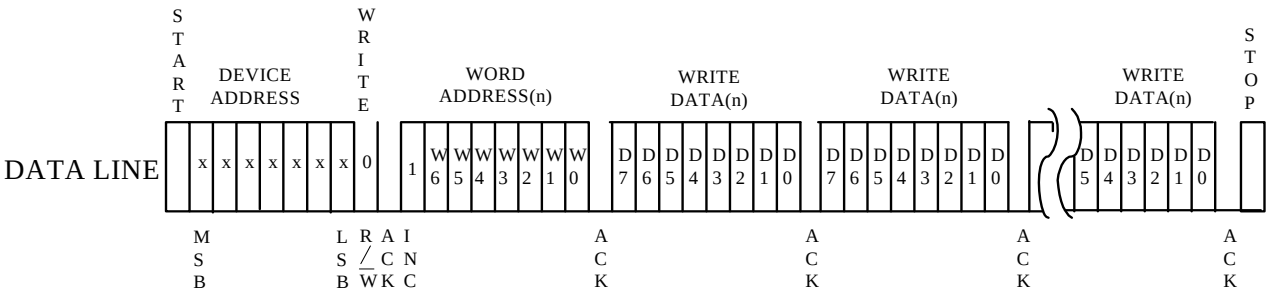


Figure 16. Address Increment OFF

Roll over function operates when address increment is ON, after a start condition, input a device address, *R / W (= 0),* a word address*(n)*, and write data *(n)*, in the same way as for a byte write. Then, input write data *(n +1)* immediately without entering a stop condition, while checking that an acknowledge signal is asserted *(0)*.
When the last address (14H) is reached, the word address is rolled over to the first address (00H) of the page.

Write Operation Example (Auto Increment OFF)

(Write to Address 00h, Data 32h)
When writing to a single address follow the sequence below.
START => DEVICE ADDRESS+WRITE => WORD ADDRESS => DATA => STOP
At this time, the Auto increment bit (=INC) can be either 'H' or 'L'.

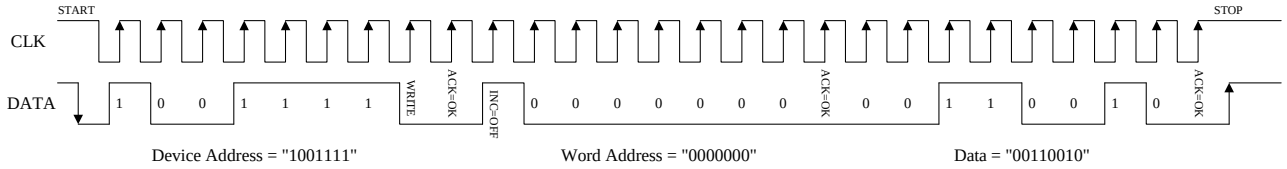


Figure 17. Write Operation Example (Auto Increment OFF)

Write Operation Example (Auto Increment ON)

(Write to Address 01h, Data 04h;
Address 02h, Data A0h;
Address 03h, Data 6Eh;
Address 04h, Data 0Fh)
When writing to multiple addresses follow the sequence below.
START => DEVICE ADDRESS+WRITE => WORD ADDRESS => DATA => DATA => DATA => DATA => STOP
At this time, the Auto increment bit (=INC) needs to be 'L'.
When writing the Word address, write the first address which you want to start writing from.

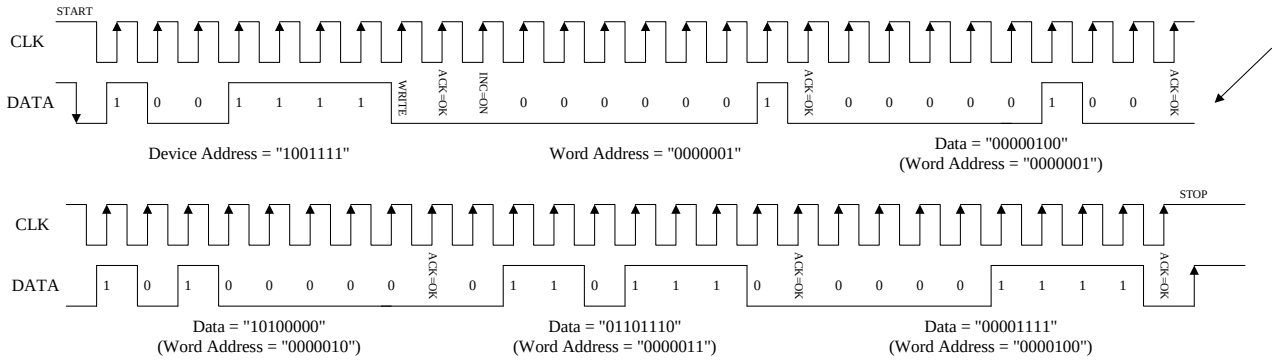


Figure 18. Write Operation Example (Auto Increment ON)

Read Operation Example (Auto Increment ON)

(Read from Address 01h, 02h, 03h, 04h, 05h)
To read from Address 01h, you must first dummy write to Address 01h.
At this time, the Auto increment bit (=INC) needs to be 'L'.
When finish reading, you must end by returning an ACK=NG ('H'), and then stop.
The read sequence would be as shown below.
START => DEVICE ADDRESS+WRITE => WORD ADDRESS => STOP => START => DEVICE ADDRESS+READ =>
DATA READ + ACK OK => DATA READ + ACK OK => DATA READ + ACK OK => DATA READ + ACK OK =>
DATA READ + ACK NG => STOP

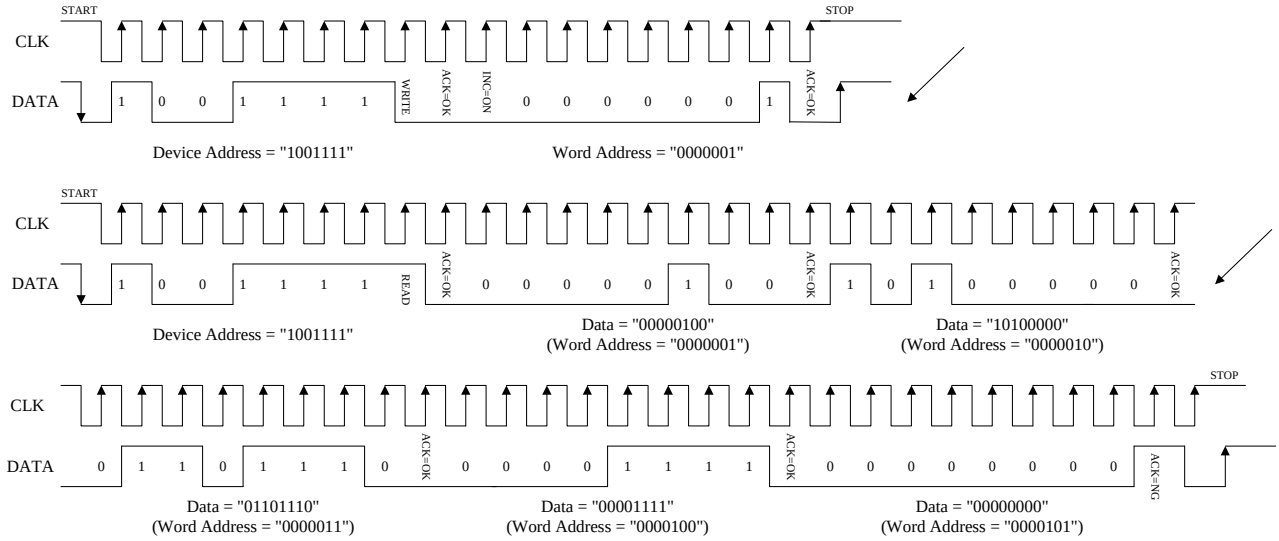


Figure 19. Read Operation Example (Auto Increment ON)

Register Map (LDO and SWREG Control)

Address	Register name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0
00h	LDOCNT1	R/W	1Bh	LDO8ON	LDO7ON	LDO6ON	LDO5ON	LDO4ON	LDO3ON	LDO2ON	LDO1ON
01h	LDOCNT2	R/W	00h	-	-	-	-	LDO12ON	LDO11ON	LDO10ON	LDO9ON
02h	SWREGCNT	R/W	17h	-	-	-	SWREG5ON	SWREG4ON	SWREG3ON	SWREG2ON	SWREG1ON
03h	LDOADJ1	R/W	DXh (Note1)	LDO2ADJ [3:0]				LDO1ADJ [3:0]			
04h	LDOADJ2	R/W	C2h	LDO4ADJ [3:0]				LDO3ADJ [3:0]			
05h	LDOADJ3	R/W	C4h	LDO6ADJ [3:0]				LDO5ADJ [3:0]			
06h	LDOADJ4	R/W	6Ch	LDO8ADJ [3:0]				LDO7ADJ [3:0]			
07h	LDOADJ5	R/W	CCh	LDO10ADJ [3:0]				LDO9ADJ [3:0]			
08h	LDOADJ6	R/W	44h	-	LDO12ADJ [2:0]			-	LDO11ADJ [2:0]		
09h	SWREGADJ1	R/W	D2h	SWREG2ADJ [3:0]				SWREG1ADJ [3:0]			
0Ah	SWREGADJ2	R/W	84h	SWREG4ADJ [3:0]				SWREG3ADJ [3:0]			
0Bh	SWREGADJ3	R/W	0Bh	-	-	-	-	SWREG5ADJ [3:0]			
0Ch	ENLD_DIS	R/W	00h	-	-	-	-	-	-	-	ENLD7_DIS
0Dh	LDOPD1_DIS	R/W	00h	LDO8PD_DIS	LDO7PD_DIS	LDO6PD_DIS	LDO5PD_DIS	LDO4PD_DIS	LDO3PD_DIS	LDO2PD_DIS	LDO1PD_DIS
0Eh	LDOPD2_DIS	R/W	00h	-	-	-	-	LDO12PD_DIS	LDO11PD_DIS	LDO10PD_DIS	LDO9PD_DIS
0Fh	SWREGPD_DIS	R/W	00h	-	-	-	SWREG5PD_DIS	SWREG4PD_DIS	SWREG3PD_DIS	SWREG2PD_DIS	SWREG1PD_DIS
10h	ANASW_CNT	R/W	00h	-	-	-	-	-	ANASW_EN	ANASW_SEL[1:0]	
11h	TCXO_CNT	R/W	40h	-	TCXO_MASK 2:0]			-	-	TCXO_EN	TCXO_SEL
12h	OSC_CNT	R/W	03h	-	-	-	-	-	-	C32KOUT_EN	OSC_EN
13h	SWREGPWM	R/W	00h	-	-	-	SWREG5 PWM	SWREG4 PWM	SWREG3 PWM	SWREG2 PWM	SWREG1 PWM
14h	SW5BYPASS	R/W	01h	-	reserved (Note2)	reserved (Note2)	BYPASS_DIS	-	VINDET5ADJ[2:0]		

(Note1) Initial value is decided by PSET pin condition.

(Note2) Please always write "0" to the reserved registers when in use.

Address 00h : LDOCNT1 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	LDOCNT1	R/W	LDO8ON	LDO7ON	LDO6ON	LDO5ON	LDO4ON	LDO3ON	LDO2ON	LDO1ON
Initial Value		1Bh	0	0	0	1	1	0	1	1

The LDO7 is controlled by EN_O7 pin by deafult.

Bit0: LDO1ON LDO1 Power ON/OFF control
"0" : OFF
"1" : ON (Initial state)

Bit1: LDO2ON LDO2 Power ON/OFF control
"0" : OFF
"1" : ON (Initial state)

Bit2: LDO3ON LDO3 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

Bit3: LDO4ON LDO4 Power ON/OFF control
"0" : OFF
"1" : ON (Initial state)

Bit4: LDO5ON LDO5 Power ON/OFF control
"0" : OFF
"1" : ON (Initial state)

Bit5: LDO6ON LDO6 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

Bit6: LDO7ON LDO7 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

Bit7: LDO8ON LDO8 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

(Note) Please refer P53

Address 01h : LDOCNT2 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	LDOCNT2	R/W	-	-	-	-	LDO12ON	LDO11ON	LDO10ON	LDO9ON
Initial Value		00h	0	0	0	0	0	0	0	0

Bit0: LDO9ON LDO9 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

Bit1: LDO10ON LDO10 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

Bit2: LDO11ON LDO11 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

Bit3: LDO12ON LDO12 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

Whenever the LDO11, 12 power VIN2 is supplied by SWREG4, the SWREG4 must be turned ON at least 250us before the LDO11, 12 is turned ON.

<ON sequence example>
SWREG4=ON
Wait for 250us or more
LDO11, 12=ON

Turning the LDO11,12 OFF will be the opposite sequence, turning OFF the LDO11,12 first, and then turning OFF the SWREG4.

<OFF sequence example>
LDO11, 12=OFF
No wait needed
SWREG4=OFF

Address 02h : SWREGCNT Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	SWREGCNT	R/W	-	-	-	SWREG5 ON	SWREG4 ON	SWREG3 ON	SWREG2 ON	SWREG1 ON
Initial Value		17h	0	0	0	1	0	1	1	1

Bit0: SWREG1ON SWREG1 Power ON/OFF control
"0" : OFF
"1" : ON (Initial state)

Bit1: SWREG2ON SWREG2 Power ON/OFF control
"0" : OFF
"1" : ON (Initial state)

Bit2: SWREG3ON SWREG3 Power ON/OFF control
"0" : OFF
"1" : ON (Initial state)

Bit3: SWREG4ON SWREG4 Power ON/OFF control
"0" : OFF (Initial state)
"1" : ON

Bit4: SWREG5ON SWREG5 Power ON/OFF control
"0" : OFF
"1" : ON (Initial state)

Address 03h : LDOADJ1 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03h	LDOADJ1	R/W	LDO2ADJ[3:0]				LDO1ADJ[3:0]			
Initial Value		DXh	1	1	0	1	X	X	X	X

Bit[3:0]: LDO1ADJ[3:0] LDO1 output voltage control

"0000" : 1.70V
"0001" : 1.75V
"0010" : 1.80V (Initial state when PSET='L')
"0011" : 1.85V
"0100" : 1.90V
"0101" : 2.50V
"0110" : 2.55V
"0111" : 2.60V (Initial state when PSET='H')
"1000" : 2.65V
"1001" : 2.70V
"1010" : 2.80V
"1011" : 2.90V
"1100" : 2.95V
"1101" : 3.00V
"1110" : 3.05V
"1111" : 3.10V

Bit[7:4]: LDO2ADJ[3:0] LDO2 output voltage control

"0000" : 2.55V
"0001" : 2.60V
"0010" : 2.65V
"0011" : 2.75V
"0100" : 2.80V
"0101" : 2.85V
"0110" : 2.90V
"0111" : 2.95V
"1000" : 3.00V
"1001" : 3.05V
"1010" : 3.10V
"1011" : 3.20V
"1100" : 3.25V
"1101" : 3.30V (Initial state)
"1110" : 3.35V
"1111" : 3.40V

Address 04h : LDOADJ2 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	LDOADJ2	R/W	LDO4ADJ[3:0]				LDO3ADJ[3:0]			
Initial Value		C2h	1	1	0	0	0	0	1	0

Bit[3:0]: LDO3ADJ[3:0] LDO3 output voltage control

"0000" : 1.70V
"0001" : 1.75V
"0010" : 1.80V (Initial state)
"0011" : 1.85V
"0100" : 1.90V
"0101" : 2.50V
"0110" : 2.60V
"0111" : 2.70V
"1000" : 2.80V
"1001" : 2.90V
"1010" : 2.95V
"1011" : 3.00V
"1100" : 3.05V
"1101" : 3.10V
"1110" : 3.20V
"1111" : 3.30V

Bit[7:4]: LDO4ADJ[3:0] LDO4 output voltage control

"0000" : 1.10V
"0001" : 1.20V
"0010" : 1.30V
"0011" : 1.70V
"0100" : 1.80V
"0101" : 1.90V
"0110" : 2.50V
"0111" : 2.55V
"1000" : 2.60V
"1001" : 2.65V
"1010" : 2.70V
"1011" : 2.75V
"1100" : 2.80V (Initial state)
"1101" : 2.85V
"1110" : 2.90V
"1111" : 3.00V

Address 05h : LDOADJ3 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
05h	LDOADJ3	R/W	LDO6ADJ[3:0]				LDO5ADJ[3:0]			
Initial Value		C4h	1	1	0	0	0	1	0	0

Bit[3:0]: LDO5ADJ[3:0] LDO5 output voltage control

"0000" : 1.00V
"0001" : 1.05V
"0010" : 1.10V
"0011" : 1.15V
"0100" : 1.20V (Initial state)
"0101" : 1.25V
"0110" : 1.30V
"0111" : 1.70V
"1000" : 1.80V
"1001" : 1.90V
"1010" : 2.60V
"1011" : 2.70V
"1100" : 2.80V
"1101" : 2.90V
"1110" : 3.00V
"1111" : 3.10V

Bit[7:4]: LDO6ADJ[3:0] LDO6 output voltage control

"0000" : 1.10V
"0001" : 1.20V
"0010" : 1.30V
"0011" : 1.70V
"0100" : 1.80V
"0101" : 1.90V
"0110" : 2.50V
"0111" : 2.55V
"1000" : 2.60V
"1001" : 2.65V
"1010" : 2.70V
"1011" : 2.75V
"1100" : 2.80V (Initial state)
"1101" : 2.85V
"1110" : 2.90V
"1111" : 3.00V

Address 06h : LDOADJ4 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	LDOADJ4	R/W	LDO8ADJ[3:0]				LDO7ADJ[3:0]			
Initial Value		6Ch	0	1	1	0	1	1	0	0

Bit[3:0]: LDO7ADJ[3:0] LDO7 output voltage control

"0000" : 1.10V
"0001" : 1.20V
"0010" : 1.30V
"0011" : 1.70V
"0100" : 1.80V
"0101" : 1.90V
"0110" : 2.50V
"0111" : 2.55V
"1000" : 2.60V
"1001" : 2.65V
"1010" : 2.70V
"1011" : 2.75V
"1100" : 2.80V (Initial state)
"1101" : 2.85V
"1110" : 2.90V
"1111" : 3.00V

Bit[7:4]: LDO8ADJ[3:0] LDO8 output voltage control

"0000" : 1.20V
"0001" : 1.30V
"0010" : 1.70V
"0011" : 1.80V
"0100" : 2.40V
"0101" : 2.45V
"0110" : 2.50V (Initial state)
"0111" : 2.55V
"1000" : 2.60V
"1001" : 2.65V
"1010" : 2.70V
"1011" : 2.75V
"1100" : 2.80V
"1101" : 2.85V
"1110" : 2.90V
"1111" : 3.00V

Address 07h : LDOADJ5 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
07h	LDOADJ5	R/W	LDO10ADJ[3:0]				LDO9ADJ[3:0]			
Initial Value		CCh	1	1	0	0	1	1	0	0

Bit[3:0]: LDO9ADJ[3:0] LDO9 output voltage control

"0000" : 1.10V
"0001" : 1.20V
"0010" : 1.30V
"0011" : 1.70V
"0100" : 1.80V
"0101" : 1.90V
"0110" : 2.50V
"0111" : 2.55V
"1000" : 2.60V
"1001" : 2.65V
"1010" : 2.70V
"1011" : 2.75V
"1100" : 2.80V (Initial state)
"1101" : 2.85V
"1110" : 2.90V
"1111" : 3.00V

Bit[7:4]: LDO10ADJ[3:0] LDO10 output voltage control

"0000" : 1.10V
"0001" : 1.20V
"0010" : 1.30V
"0011" : 1.70V
"0100" : 1.80V
"0101" : 1.90V
"0110" : 2.50V
"0111" : 2.55V
"1000" : 2.60V
"1001" : 2.65V
"1010" : 2.70V
"1011" : 2.75V
"1100" : 2.80V (Initial state)
"1101" : 2.85V
"1110" : 2.90V
"1111" : 3.00V

LDOADJ6 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08h	LDOADJ6	R/W	-	LDO12ADJ[2:0]			-	LDO11ADJ[2:0]		
Initial Value		44h	0	1	0	0	0	1	0	0

Bit[3:0]: LDO11ADJ[3:0] LDO11 output voltage control

"000" : 1.00V
"001" : 1.05V
"010" : 1.10V
"011" : 1.15V
"100" : 1.20V (Initial state)
"101" : 1.25V
"110" : 1.30V
"111" : 1.35V

Bit[7:4]: LDO12ADJ[3:0] LDO12 output voltage control

"000" : 1.00V
"001" : 1.05V
"010" : 1.10V
"011" : 1.15V
"100" : 1.20V (Initial state)
"101" : 1.25V
"110" : 1.30V
"111" : 1.35V

Address 09h : SWREGADJ1 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
09h	SWREGADJ1	R/W	SWREG2ADJ[3:0]				SWREG1ADJ[3:0]			
Initial Value		D2h	1	1	0	1	0	0	1	0

Bit[3:0]: SWREG1ADJ[3:0] SWREG1 output voltage control

"0000" : 1.00V
"0001" : 1.05V
"0010" : 1.10V (Initial state)
"0011" : 1.15V
"0100" : 1.20V
"0101" : 1.25V
"0110" : 1.30V
"0111" : 1.35V
"1000" : 1.40V
"1001" : 1.45V
"1010" : 1.50V
"1011" : 1.70V
"1100" : 1.75V
"1101" : 1.80V
"1110" : 1.85V
"1111" : 1.90V

Bit[7:4]: SWREG2ADJ[3:0] SWREG2 output voltage control

"0000" : 1.00V
"0001" : 1.05V
"0010" : 1.10V
"0011" : 1.15V
"0100" : 1.20V
"0101" : 1.25V
"0110" : 1.30V
"0111" : 1.35V
"1000" : 1.40V
"1001" : 1.45V
"1010" : 1.50V
"1011" : 1.70V
"1100" : 1.75V
"1101" : 1.80V (Initial state)
"1110" : 1.85V
"1111" : 1.90V

Address 0Ah : SWREGADJ2 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ah	SWREGADJ2	R/W	SWREG4ADJ[3:0]				SWREG3ADJ[3:0]			
Initial Value		84h	1	0	0	0	0	1	0	0

Bit[3:0]: SWREG3ADJ[3:0] SWREG3 output voltage control

"0000" : 1.00V
"0001" : 1.05V
"0010" : 1.10V
"0011" : 1.15V
"0100" : 1.20V (Initial state)
"0101" : 1.25V
"0110" : 1.30V
"0111" : 1.35V
"1000" : 1.40V
"1001" : 1.45V
"1010" : 1.50V
"1011" : 1.70V
"1100" : 1.75V
"1101" : 1.80V
"1110" : 1.85V
"1111" : 1.90V

Bit[7:4]: SWREG4ADJ[3:0] SWREG4 output voltage control

"0000" : 1.00V
"0001" : 1.05V
"0010" : 1.10V
"0011" : 1.15V
"0100" : 1.20V
"0101" : 1.25V
"0110" : 1.30V
"0111" : 1.35V
"1000" : 1.40V (Initial state)
"1001" : 1.45V
"1010" : 1.50V
"1011" : 1.70V
"1100" : 1.75V
"1101" : 1.80V
"1110" : 1.85V
"1111" : 1.90V

When this output is used as the power source VIN2 which is used for LDO11 and LDO12, it must be set to meet the minimum input voltage condition.

Address 0Bh : SWREGADJ3 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	SWREGADJ3	R/W	-	-	-	-	SWREG5ADJ[3:0]			
Initial Value		0Bh	0	0	0	0	1	0	1	1

Bit[3:0]: SWREG5ADJ[3:0] SWREG5 output voltage control

"0000" : 1.20V
"0001" : 1.40V
"0010" : 1.70V
"0011" : 1.75V
"0100" : 1.80V
"0101" : 1.85V
"0110" : 1.90V
"0111" : 3.00V
"1000" : 3.05V
"1001" : 3.10V
"1010" : 3.15V
"1011" : 3.20V (Initial state)
"1100" : 3.25V
"1101" : 3.30V
"1110" : 3.35V
"1111" : 3.40V

When this output is used as the power source VIN1 which is used for LDO1, 4, 5, 6, 7, 8, 9, 10, it must be set to meet the minimum input voltage condition.

Address 0Ch : ENLD_DIS Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	ENLD_DIS	R/W	-	-	-	-	-	-	-	ENLD7_DIS
Initial Value		00h	0	0	0	0	0	0	0	0

Bit [0]: ENLD7_DIS EN_O7 external control pin disable register

"0" : EN_O7 control enabled (Initial State)

"1" : EN_O7 control disabled

(LDO7,8,11,12 and SWREG4 is controlled by I2C command)

Address 0Dh : LDOPD1_DIS Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Dh	LDOPD1_DIS	R/W	LDO8PD_DIS	LDO7PD_DIS	LDO6PD_DIS	LDO5PD_DIS	LDO4PD_DIS	LDO3PD_DIS	LDO2PD_DIS	LDO1PD_DIS
Initial Value		00h	0	0	0	0	0	0	0	0

Bit0: LDO1PD_DIS LDO1 Discharge resistor ON/OFF control
"0" : Discharge enabled (Initial state)
"1" : Discharge disabled

Bit1: LDO2PD_DIS LDO2 Discharge resistor ON/OFF control
"0" : Discharge enabled (Initial state)
"1" : Discharge disabled

Bit2: LDO3PD_DIS LDO3 Discharge resistor ON/OFF control
"0" : Discharge enabled (Initial state)
"1" : Discharge disabled

Bit3: LDO4PD_DIS LDO4 Discharge resistor ON/OFF control
"0" : Discharge enabled (Initial state)
"1" : Discharge disabled

Bit4: LDO5PD_DIS LDO5 Discharge resistor ON/OFF control
"0" : Discharge enabled (Initial state)
"1" : Discharge disabled

Bit5: LDO6PD_DIS LDO6 Discharge resistor ON/OFF control
"0" : Discharge enabled (Initial state)
"1" : Discharge disabled

Bit6: LDO7PD_DIS LDO7 Discharge resistor ON/OFF control
"0" : Discharge enabled (Initial state)
"1" : Discharge disabled

Bit7: LDO8PD_DIS LDO8 Discharge resistor ON/OFF control
"0" : Discharge enabled (Initial state)
"1" : Discharge disabled

Address 0Eh : LDOPD2_DIS Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	LDOPD2_DIS	R/W	-	-	-	-	LDO12PD_DIS	LDO11PD_DIS	LDO10PD_DIS	LDO9PD_DIS
Initial Value		00h	0	0	0	0	0	0	0	0

Bit0: LDO9PD_DIS LDO9 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Bit1: LDO10PD_DIS LDO10 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Bit2: LDO11PD_DIS LDO11 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Bit3: LDO12PD_DIS LDO12 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Address 0Fh : SWREGPD_DIS Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	SWREGPD_DIS	R/W	-	-	-	SWREG5PD_DIS	SWREG4PD_DIS	SWREG3PD_DIS	SWREG2PD_DIS	SWREG1PD_DIS
Initial Value		00h	0	0	0	0	0	0	0	0

Bit0: SWREG1PD_DIS SWREG1 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Bit1: SWREG2PD_DIS SWREG2 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Bit2: SWREG3PD_DIS SWREG3 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Bit3: SWREG4PD_DIS SWREG4 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Bit4: SWREG5PD_DIS SWREG5 Discharge resistor ON/OFF control

"0" : Discharge enabled (Initial state)

"1" : Discharge disabled

Address 10h : ANASW_CNT Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	ANASW_CNT	R/W	-	-	-	-	-	ANASW_EN	ANASW_SEL[1:0]	
Initial Value		00h	0	0	0	0	0	0	0	0

Bit[1:0]: ANASW_SEL[1:0] Analog Switch input select control

"00" : ASWIN1 select (Initial state)

"01" : ASWIN2 select

"10" : ASWIN3 select

"11" : ASWIN4 select

Bit2: ANASW_EN Analog Switch ON/OFF control

"0" : Fixed 'L' output (Initial state)

"1" : Output enabled

Address 11h : TCXO_CNT Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11h	TCXO_CNT	R/W	-	TCXO_MASK[2:0]			-	-	TCXO_EN	TCXO_SEL
Initial Value		40h	0	1	0	0	0	0	0	0

Bit[0]: TCXO_SEL TCXO buffer control select

"0" : LDO7 ON/OFF synchronous control (Initial state)

LDO7=OFF: TCXO=OFF
LDO7=ON: TCXO=ON

"1" : TCXO_EN register control mode

Bit[1]: TCXO_EN TCXO buffer ON/OFF register control

"0" : Buffer OFF (Initial state)

"1" : Buffer ON

The TCXO buffer control follows the control table shown below.

TCXO_SEL register	TCXO_EN register	ENLD7_DIS register	EN_O7 pin	LDO7ON register	TCXO buffer control
0	*	0	0	*	OFF
0	*	0	1	*	ON
0	*	1	*	0	OFF
0	*	1	*	1	ON
1	0	*	*	*	OFF
1	1	*	*	*	ON

Bit[6:4]: TCXO_MASK TCXO buffer output mask length control

"000" : 155us
"001" : 250us
"010" : 345us
"011" : 440us
"100" : 530us (Initial state)
"101" : 655us
"110" : 750us
"111" : 845us

Address 12h : OSC_CNT Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
12h	OSC_CNT	R/W	-	-	-	-	-	-	C32KOUT_EN	OSC_EN
Initial Value		03h	0	0	0	0	0	0	1	1

Bit[0]: OSC_EN OSC ON/OFF control

"0" : Oscillation OFF

"1" : Oscillation ON (Initial state)

Bit[1]: C32KOUT_EN C32KOUT buffer output control

"0" : Buffer OFF

"1" : Buffer ON (Initial state)

Address 13h : SWREGPWM Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13h	SWREGPWM	R/W	-	-	-	SWREG5 PWM	SWREG4 PWM	SWREG3 PWM	SWREG2 PWM	SWREG1 PWM
Initial Value		00h	0	0	0	0	0	0	0	0

Bit0: SWREG1PWM SWREG1 PWM fixed mode enable control
"0" : PFM/PWM auto mode (Initial state)
"1" : PWM fixed mode

Bit1: SWREG2PWM SWREG2 PWM fixed mode enable control
"0" : PFM/PWM auto mode (Initial state)
"1" : PWM fixed mode

Bit2: SWREG3PWM SWREG3 PWM fixed mode enable control
"0" : PFM/PWM auto mode (Initial state)
"1" : PWM fixed mode

Bit3: SWREG4PWM SWREG4 PWM fixed mode enable control
"0" : PFM/PWM auto mode (Initial state)
"1" : PWM fixed mode

Bit4: SWREG5PWM SWREG5 PWM fixed mode enable control
"0" : PFM/PWM auto mode (Initial state)
"1" : PWM fixed mode

Address 14h : SW5BYPASS Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14h	SW5BYPASS	R/W	-	reserved	reserved	BYPASS_DIS	-	VINDET5ADJ[2:0]		
Initial Value		01h	0	0	0	0	0	0	0	1

Bit[2:0]: VINDET5ADJ[2:0] SWREG5 VBAT Bypass mode detect level

"000" : 3.30V
"001" : 3.35V (Initial state)
"010" : 3.40V
"011" : 3.45V
"100" : 3.50V
"101" : 3.55V
"110" : 3.60V
"111" : 3.65V

Bit4: BYPASS_DIS SWREG5 VBAT Bypass mode control

"0" : Bypass mode enable (Initial state)
"1" : Bypass mode disable

Please always write "0" to the reserved registers when in use.

Typical Characteristics

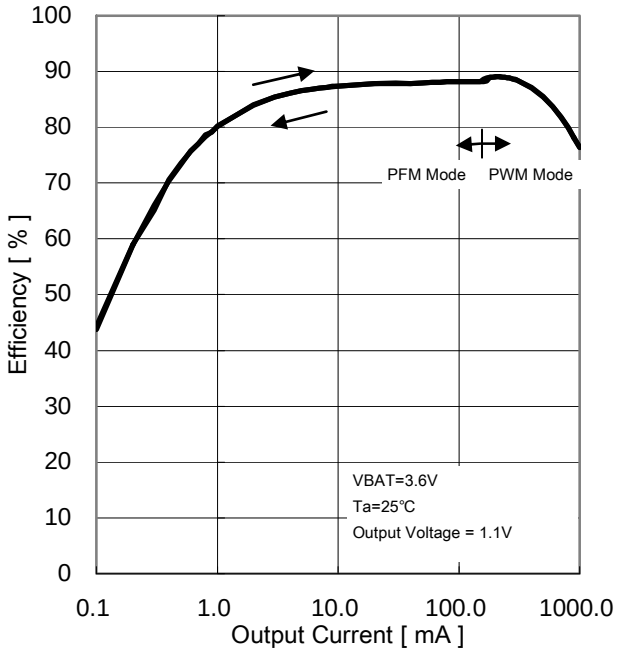


Figure 20. Efficiency vs Output Current
(SWREG1 Efficiency)

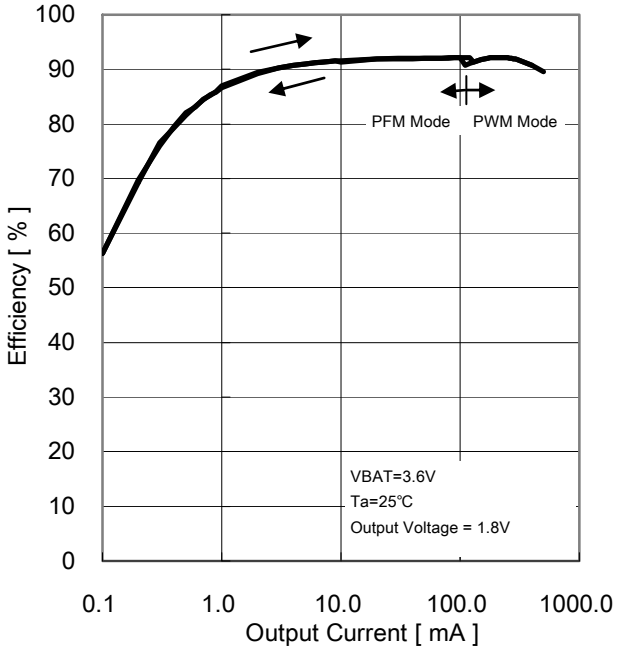


Figure 21. Efficiency vs Output Current
(SWREG2 Efficiency)

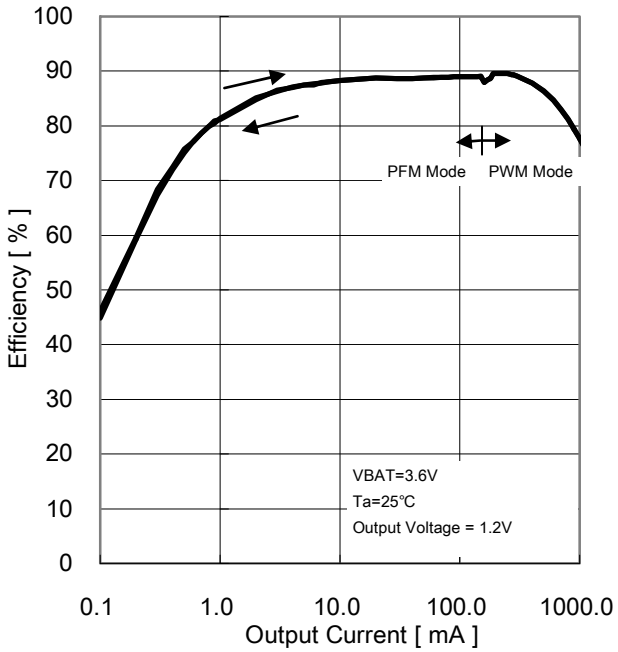


Figure 22. Efficiency vs Output Current
(SWREG3 Efficiency)

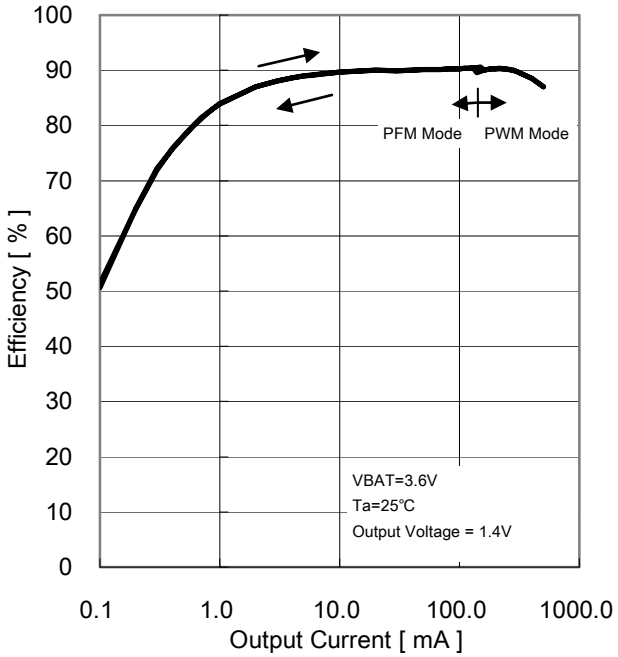


Figure 23. Efficiency vs Output Current
(SWRE4 Efficiency)

Typical Characteristics

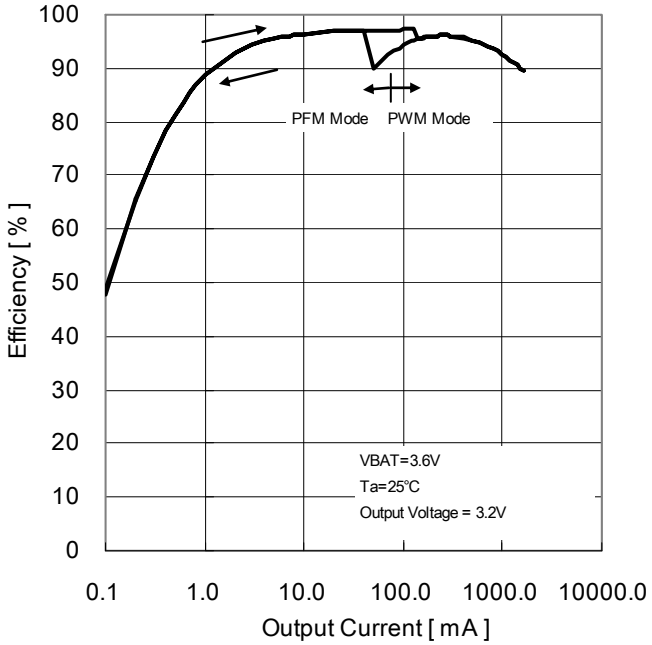


Figure 24. Efficiency vs Output Current
(SWRE5 Efficiency)

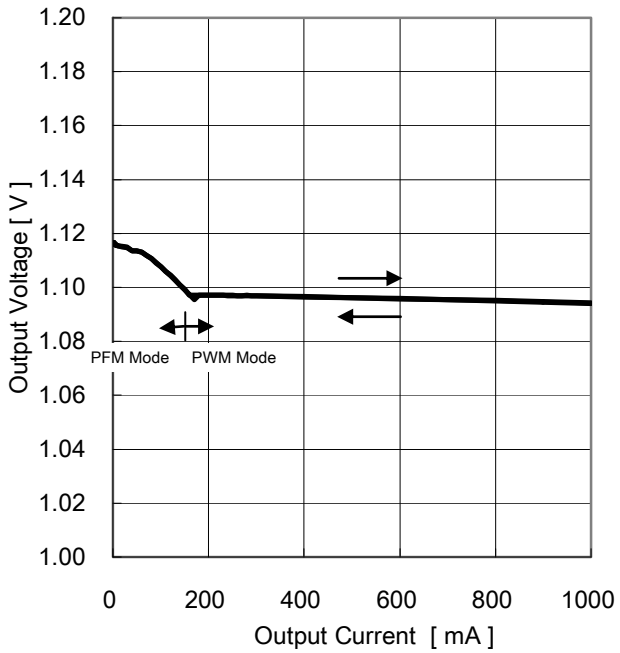


Figure 25. Output Voltage vs Output Current
(SWREG1 Load Regulation)

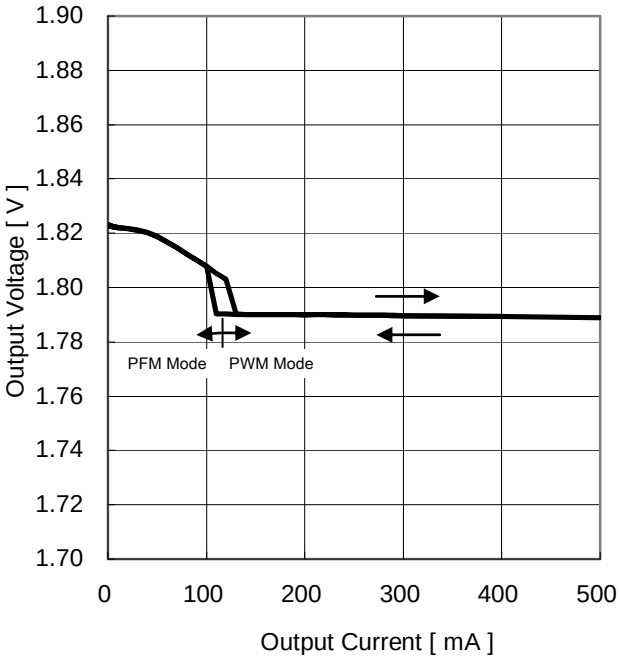


Figure 26. Output Voltage vs Output Current
(SWREG2 Load Regulation)

Typical Characteristics

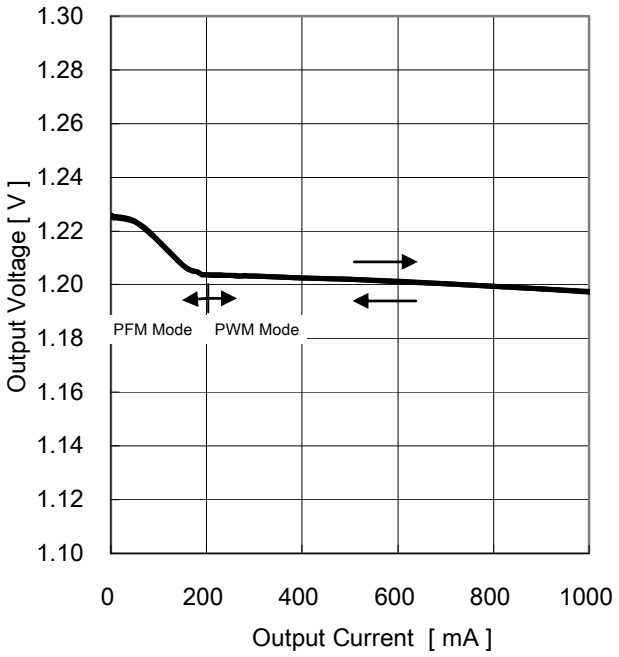


Figure 27. Output Voltage vs Output Current
(SWREG3 Load Regulation)

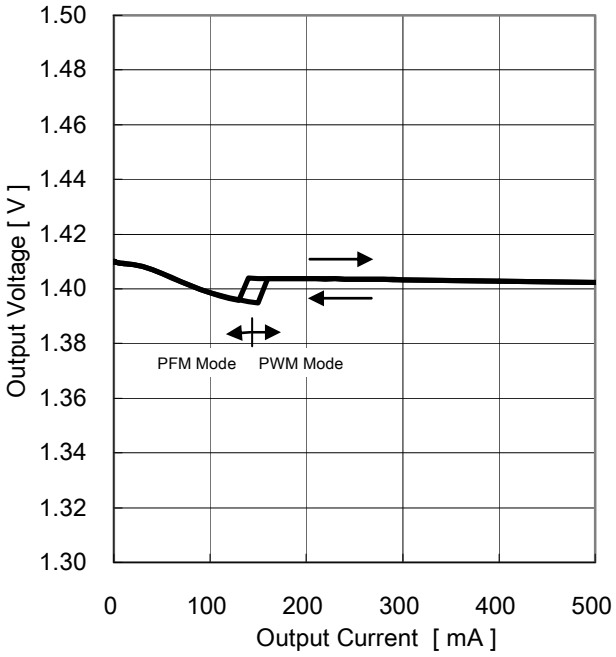


Figure 28. Output Voltage vs Output Current
(SWREG4 Load Regulation)

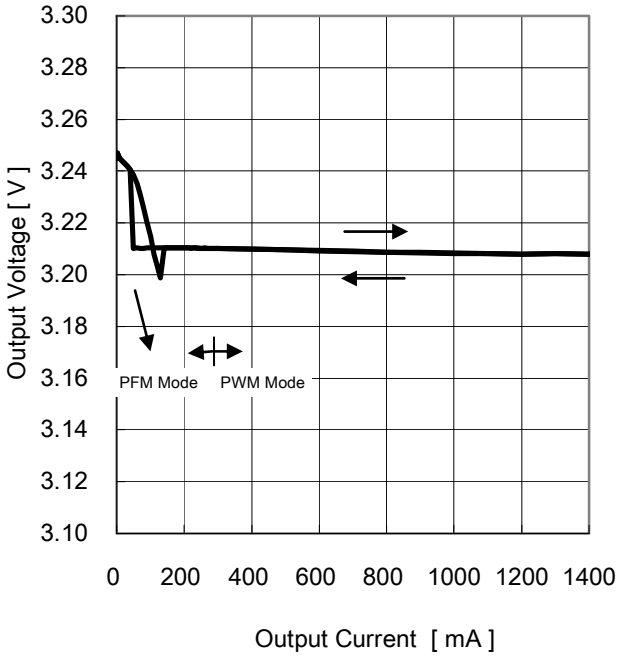


Figure 29. Output Voltage vs Output Current
(SWREG5 Load Regulation)

Typical Characteristics

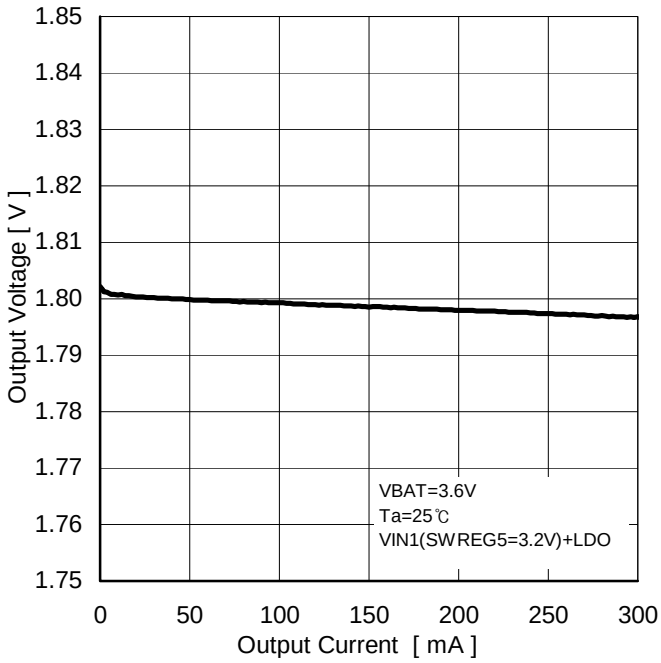


Figure 30. Output Voltage vs Output Current
(LDO1 Load Regulation)

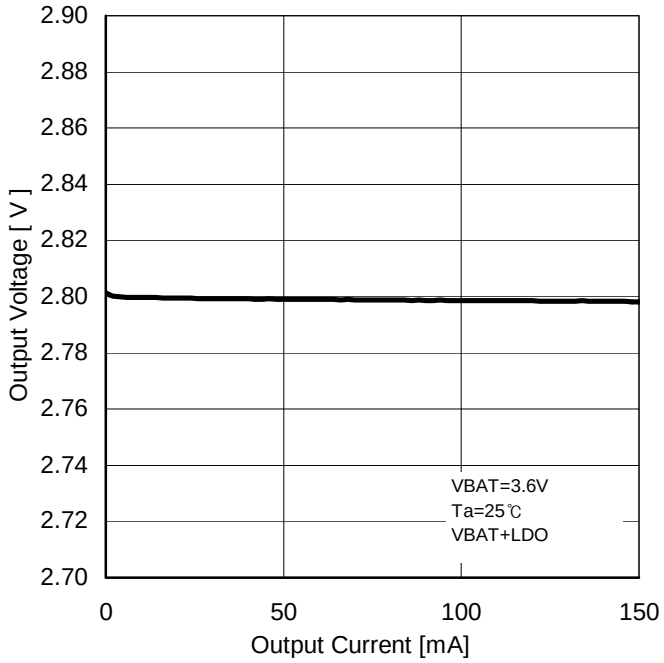


Figure 31. Output Voltage vs Output Current
(LDO2 Load Regulation)

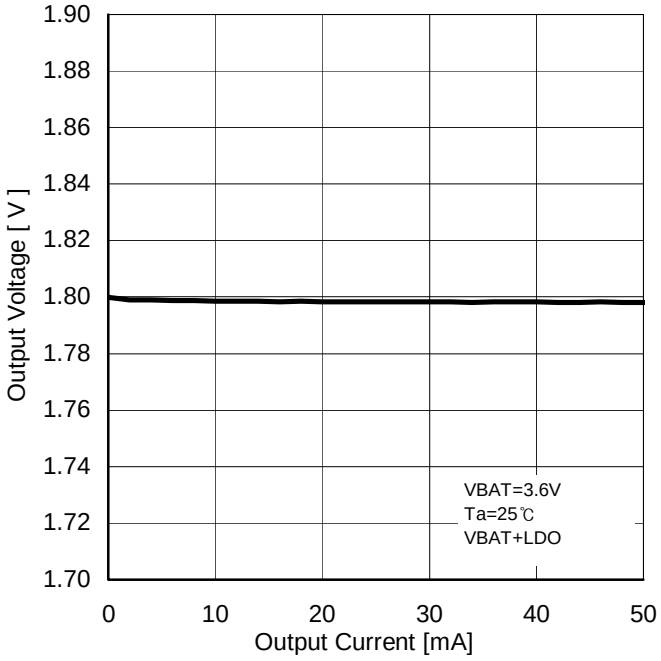


Figure 32. Output Voltage vs Output Current
(LDO3 Load Regulation)

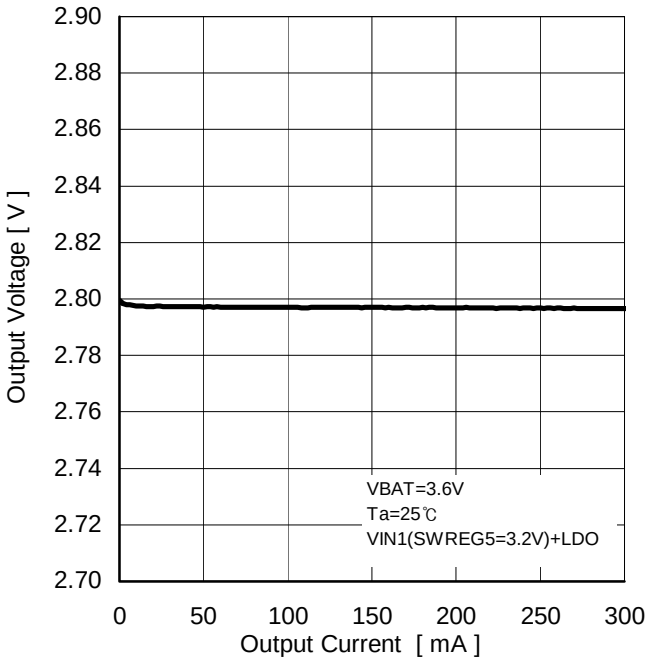


Figure 33. Output Voltage vs Output Current
(LDO4 Load Regulation)

Typical Characteristics

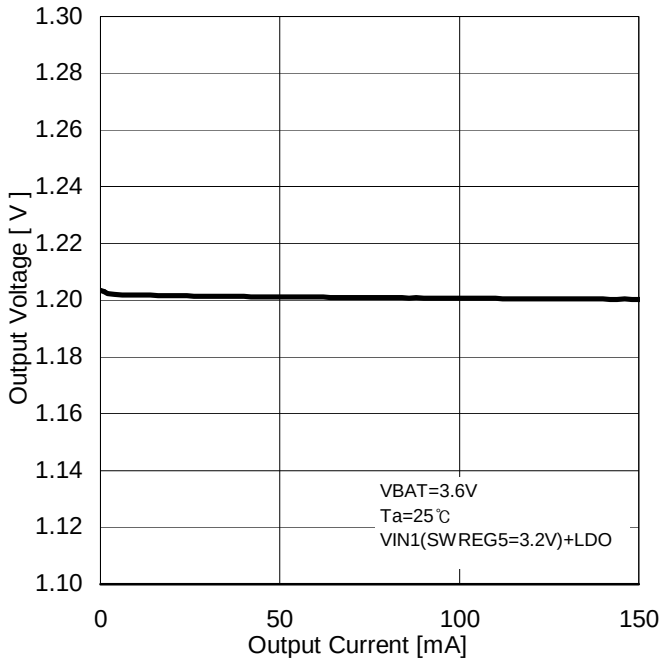


Figure 34. Output Voltage vs Output Current
(LDO5 Load Regulation)

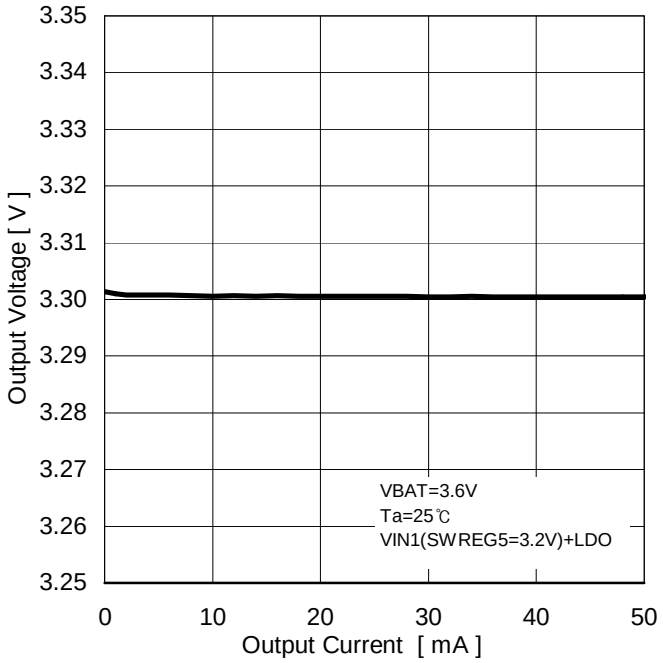


Figure 35. Output Voltage vs Output Current
(LDO6 Load Regulation)

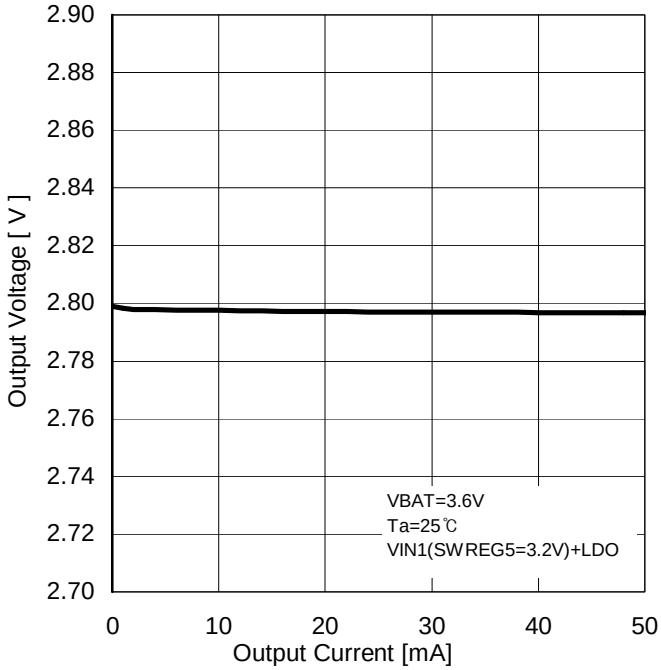


Figure 36. Output Voltage vs Output Current
(LDO7 Load Regulation)

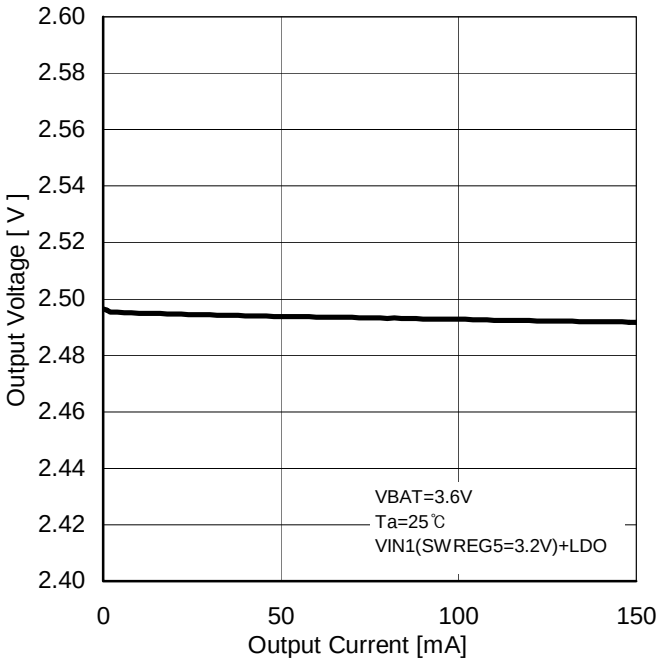


Figure 37. Output Voltage vs Output Current
(LDO8 Load Regulation)

Typical Characteristics

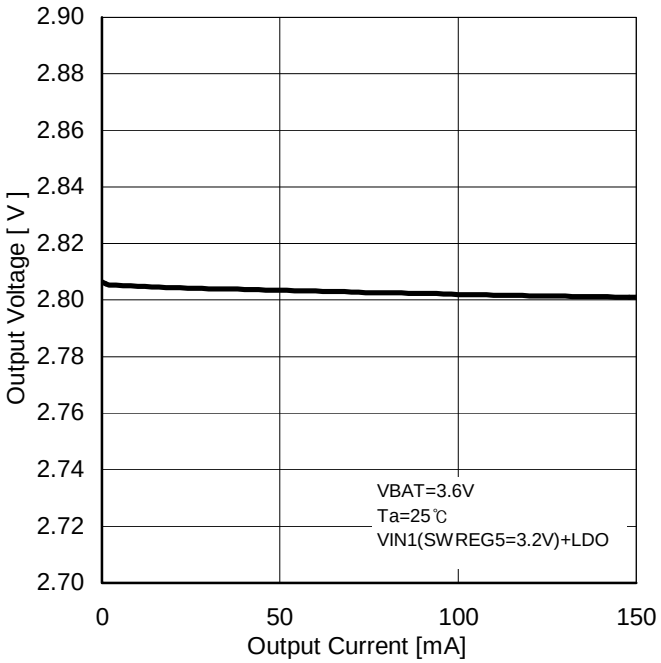


Figure 38. Output Voltage vs Output Current
(LDO9 Load Regulation)

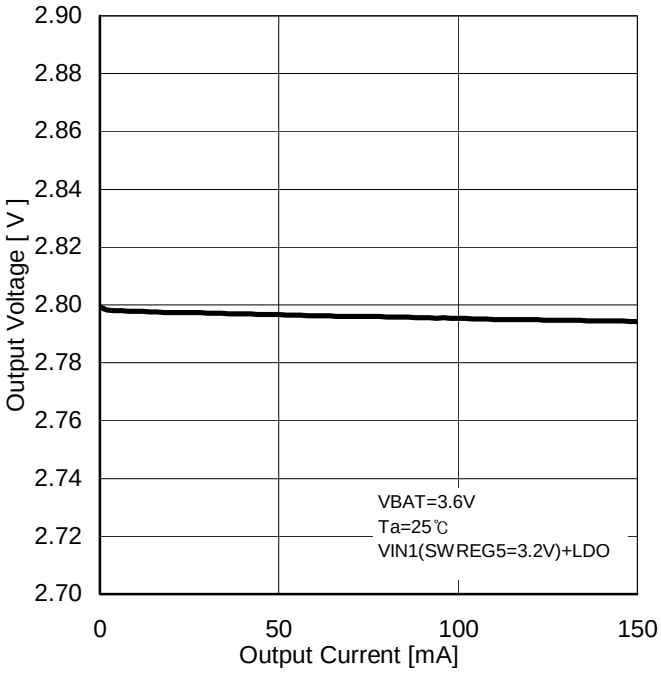


Figure 39. Output Voltage vs Output Current
(LDO10 Load Regulation)

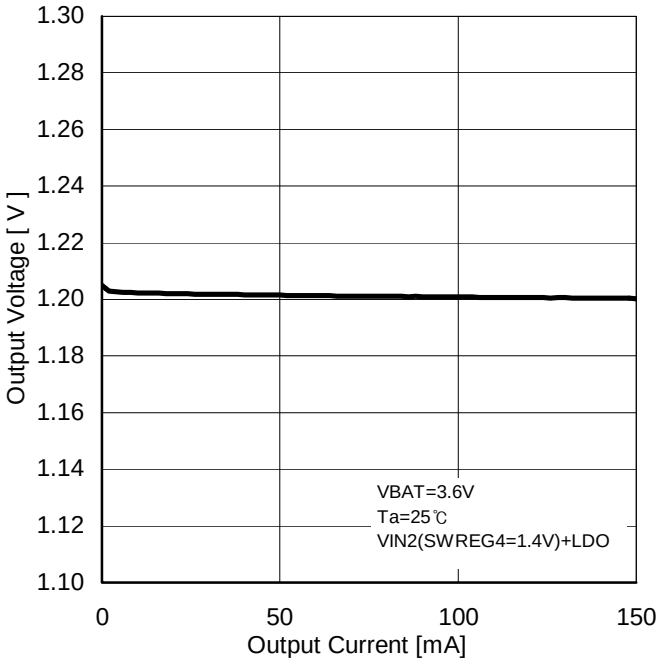


Figure 40. Output Voltage vs Output Current
(LDO11 Load Regulation)

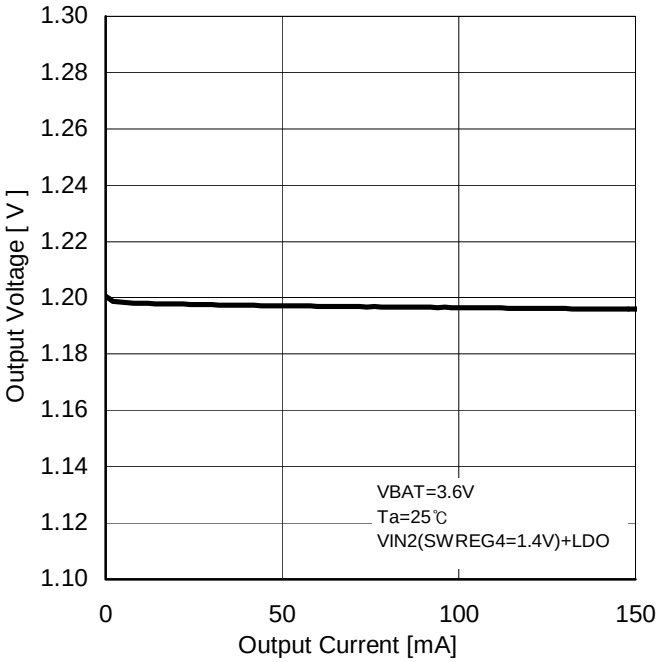


Figure 41. Output Voltage vs Output Current
(LDO12 Load Regulation)

PCB Layout Guidelines

To achieve the best efficiency, stability, and regulation, it is necessary to meet following rules.

1) Bypass Capacitor (CPBAT) should be placed as close as possible to the IC pins.
2) Bypass Capacitor (CPBAT) should be connected by TOP Layer. (It is better not used via)
3) The inductor (L) and output capacitor (Cout) should be also placed to near side.
4) The Feed Back line of buck converter (FB) is wired as short as possible.
5) It is better don't place the GND cupper trace under the chip Inductor for reducing the effective of noise
6) To further reduce the noise interference on sensitive nodes use the ground plane layout. When you connect to the GND plane, please reduce the impedance using VIA plurality of contacts.

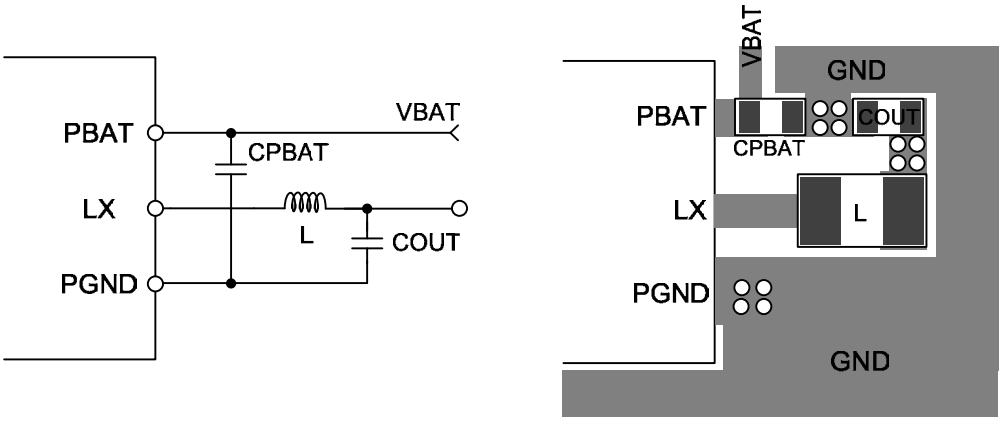


Figure 42. Schematic & PCB Layout Ideal Image (DCDC)

7) To keep the good stability, don't placed GND trace under the Crystal.
Please keep the distance between the Crystal and noisy device.
Please be as short as possible the distance of crystal and BD7187GW because it is a sensitive device.
8) This device includes the noisy block. (Buck converter, SIM interface, 32 KHz oscillator)
There is a possibility that these noises affect the other electric components of the mobile instruments.
Please check thoroughly with your set about the effect of noise. The good PCB artwork reduces the effective of noise.
To prevent it from BD71801GWL, please consider to use metal can shielding or chip bead.

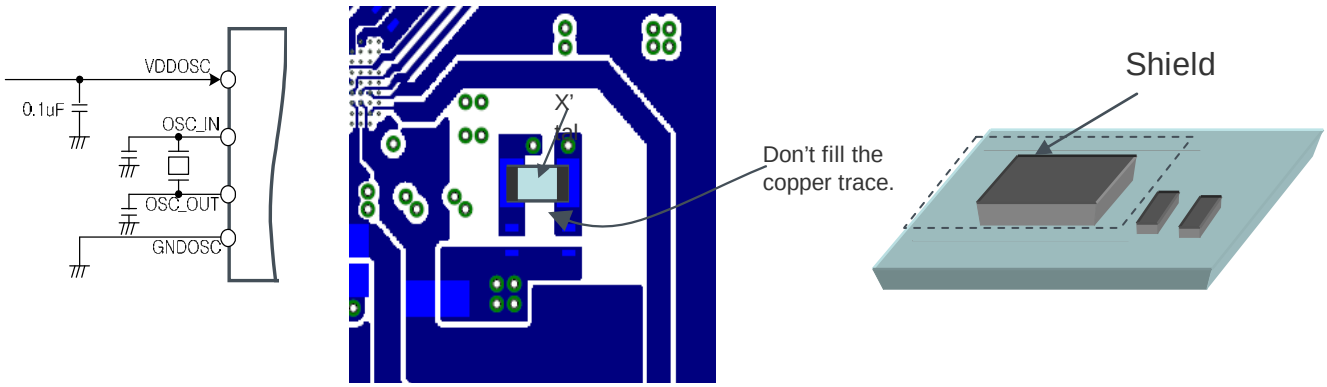


Figure 43. Schematic & PCB Layout Image (X'tal)

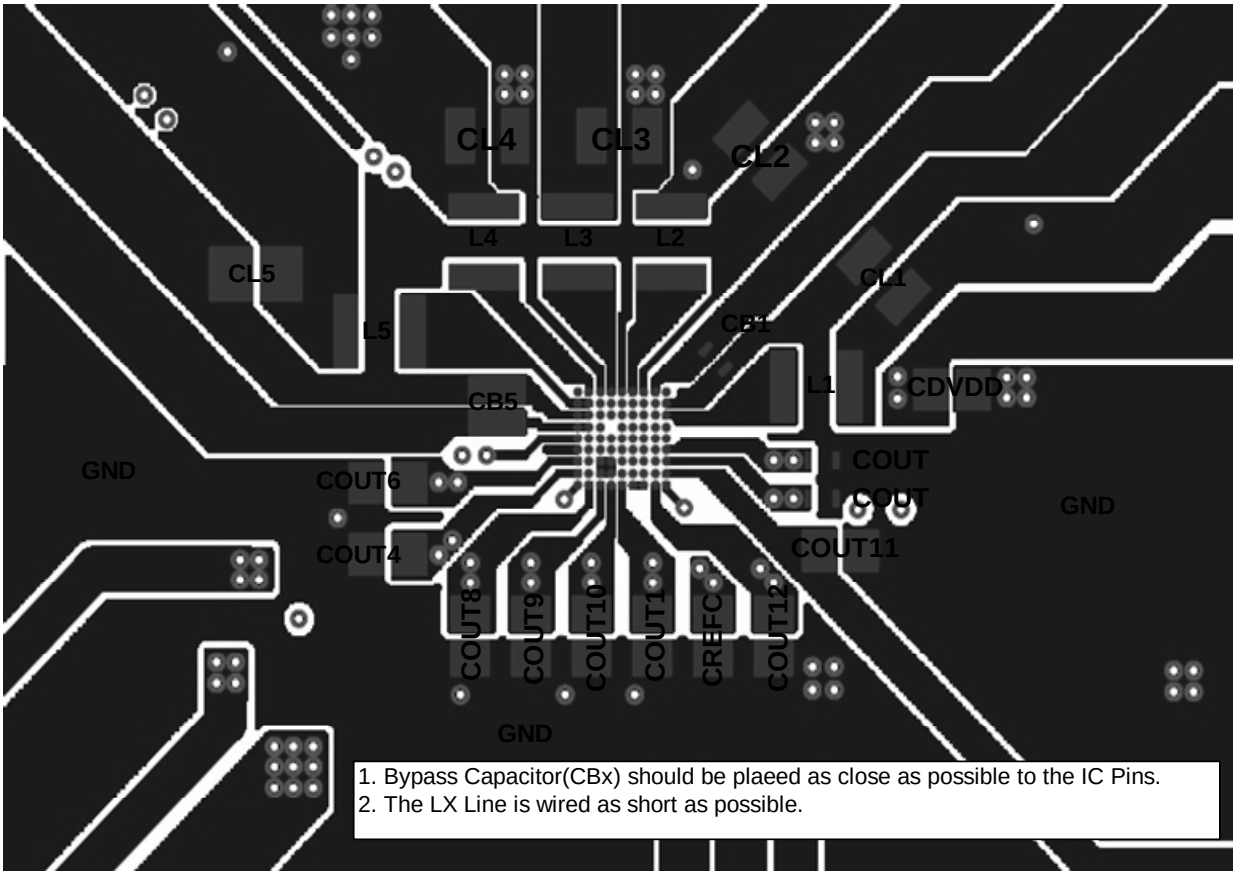


Figure 44. PCB Layout Image (Top Layer)

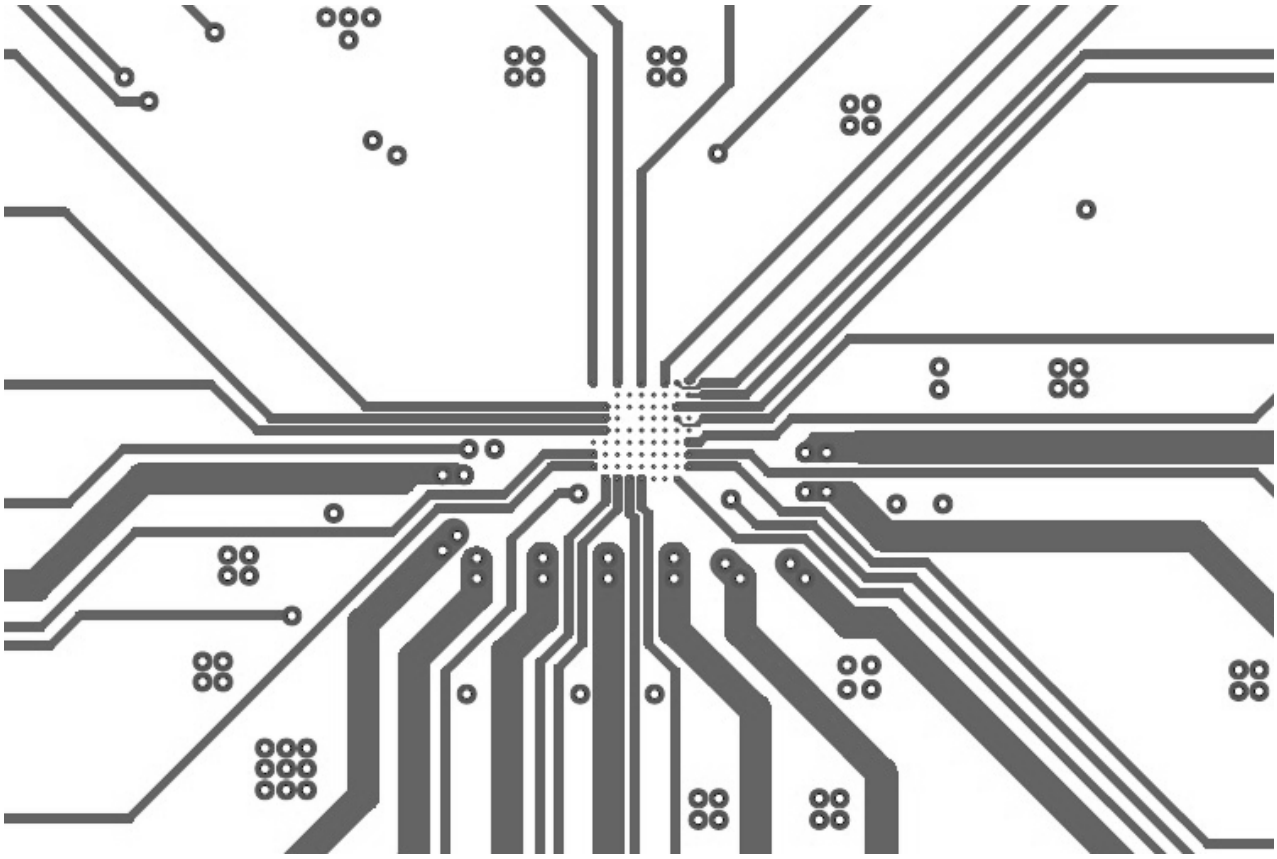


Figure 45. PCB Layout Image (Mid1 Layer)

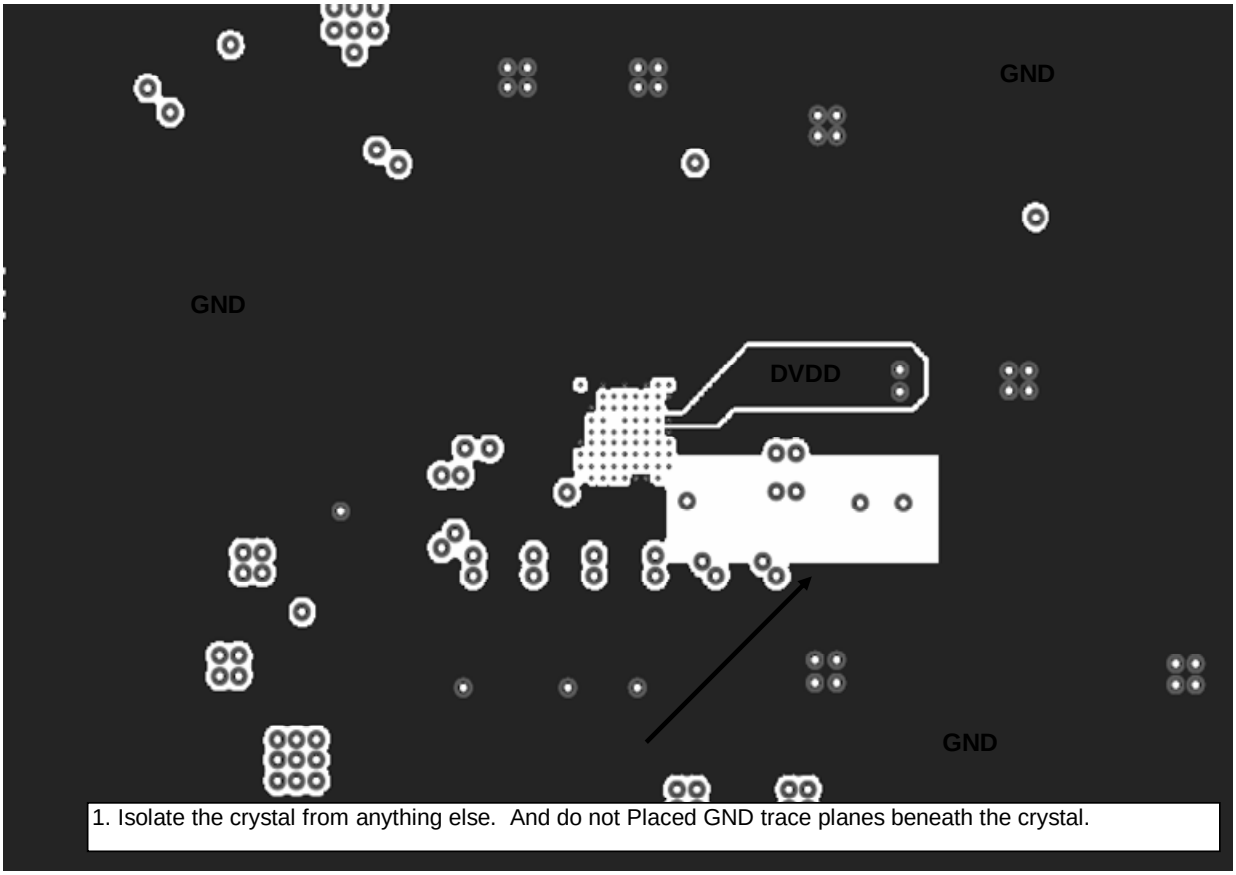


Figure 46. PCB Layout Image (Mid2 Layer)

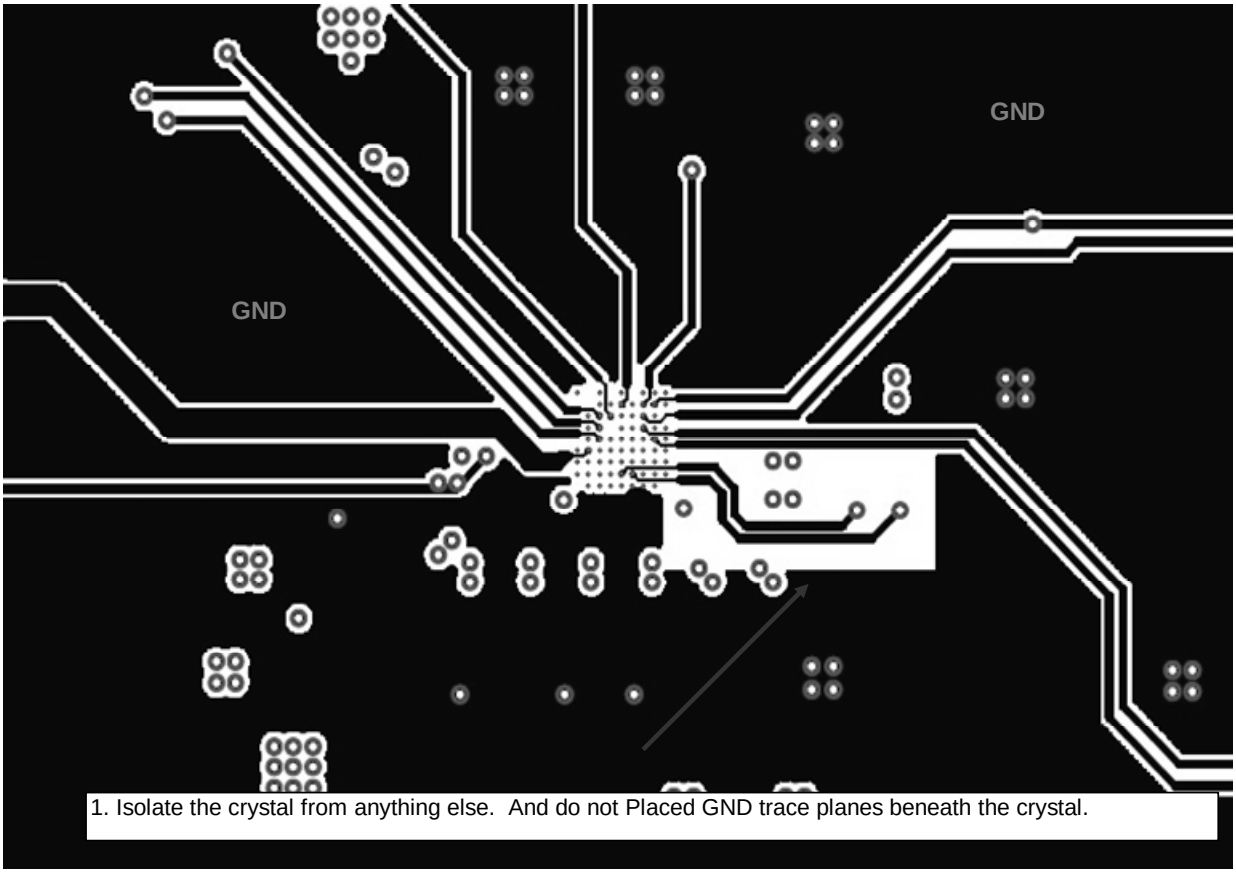


Figure 47. PCB Layout Image (Mid3 Layer)

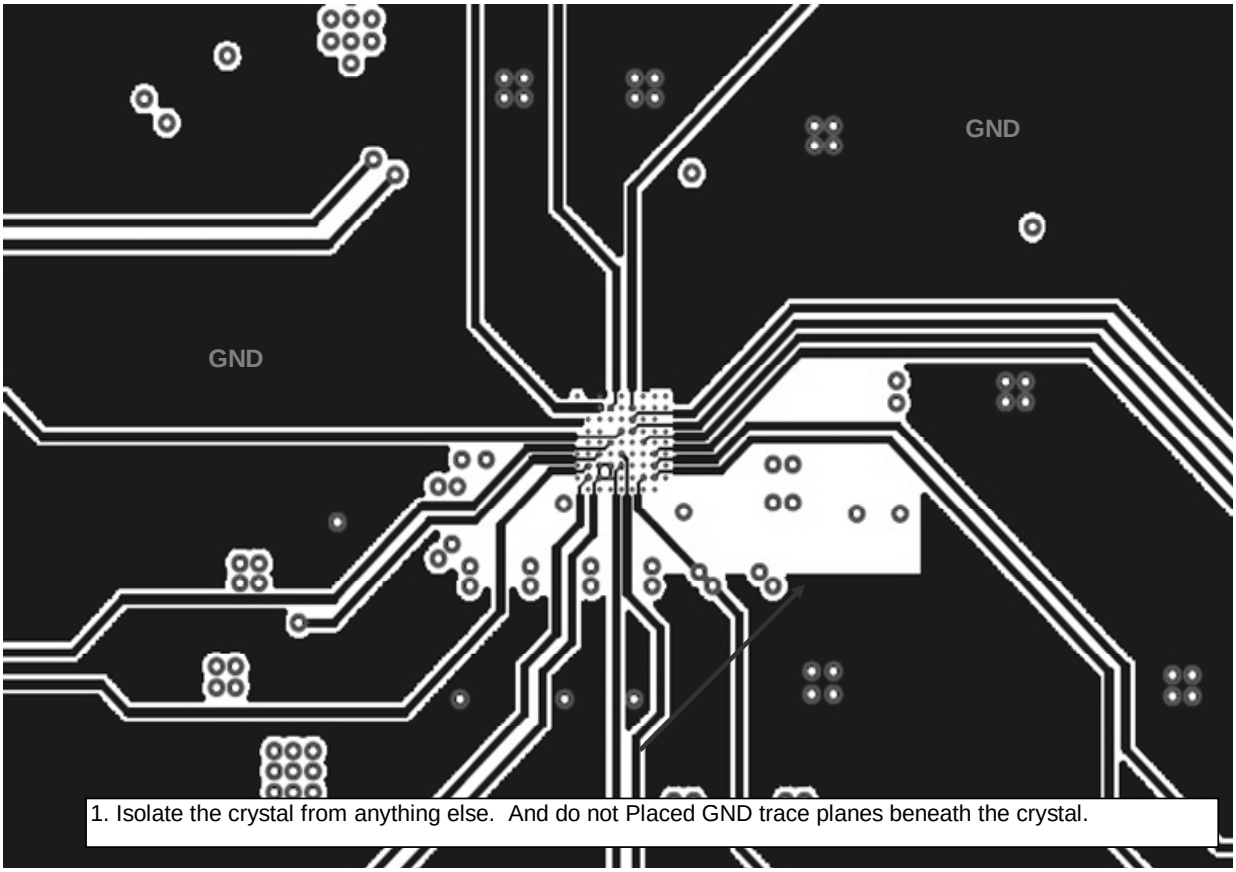


Figure 48. PCB Layout Image (Mid4 Layer)

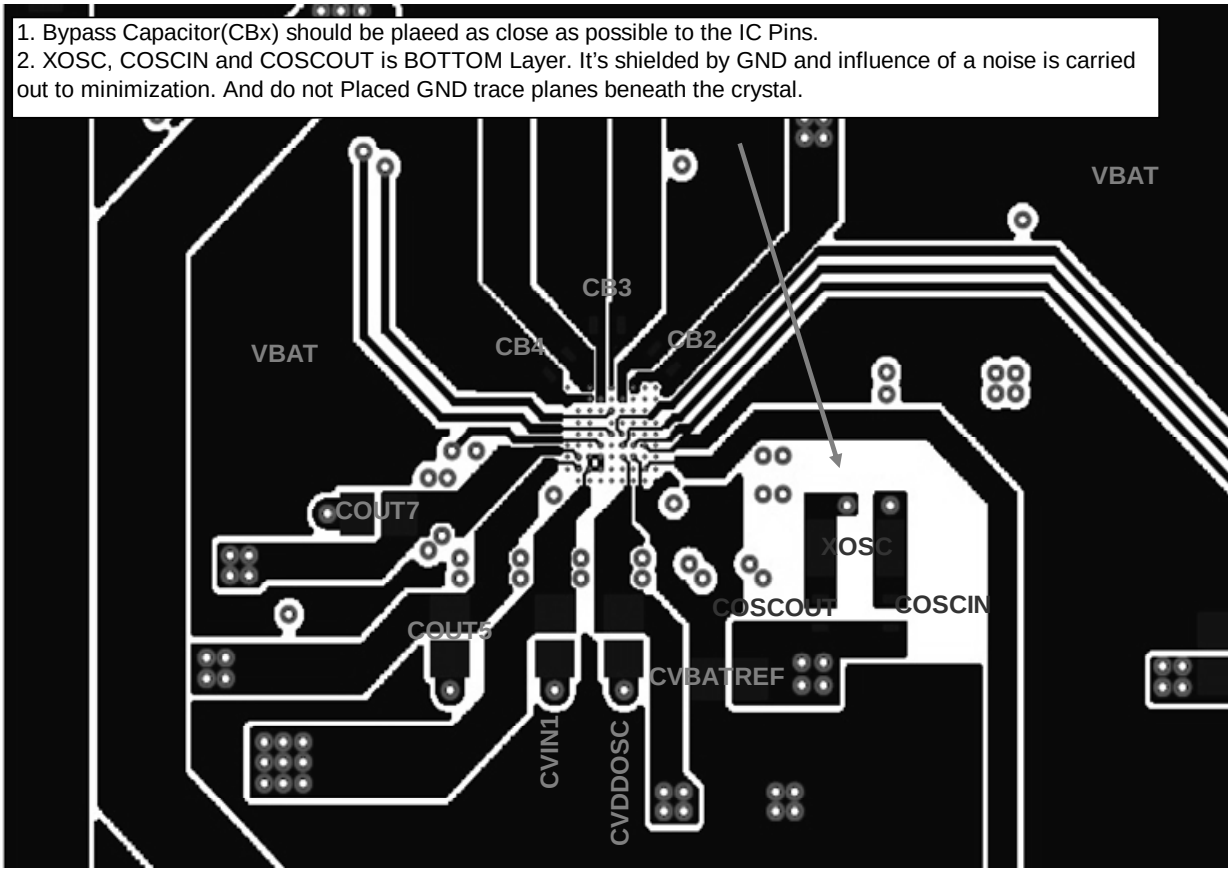


Figure 49. PCB Layout Image (Mid4 Layer)

Ordering Information

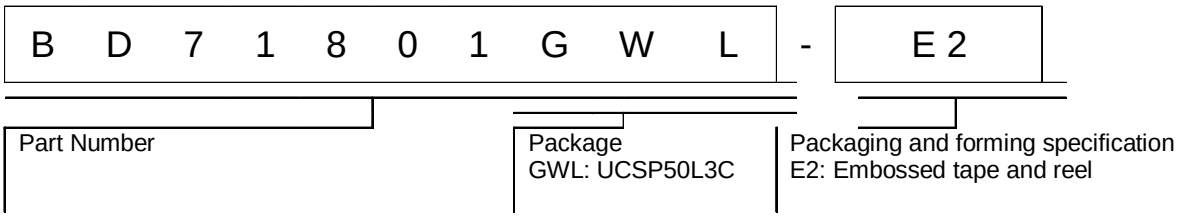
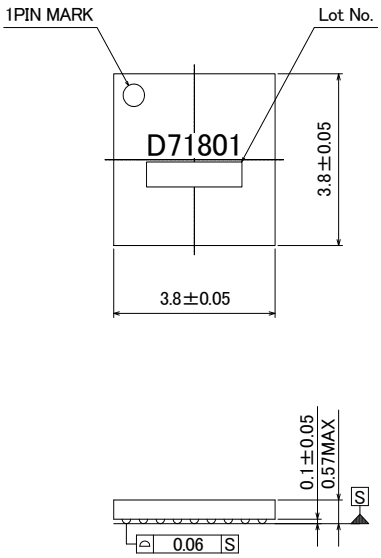


Figure 50. Ordering Information

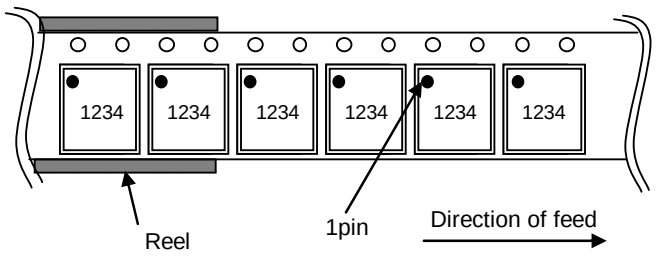
Physical Dimension Tape and Reel Information

UCSP50L3C	BD71801GWL



< Tape and Reel Information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of Feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand.



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

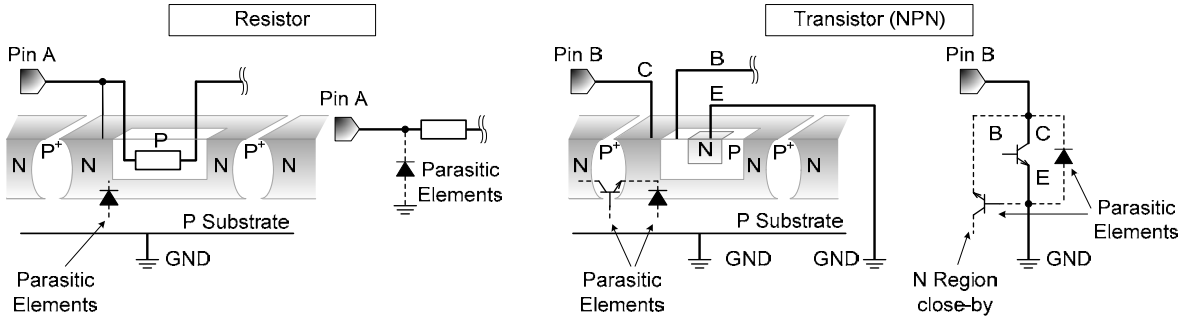


Figure 50. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Revision History

Date	Revision	Changes
2013.09.27	001	New release
2013.11.18	002	Page2. Absolute maximum Ratings (DVDD Voltage add) Page12 Power On Sequence (Time of UVLO to DCDC5) Page68.Correction typographical error

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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